1MHz Step-Down DC/DC Converters in SOT-23

FEATURES

- **Tiny 5-Lead SOT-23 Package**
- **Uses Tiny Capacitors and Inductor**
- **High Frequency Operation: 1MHz**
- **High Output Current: 500mA**
- **Low $R_{DS(ON)}$ Internal Switch: 0.28Ω**
- High Efficiency: Up to 94%
- Current Mode Operation for Excellent Line and Load Transient Response
- Short-Circuit Protected
- Low Quiescent Current: 135µA (LTC1701)
- Low Dropout Operation: 100% Duty Cycle
- Ultralow Shutdown Current: I_Q < 1µA
- Peak Inductor Current Independent of Inductor Value
- Output Voltages from 5V Down to 1.25V

APPLICATIONS

- PDAs/Palmtop PCs
- Digital Cameras
- Cellular Phones
- Portable Media Players
- PC Cards
- Handheld Equipment

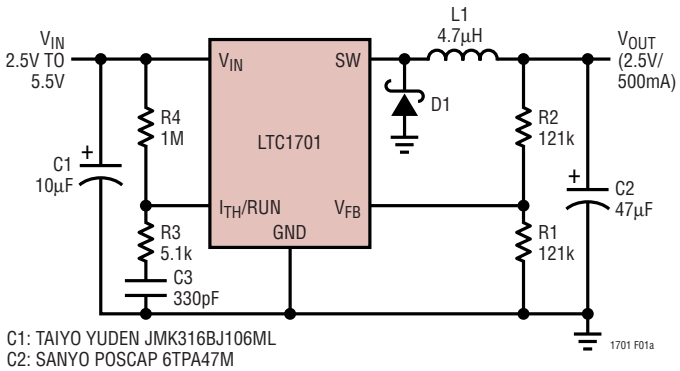
DESCRIPTION

The LTC®1701/LTC1701B are the industry's first SOT-23 step-down, current mode, DC/DC converters. Intended for low to medium power applications, they operate from 2.5V to 5.5V input voltage range and switch at 1MHz, allowing the use of tiny, low cost capacitors and inductors 2mm or less in height. The output voltage is adjustable from 1.25V to 5V. A built-in 0.28Ω switch allows up to 0.5A of output current at high efficiency. OPTI-LOOP™ compensation allows the transient response to be optimized over a wide range of loads and output capacitors.

The LTC1701 incorporates automatic power saving Burst Mode™ operation to reduce gate charge losses when the load current drops below the level required for continuous operation. The LTC1701B operates continuously to very low load currents to provide low ripple at the expense of light load efficiency. With no load, the LTC1701 draws only 135µA. In shutdown, both devices draw less than 1µA, making them ideal for current sensitive applications.

Their small size and switching frequency enables a complete DC/DC converter function to consume less than 0.3 square inches of PC board area.

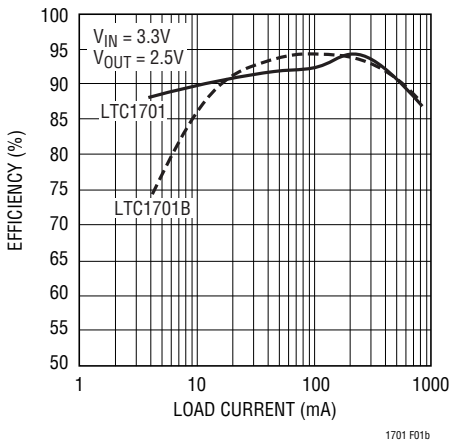
TYPICAL APPLICATION



C1: TAIYO YUDEN JMK316BJ106ML
C2: SANYO POSCAP 6TPA47M
D1: MBRM120L
L1: SUMIDA CD43-4R7

Figure 1. 2.5V/500mA Step-Down Regulator

Efficiency Curve



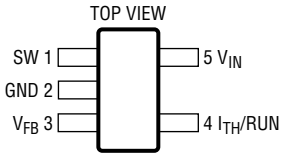
ABSOLUTE MAXIMUM RATINGS

(Note 1)

(Voltages Referred to GND Pin)

V_{IN} Voltage (Pin 5) ..... –0.3V to 6V
I_{TH}/RUN Voltage (Pin 4) ..... –0.3V to 3V
V_{FB} Voltage (Pin 3) ..... –0.3V to 3V
V_{IN} – SW (Max Switch Voltage) ..... 8.5V to –0.3V
Operating Temperature Range (Note 2) .. –40°C to 85°C
Junction Temperature (Note 5) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S5 PACKAGE
5-LEAD PLASTIC SOT-23

T_{JMAX} = 125°C, θ_{JA} = 250°C/W

SEE THE APPLICATION INFORMATION SECTION

ORDER PART NUMBER
LTC1701ES5 LTC1701BES5
S5 PART MARKING
LTKG LTUD

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V, $R_{ITH/RUN}$ = 1Meg (from V_{IN} to I_{TH}/RUN) unless otherwise specified. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage Range			2.5		5.5	V
I_{FB}	Feedback Pin Input Current	(Note 3)				±0.1	µA
V_{FB}	Feedback Voltage	(Note 3)	●	1.22	1.25	1.28	V
$\Delta V_{LINE\ REG}$	Reference Voltage Line Regulation	V_{IN} = 2.5V to 5V (Note 3)			0.04	0.1	%/V
$\Delta V_{LOAD\ REG}$	Output Voltage Load Regulation	Measured in Servo Loop, V_{ITH} = 1.5V, (Note 3) Measured in Servo Loop, V_{ITH} = 1.9V, (Note 3)			0.01 –0.80	0.70 –1.50	% %
	Input DC Supply Current (Note 4) Active Mode Sleep Mode Shutdown	 V_{FB} = 0V V_{FB} = 1.4V (LTC1701 only) $V_{ITH/RUN}$ = 0V			 185 135 0.25	 300 200 1	 µA µA µA
$V_{ITH/RUN}$	Run Threshold High Run Threshold Low	$I_{TH/RUN}$ Ramping Down $I_{TH/RUN}$ Ramping Up		 0.3	1.4 0.6	1.6	V V
$I_{ITH/RUN}$	Run Pullup Current	$V_{ITH/RUN}$ = 1V		50	100	300	µA
$I_{SW(PEAK)}$	Peak Switch Current Threshold	V_{FB} = 0V		0.9	1.1		A
$R_{DS(ON)}$	Switch ON Resistance	V_{IN} = 5V, V_{FB} = 0V V_{IN} = 3.3V, V_{FB} = 0V V_{IN} = 2.5V, V_{FB} = 0V			0.28 0.30 0.35		Ω Ω Ω
$I_{SW(LKG)}$	Switch Leakage Current	V_{IN} = 5V, $V_{ITH/RUN}$ = 0V, V_{FB} = 0V			0.01	1	µA
t_{OFF}	Switch Off-Time			400	500	600	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC1701E/LTC1701BE guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: The LTC1701/LTC1701B are tested in a feedback loop which servos V_{FB} to the midpoint for the error amplifier without $R_{ITH/RUN}$ = 1MHz (V_{ITH} = 1.7V unless otherwise specified).

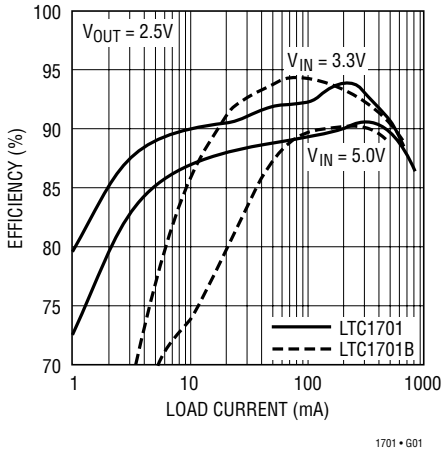
Note 4: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 5: T_J is calculated from the ambient T_A and power dissipation P_D according to the following formula:

LTC1701ES5/LTC1701BES5: $T_J = T_A + (P_D \bullet 250°C/W)$

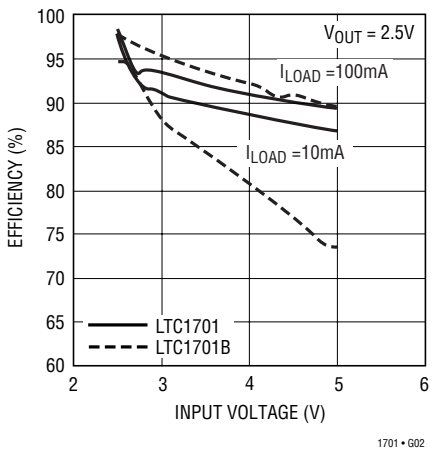
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Load Current



1701 • G01

Efficiency vs Input Voltage



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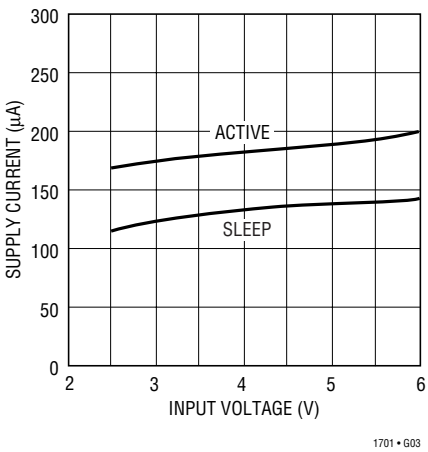
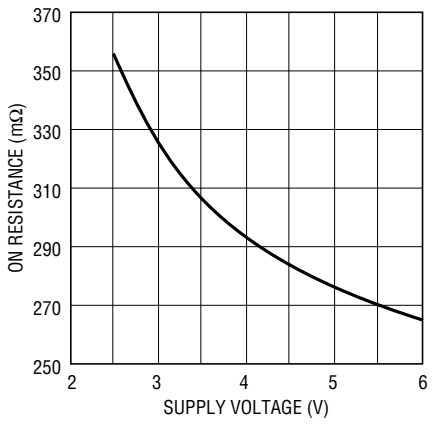
DC Supply Current



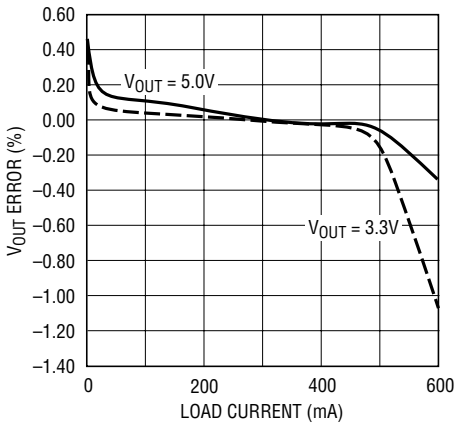
1701 • G03

Switch Resistance vs Supply Voltage



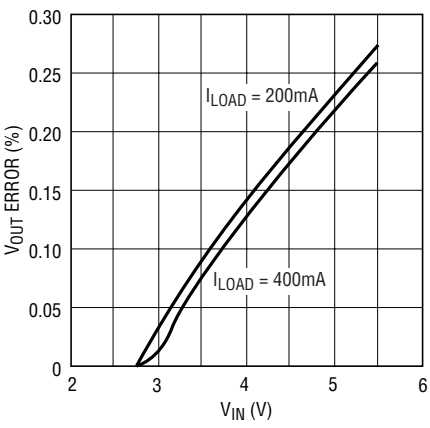
1701 • G04

Load Regulation



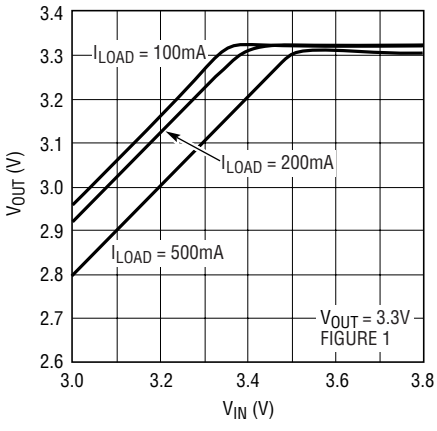
1701 • G05

Line Regulation



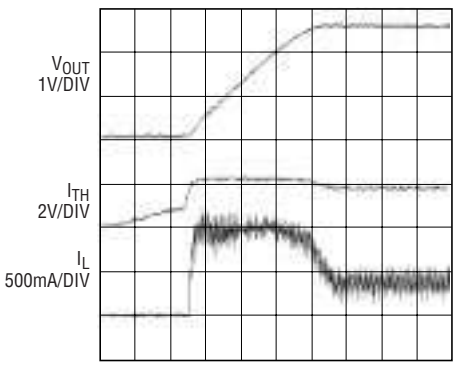
1701 • G06

Dropout Characteristics



701 • G07

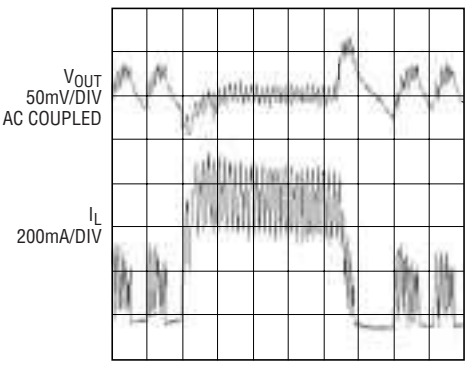
Start-Up



VIN = 3.3V, VOUT = 2.5V
CIRCUIT OF FIGURE 1
RLOAD = 6Ω

1701 G08

Transient Response



VIN = 3.3V, VOUT = 2.5V
CIRCUIT OF FIGURE 1
ILOAD = 100mA TO 500mA STEP

1701 G09

PIN FUNCTIONS

SW (Pin 1): The Switch Node Connection to the Inductor. This pin swings from V_{IN} to a Schottky diode (external) voltage drop below ground. The cathode of the Schottky diode must be closely connected to this pin.

GND (Pin 2): Ground Pin. Connect to the (–) terminal of C_{OUT}, the Schottky diode and (–) terminal of C_{IN}.

V_{FB} (Pin 3): Receives the feedback voltage from the external resistive divider across the output. Nominal voltage for this pin is 1.25V.

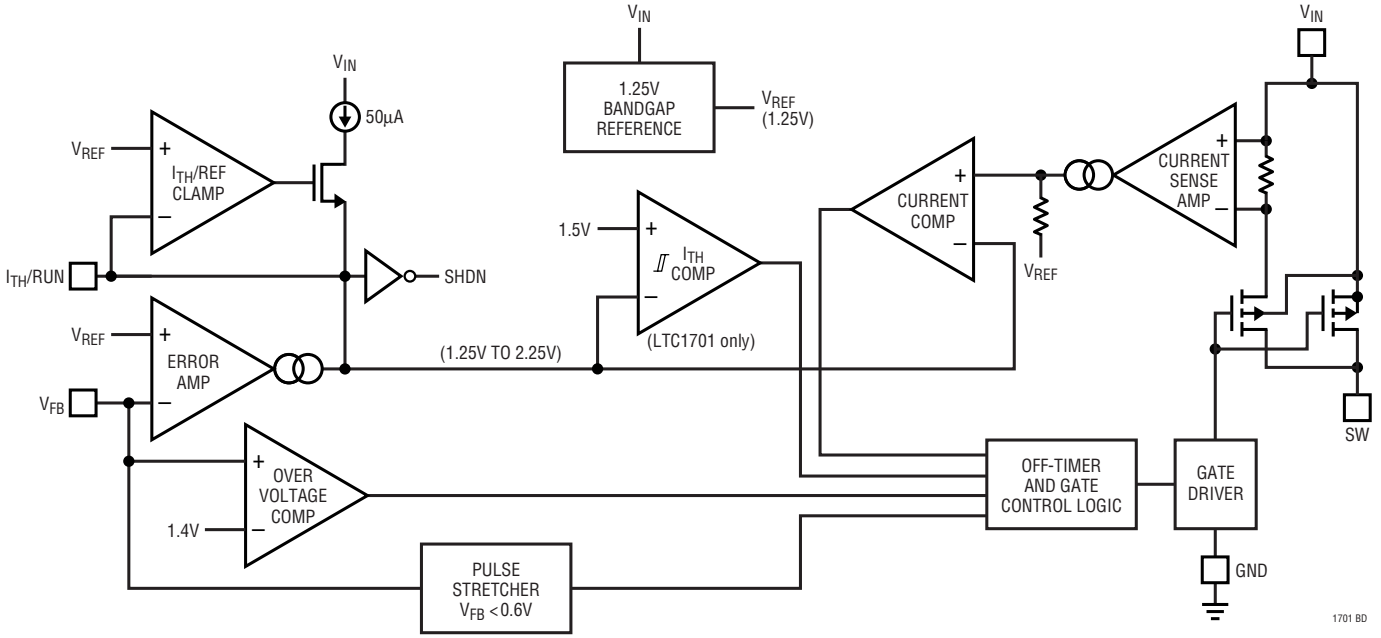
I_{TH}/RUN (Pin 4): Combination of Error Amplifier Compensation Point and Run Control Input. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 1.25V to 2.25V. Forcing this pin below 0.8V causes the device to be shut down. In shutdown all functions are disabled.

V_{IN} (Pin 5): Main Supply Pin and the (+) Input to the Current Comparator. Must be closely decoupled to ground.

Pin Limit Table

PIN	NAME	DESCRIPTION	NOMINAL (V) MIN	NOMINAL (V) TYP	NOMINAL (V) MAX	ABSOLUTE MAX (V) MIN	ABSOLUTE MAX (V) MAX
1	SW	Switch Node	–0.3		V_{IN}	V_{IN} – 8.5	V_{IN} + 0.3
2	GND	Ground Pin		0			
3	V_{FB}	Output Feedback Pin	0	1.25	1.35	–0.3	3
4	I_{TH}/RUN	Error Amplifier Compensation and RUN Pin	0		2.25	–0.3	3
5	V_{IN}	Main Power Supply	2.5		5.5	–0.3	6

BLOCK DIAGRAM



OPERATION

The LTC1701 uses a contant off-time, current mode architecture. The operating frequency is then determined by the off-time and the difference between V_{IN} and V_{OUT}.

The output voltage is set by an external divider returned to the V_{FB} pin. An error amplfier compares the divided output voltage with a reference voltage of 1.25V and adjusts the peak inductor current accordingly.

Main Control Loop

During normal operation, the internal PMOS switch is turned on when the V_{FB} voltage is below the reference voltage. The current into the inductor and the load increases until the current limit is reached. The switch turns off and energy stored in the inductor flows through the external Schottky diode into the load. After the constant off-time interval, the switch turns on and the cycle repeats.

The peak inductor current is controlled by the voltage on the I_{TH}/RUN pin, which is the output of the error amplifier. This amplifier compares the V_{FB} pin to the 1.25V reference. When the load current increases, the FB voltage decreases slightly below the reference. This decrease causes the error amplifier to increase the I_{TH}/RUN voltage until the average inductor current matches the new load current.

The main control loop is shut down by pulling the I_{TH}/RUN pin to ground. When the pin is released an external resistor is used to charge the compensation capacitor. When the voltage at the I_{TH}/RUN pin reaches 0.8V, the main control loop is enabled and the error amplifier drives the I_{TH}/RUN pin. Soft-start can be implemented by ramping the voltage on the I_{TH}/RUN pin (see Applications Information section).

Low Current Operation

To optimize efficiency when the load is relatively light, the LTC1701 automatically switches to Burst Mode operation in which the internal PMOS switch operates intermittently based on load demand. The main control loop is interrupted when the output voltage reaches the desired regulated value. The hysteretic voltage comparator trips when I_{TH}/RUN is below 1.5V, shutting off the switch and reducing the power consumed. The output capacitor and the inductor supply the power to the load until the output voltage drops slightly and the I_{TH}/RUN pin exceeds 1.5V, turning on the switch and the main control loop which starts another cycle.

For reduced output ripple, the LTC1701B doesn't use Burst Mode operation and operates continuously down to very low currents where the part starts skipping cycles.

Dropout Operation

In dropout, the internal PMOS switch is turned on continuously (100% duty cycle) providing low dropout operation with V_{OUT} at V_{IN}. Since the LTC1701 does not incorporate an under voltage lockout, care should be taken to shut down the LTC1701 for $V_{IN} < 2.5V$.

APPLICATIONS INFORMATION

The basic LTC1701 application circuit is shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of L1. Once L1 is chosen, the Schottky diode D1 can be selected followed by C_{IN} and C_{OUT}.

L Selection and Operating Frequency

The operating frequency is fixed by V_{IN}, V_{OUT} and the constant off-time of about 500ns. The complete expression for operating frequency is given by:

$$f_O = \left(\frac{V_{IN} - V_{OUT}}{V_{IN} + V_D}\right)\left(\frac{1}{T_{OFF}}\right)$$

Although the inductor does not influence the operating frequency, the inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance and increases with higher V_{IN} or V_{OUT}:

$$\Delta I_L = \left(\frac{V_{IN} - V_{OUT}}{fL}\right)\left(\frac{V_{OUT} + V_D}{V_{IN} + V_D}\right)$$

where V_D is the output Schottky diode forward drop.

APPLICATIONS INFORMATION

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is ΔI_L = 0.4A.

The inductor value also has an effect on low current operation. Lower inductor values (higher ΔI_L) will cause Burst Mode operation to begin at higher load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

Inductor Core Selection

Once the value for L is selected, the type of inductor must be chosen. Basically, there are two kinds of losses in an inductor —core and copper losses.

Core losses are dependent on the peak-to-peak ripple current and core material. However, it is independent of the physical size of the core. By increasing inductance, the peak-to-peak inductor ripple current will decrease, therefore reducing core loss. Unfortunately, increased inductance requires more turns of wire and, therefore, copper losses will increase.

High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. Ferrite designs have very low core loss and are preferred at high switching frequencies. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ core material. Toroids are very space efficient, expecially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, surface mount designs that do not increase the height significantly are available

Catch Diode Selection

The diode D1 shown in Figure 1 conducts during the off-time. It is important to adequately specify the diode peak current and average power dissipation so as not to exceed the diode ratings.

Losses in the catch diode depend on forward drop and switching times. Therefore, Schottky diodes are a good choice for low drop and fast switching times.

Since the catch diode carries the load current during the off-time, the average diode current is dependent on the switch duty cycle. At high input voltages, the diode conducts most of the time. As V_{IN} approaches V_{OUT}, the diode conducts only a small fraction of the time. The most stressful condition for the diode is when the regulator output is shorted to ground.

Under short-circuit conditions (V_{OUT} = 0V), the diode must safely handle $I_{SC(PK)}$ at close to 100% duty cycle. Under normal load conditions, the average current conducted by the diode is simply:

$$I_{DIODE(avg)} = I_{LOAD(avg)}\left(\frac{V_{IN} - V_{OUT}}{V_{IN} + V_D}\right)$$

Remember to keep lead lengths short and observe proper grounding (see Board Layout Considerations) to avoid ringing and increased dissipation.

The forward voltage drop allowed in the diode is calculated from the maximum short-circuit current as:

$$V_D \approx \left(\frac{P_D}{I_{SC(avg)}}\right)\left(\frac{V_{IN} + V_D}{V_{IN}}\right)$$

where P_D is the allowable diode power dissipation and will be determined by efficiency and/or thermal requirements (see Efficiency Considerations).

Most LTC1701 circuits will be well served by either an MBR0520L or an MBRM120L. An MBR0520L is a good choice for $I_{OUT(MAX)} \leq$ 500mA, as long as the output doesn't need to sustain a continuous short.

Kool Mμ is a registered trademark of Magnetics, Inc.

APPLICATIONS INFORMATION

Input Capacitor (C_{IN}) Selection

In continuous mode, the input current of the converter is a square wave with a duty cycle of approximately V_{OUT}/V_{IN}. To prevent large voltage transients, a low equivalent series resistance (ESR) input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{MAX} \frac{\sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)}}{V_{IN}}$$

where the maximum average output current I_{MAX} equals the peak current (1 Amp) minus half the peak-to-peak ripple current, $I_{MAX} = 1 - \Delta I_L/2$.

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case is commonly used to design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours lifetime. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. An additional 0.1µF to 1µF ceramic capacitor is also recommended on V_{IN} for high frequency decoupling.

Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is driven by the required ESR. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. With $\Delta I_L = 0.4\ I_{OUT(MAX)}$ the output ripple will be less than 100mV with:

$$ESR_{COUT} < 100m\Omega$$

Once the ESR requirements for C_{OUT} have been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

When the capacitance of C_{OUT} is made too small, the output ripple at low frequencies will be large enough to trip the I_{TH} comparator. This causes Burst Mode operation to be activated when the LTC1701 would normally be in continuous mode operation. The effect can be improved at higher frequencies with lower inductor values.

In surface mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirement of the application. Aluminum electrolyte and dry tantulum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS, AVX TPSV and KEMET T510 series of surface mount tantalums, avalable in case heights ranging from 2mm to 4mm. Other capacitor types include Nichicon PL series, Sanyo POSCAP and Panasonic SP.

Ceramic Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. These are tempting for switching regulator use because of their very low ESR. Unfortunately, the ESR is so low that it can cause loop stability problems. Solid tantalum capacitor ESR generates a loop "zero" at 5kHz to 50kHz that is instrumental in giving acceptable loop phase margin. Ceramic capacitors remain capacitive to beyond 300kHz and usually resonate with their ESL before ESR becomes effective. Also, ceramic caps are prone to temperature effects which requires the designer to check loop stability over the operating temperature range.

For these reasons, most of the input and output capacitance should be composed of tantalum capacitors for stability combined with about 0.1µF to 1µF of ceramic capacitors for high frequency decoupling. Great care must be taken when using only ceramic input and output capacitors. The OPTI-LOOP compensation allows transient response to be optimized for all types of output capacitors, including low ESR ceramics.

Setting the Output Voltage

The LTC1701 develops a 1.25V reference voltage between the feedback pin, V_{FB}, and the signal ground as shown in

APPLICATIONS INFORMATION

Figure 2. The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 1.25V(1 + R2/R1)$$

To prevent stray pickup, a capacitor of about 5pF can be added across R1, located close to the LTC1701. Unfortunately, the load step response is degraded by this capacitor. Using a good printed circuit board layout eliminates the need for this capacitor. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

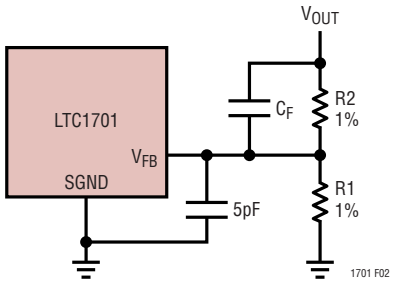


Figure 2. Setting the Output Voltage

Transient Response

The OPTI-LOOP compensation allows the transient response to be optimized for a wide range of loads and output capacitors. The availability of the I_{TH} pin not only allows optimization of the control loop behavior but also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominately second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin.

The I_{TH} external components shown in the Figure 1 circuit will provide an adequate starting point for most applications. The series R3-C3 filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop feedback factor gain and phrase. An output current pulse of 20% to 100% of full-load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second-order overshoot/DC ratio cannot be used to determine phase margin. The gain of the loop increases with R3 and the bandwidth of the loop increases with decreasing C3. If R3 is increased by the same factor that C3 is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. In addition, a feed-forward capacitor, C_F, can be added to improve the high frequency response, as shown in Figure 2. Capacitor C_F provides phase lead by creating a high frequency zero with R2 which improves the phase margin.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

RUN Function

The I_{TH}/RUN pin is a dual purpose pin that provides the loop compensation and a means to shut down the LTC1701. Soft-start can also be implemented with this pin. Soft-start reduces surge currents from V_{IN} by gradually increasing the internal peak inductor current. Power supply sequencing can also be accomplished using this pin.

An external pull-up is required to charge the external capacitor C3 in Figure 1. Typically, a 1M resistor between V_{IN} and I_{TH}/RUN is used. When the voltage on I_{TH}/RUN reaches about 0.8V the LTC1701 begins operating. At this point the error amplifier pulls up the I_{TH}/RUN pin to the normal operating range of 1.25V to 2.25V.

Soft-start can be implemented by ramping the voltage on I_{TH}/RUN during start-up as shown in Figure 3(b). As the voltage on I_{TH}/RUN ramps through its operating range the internal peak current limit is also ramped at a proportional linear rate.

APPLICATIONS INFORMATION

During normal operation the voltage on the I_{TH}/RUN pin will vary from 1.25V to 2.25V depending on the load current. Pulling the I_{TH}/RUN pin below 0.8V puts the LTC1701 into a low quiescent current shutdown mode (I_Q < 1μA). This pin can be driven directly from logic as shown in Figures 3(a).

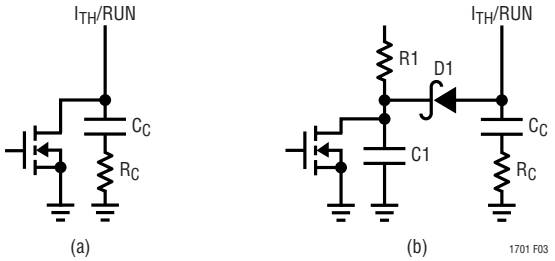


Figure 3. I_{TH}/RUN Pin Interfacing

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and what change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, 4 main sources usually account for most of the losses in LTC1701 circuits: 1) LTC1701 V_{IN} current, 2) switching losses, 3) I^2R losses, 4) Schottky diode losses.

1) The V_{IN} current is the DC supply current given in the electrical characteristics which excludes MOSFET driver and control currents. V_{IN} current results in a small (<0.1%) loss that increases with V_{IN}, even at no load.

2) The switching current is the sum of the internal MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFET. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f \bullet Q_P$, where Q_P is the gate charge of the internal MOSFET switch.

3) I^2R Losses are predicted from the DC resistances of the MOSFET and inductor. In continuous mode the average output current flows through L, but is "chopped" between the topside internal MOSFET and the Schottky diode. At low supply voltages where the switch on-resistance is higher and the switch is on for longer periods due to the higher duty cycle, the switch losses will dominate. Using a larger inductance helps minimize these switch losses. At high supply voltages, these losses are proportional to the load. I^2R losses cause the efficiency to drop at high output currents.

4) The Schottky diode is a major source of power loss at high currents and gets worse at low output voltages. The diode loss is calculated by multiplying the forward voltage drop times the diode duty cycle multiplied by the load current.

Other "hidden" losses such as copper trace and internal battery resistances can account for additional efficiency degradations in portable systems. It is very important to include these "system" level losses in the design of a system. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. Other losses including Schottky conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

THERMAL CONSIDERATIONS

The power handling capability of the device at high ambient temperatures will be limited by the maximum rated junction temperature (125°C). It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

APPLICATIONS INFORMATION

The following table lists thermal resistance for several different board sizes and copper areas. All measurements were taken in still air on 3/32" FR-4 board with one ounce copper.

Table 1. Measured Thermal Resistance

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	θ_{JA}
2500mm^2	2500mm^2	2500mm^2	125°C/W
1000mm^2	2500mm^2	2500mm^2	125°C/W
225mm^2	2500mm^2	2500mm^2	130°C/W
100mm^2	2500mm^2	2500mm^2	135°C/W
50mm^2	2500mm^2	2500mm^2	150°C/W

*Device is mounted on topside.

Calculating Junction Temperature

In a majority of applications, the LTC1701 does not dissipate much heat due to its high efficiency. However, in applications where the switching regulator is running at high duty cycles or the part is in dropout with the switch turned on continuously (DC), some thermal analysis is required. The goal of the thermal analysis is to determine whether the power dissipated by the regulator exceeds the maximum junction temperature. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature is given by:

$$T_J = T_{RISE} + T_{AMBIENT}$$

As an example, consider the case when the LTC1701 is in dropout at an input voltage of 3.3V with a load current of 0.5A. The ON resistance of the P-channel switch is approximately 0.30Ω. Therefore, power dissipated by the part is:

$$P_D = I^2 \bullet R_{DS(ON)} = 75mW$$

The SOT package junction-to-ambient thermal resistance, θ_{JA}, will be in the range of 125°C/W to 150°C/W. Therefore, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately:

$$T_J = 0.075 \bullet 150 + 25 = 36°C$$

Remembering that the above junction temperature is obtained from a $R_{DS(ON)}$ at 25°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. However, we can safely assume that the actual junction temperature will not exceed the absolute maximum junction temperature of 125°C.

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1701. These items are also illustrated graphically in the layout diagram of Figure 4. Check the following in your layout:

1. Does the capacitor C_{IN} connect to the power V_{IN} (Pin 5) and GND (Pin 2) as close as possible? This capacitor provides the AC current to the internal P-channel MOSFET and its driver.

2. Is the Schottky diode closely connected between the ground (Pin 2) and switch output (Pin 1)?

3. Are the C_{OUT}, L1 and D1 closely connected? The Schottky anode should connect directly to the input capacitor ground.

4. The resistor divider, R1 and R2, must be connected between the (+) plate of C_{OUT} and a ground line terminated near GND (Pin 2). The feedback signal FB should be routed away from noisy components and traces, such as the SW line (Pin 1).

5. Keep sensitive components away from the SW pin. The input capacitor C_{IN}, the compensation capacitor C_C and all the resistors R1, R2, R_C and R_S should be routed away from the SW trace and the components L1 and D1.

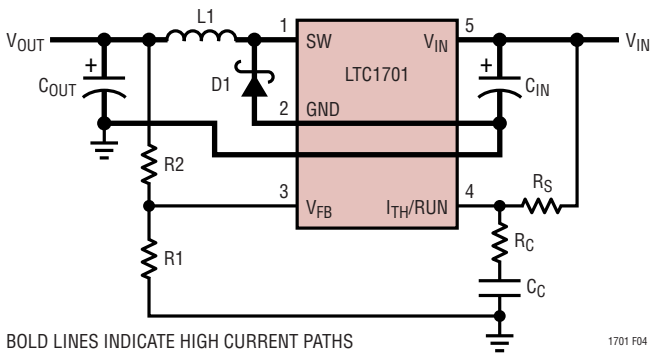
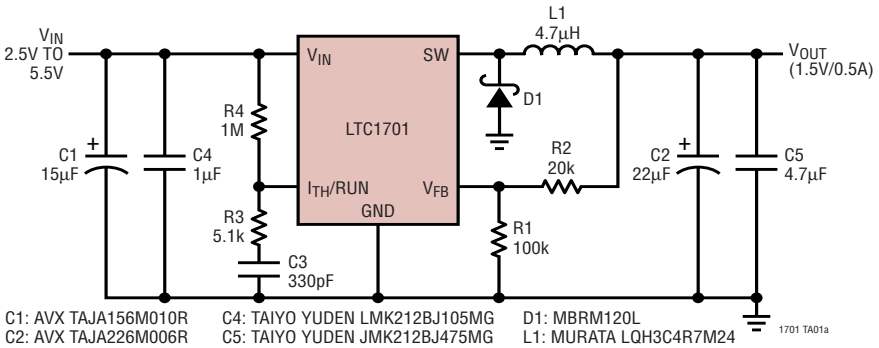


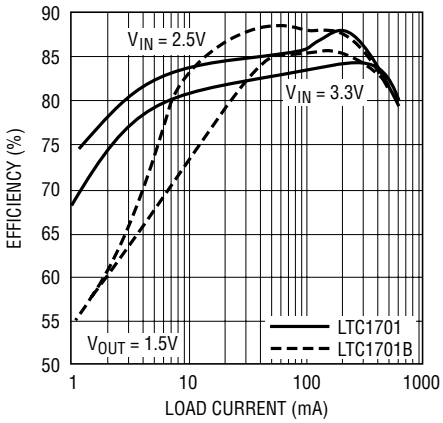
Figure 4. LTC1701 Layout Diagram (See Board Layout Checklist)

TYPICAL APPLICATIONS

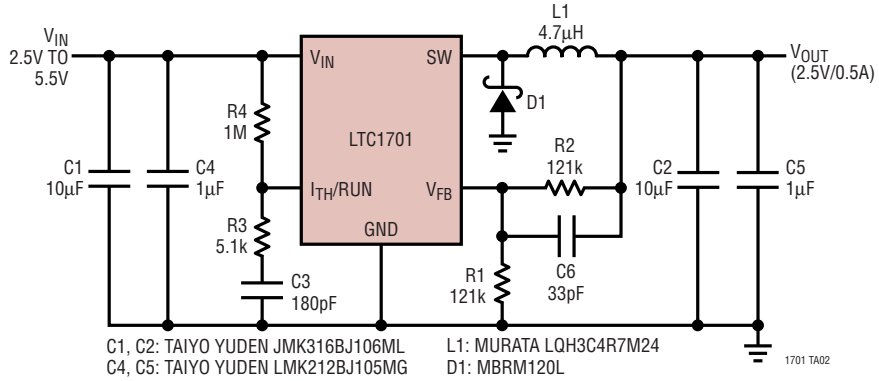
2mm Nominal Height 1.5V Converter



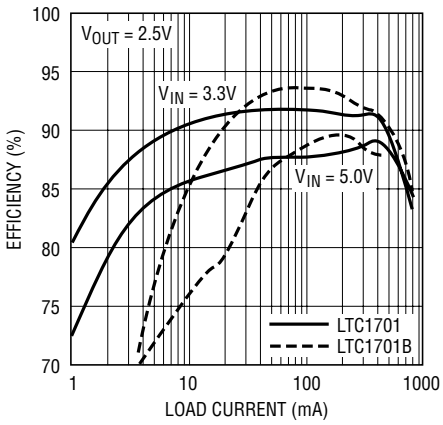
Efficiency Curve



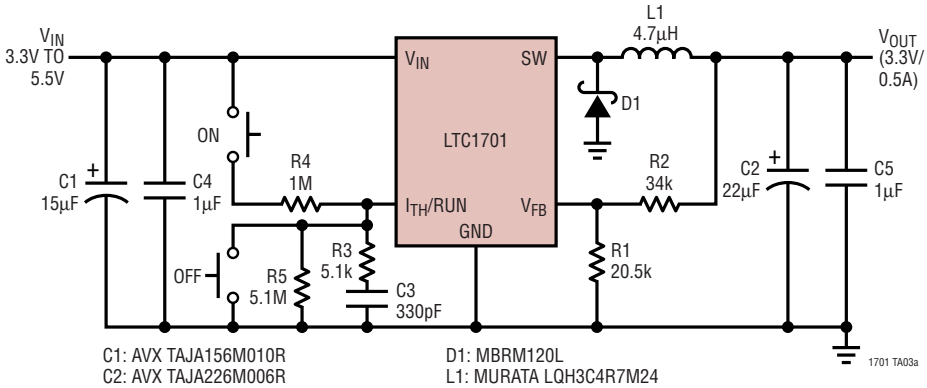
All Ceramic Capacitor 2.5V Converter



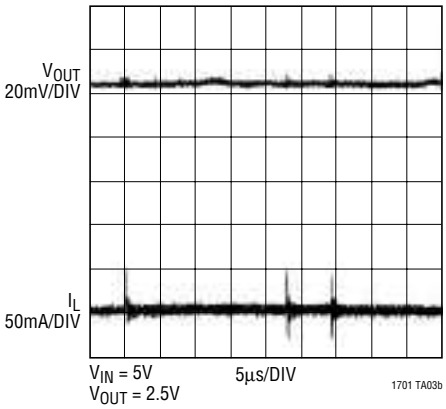
Efficiency Curve



5V to 3.3V Converter with Push-Button On/Off

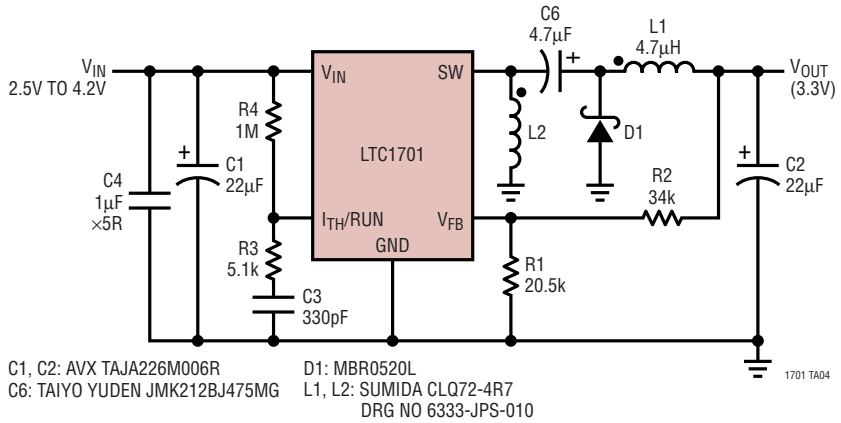


LTC1701B Low Current Pulse Skip



TYPICAL APPLICATION

Single Cell Li-Ion to 3.3V Zeta Converter



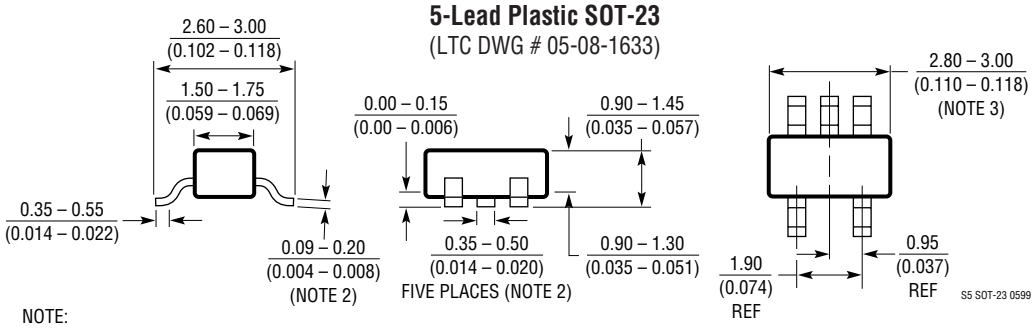
V_{IN}	$I_{OUT(MAX)}$
2.5V	200mA
3.0V	225mA
3.5V	250mA
4.0V	280mA
4.2V	290mA

C1, C2: AVX TAJA226M006R
C6: TAIYO YUDEN JMK212BJ475MG
D1: MBR0520L
L1, L2: SUMIDA CLQ72-4R7
DRG NO 6333-JPS-010

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S5 Package
5-Lead Plastic SOT-23
(LTC DWG # 05-08-1633)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS ARE INCLUSIVE OF PLATING
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
4. MOLD FLASH SHALL NOT EXCEED 0.254mm
5. PACKAGE EIAJ REFERENCE IS SC-74A (EIAJ)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1174/LTC1174-3.3/ LTC1174-5	High Efficiency Step-Down and Inverting DC/DC Converters	Monolithic Switching Regulator, Burst Mode Operation, I_{OUT} Up to 300mA, SO-8
LTC1265	1.2A, High Efficiency Step-Down DC/DC Converter	Monolithic, Burst Mode Operation, High Efficiency
LT1375/LT1376	1.5A, 500kHz Step-Down Switching Regulators	High Frequency, Small Inductor, High Efficiency, SO-8
LTC1474/LTC1475	Low Quiescent Current High Efficiency Step-Down Converters	10µA I_Q, 8-Pin MSOP and SO Packages
LTC1622	Low Input Voltage Current Mode Step-Down DC/DC Controller	High Frequency, High Efficiency, 8-Pin MSOP
LTC1627	Monolithic Synchronous Step-Down Switching Regulator	SO-8, 2.65V ≤ V_{IN} ≤ 10V, I_{OUT} Up to 500mA
LTC1707	Monolithic Synchronous Step-Down Switching Regulator	SO-8, 2.95V ≤ V_{IN} ≤ 10V, V_{REF} Output
LTC1771	Low Quiescent Current, High Efficiency Step-Down Controller	10µA I_Q, 8-Pin MSOP and SO Packages
LTC1772	Low Input Voltage Current Mode Step-Down DC/DC Controller	550kHz, 6-Pin SOT-23, I_{OUT} Up to 5A, 2.2V < V_{IN} < 10V
LTC1877/LTC1878	High Efficiency, Monolithic Synchronous Step-Down Regulators	10µA I_Q, 2.65 ≤ V_{IN} ≤ 10V, MSOP Package, up to 600mA
LTC3404	1.4MHz High Efficiency Monolithic Synchronous Step-Down Reg	95% Efficiency, 10µA I_Q, MSOP Package, up to 600mA

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