

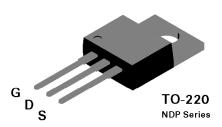
NDP6060L / NDB6060L N-Channel Logic Level Enhancement Mode Field Effect Transistor

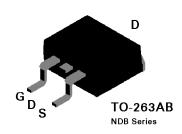
General Description

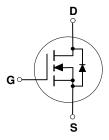
These logic level N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- $\blacksquare \quad \text{48A, 60V. } \mathsf{R}_{\mathsf{DS}(\mathsf{ON})} = 0.025\Omega \ \textcircled{0} \ \mathsf{V}_{\mathsf{GS}} = \mathsf{5V}.$
- Low drive requirements allowing operation directly from logic drivers. V_{GS(TH)} < 2.0V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175 °C maximum junction temperature rating.
- High density cell design for extremely low R_{DS(ON)}.
- TO-220 and TO-263 (D²PAK) package for both through hole and surface mount applications.







Absolute Maximum Ratings

T_C = 25 ℃ unless otherwise noted

Symbol	Parameter	NDP6060L	NDB6060L	Units			
V _{DSS}	Drain-Source Voltage	60	V				
V_{DGR}	Drain-Gate Voltage ($R_{GS} \le 1 M\Omega$)	60	V				
V_{GSS}	Gate-Source Voltage - Continuous	±16					
	- Nonrepetitive (t _P < 50 μs)	±25					
I _D	Drain Current - Continuous	48					
	- Pulsed	144					
P_{D}	Total Power Dissipation @ T _C = 25 ℃	er Dissipation @ $T_C = 25$ °C 100					
	Derate above 25 ℃	0.67					
T_J, T_{STG}	Operating and Storage Temperature	-65 to 175	∞				
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		€			

Symbol	Parameter	Conditions	Min	Тур	Max	Units	
DRAIN-S	OURCE AVALANCHE RATINGS (Note 1)				•		
W _{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 25 \text{ V}, I_{D} = 48 \text{ A}$				200	mJ
I _{AR}	Maximum Drain-Source Avalanche Cur	rent			48	Α	
OFF CH	ARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	60			V	
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$				250	μΑ
			T _J = 125℃			1	mA
I _{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 16 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -16 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
ON CHAP	RACTERISTICS (Note 1)				•		
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		1		2	V
			T _J = 125℃	0.65		1.5	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = 5 \text{ V}, I_D = 24 \text{ A}$	<u>.</u>			0.025	Ω
			T _J = 125℃			0.04	
		$V_{GS} = 10 \text{ V}, I_{D} = 24 \text{ A}$	<u>.</u>			0.02	•
I _{D(on)}	On-State Drain Current	$V_{GS} = 5 \text{ V}, V_{DS} = 10 \text{ V}$		48			Α
g _{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_{D} = 24 \text{ A}$		10			S
DYNAMIC	CHARACTERISTICS						
C _{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, \ V_{GS} = 0 \text{ V}, $ f = 1.0 MHz			1630	2000	pF
C _{oss}	Output Capacitance	f = 1.0 MHz	f = 1.0 MHz		460	800	pF
C _{rss}	Reverse Transfer Capacitance				150	400	pF
	NG CHARACTERISTICS (Note 1)					•	
t _{D(on)}	Turn - On Delay Time	$V_{DD} = 30 \text{ V}, I_{D} = 48 \text{ A},$			15	30	nS
t _r	Turn - On Rise Time	$V_{GS} = 5 \text{ V}, R_{GEN} = 15 \Omega,$		320	500	nS	
t _{D(off)}	Turn - Off Delay Time	$R_{GS} = 15 \Omega$		49	100	nS	
t _f	Turn - Off Fall Time				161	300	nS
Q _g	Total Gate Charge	V _{DS} = 48 V,			36	60	nC
$\overline{Q_{gs}}$	Gate-Source Charge	$I_D = 48 \text{ A}, V_{GS} = 5 \text{ V}$			8.2		nC
Q _{gd}	Gate-Drain Charge	1		21		nC	

Symbol	Parameter	Conditions		Min	Тур	Max	Units
DRAIN-S	OURCE DIODE CHARACTERISTICS						
l _s	Maximum Continuos Drain-Source Diode			48	Α		
I _{SM}	Maximum Pulsed Drain-Source Diode Fo			144	Α		
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 24 A (Note 1)			1.3	V	
			T _J = 125℃			1.2	
t _{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{F} = 48 \text{ A},$ $dI_{F}/dt = 100 \text{ A/}\mu\text{s}$		35	75	140	ns
l _m	Reverse Recovery Current	$di_{F}/dt = 100 A/\mu S$		2	3.6	8	Α
THERMA	L CHARACTERISTICS						
R _{eJC}	Thermal Resistance, Junction-to-Case			1.5	%/W		
R _{øJA}	Thermal Resistance, Junction-to-Ambier			62.5	℃/W		

Note: 1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

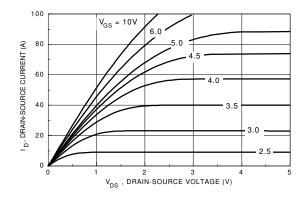


Figure 1. On-Region Characteristics.

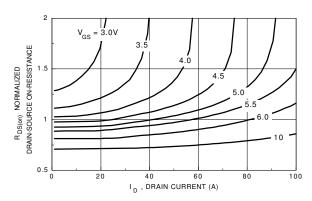


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

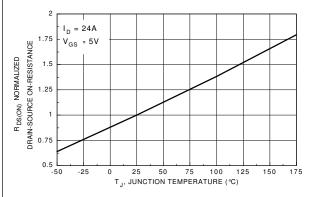


Figure 3. On-Resistance Variation with Temperature.

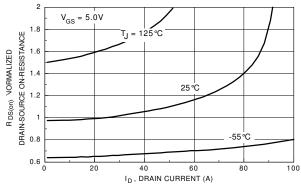


Figure 4. On-Resistance Variation with Drain Current and Temperature.

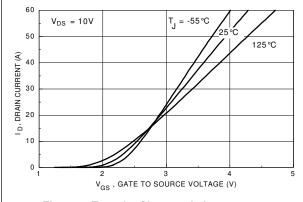


Figure 5. Transfer Characteristics.

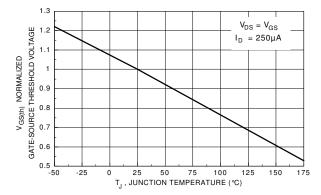


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

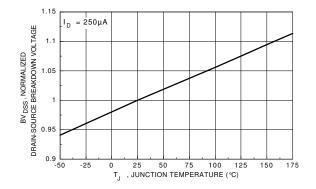


Figure 7. Breakdown Voltage Variation with Temperature.

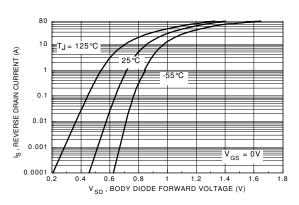


Figure 8. Body Diode Forward Voltage
Variation with Current and Temperature.

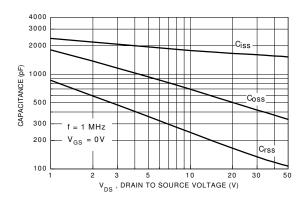


Figure 9. Capacitance Characteristics.

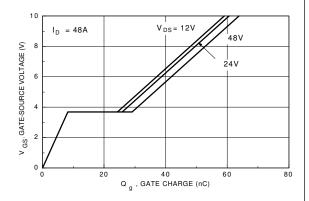


Figure 10. Gate Charge Characteristics.

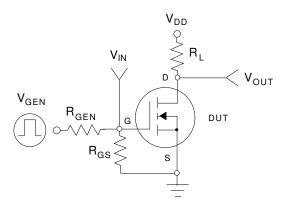


Figure 11. Switching Test Circuit.

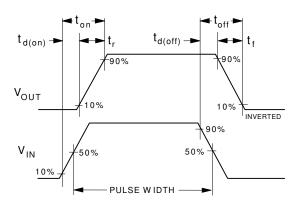
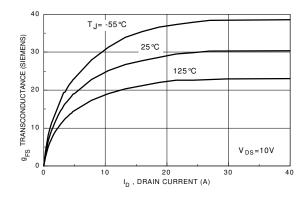


Figure 12. Switching Waveforms.

Typical Electrical Characteristics (continued)



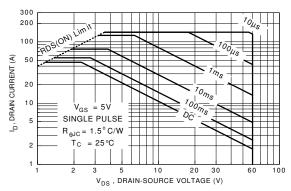


Figure 13. Transconductance Variation with Drain Current. and Temperature

Figure 14. Maximum Safe Operating. Area

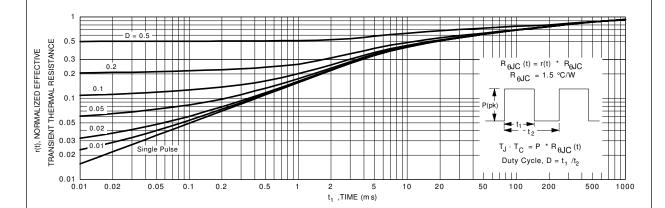
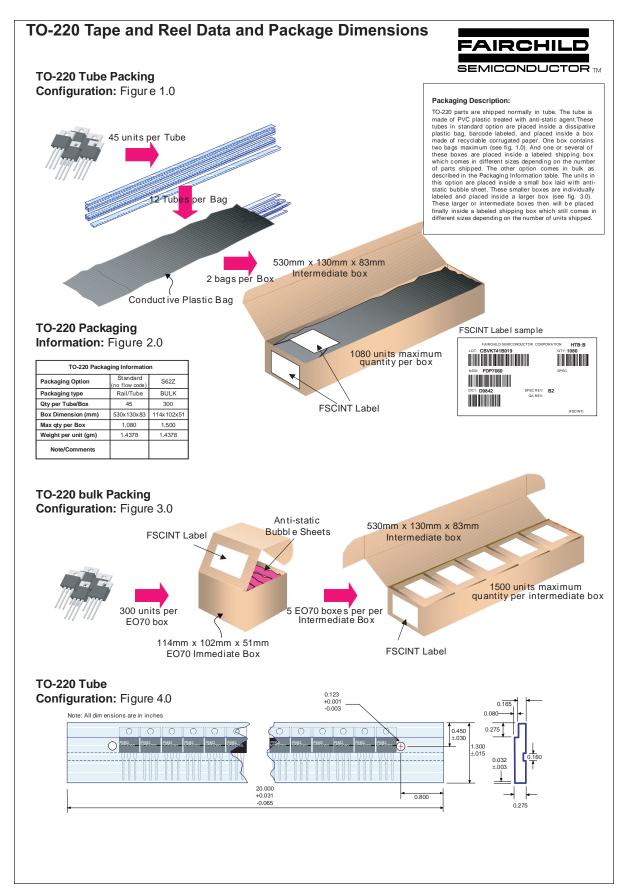
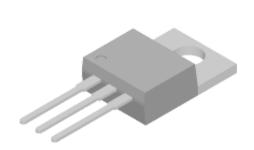


Figure 15. Transient Thermal Response Curve.

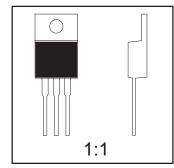


TO-220 Tape and Reel Data and Package Dimensions, continued

TO-220 (FS PKG Code 37)

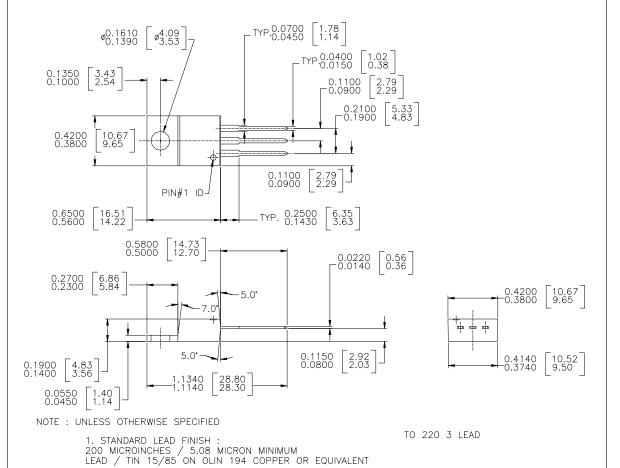


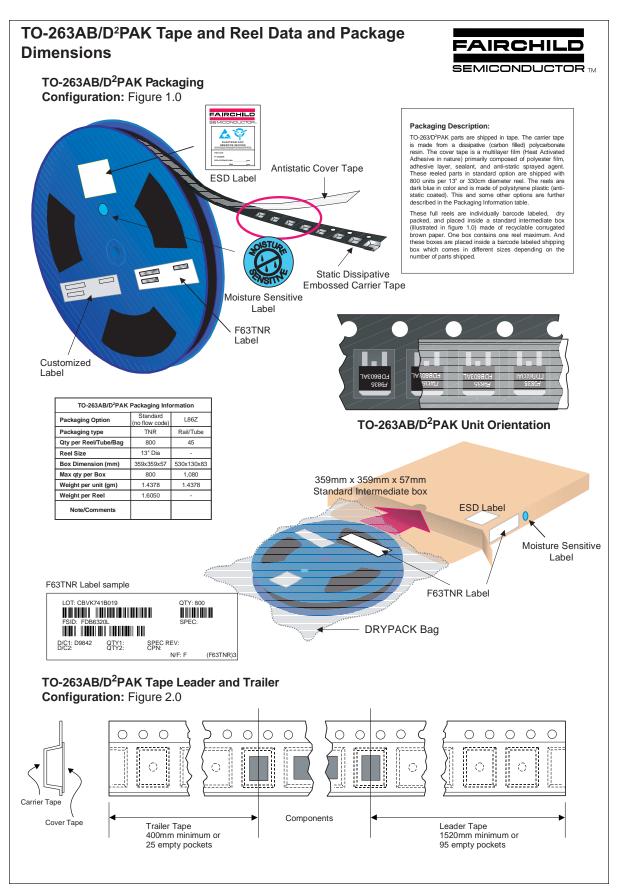
2. DIMENSION BASED ON JEDEC STANDARD TO-220 VARIATION AB, ISSUE J, DATED 3/24/87



Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

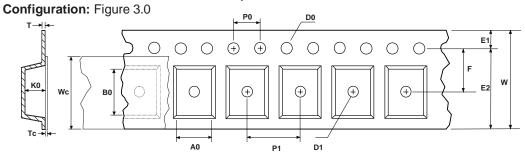
Part Weight per unit (gram): 1.4378





TO-263AB/D²PAK Tape and Reel Data and Package Dimensions, continued

TO-263AB/D²PAK Embossed Carrier Tape



User Direction of Feed

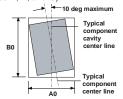
Dimensions are in millimeter														
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	Т	Wc	Тс
TO263AB/ D ² PAK (24mm)	10.60 +/-0.10	15.80 +/-0.10	24.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	22.25 min	11.50 +/-0.10	16.0 +/-0.1	4.0 +/-0.1	4.90 +/-0.10	0.450 +/-0.150	21.0 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)

Component Rotation



Sketch B (Top View)
Component Rotation

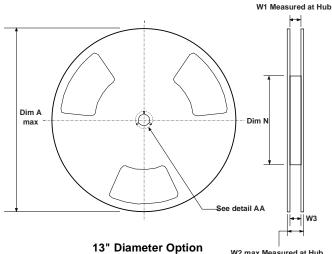


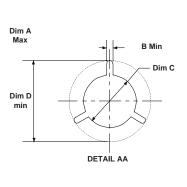
Sketch C (Top View)

Component lateral movement

TO-263AB/D²PAK Reel Configuration: Figure 4.0







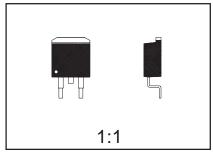
W2 max Measured at Hub

Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
24mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.961 +0.078/-0.000 24.4 +2/0	1.197 30.4	0.941 - 0.1.079 23.9 - 27.4

TO-263AB/D²PAK Tape and Reel Data and Package Dimensions, continued

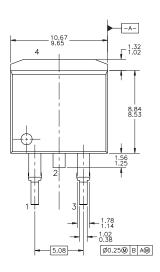
TO-263AB/D²PAK (FS PKG Code 45)

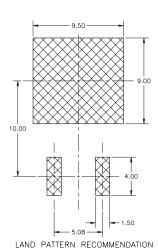


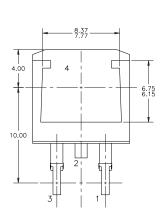


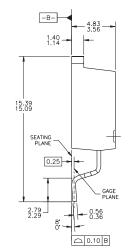
Scale 1:1 on letter size paper Dimensions shown below are in: inches [millimeters]

Part Weight per unit (gram): 1.4378









- NOTES: UNLESS OTHERWISE SPECIFIED

 A) ALL DIMENSIONS ARE IN MILLIMETERS.
 B) STANDARD LEAD FINISH:
 200 MICROINCHES / 5.08 MICROMETERS MIN.
 LEAD/TIN 15/85 ON OLIN 194 COPPER OR
 EQUIVALENT.
 C) MAXIMUM YERTICAL BURR ON HEATSINK NOT
 TO EXCEED 0.003 INCH / 0.05mm.
 D) NO PACKAGE CHIPS, CRACKS OR SURFACE
 IDENTIFICATION ALLOWED AFTER FORMING.
 E) REFERENCE JEDEC, TO—263, ISSUE C,
 VARIATION AB, DATED 2/92.

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FACT $^{\text{TM}}$ QFET $^{\text{TM}}$ FACT Quiet Series $^{\text{TM}}$ QS $^{\text{TM}}$

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.