**FAIRCHILD**

SEMICONDUCTOR ™

NDP6030PL / NDB6030PL
P-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

These P-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as DC/DC converters and high efficiency switching circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -30 A, -30 V. $R_{DS(ON)}$ = 0.042 Ω @ V_{GS}= -4.5 V
  $R_{DS(ON)}$ = 0.025 Ω @ V_{GS}= -10 V.

- Critical DC electrical parameters specified at elevated temperature.

- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.

- High density cell design for extremely low $R_{DS(ON)}$.

- 175°C maximum junction temperature rating.

TO-220
NDP Series

TO-263AB
NDB Series
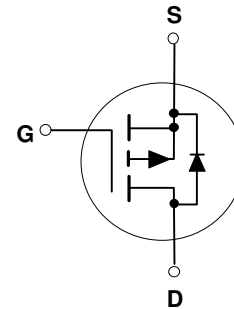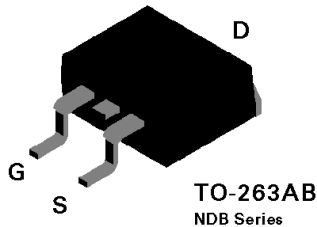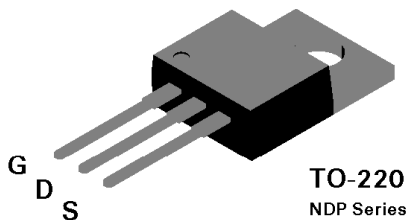
Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP6030PL	NDB6030PL	Units
V_{DSS}	Drain-Source Voltage	-30		V
V_{GSS}	Gate-Source Voltage - Continuous	±16		V
I_D	Drain Current - Continuous	-30		A
	- Pulsed	-90		
P_D	Total Power Dissipation @ T_C = 25°C	75		W
	Derate above 25°C	0.5		
T_J, T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C
T_J, T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
THERMAL CHARACTERISTICS				
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5		°C/W

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA		-30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = -250 µA, Referenced to 25°C			-36		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V				-250	µA
			T_J = 125°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 16 V, V_{DS} = 0 V				-100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -16 V, V_{DS} = 0 V				-100	nA
ON CHARACTERISTICS (Note)							
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	I_D = -250 µA, Referenced to 25°C			2.2		mV/°C
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D= -250 µA		-1	-1.4	-2	V
			T_J = 125°C	-0.8	-1.08	-1.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -15 A			0.037	0.042	Ω
			T_J = 125°C		0.053	0.075	
		V_{GS} = -10 V, I_D = -19 A			0.021	0.025	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V		-20			A
g_{FS}	Forward Transconductance	V_{DS} = -4.5 V, I_D = -19 A			20		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz			1570		pF
C_{oss}	Output Capacitance				975		pF
C_{rss}	Reverse Transfer Capacitance				360		pF
SWITCHING CHARACTERISTICS (Note)							
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -15 V, I_D = -5 A, V_{GS} = -5 V, R_{GEN} = 6 Ω			12.5	25	nS
t_r	Turn - On Rise Time				60	120	nS
$t_{D(off)}$	Turn - Off Delay Time				50	100	nS
t_f	Turn - Off Fall Time				52	100	nS
Q_g	Total Gate Charge	V_{DS} = -12 V, I_D = -30 A, V_{GS} = -5 V			26	36	nC
Q_{gs}	Gate-Source Charge				6.5		nC
Q_{gd}	Gate-Drain Charge				11.5		nC
DRAIN-SOURCE DIODE CHARACTERISTICS							
I_S	Maximum Continuos Drain-Source Diode Forward Current					-30	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current					-100	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -15 A (Note)			-0.92	-1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = -30 A, dI_F/dt = 100 A/µs			58		ns
I_{rr}	Reverse Recovery Current				-1.5		A

Note:
 Pulse Test: Pulse Width $\leq$ 300 µs, Duty Cycle $\leq$ 2.0%.
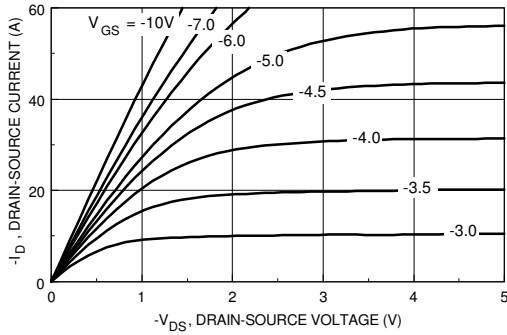
Typical Electrical Characteristics

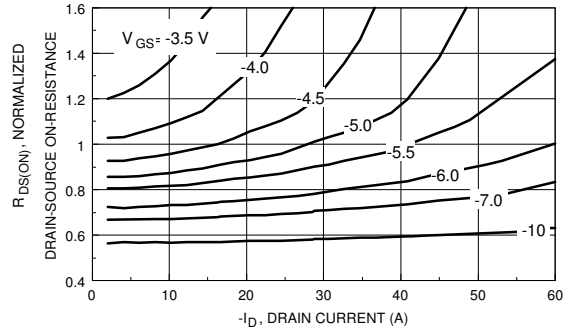Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation
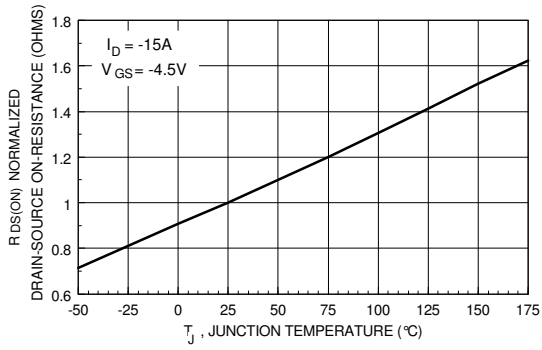with Drain Current and Gate Voltage.

Figure 3. On-Resistance Variation
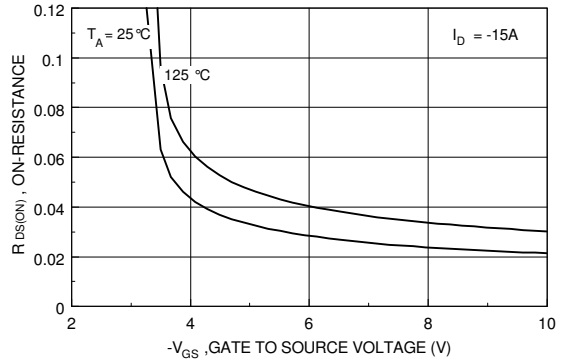with Temperature.

Figure 4. On Resistance Variation with
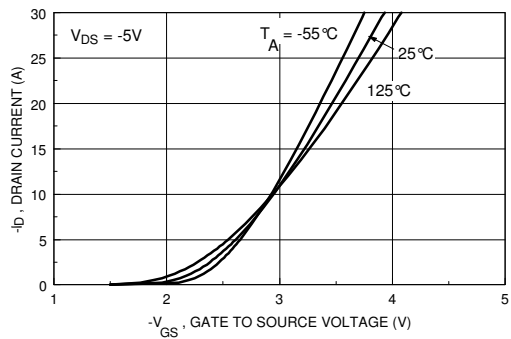Gate-To- Source Voltage.
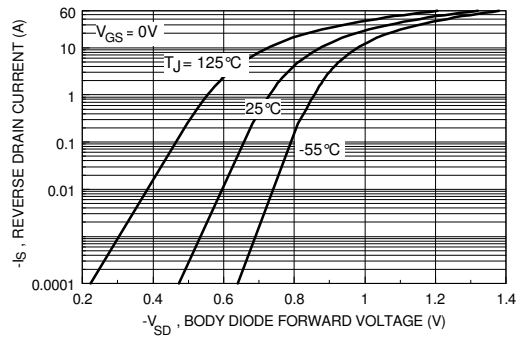

Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage
Variation with Source Current and
Temperature.

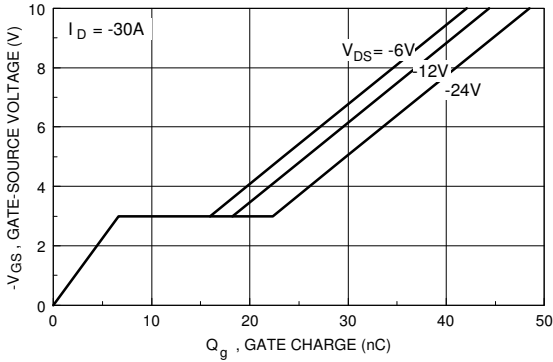# Typical Electrical Characteristics (continued)
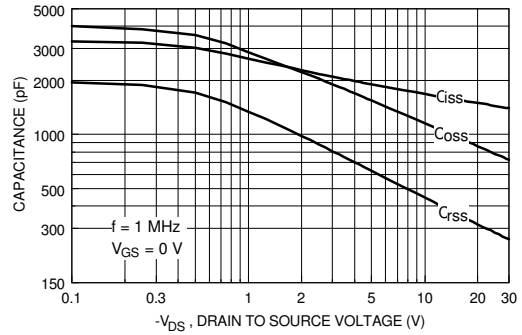

Figure 7. Gate Charge Characteristics.
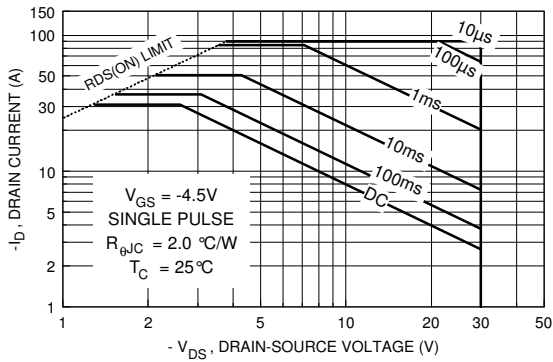

Figure 8. Capacitance Characteristics.

Figure 9. Maximum Safe Operating Area.

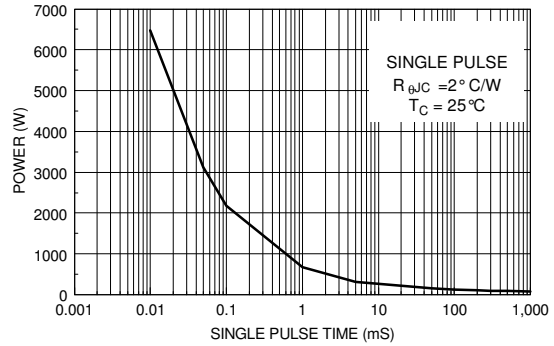Figure 10. Single Pulse Maximum Power Dissipation.

$$R_{\theta JC}(t) = r(t) * R_{\theta JC}$$
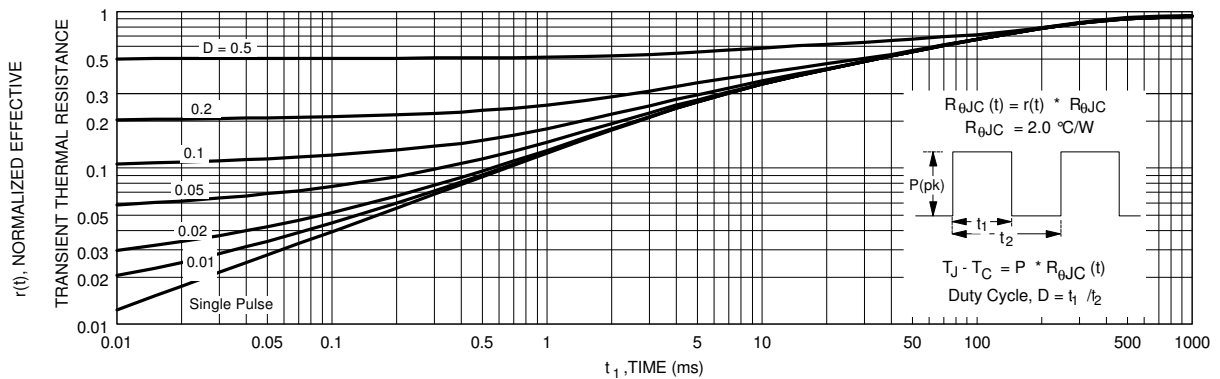$$R_{\theta JC} = 2.0 \; ^\circ C/W$$

$$T_J - T_C = P * R_{\theta JC}(t)$$
Duty Cycle, $D = t_1 / t_2$

Figure 11. Transient Thermal Response Curve.