

74AC244, 74ACT244

Octal Buffer/Line Driver with 3-STATE Outputs

Features

- I_{CC} and I_{OZ} reduced by 50%
- 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24mA
- ACT244 has TTL-compatible inputs

General Description

The AC/ACT244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver which provides improved PC board density.

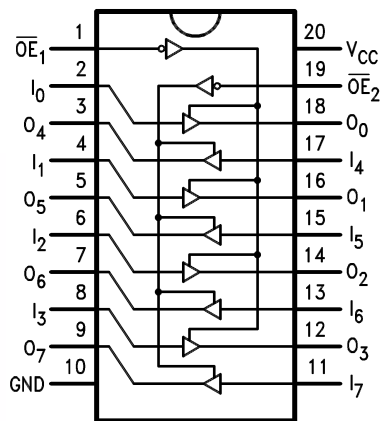
Ordering Information

Order Number	Package Number	Package Description
74AC244SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC244SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC244MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC244PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT244SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT244SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT244MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74ACT244MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT244PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

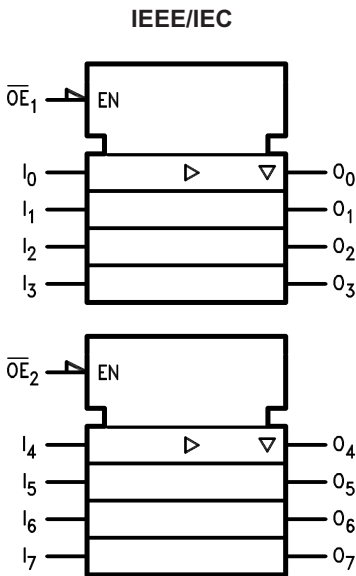
Connection Diagram



Pin Description

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs
I_0 – I_7	Inputs
O_0 – O_7	Outputs

Logic Symbol



Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_n	(Pins 12, 14, 16, 18)
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_n	(Pins 3, 5, 7, 9)
L	L	L
L	H	H
H	X	Z

X = Immaterial
Z = High Impedance

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
I_{IK}	DC Input Diode Current $V_I = -0.5V$	–20mA
	$V_I = V_{CC} + 0.5$	+20mA
V_I	DC Input Voltage	–0.5V to $V_{CC} + 0.5V$
I_{OK}	DC Output Diode Current $V_O = -0.5V$	–20mA
	$V_O = V_{CC} + 0.5V$	+20mA
V_O	DC Output Voltage	–0.5V to $V_{CC} + 0.5V$
I_O	DC Output Source or Sink Current	±50mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage AC	2.0V to 6.0V
	ACT	4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	–40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% of V_{CC} , V_{CC} @ 3.3V, 4.5V, 5.5V	125mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	125mV/ns

DC Electrical Characteristics for AC

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C		T _A = −55°C to +125°C	T _A = −40°C to +85°C	Units
				Typ.	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage	3.0	V _{OUT} = 0.1V or V _{CC} − 0.1V	1.5	2.1	2.1	2.1	V
		4.5		2.25	3.15	3.15	3.15	
		5.5		2.75	3.85	3.85	3.85	
V _{IL}	Maximum LOW Level Input Voltage	3.0	V _{OUT} = 0.1V or V _{CC} − 0.1V	1.5	0.9	0.9	0.9	V
		4.5		2.25	1.35	1.35	1.35	
		5.5		2.75	1.65	1.65	1.65	
V _{OH}	Minimum HIGH Level Output Voltage	3.0	I _{OUT} = −50μA	2.99	2.9	2.9	2.9	V
		4.5		4.49	4.4	4.4	4.4	
		5.5		5.49	5.4	5.4	5.4	
		3.0	V _{IN} = V _{IL} or V _{IH} , I _{OH} = 12mA		2.56	2.4	2.46	
		4.5	V _{IN} = V _{IL} or V _{IH} , I _{OH} = 24mA		3.86	3.7	3.76	
		5.5	V _{IN} = V _{IL} or V _{IH} , I _{OH} = 24mA ⁽¹⁾		4.86	4.7	4.76	
V _{OL}	Maximum LOW Level Output Voltage	3.0	I _{OUT} = 50μA	0.002	0.1	0.1	0.1	V
		4.5		0.001	0.1	0.1	0.1	
		5.5		0.001	0.1	0.1	0.1	
		3.0	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 12mA		0.36	0.50	0.44	
		4.5	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA		0.36	0.50	0.44	
		5.5	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ⁽¹⁾		0.36	0.50	0.44	
I _{IN} ⁽²⁾	Maximum Input Leakage Current	5.5	V _I = V _{CC} , GND		±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum 3-STATE Leakage Current	5.5	V _I (OE) = V _{IL} , V _{IH} ; V _I = V _{CC} , V _{GND} ; V _O = V _{CC} , GND		±0.25	±5.0	±2.5	μA
I _{OLD}	Minimum Dynamic Output Current ⁽³⁾	5.5	V _{OLD} = 1.65V Max.			50	75	mA
I _{OHD}		5.5	V _{OHD} = 3.85V Min.			−50	−75	mA
I _{CC} ⁽²⁾	Maximum Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND		4.0	80.0	40.0	μA

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
3. Maximum test duration 2.0ms, one output loaded at a time.

DC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C		T _A = -55°C to +125°C	T _A = -40°C to +85°C	Units
				Typ.	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	2.0	2.0	2.0	V
		5.5		1.5	2.0	2.0	2.0	
V _{IL}	Maximum LOW Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	0.8	0.8	0.8	V
		5.5		1.5	0.8	0.8	0.8	
V _{OH}	Minimum HIGH Level Output Voltage	4.5	I _{OUT} = -50μA	4.49	4.4	4.4	4.4	V
		5.5		5.49	5.4	5.4	5.4	
		4.5	V _{IN} = V _{IL} or V _{IH} , I _{OH} = 24mA		3.86	3.70	3.76	
		5.5	V _{IN} = V _{IL} or V _{IH} , I _{OH} = 24mA ⁽⁴⁾		4.86	4.70	4.76	
V _{OL}	Maximum LOW Level Output Voltage	4.5	I _{OUT} = 50μA	0.001	0.1	0.1	0.1	V
		5.5		0.001	0.1	0.1	0.1	
		4.5	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA		0.36	0.50	0.44	
		5.5	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ⁽⁴⁾		0.36	0.50	0.44	
I _{IN}	Maximum Input Leakage Current	5.5	V _I = V _{CC} , GND		±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum 3-STATE Leakage Current	5.5	V _I = V _{IL} , V _{IH} ; V _O = V _{CC} , GND		±0.25	±5.0	±2.5	μA
I _{CCT}	Maximum I _{CC} /Input	5.5	V _I = V _{CC} - 2.1V	0.6		1.6	1.5	mA
I _{OLD}	Minimum Dynamic Output Current ⁽⁵⁾	5.5	V _{OLD} = 1.65V Max.			50	75	mA
I _{OHD}		5.5	V _{OHD} = 3.85V Min.			-50	-75	mA
I _{CC}	Maximum Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND		4.0	80.0	40.0	μA

Notes:

4. All outputs loaded; thresholds on input associated with output under test.
5. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V) ⁽⁶⁾	$T_A = +25^\circ\text{C}$, $C_L = 50\text{pF}$			$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $C_L = 50\text{pF}$		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $C_L = 50\text{pF}$		Units
			Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, Data to Output	3.3	2.0	6.5	9.0	1.0	12.5	1.5	10.0	ns
		5.0	1.5	5.0	7.0	1.0	9.5	1.0	7.5	
t_{PHL}	Propagation Delay, Data to Output	3.3	2.0	6.5	9.0	1.0	12.0	2.0	10.0	ns
		5.0	1.5	5.0	7.0	1.0	9.0	1.0	7.5	
t_{PZH}	Output Enable Time	3.3	2.0	6.0	10.5	1.0	11.5	1.5	11.0	ns
		5.0	1.5	5.0	7.0	1.0	9.0	1.5	8.0	
t_{PZL}	Output Enable Time	3.3	2.5	7.5	10.0	1.0	13.0	2.0	11.0	ns
		5.0	1.5	5.5	8.0	1.0	10.5	1.5	8.5	
t_{PHZ}	Output Disable Time	3.3	3.0	7.0	10.0	1.0	12.5	1.5	10.5	ns
		5.0	2.5	6.5	9.0	1.0	10.5	1.0	9.5	
t_{PLZ}	Output Disable Time	3.3	2.5	7.5	10.5	1.0	13.0	2.5	11.5	ns
		5.0	2.0	6.5	9.0	1.0	11.0	2.0	9.5	

Note:

6. Voltage range 3.3 is $3.3\text{V} \pm 0.3\text{V}$. Voltage range 5.0 is $5.0\text{V} \pm 0.5\text{V}$.

AC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V) ⁽⁷⁾	$T_A = +25^\circ\text{C}$, $C_L = 50\text{pF}$			$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $C_L = 50\text{pF}$		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $C_L = 50\text{pF}$		Units
			Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, Data to Output	5.0	2.0	6.5	9.0	1.0	10.0	1.5	10.0	ns
t_{PHL}	Propagation Delay, Data to Output	5.0	2.0	7.0	9.0	1.0	10.0	1.5	10.0	ns
t_{PZH}	Output Enable Time	5.0	1.5	6.0	8.5	1.0	9.5	1.0	9.5	ns
t_{PZL}	Output Enable Time	5.0	2.0	7.0	9.5	1.0	11.0	1.5	10.5	ns
t_{PHZ}	Output Disable Time	5.0	2.0	7.0	9.5	1.0	11.0	1.5	10.5	ns
t_{PLZ}	Output Disable Time	5.0	2.5	7.5	10.0	1.0	11.5	2.0	10.5	ns

Note:

7. Voltage range 5.0 is $5.0\text{V} \pm 0.5\text{V}$.

Capacitance

Symbol	Parameter	Conditions	Typ	Units
C_{IN}	Input Capacitance	$V_{CC} = \text{OPEN}$	4.5	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 5.0\text{V}$	45.0	pF

Physical Dimensions

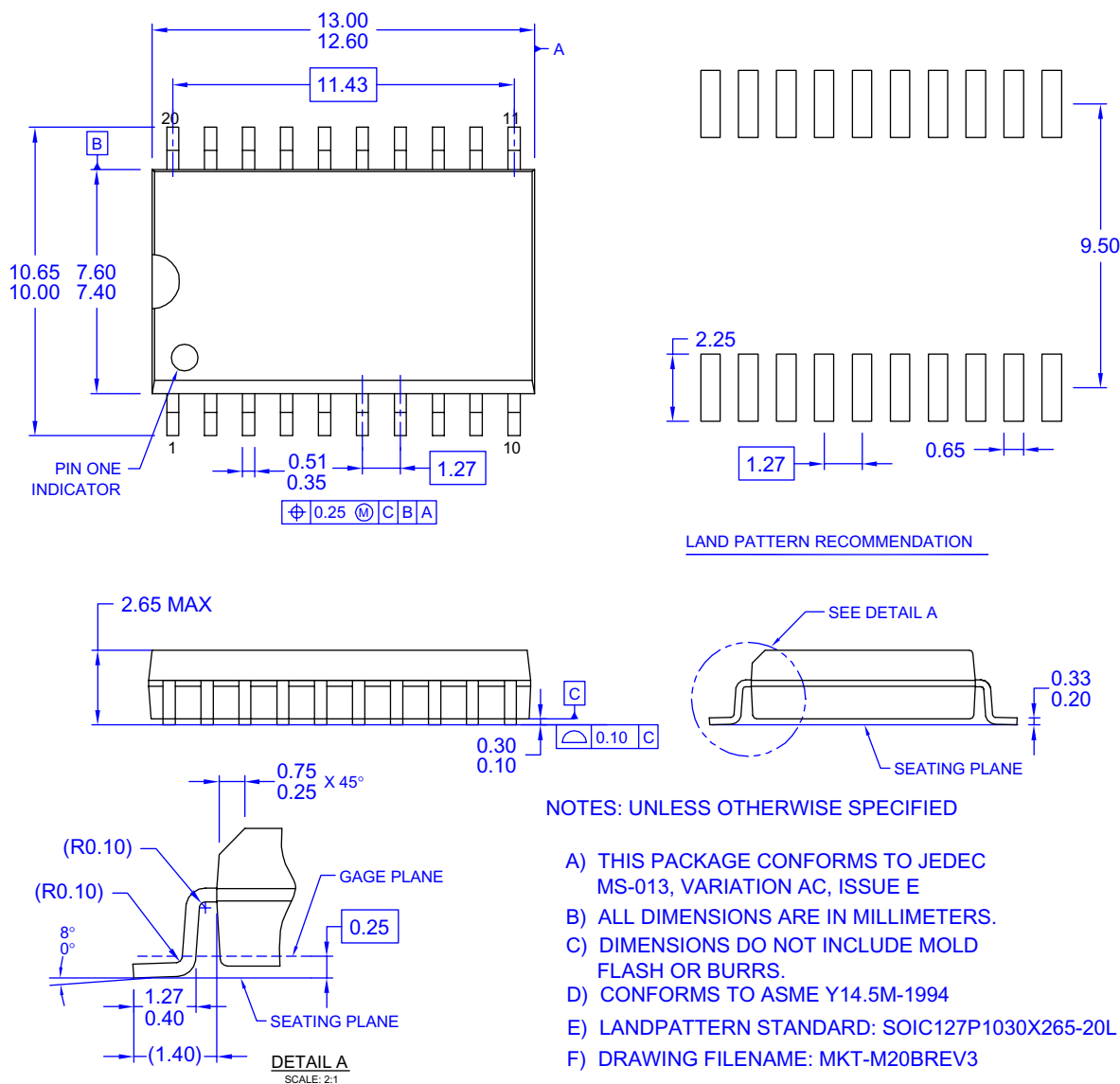


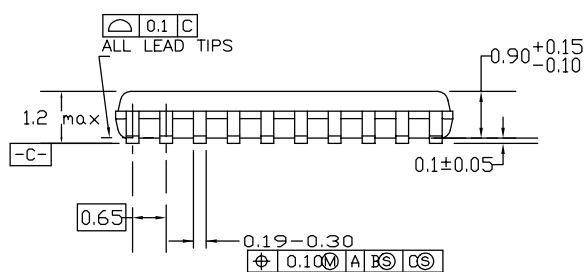
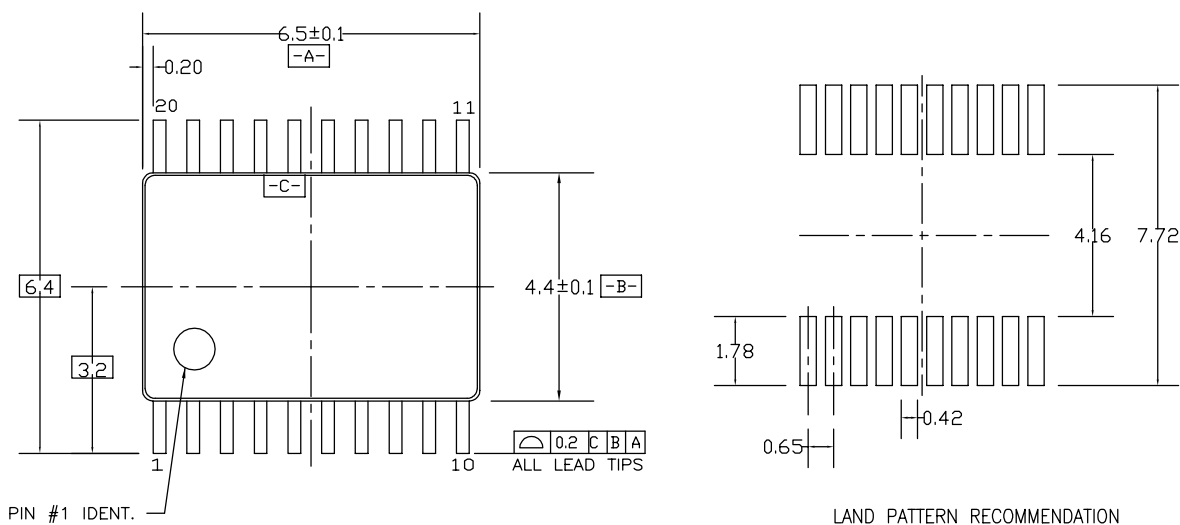
Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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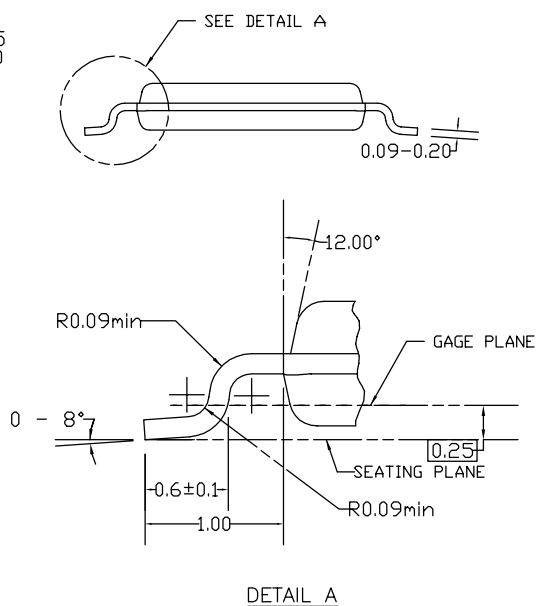
Physical Dimensions (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

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- DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.



MTC20REV D1

Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Physical Dimensions (Continued)

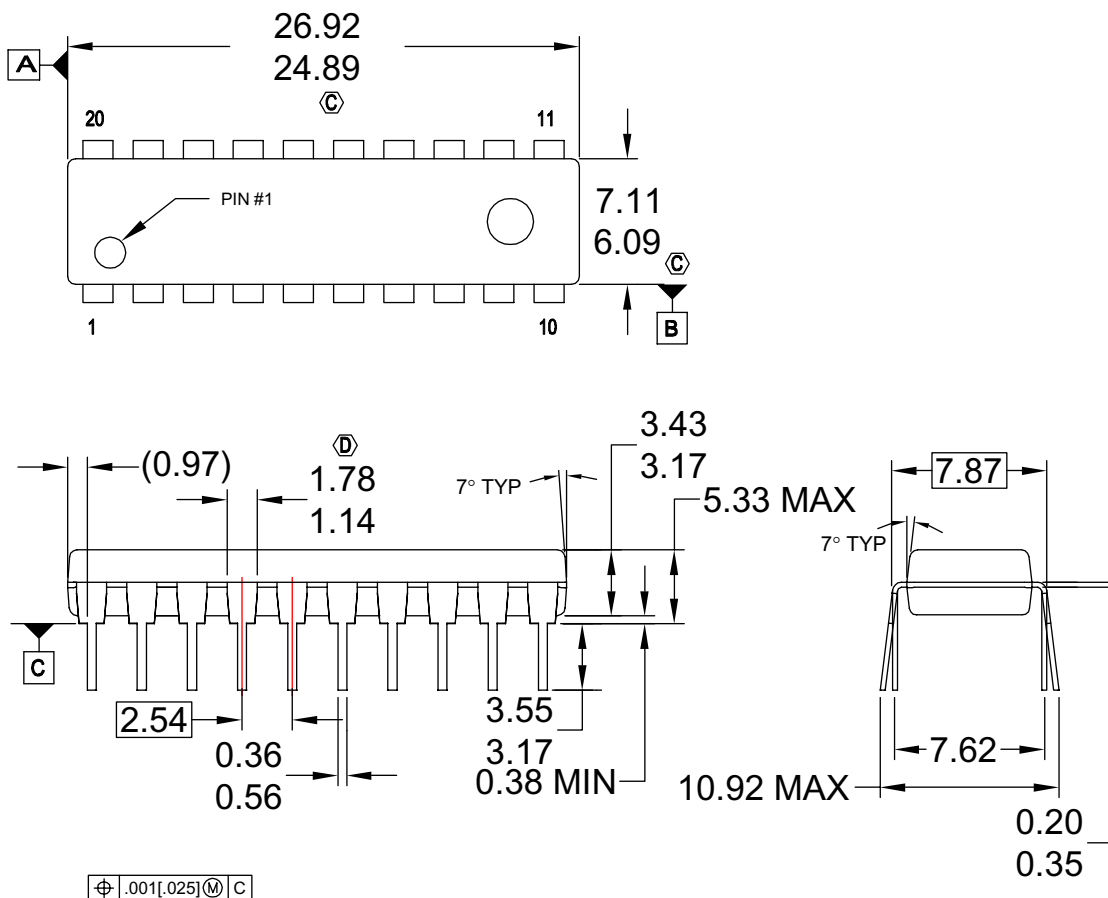


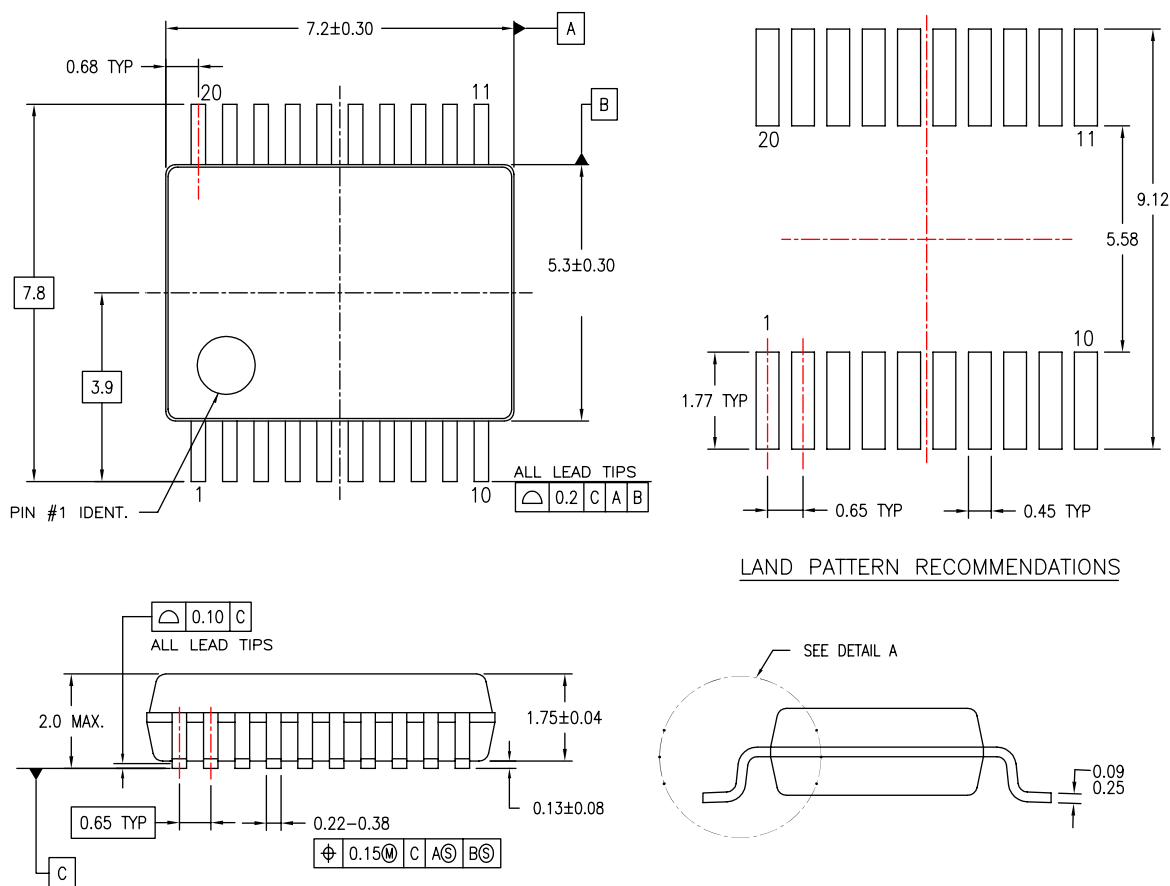
Figure 4. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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Physical Dimensions (Continued)



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MSA20REVB

Figure 5. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

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