



LIMITED DATASHEET

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to request the full datasheet.

October 2010



FUSB2805

USB2.0 High-Speed OTG Transceiver with ULPI Interface

Features

- Complies with USB 2.0, OTG Rev 1.3 Supplement, and ULPI Rev 1.1 Specifications
- Supports 480 Mbps, 12Mbps, and 1.5Mbps USB2.0 Speeds
 - Integrated Termination Resistors Meet USB2.0 Resistor ECN
 - Integrated Serializer and Deserializer
 - Insertion and Removal of Stuffed Bits as Appropriate
 - USB Clock and Data Recovery to ± 150 ppm
- Supports USB OTG Rev 1.3 Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- 15KV ESD, IEC 61000 Board Level, Air Gap

Applications

- Set-Top Box Video Camera, MP3 Player
- Cell Phone, Digital Still Camera, PDA
- DVD Recorder, Scanner, Printer

Description

The FUSB2805 is a UTMI+ Low-Pin Interface (ULPI) USB2.0 OTG transceiver. It is compliant with the Universal Serial Bus Specification Rev 2.0 (USB2.0), the ULPI Specification Rev. 1.1, and the On-The-Go (OTG) supplement to USB2.0, Rev. 1.3.

The FUSB2805 is optimized to connect the USB2.0 host, peripheral, or OTG-controller to the USB connector via the ULPI link. Data can be transmitted and received at high speed (480Mbps), full speed (12Mbps), and low speed (1.5Mbps) through a 12-bit (SDR) interface.

Related Resources

UTMI+ Low Pin Interface Specification (ULPI), Revision 1.1, October 20, 2004. <http://www.ulpi.org>

UTMI+ Specification, Revision 1.0, February 22, 2004. <http://www.ulpi.org>

For additional performance information, please contact analogswitch@fairchildsemi.com.

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FUSB2805MLX	FUSB2805	-40 to +85°C	32-Terminal, Molded Leadless Package (MLP), Quad, JEDEC MO-220

Block Diagram

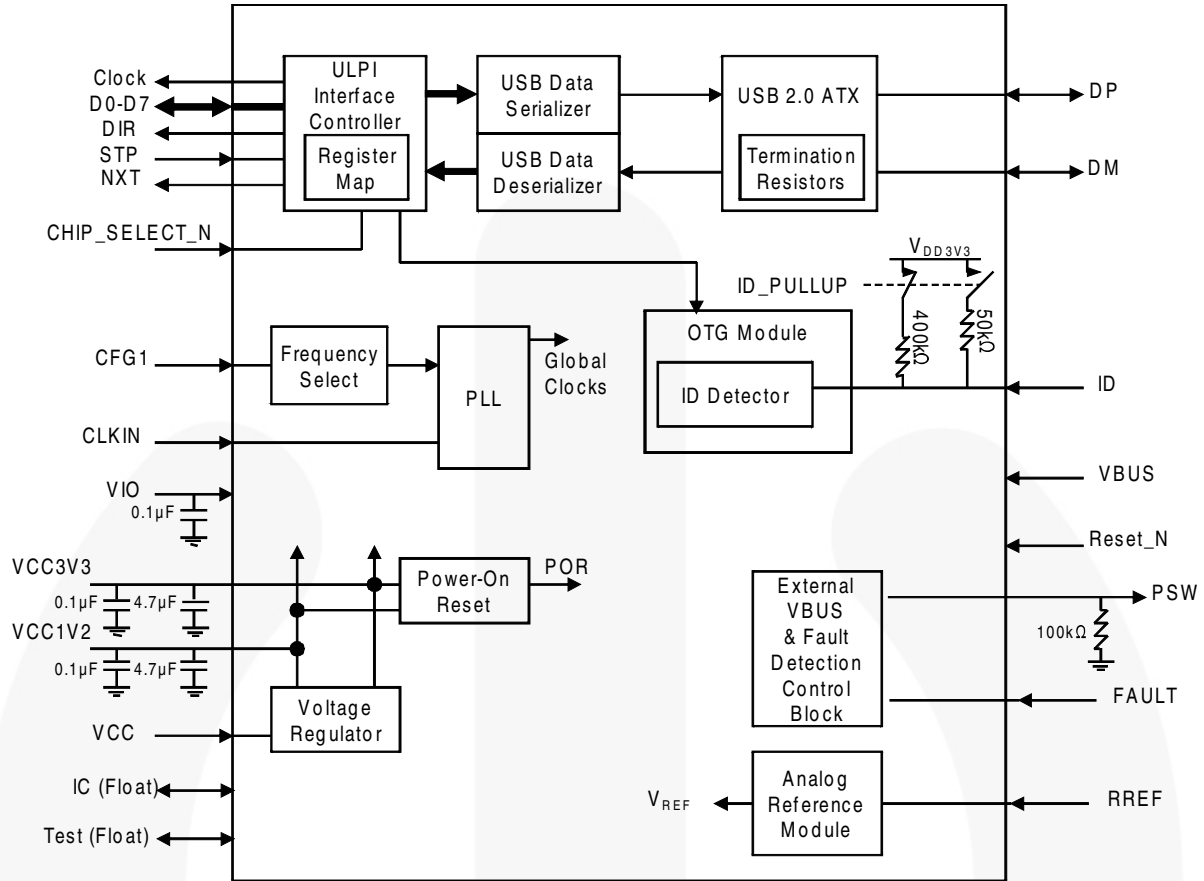


Figure 1. Functional Block Diagram

Pin Configuration

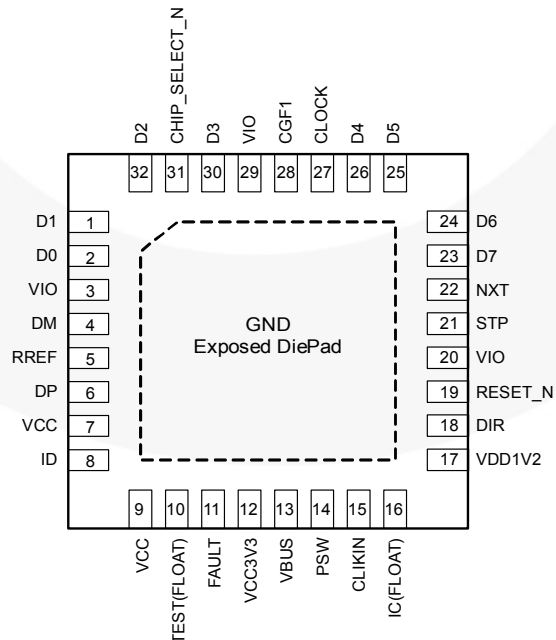


Figure 2. Pin Assignments (Through View)

Pin Definitions

Symbol	Type ⁽¹⁾	Description
Chip Select_N	I	Active LOW. HIGH – ULPI pin three-stated; LOW – ULPI operates normally. TTL compatible; CMOS input with hysteresis.
R _{REF}	AI/O	Resistor reference. Connect through 12kΩ ±1% to GND.
DM	AI/O	USB D- pin. USB mode: data minus (D-) pin of the USB cable.
DP	AI/O	USB D+ pin. USB mode: data plus (D+) pin of the USB cable.
FAULT	I	FAULT is used to signal a V _{BUS} over-current/over-voltage condition from an external SMPS or power management IC. The link must enable this function via the ExternalVbusFault register bit and the polarity must be set via the ExternalVbusActiveLow register bit.
ID	I	Identification (ID) pin of the micro-USB cable. TTL; if not used, connect to 3V3.
VCC	P	Input supply voltage or battery source.
PSW	O	Controls an external, active HIGH, V _{BUS} power switch/charge pump and/or an SMPS charger IC. An external 100KΩ pull-down resistor is required. Open source, slew-rate-controlled output; this pin is referenced to V _{CC3V3} .
V _{BUS}	AI/O	Should be connected to the VBUS pin of the USB cable. Leave open circuit if not used. An internal 90KΩ ±11% pull-down resistor is present on this pin.
V _{CC3V3}	P	3.3V regulator output requiring capacitors. Internally powers OTG, analog core, and ATX.
CLKIN	I	Clock input; frequency depends on the CFG1 pin. This is a digital input buffer, not analog for a crystal.
I.C.	I/O	Internally connected; float pin.
TEST	I/O	Internally connected; float pin.
CFG1	I	Configures the clock frequency; 0: input is 19.2MHz. 1: input is 26MHz.
V _{DD1V2}	P	1.2V regulator output requiring capacitors. Internally powers the digital core and analog core.
V _{IO}	P	Input I/O supply rail; 0.1μF capacitor connected to power input.
Reset_N	I	Connect to V _{IO} when not used. Resets the transceiver; active LOW.
GND	P	Connect to ground.
DIR	O	ULPI direction output signal.
STP	I	ULPI stop input signal; CMOS input.
NXT	O	ULPI next output signal.
D7	I/O	ULPI data pin 7; three-state output.
D6	I/O	ULPI data pin 6; three-state output.
D5	I/O	ULPI data pin 5; three-state output.
D4	I/O	ULPI data pin 4; three-state output.
D3	I/O	ULPI data pin 3; three-state output.
D2	I/O	ULPI data pin 2; three-state output.
D1	I/O	ULPI data pin 1; three-state output.
D0	I/O	ULPI data pin 0; three-state output.
CLOCK	O	60MHz clock output when digital 19.2MHz (or 26MHz) clock is applied; Push-pull output.

Notes:

1. I=input; O=output; I/O=digital input/output; OD=open-drain output; AI/O=analog input/output; P=power or ground.
2. Per USB2.0, below a supply of 2.97V, USB full-speed and low-speed transactions are not guaranteed; although some devices may continue to function with the FUSB2805 at the lower supply rail.

Physical Dimensions

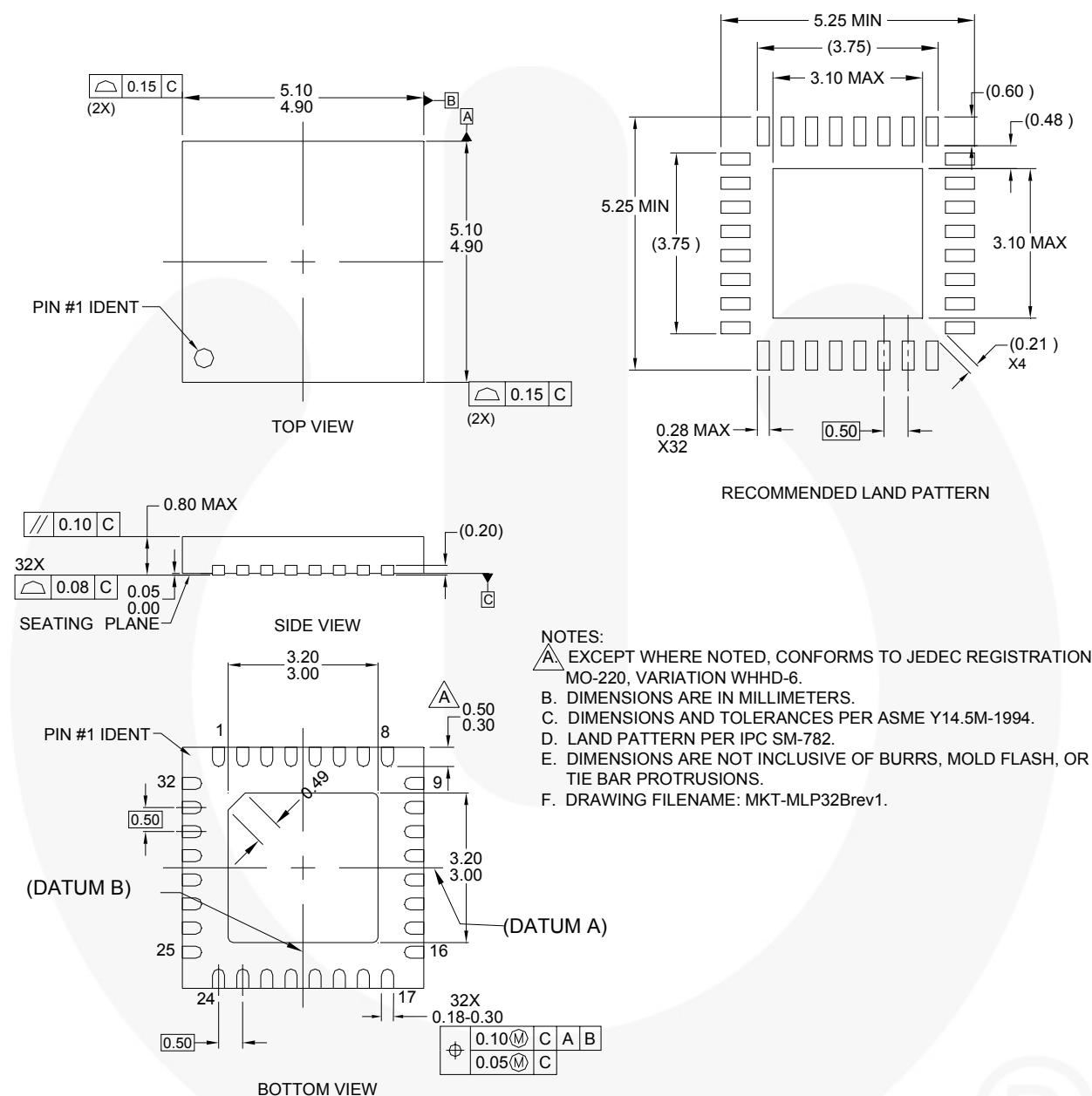


Figure 23. 32-Lead, Molded Leadless Package (MLP)

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