

FT7511

Reset Timer with Fixed Delay and Reset Pulse

Features

- Fixed Reset Delay: 7.5 Seconds
- One Input Reset Pin
- Open-Drain Output Pin with Fixed 80ms Pulse
- 1.8V to 5.0V Operation ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)
- 1.7V to 5.0V Operation ($T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$)
- 1.65V to 5.0V Operation ($T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$)
- $<1\mu\text{A}$ I_{CCQ} Consumption
- Zero-Second Test Mode Enable

Applications

- Cell Phones
- Portable Media Players
- Tablets
- Mobile Devices
- Consumer Medical

Description

The FT7511 is a timer for resetting a mobile device where long reset times are needed. The long delay helps avoid unintended resets caused by accidental key presses. It has a fixed delay of $7.5 \pm 20\%$ seconds. The DSR pin enables Test Mode operation by immediately forcing /RST1 LOW for factory testing.

The FT7511 has one input for single-button resetting capability. The device has a single open-drain output with 0.5mA pull-down drive.

FT7511 draws minimal I_{CC} current when inactive and functions over a power supply range of 1.65V to 5.0V.

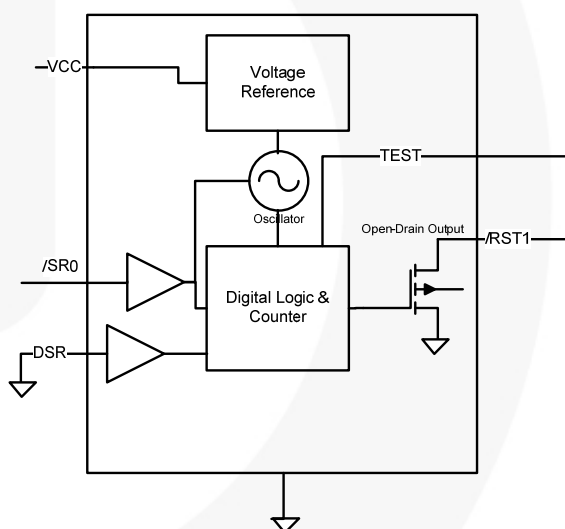


Figure 1. Block Diagram

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FT7511L6X	-40°C to $+85^\circ\text{C}$	PD	6-Lead, MicroPak™ 1.0 x 1.45mm, JEDEC MO-252	5000 Units on Tape and Reel

Pin Configuration

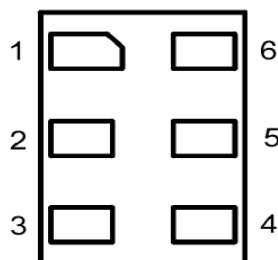


Figure 2. Pad Assignments (Top-Through View)

Pin Definitions

Pin #	Name	Description	
		Normal Operation	0-Second Factory-Test Mode
1	/RST1	Open-Drain Output, Active LOW	Open-Drain Output, Active LOW
2	GND	GND	GND
3	/SR0	Reset Input, Active LOW	Reset Input, Active LOW
4	VCC	Power Supply	Power Supply
5	DSR	Delay Selection Input. Tie to GND ⁽¹⁾ during normal operation.	Delay Selection Input. Pull HIGH to enable the 0-second delay for factory test.
6	TEST	Used for device testing; should be tied to GND during normal operation.	Used for device testing; should be tied to GND during normal operation.

Note:

1. The DSR pin must always be tied to either GND or VCC; it must not float.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Condition	Min.	Max.	Unit
V _{CC}	Supply Voltage		-0.5	7.0	V
V _{IN}	DC Input Voltage	/SR0, DSR	-0.5	7.0	V
V _{OUT}	Output Voltage ⁽²⁾	/RST1	-0.5	7.0	V
I _{IK}	DC Input Diode Current	V _{IN} < 0V		-50	mA
I _{OK}	DC Output Diode Current	V _{OUT} < 0V		-50	mA
I _{OL}	DC Output Sink Current			+50	mA
I _{CC}	DC V _{CC} or Ground Current per Supply Pin			±100	mA
T _{STG}	Storage Temperature Range		-65	+150	°C
T _J	Junction Temperature Under Bias			+150	°C
T _L	Junction Lead Temperature, Soldering 10 Seconds			+260	°C
P _D	Power Dissipation			5	mW
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		4	kV
		Charged Device Model, JESD22-C101		2	

Note:

2. All output current Absolute Maximum Ratings must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Condition	Min.	Max.	Unit
V _{CC}	Supply Voltage ⁽³⁾	-40°C to +85°C	1.8	5.0	V
		-25°C to +85°C	1.7	5.0	
		0°C to +85°C	1.65	5.00	
t _{RFC}	V _{CC} Recovery Time After Power Down	V _{CC} =0V After Power Down, Rising to 0.5V	5		ms
V _{IN}	Input Voltage ⁽³⁾	/SR0	0	5	V
V _{OUT}	Output Voltage	/RST1	0	5	V
I _{OL}	DC Output Sink Current	/RST1, V _{CC} =1.8V to 5.0V		+0.5	mA
T _A	Free-Air Operating Temperature		-40	+85	°C
Θ _{JA}	Thermal Resistance			350	°C/W

Note:

3. V_{CC} should never be allowed to float while input pins are driven.

DC Electrical Characteristics

Unless otherwise specified; conditions of $T_A = -40$ to 80°C with $V_{CC} = 1.8 - 5.0\text{V}$, OR $T_A = -25$ to 85°C with $V_{CC} = 1.7 - 5\text{V}$, OR $T_A = 0$ to 85°C with $V_{CC} = 1.65 - 5\text{V}$ produce the performance characteristics below.

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IH}	Input High Voltage	DSR, /SR0	$0.65 \times V_{CC}$		V
V_{IL}	Input Low Voltage	DSR, /SR0		$0.25 \times V_{CC}$	V
V_{OL}	Low Level Output Voltage	RST, $I_{OL} = 500\mu\text{A}$		0.3	V
I_{IN}	Input Leakage Current (/SR0, DSR)	$0\text{V} \leq V_{IN} \leq 5.0\text{V}$		± 1.0	μA
I_{CC}	Quiescent Supply Current (Timer Inactive)	/SR0= V_{CC}		1	μA
	Dynamic Supply Current (Timer Active)	/SR0=0V		100	μA

AC Electrical Characteristics

Unless otherwise specified; conditions of $T_A = -40$ to 80°C with $V_{CC} = 1.8 - 5.0\text{V}$, OR $T_A = -25$ to 85°C with $V_{CC} = 1.7 - 5\text{V}$, OR $T_A = 0$ to 85°C with $V_{CC} = 1.65 - 5\text{V}$ produce the performance characteristics below.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{PHL1}	Timer Delay, /SR0 to RST (DSR=0)	$C_L = 5\text{pF}$, $R_L = 5\text{K}\Omega$, See Figure 6	6.0	7.5	9.0	s
t_{REC}	Reset Timeout Delay		60	80	100	ms

Capacitance Specifications

$T_A = +25^\circ\text{C}$.

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	$V_{CC} = \text{GND}$	4.0	pF
C_{OUT}	Output Capacitance	$V_{CC} = 5.0\text{V}$	5.0	pF

Functional Description

Device default operation time N is 7.5s. If the DSR pin is pulled HIGH prior to V_{CC} ramp, the FT7511 enters Test Mode and the reset output, /RST1, is immediately pulled LOW for factory testing. The DSR pin MUST be forced to GND during normal operation. The DSR pin should never be driven HIGH or left to float during normal operation. The DSR pin state should never be changed during device operation; it must be biased prior to supplying the V_{CC} supply. If there is a need to use the DSR= V_{CC} Test Mode, the /SR0 must be HIGH when the DSR pin is moved from LOW to HIGH to enter Zero-Second Factory-Test Mode. To return to the standard 7.5-second reset time, the same procedure must be followed with DSR=GND. The DSR pin should never be allowed to change state while the /SR0 pin is LOW.

Operation Modes

A low input signal on /SR0 starts the oscillator. There are two scenarios for counting: short duration and long duration. In the short-duration scenario, output /RST1 is not affected. In the long-duration scenario, the output /RST1 goes LOW after /SR0 has been held LOW for at least 7.5 seconds. The /RST1 output returns to its

original HIGH state 80ms after time t_{REC} has expired, regardless of the state of /SR0. The /RST1 output is an open-drain driver. When the count time exceeds 7.5 seconds, the /RST1 output pulls LOW.

Short Duration ($t_w < 7.5s$)

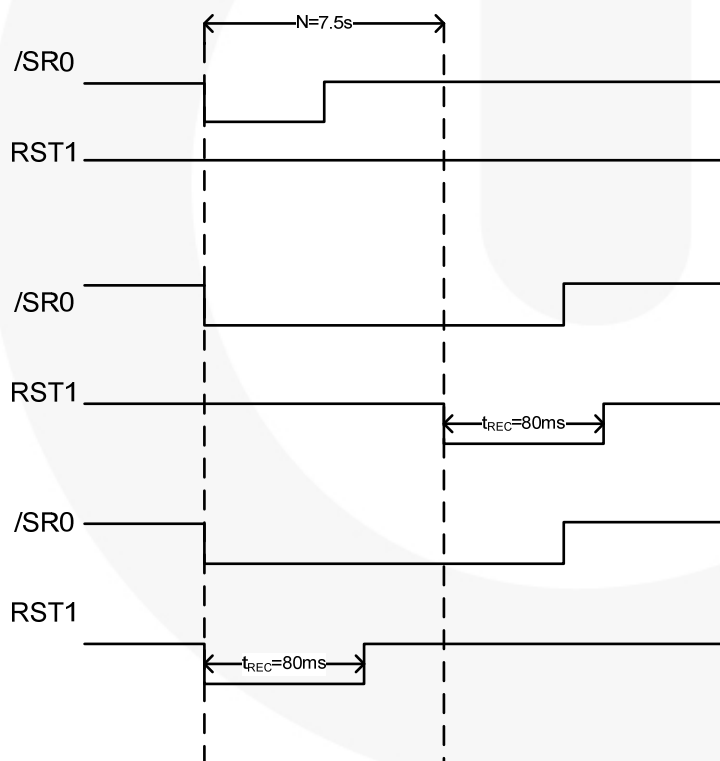
When the /SR0 input goes LOW, the internal timer starts counting. If the /SR0 input goes HIGH before 7.5s has elapsed, the timer stops counting and resets; no changes occur on the outputs.

Long Duration ($t_w > 7.5s$)

When the /SR0 input goes LOW, the internal timer starts counting. If the /SR0 input stays LOW for at least 7.5s, the RST output is enabled and pulled LOW. The output RST is held LOW for t_{REC} , 80ms, as soon as the reset time of 7.5s is met, regardless of the state of the /SR0 pin. When the /SR0 input has returned HIGH and t_{REC} has expired, the internal timer resets and awaits the next RESET event.

0-Second Test Mode

/RST1 goes LOW immediately after /SR0 goes LOW.



**Short-Duration,
Normal Operation**
/RST1 never goes LOW because
/SR0 LOW duration did not meet
requirement: reset time $N=7.5s$

**Long-Duration,
Normal Operation**
/RST1 goes LOW because
/SR0 LOW duration exceeded
requirement: reset time $N=7.5s$

0-Second Factory-Test Mode
/RST1 goes LOW immediately
after /SR0 goes LOW

Figure 3. Reset Timing Waveforms

Application Diagram

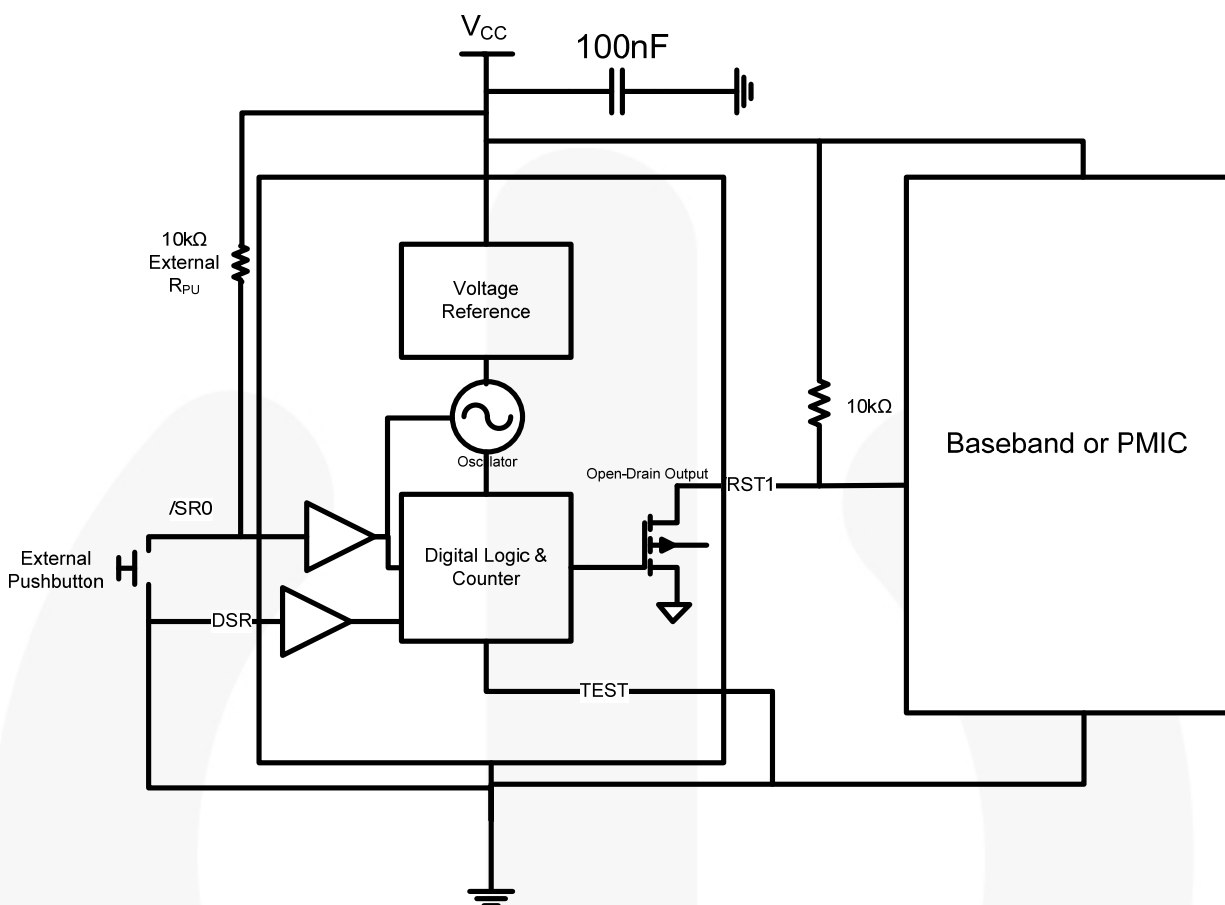


Figure 4. Recommended Application Diagram

AC Test Circuit and Waveforms

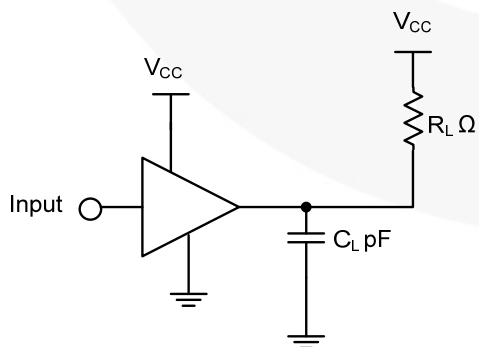


Figure 5. AC Test Circuit

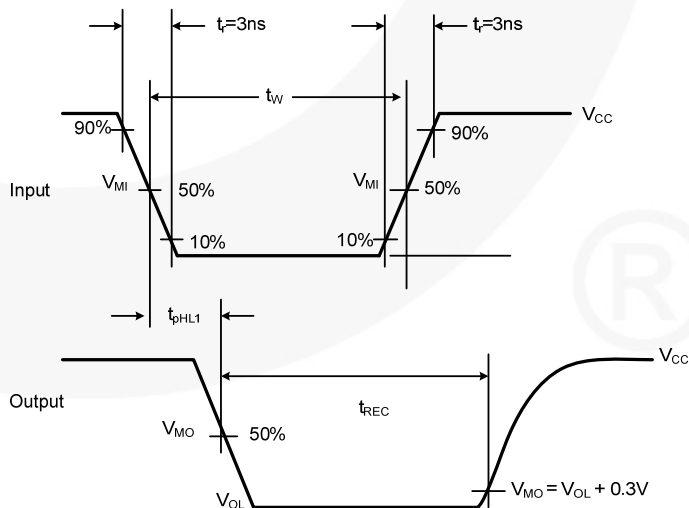


Figure 6. Waveforms for /RST1 Output



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