

FSL138MRT

Green-Mode Fairchild Power Switch (FPS™) for High Input Voltage

Features

- Internal Avalanched-Rugged 800V SenseFET
- Advanced Soft Burst-Mode Operation for Low Standby Power and Low Audible Noise
- Under 40mW Standby Power Consumption at 265V_{AC} and No-load Condition
- Random Frequency Fluctuation for Low EMI
- Pulse-by-Pulse Current Limit
- Various Protection Functions: Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD) with Hysteresis and Under-Voltage Lockout (UVLO) with Hysteresis
- Low Operating Current (0.4mA) in Burst Mode
- Internal Startup Circuit
- Built-in Soft-Start: 15ms
- Auto-Restart Mode

Applications

- Power Supply for STB Home Appliances and Industrial for High AC Input

Description

The FSL138MRT is an integrated Pulse Width Modulation (PWM) controller and SenseFET specifically designed for offline Switched-Mode Power Supplies (SMPS) with minimal external components. The PWM controller includes an integrated fixed-frequency oscillator, Under-Voltage Lockout (UVLO), Leading-Edge Blanking (LEB), optimized gate driver, internal soft-start, temperature-compensated precise current sources for loop compensation, and self-protection circuitry. Compared with a discrete MOSFET and PWM controller solution, the FSL138MRT can reduce total cost, component count, size, and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform suited for cost-effective design of a flyback converter.

Ordering Information

Part Number	Package	Operating Junction Temperature	Current Limit	R _{DS(ON)} (Max.)	Output Power Table ⁽²⁾				Replaces Device
					230V _{AC} ± 15% ⁽³⁾		85~265V _{AC}		
					Adapter ⁽⁴⁾	Open Frame ⁽⁵⁾	Adapter ⁽⁴⁾	Open Frame ⁽⁵⁾	
FSL138MRT	TO-220F 6-Lead W-Forming ⁽¹⁾	-40°C ~ +125°C	2.15A	5Ω	35W	50W	24W	35W	KA5M0380RY DTU

Notes:

1. Pb-free package per JEDEC J-STD-020B.
2. The junction temperature can limit the maximum output power.
3. 230V_{AC} or 100/115V_{AC} with voltage doubler.
4. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient temperature.
5. Maximum practical continuous power in an open-frame design at 50°C ambient temperature.

Pin Configuration

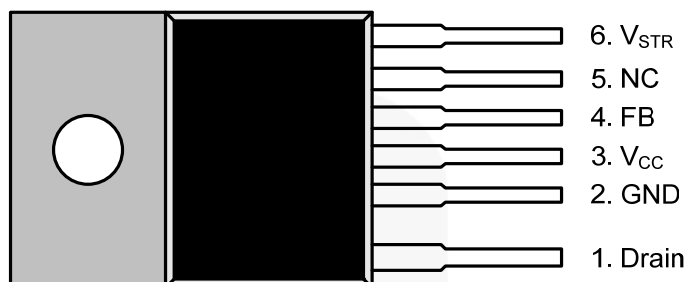


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	Drain	SenseFET Drain. High-voltage power SenseFET drain connection.
2	GND	Ground. This pin is the control ground and the SenseFET source.
3	V _{CC}	Power Supply. This pin is the positive supply input, which provides the internal operating current for both startup and steady-state operation.
4	FB	Feedback. This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 7V, the overload protection triggers, which shuts down the FPS.
5	NC	No Connection
6	V _{STR}	Startup. This pin is connected directly, or through a resistor, to the high-voltage DC link. At startup, the internal high-voltage current source supplies internal bias and charges the external capacitor connected to the V _{CC} pin. Once V _{CC} reaches 12V, the internal current source (I _{CH}) is disabled.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{STR}	V_{STR} Pin Voltage		650	V
V_{DS}	Drain Pin Voltage		800	V
V_{CC}	V_{CC} Pin Voltage		26	V
V_{FB}	Feedback Pin Voltage	-0.3	10.0	V
I_{DM}	Drain Current Pulsed ⁽⁶⁾		12	A
I_{DS}	Continuous Switching Drain Current		3	A
E_{AS}	Single Pulsed Avalanche Energy ⁽⁷⁾		134	mJ
P_D	Total Power Dissipation ($T_C=25^\circ\text{C}$) ⁽⁸⁾		45	W
T_J	Maximum Junction Temperature		150	$^\circ\text{C}$
	Operating Junction Temperature ⁽⁹⁾	-40	+125	$^\circ\text{C}$
T_{STG}	Storage Temperature	-55	+150	$^\circ\text{C}$

Notes:

6. Repetitive peak switching current when the inductive load is assumed: Limited by maximum duty ($D_{MAX}=0.74$) and junction temperature (see Figure 4).
7. $L=10\text{mH}$, starting $T_J=25^\circ\text{C}$.
8. Infinite cooling condition (refer to the SEMI G30-88).
9. Although this parameter guarantees IC operation, it does not guarantee all electrical characteristics.

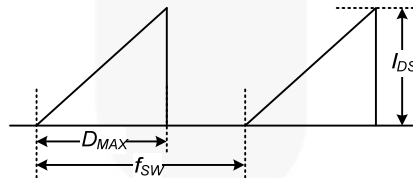


Figure 4. Repetitive Peak Switching Current

ESD Capability

Symbol	Parameter	Value	Unit
ESD	Human Body Model, JESD22-A114	5	KV
	Charged Device Model, JESD22-C101	2	

Thermal Impedance

$T_A=25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Impedance ⁽¹⁰⁾	63.5	$^\circ\text{C/W}$
θ_{JC}	Junction-to-Case Thermal Impedance ⁽¹¹⁾	2.8	$^\circ\text{C/W}$

Notes:

10. Free standing without heat sink under natural convection condition, per JEDEC 51-2 and 1-10.
11. Infinite cooling condition per Mil Std. 883C method 1012.1.

Electrical Characteristics

$T_J=25^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SenseFET Section						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{CC} =0V, I _D =250μA	800			V
I _{DSS}	Zero-Gate-Voltage Drain Current	V _{DS} =640V, T _A =125°C			250	μA
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =1A		4.0	5.0	Ω
C _{ISS}	Input Capacitance ⁽¹²⁾	V _{DS} =25V, V _{GS} =0V, f=1MHz		418		pF
C _{OSS}	Output Capacitance ⁽¹²⁾	V _{DS} =25V, V _{GS} =0V, f=1MHz		50.5		pF
C _{RSS}	Reverse Transfer Capacitance ⁽¹²⁾	V _{DS} =25V, V _{GS} =0V, f=1MHz		5.1		pF
t _r	Rise Time	V _{DS} =400V, I _D =3A, R _G =25Ω		29.2		ns
t _f	Fall Time	V _{DS} =400V, I _D =3A, R _G =25Ω		24.6		ns
t _{d(on)}	Turn-On Delay	V _{DS} =400V, I _D =3A, R _G =25Ω		15.4		ns
t _{d(off)}	Turn-Off Delay	V _{DS} =400V, I _D =3A, R _G =25Ω		23.7		ns
Control Section						
f _S	Switching Frequency ⁽¹²⁾	V _{CC} =14V, V _{FB} =4V	61	67	73	kHz
Δf _S	Switching Frequency Variation ⁽¹²⁾	−25°C < T _J < 125°C		±5	±10	%
D _{MAX}	Maximum Duty Ratio	V _{CC} =14V, V _{FB} =4V	61	67	73	%
D _{MIN}	Minimum Duty Ratio	V _{CC} =14V, V _{FB} =0V			0	%
I _{FB}	Feedback Source Current	V _{FB} =0	65	90	115	μA
V _{START}	UVLO Threshold Voltage	V _{FB} =0V, V _{CC} Sweep	11	12	13	V
V _{STOP}		After Turn-on, V _{FB} =0V	7.0	7.5	8.0	V
t _{S/S}	Internal Soft-Start Time	V _{CC} Sweep		15		ms
Burst-Mode Section						
V _{BURH}	Burst-Mode Voltage	V _{CC} =14V, V _{FB} Sweep	0.39	0.45	0.51	V
V _{BURL}			0.26	0.30	0.34	V
Hys				150		mV
Protection Section						
I _{LIM}	Peak Drain Current Limit	di/dt=300mA/μs	1.89	2.15	2.41	A
V _{SD}	Shutdown Feedback Voltage	V _{CC} =14V, V _{FB} Sweep	6.45	7.0	7.55	V
I _{DELAY}	Shutdown Delay Current	V _{CC} =14V, V _{FB} =4V	1.2	2.0	2.8	μA
t _{LEB}	Leading-Edge Blanking Time ⁽¹²⁾⁽¹³⁾			350		ns
V _{OVP}	Over-Voltage Protection	V _{CC} Sweep	23.0	24.5	26.0	V
T _{SD}	Thermal Shutdown Temperature ⁽¹²⁾	Shutdown Temperature	130	140	150	°C
Hys		Hysteresis		60		°C

Continued on the following page...

Electrical Characteristics (Continued)T_J=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device Section						
I _{OP}	Operating Supply Current, (Control Part in Burst Mode)	V _{CC} =14V, V _{FB} =0V	0.3	0.4	0.5	mA
I _{OPS}	Operating Switching Current, (Control Part and SenseFET Part)	V _{CC} =14V, V _{FB} =2V		1.0	1.4	mA
I _{START}	Start Current	V _{CC} =11V (Before V _{CC} Reaches V _{START})	85	120	155	μA
I _{CH}	Startup Charging Current	V _{CC} =V _{FB} =0V, V _{STR} =40V	0.7	1.0	1.3	mA
V _{STR}	Minimum V _{STR} Supply Voltage	V _{CC} =V _{FB} =0V, V _{STR} Sweep		26		V

Notes:

12. Although these parameters are guaranteed, they are not 100% tested in production.
 13. t_{LEB} includes gate turn-on time.
 14. Average value.

Comparison of KA5M0380R and FSL138MRT

Function	KA5M0380RYDTU	FSL138MRT	Advantages of FSL138MRT
Random Frequency Fluctuation	N/A	Built-in	Low EMI
Operating Current	7mA	0.4mA	Very low standby power
High-Voltage Startup Circuit	N/A	Built-in	
Protections	OLP OVP TSD	OLP OVP AOCP TSD with Hysteresis	Enhanced protections and high reliability
Power Balance	Long t _{CLD}	Very Short t _{CLD}	The difference of input power between the low and high input voltage is quite small

Typical Performance Characteristics

Characteristic graphs are normalized at $T_A=25^\circ\text{C}$.

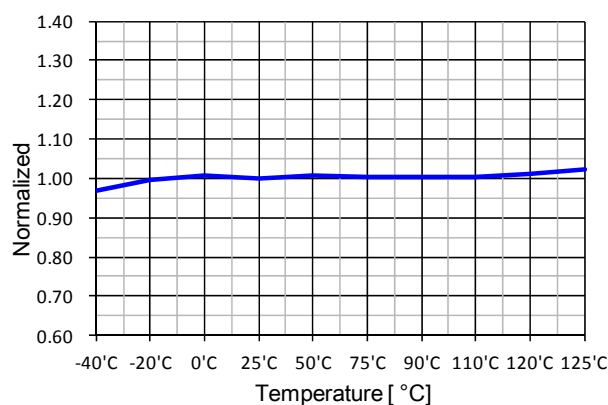


Figure 5. Operating Supply Current (I_{OP}) vs. T_A

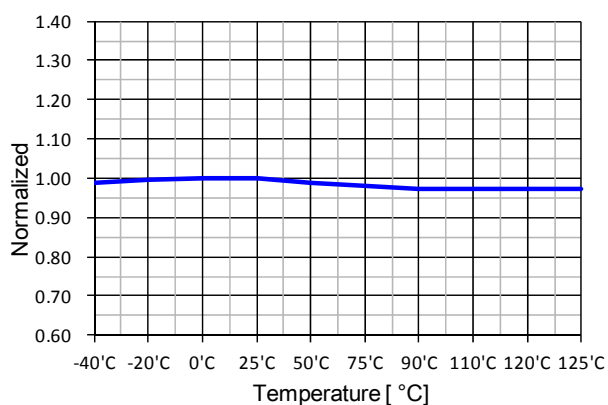


Figure 6. Operating Switching Current (I_{OPS}) vs. T_A

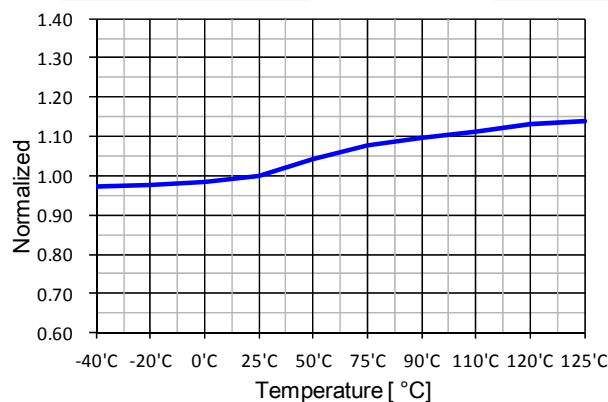


Figure 7. Startup Charging Current (I_{CH}) vs. T_A

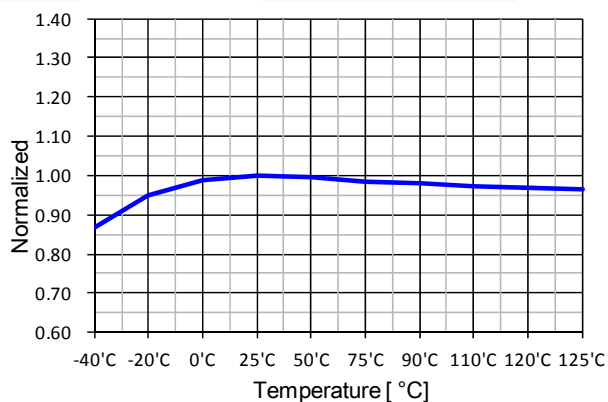


Figure 8. Peak Drain Current Limit (I_{LIM}) vs. T_A

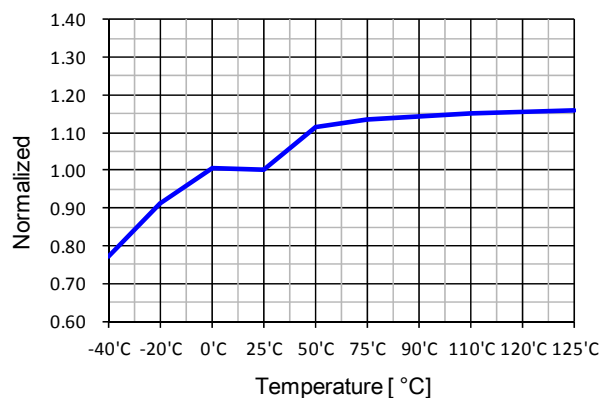


Figure 9. Feedback Source Current (I_{FB}) vs. T_A

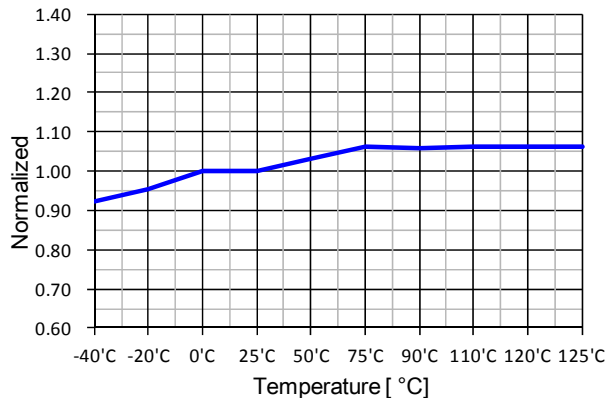


Figure 10. Shutdown Delay Current (I_{DELAY}) vs. T_A

Typical Performance Characteristics

Characteristic graphs are normalized at $T_A=25^\circ\text{C}$.

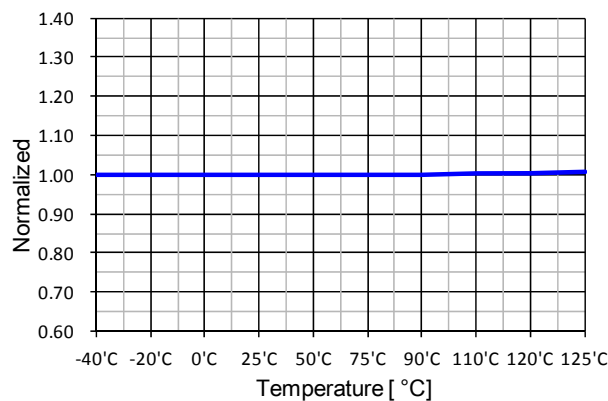


Figure 11. UVLO Threshold Voltage (V_{START}) vs. T_A

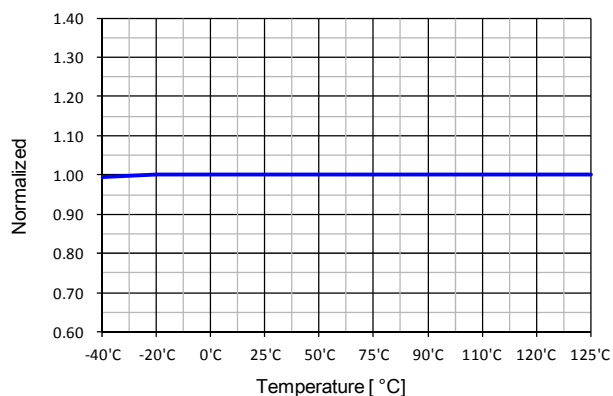


Figure 12. UVLO Threshold Voltage (V_{STOP}) vs. T_A

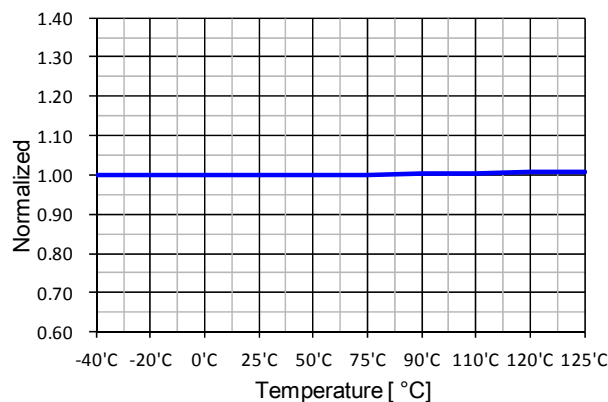


Figure 13. Shutdown Feedback Voltage (V_{SD}) vs. T_A

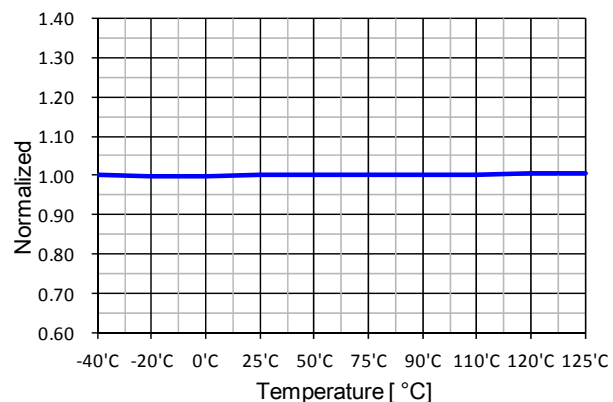


Figure 14. Over-Voltage Protection (V_{OVP}) vs. T_A

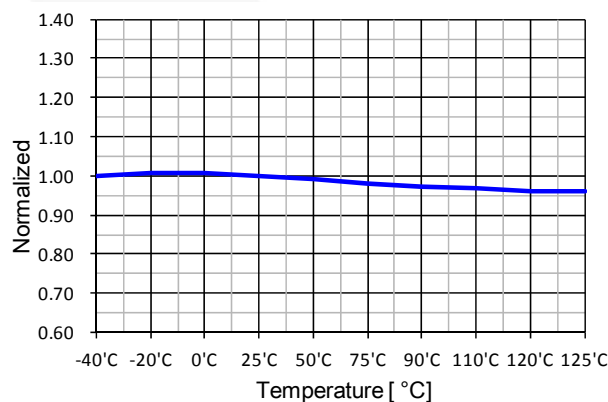


Figure 15. Switching Frequency (f_s) vs. T_A

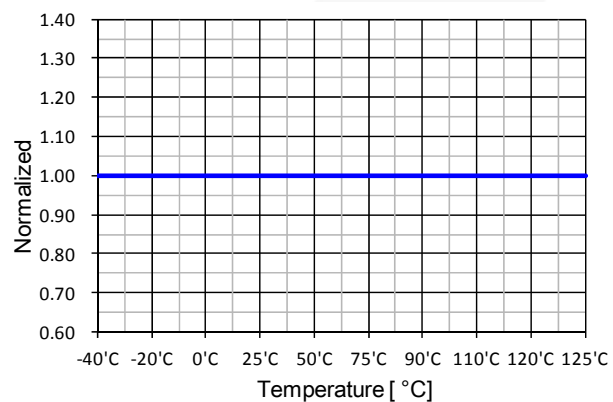


Figure 16. Maximum Duty Ratio (D_{MAX}) vs. T_A

4. Protection Circuits: The FSL138MRT has several self-protective functions, such as Overload Protection (OLP), Abnormal Over-Current Protection (AOCP), Over-Voltage Protection (OVP), and Thermal Shutdown (TSD). All the protections are implemented as auto-restart. Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} falls to the Under-Voltage Lockout (UVLO) stop voltage of 7.5V, the protection is reset and the startup circuit charges the V_{CC} capacitor. When V_{CC} reaches the start voltage of 12.0V, the FSL138MRT resumes normal operation. If the fault condition is not removed, the SenseFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, reliability is improved without increasing cost.

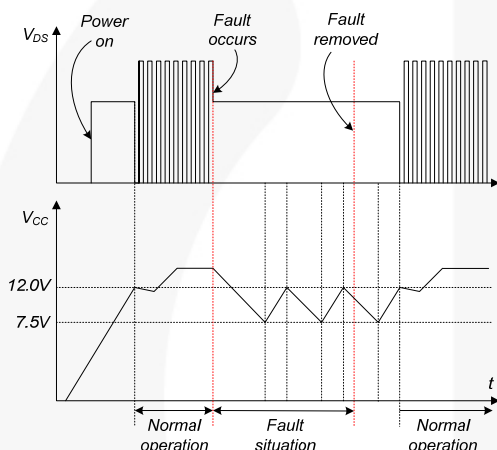


Figure 19. Auto-Restart Protection Waveforms

4.1 Overload Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the SenseFET is limited and, therefore, the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_{OUT}) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.4V, D1 is blocked and the 2.0 μ A current source starts to charge V_{FB} slowly up. In this condition, V_{FB} continues increasing until it reaches 7.0V, when the switching operation is terminated, as shown in Figure 20. The delay for shutdown is the time required to charge CFB from 2.4V to 7.0V with 2.0 μ A. This protection is implemented in Auto-Restart Mode.

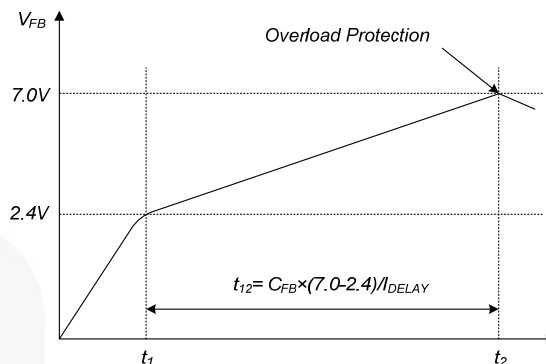


Figure 20. Overload Protection

4.2 Abnormal Over-Current Protection (AOCP): When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the SenseFET during the minimum turn-on time. Even though the FSL138MRT has overload protection, it is not enough to protect the FSL138MRT in that abnormal case; due to the severe current stress imposed on the SenseFET until OLP is triggered. The internal AOCP circuit is shown in Figure 21. When the gate turn-on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the set signal is applied to the S-R latch, resulting in the shutdown of the SMPS.

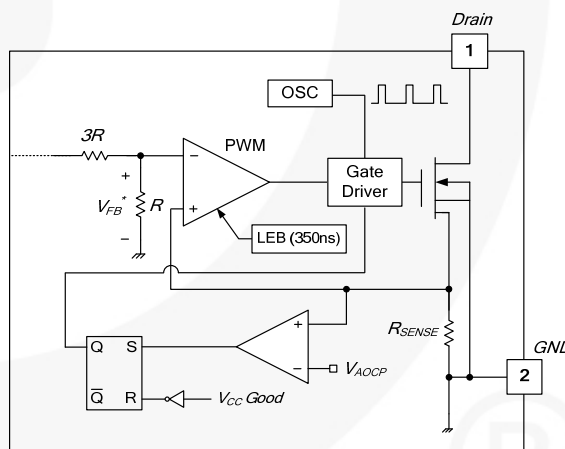


Figure 21. Abnormal Over-Current Protection

4.4 Over-Voltage Protection (OVP): If the secondary-side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is triggered. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection is triggered, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. In general, the V_{CC} is proportional to the output voltage and the FSL138MRT uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 24.5V, an OVP circuit is triggered, resulting in the termination of the switching operation. To avoid undesired activation of OVP during normal operation, V_{CC} should be designed to be below 24.5V.

4.5 Thermal Shutdown (TSD): The SenseFET and the control IC on a die in one package makes it easier for the control IC to detect the over temperature of the SenseFET. If the temperature exceeds 140°C, the thermal shutdown is triggered and stops operation. The FSL138MRT operates in Auto-Restart Mode until the temperature decreases to around 80°C, when normal operation resumes.

5. Soft Burst-Mode Operation: To minimize power dissipation in Standby Mode, the FSL138MRT enters Burst-Mode operation. As the load decreases, the feedback voltage decreases. The device automatically enters Burst Mode when the feedback voltage drops below V_{BURL} (300mV), as shown in Figure 22. At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (450mV), switching resumes. The feedback voltage then falls and the process repeats. Burst Mode alternately enables and disables switching of the SenseFET, reducing switching loss in Standby Mode.

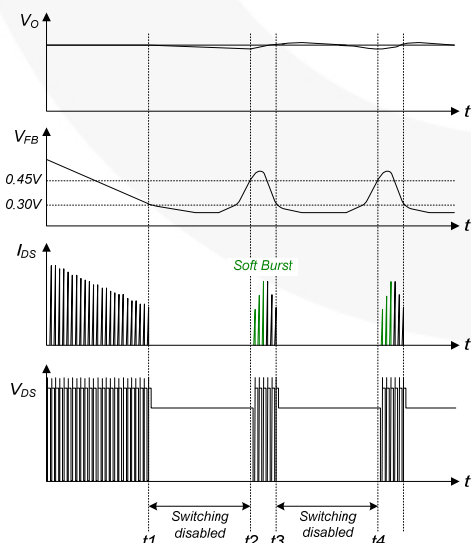


Figure 22. Burst-Mode Operation

6. Random Frequency Fluctuation (RFF): Fluctuating switching frequency of an SMPS can reduce EMI by spreading the energy over a wide frequency range. The amount of EMI reduction is directly related to the switching frequency variation, which is limited internally. The switching frequency is determined randomly by external feedback voltage and an internal free-running oscillator at every switching instant. This random frequency fluctuation scatters the EMI noise around typical switching frequency (67kHz) effectively and can reduce the cost of the input filter included to meet the EMI requirements (e.g. EN55022).

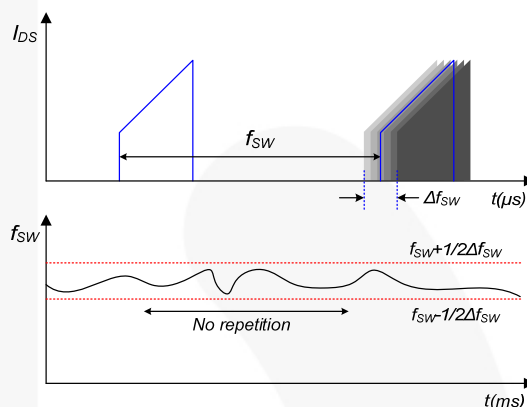


Figure 23. Random Frequency Fluctuation

Physical Dimensions

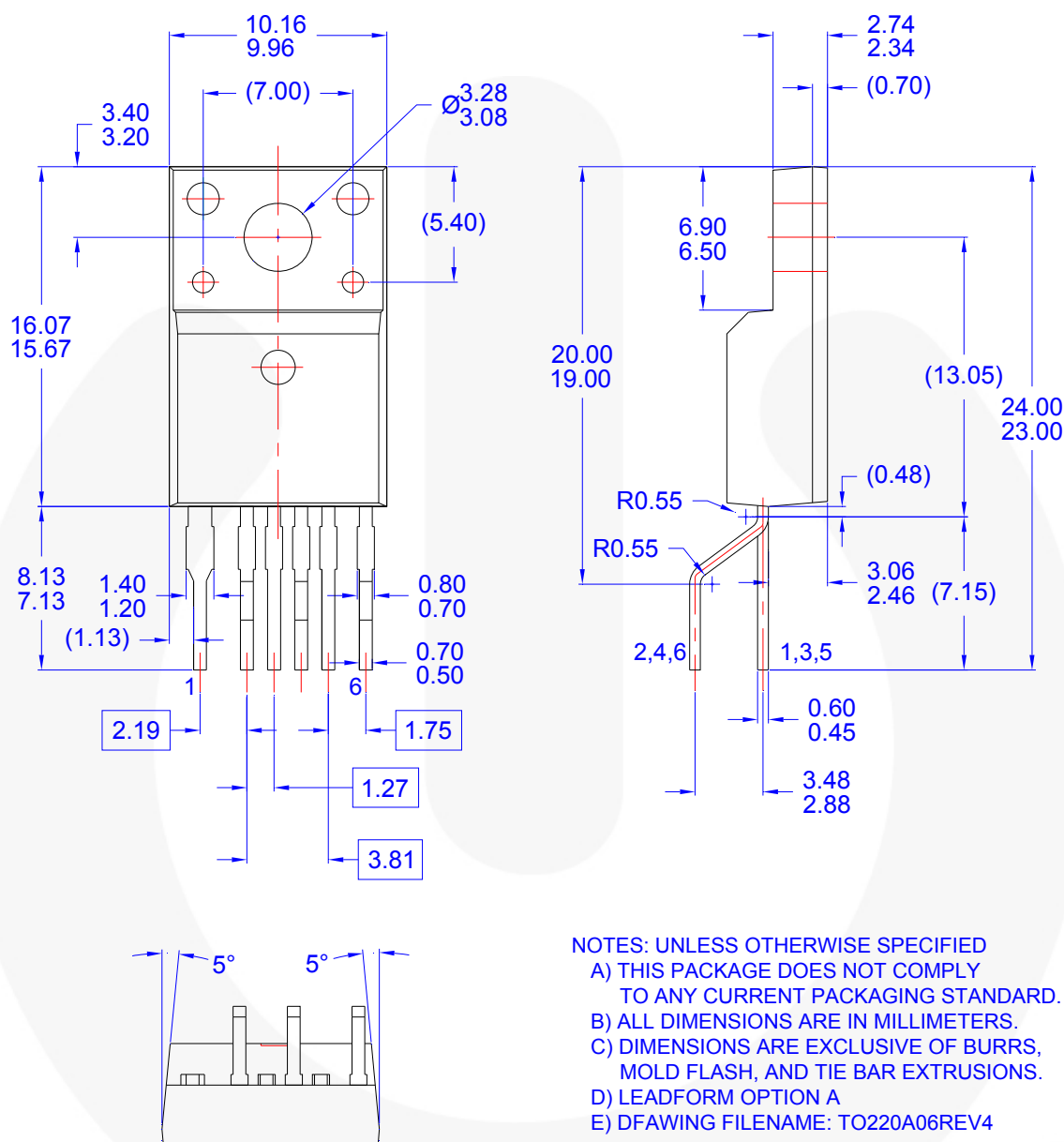


Figure 24. TO-220F-6L (W-Forming)

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I62