FAIRCHILD
SEMICONDUCTOR®

January 2009

QFET®

FQD17P06 / FQU17P06

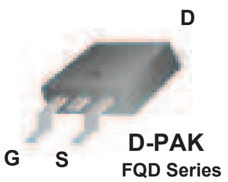
60V P-Channel MOSFET

General Description

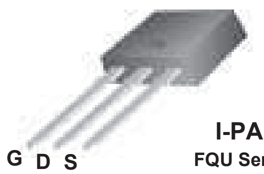
These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand a high energy pulse in the avalanche and commutation modes. These devices are well suited for low voltage applications such as automotive, DC/DC converters, and high efficiency switching for power management in portable and battery operated products.

Features

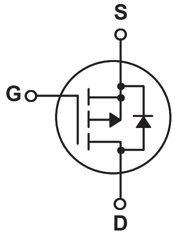
- -12A, -60V, $R_{DS(on)}$ = 0.135Ω @V_{GS} = -10 V
- Low gate charge (typical 21 nC)
- Low Crss (typical 80 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS Compliant



D-PAK
FQD Series



I-PAK
FQU Series



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	FQD17P06 / FQU17P06	Units
V_{DSS}	Drain-Source Voltage	-60	V
I_D	Drain Current - Continuous (T_C = 25°C)	-12	A
	- Continuous (T_C = 100°C)	-7.6	A
I_{DM}	Drain Current - Pulsed (Note 1)	-48	A
V_{GSS}	Gate-Source Voltage	± 25	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	300	mJ
I_{AR}	Avalanche Current (Note 1)	-12	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	4.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-7.0	V/ns
P_D	Power Dissipation (T_A = 25°C) *	2.5	W
	Power Dissipation (T_C = 25°C)	44	W
	- Derate above 25°C	0.35	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	2.85	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

Elerical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-60	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = -250 µA, Referenced to 25°C	--	-0.06	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -60 V, V_{GS} = 0 V	--	--	-1	µA
		V_{DS} = -48 V, T_C = 125°C	--	--	-10	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = -25 V, V_{DS} = 0 V	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = 25 V, V_{DS} = 0 V	--	--	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-2.0	--	-4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -6.0 A	--	0.11	0.135	Ω
g_{FS}	Forward Transconductance	V_{DS} = -30 V, I_D = -6.0 A (Note 4)	--	8.7	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz	--	690	900	pF
C_{oss}	Output Capacitance		--	325	420	pF
C_{rss}	Reverse Transfer Capacitance		--	80	105	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -30 V, I_D = -8.5 A, R_G = 25 Ω (Note 4, 5)	--	13	35	ns
t_r	Turn-On Rise Time		--	100	210	ns
$t_{d(off)}$	Turn-Off Delay Time		--	22	55	ns
t_f	Turn-Off Fall Time		--	60	130	ns
Q_g	Total Gate Charge	V_{DS} = -48 V, I_D = -17 A, V_{GS} = -10 V (Note 4, 5)	--	21	27	nC
Q_{gs}	Gate-Source Charge		--	4.2	--	nC
Q_{gd}	Gate-Drain Charge		--	10	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-12	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-48	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -12 A	--	--	-4.0	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = -17 A, dI_F / dt = 100 A/µs (Note 4)	--	92	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.32	--	µC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 2.4mH, I_{AS} = -12A, V_{DD} = -25V, R_G = 25 Ω, Starting T_J = 25°C
3. $I_{SD} \leq$ -17A, di/dt $\leq$ 300A/µs, $V_{DD} \leq BV_{DSS,}$ Starting T_J = 25°C
4. Pulse Test : Pulse width $\leq$ 300µs, Duty cycle $\leq$ 2%
5. Essentially independent of operating temperature

Typical Characteristics

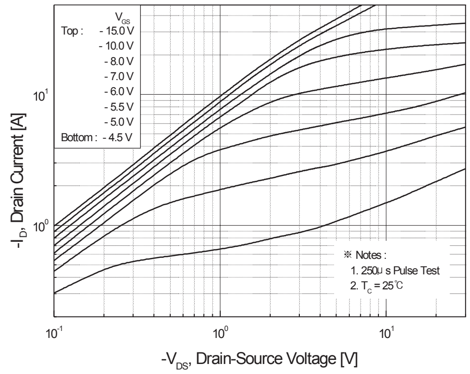


Figure 1. On-Region Characteristics

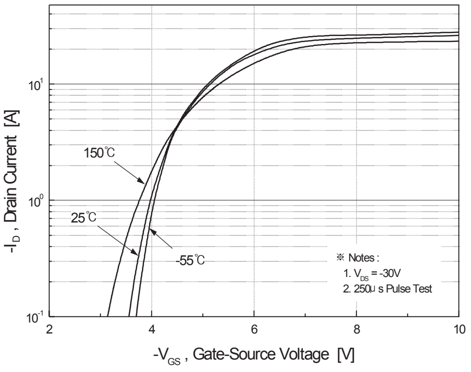


Figure 2. Transfer Characteristics

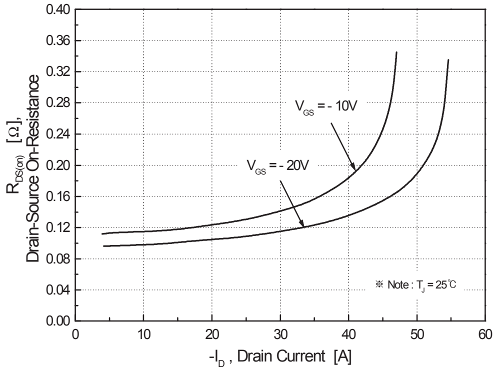


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

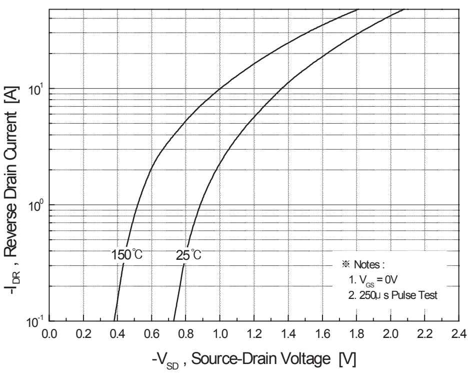


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

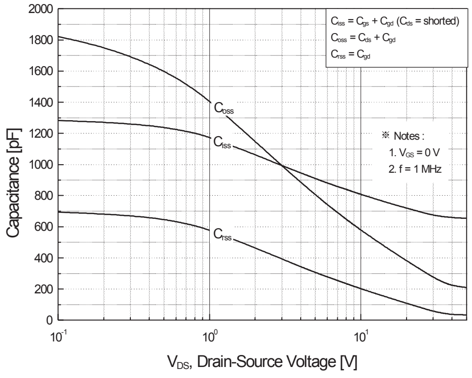


Figure 5. Capacitance Characteristics

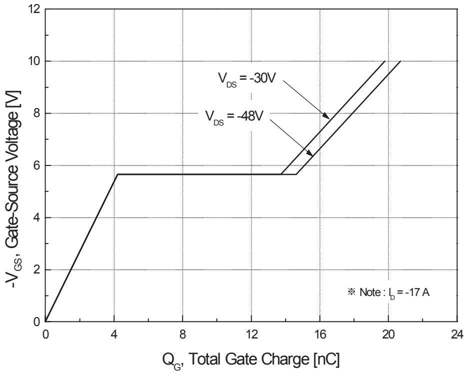


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

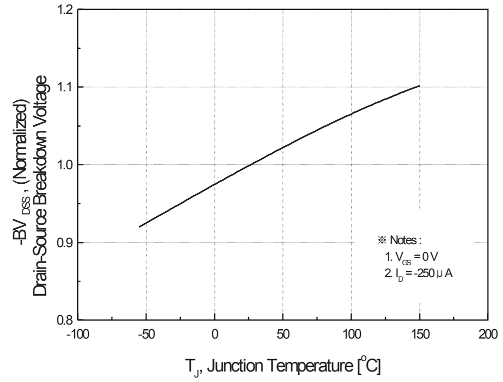


Figure 7. Breakdown Voltage Variation vs. Temperature

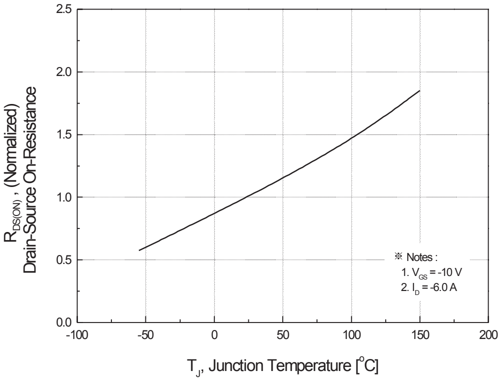


Figure 8. On-Resistance Variation vs. Temperature

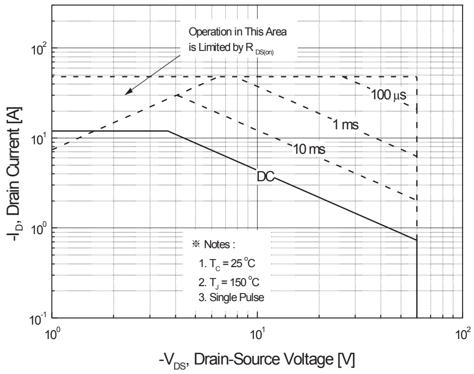


Figure 9. Maximum Safe Operating Area

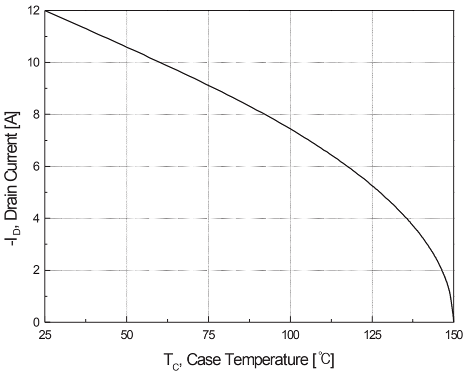


Figure 10. Maximum Drain Current vs. Case Temperature

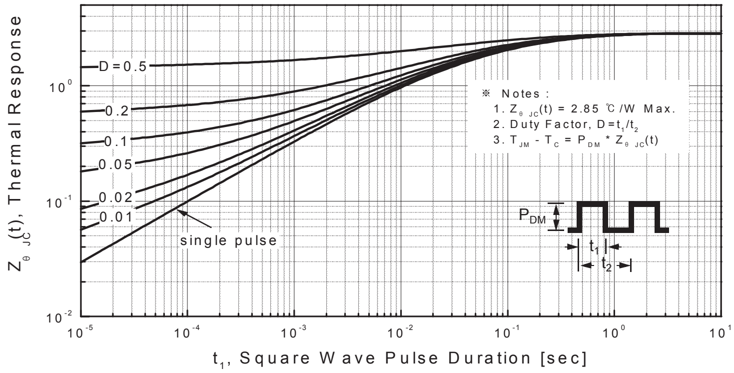
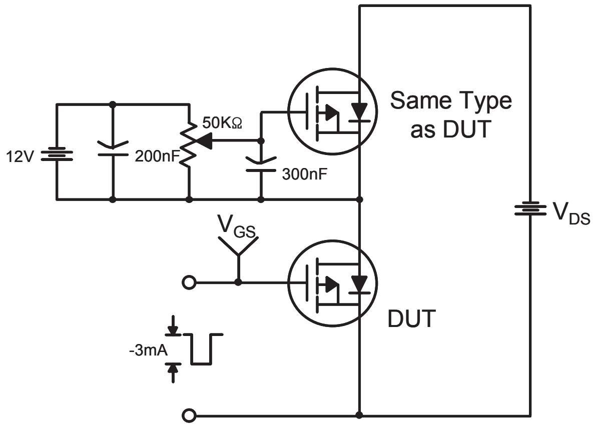
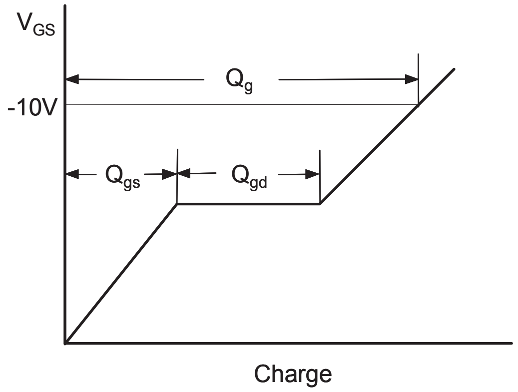


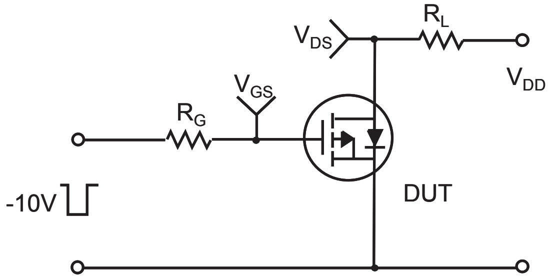
Figure 11. Transient Thermal Response Curve

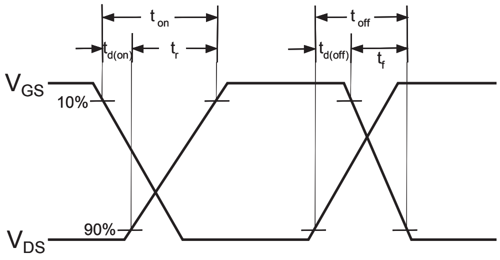
Gate Charge Test Circuit & Waveform



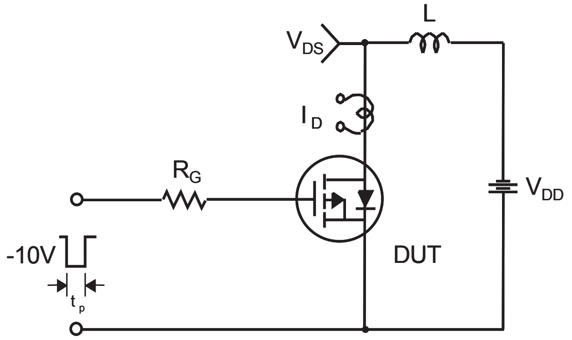


Resistive Switching Test Circuit & Waveforms

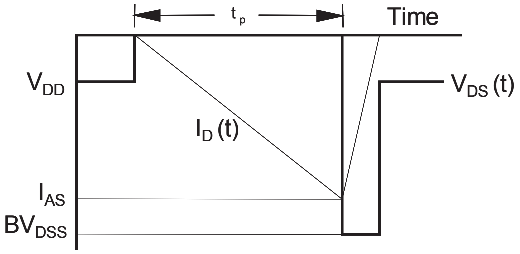




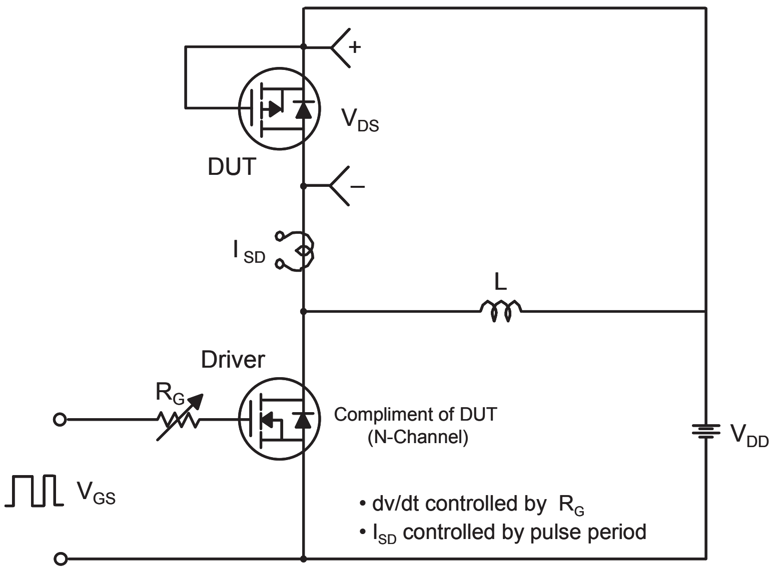
Unclamped Inductive Switching Test Circuit & Waveforms

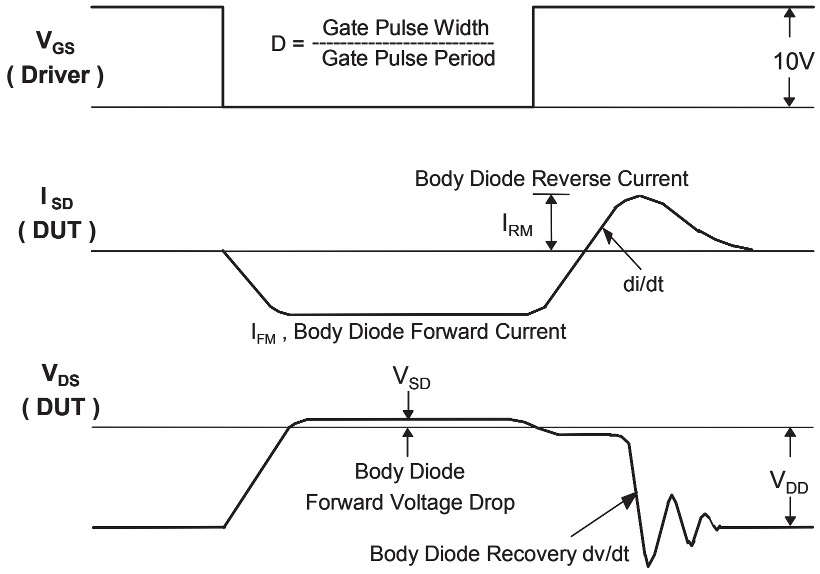


$$E_{AS} = \frac{1}{2} L I_{AS}^{2} \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



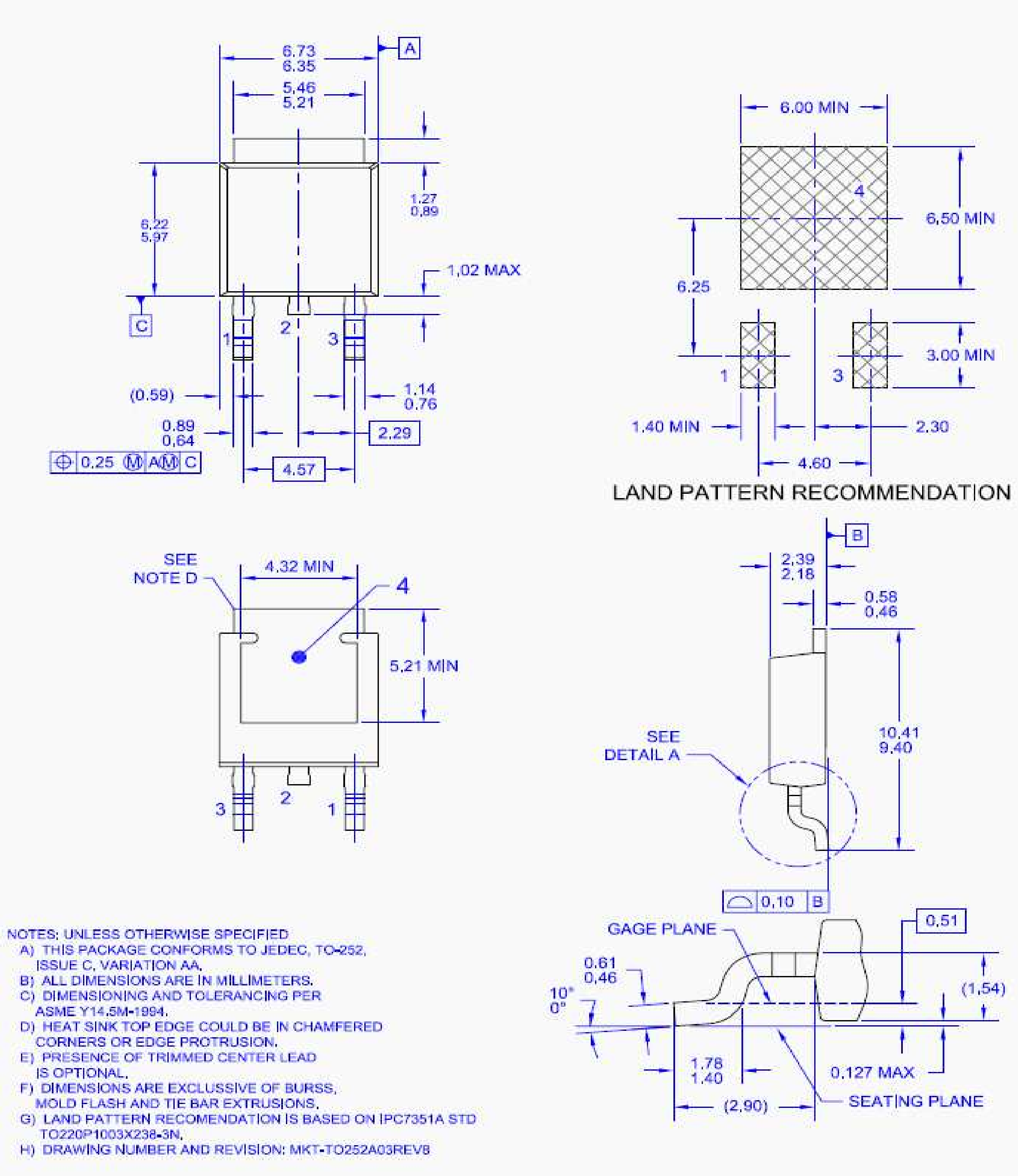
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Package Dimensions

D-PAK



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.

E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

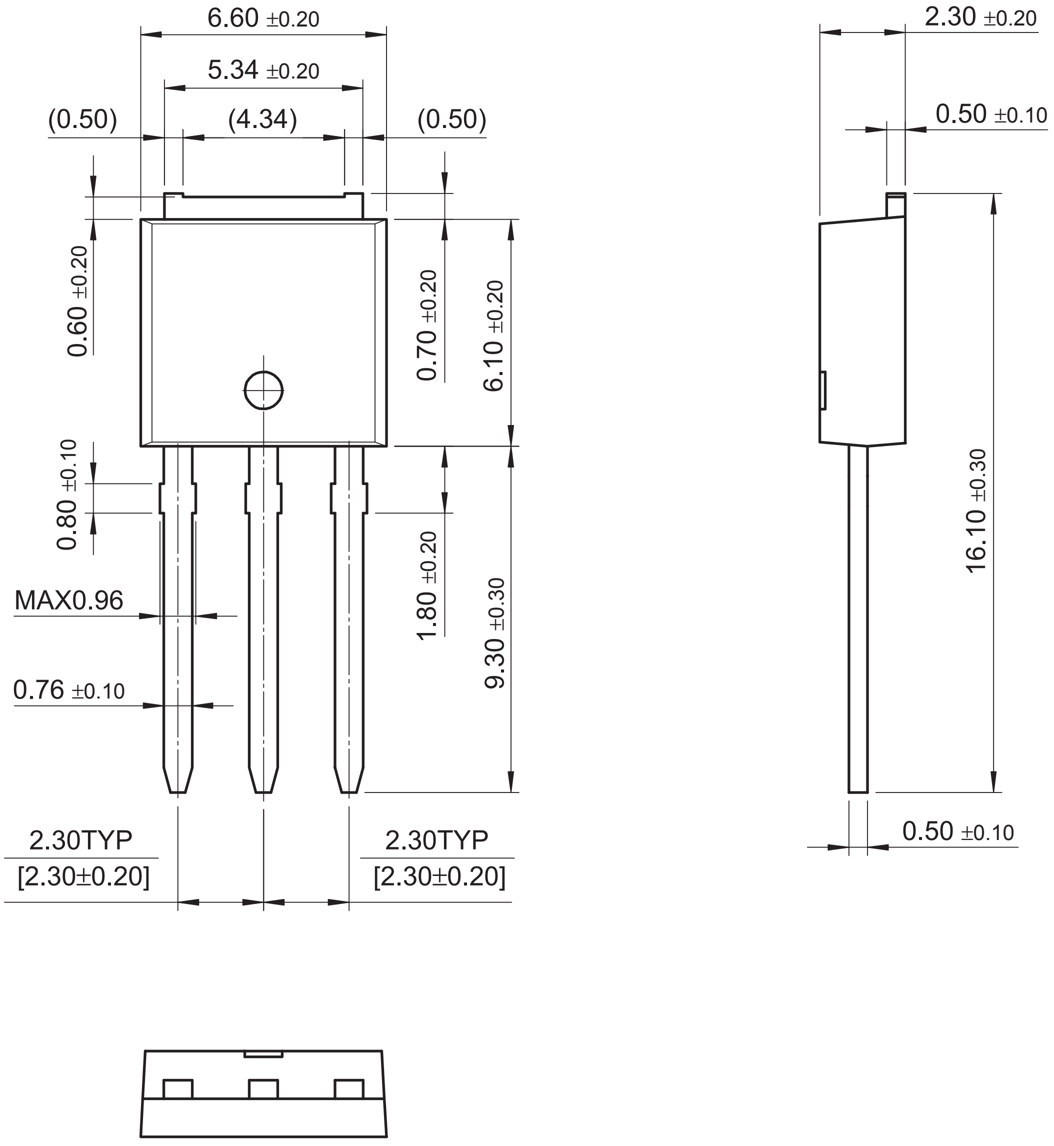
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.

G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.

H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV8

Package Dimensions (Continued)

IPAK



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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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