

April 2008

FJD5553 NPN Silicon Transistor

High Voltage Switch Mode Application

- Fast Speed Switching
- Wide Safe Operating Area
- Suitable for ElectronicBallast Application



Absolute Maximum Ratings * T_C=25°C unless otherwise noted

Symbol	Parameter	Value	Units
BV _{CBO}	Collector-Base Voltage	1050	V
BV _{CEO}	Collector-Emitter Voltage	400	V
BV _{EBO}	Emitter-Base Voltage	14	V
I _C	Collector Current (DC)	3	А
I _{CP} Collector Current (Pulse)		6	A
I _B	Base Current (DC)	1	А
I _{BP}	Collector Current (Pulse)	2	А
P _C	Collector Dissipation	1.25	W
TJ	Junction Temperature	150	°C
T _{STG}	Storage Junction Temperature Range	- 55 ~ 150	°C

^{*} These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Thermal Characteristics Ta=25°C unless otherwise noted

Symbol	Parameter	Value	Units
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	100	°C/W

^{*} Device mounted on minimum pad size

Ordering Information

Part Number	Marking	Package	Packing Method	Remarks
FJD5553TM	J5553	D-PAK	Tape & Reel	

Electrical Characteristics * T_C =25°C unless otherwise noted

Symbol	Parameter	Conditions	Min.	Тур.	Max	Units
BV _{CBO}	Collector-Base Breakdown Voltage	I _C =500μA, I _E =0	1050			٧
BV _{CEO}	Collector-Emitter Breakdown Voltage	I _C =5mA, I _B =0	400			٧
BV _{EBO}	Emitter-Base Breakdown Voltage	I _E =500μA, I _C =0	14			٧
h _{FE}	* DC Current Gain	V _{CE} =5V, I _C =10mA	10			
		V _{CE} =3V, I _C =0.4A	30		60	
V _{CE} (sat)	Collector-Emitter Saturation Voltage	I _C =1A, I _B =0.2A		0.23	0.5	V
V _{BE} (sat)	Base-Emitter Saturation Voltage	I _C =1A, I _B =0.2A			1.2	V
C _{ob}	Output Capacitance	V _{CB} =10V, f=1MHz		45		pF
t _{ON}	Turn On Time	V _{CC} =125V, I _C =0.5A			1.0	μS
t _{STG}	Storage Time	I _{B1} =45mA, I _{B2} =0.5A R _L =250Ω			1.2	μS
t _F	Fall Time			0.3		μS
t _{ON}	Turn On Time	V _{CC} =250V, I _C =2.5A			2.0	μS
t _{STG}	Storage Time	I _{B1} =0.5A, I _{B2} =1.0A R _L =100Ω			2.5	μS
t _F	Fall Time				0.3	μS
EAS	Avalanche Energy	L= 2mH	3.5			mJ

^{*} Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%

Typical Characteristics

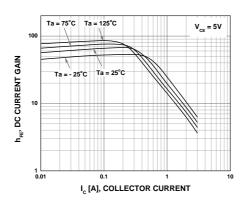


Figure 1. DC Current Gain

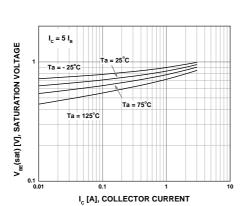


Figure 3. Saturation Voltage

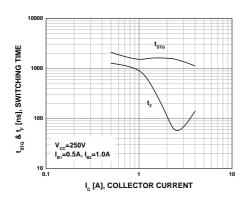


Figure 5. Resistive Load Switching

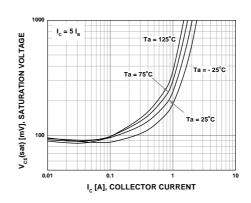


Figure 2. Saturation Voltage

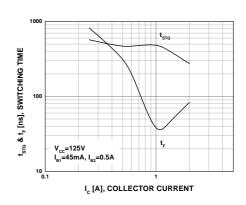


Figure 4. Resistive Load Switching

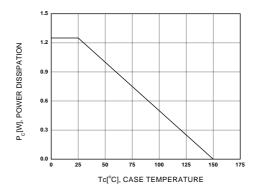
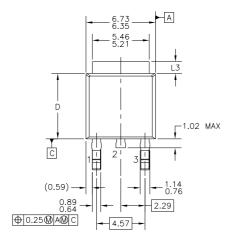
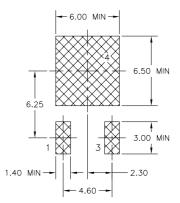


Figure 6. Power Derating

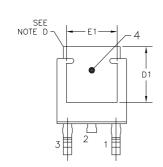
Mechanical Dimensions

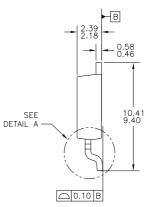
D-PAK

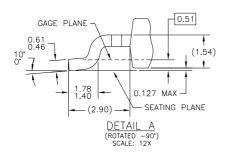




LAND PATTERN RECOMMENDATION







- NOTES: UNLESS OTHERWISE SPECIFIED

 A) ALL DIMENSIONS ARE IN MILLIMETERS.

 B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.

 C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

 D) HEAT SINK TOP EOGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.

 E) DIMENSIONS L3,D,E1&D1 TABLE:

 [OPTION AA | OPTION AB]

		OPTION AA	OPTION AB	
	L3	0.89-1.27	1.52-2.03	
	D	5.97-6.22	5.33-5.59	
	E1	4.32 MIN	3.81 MIN	
	D1	5.21 MIN	4.57 MIN	
_ :				

PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Dimensions in Millimeters





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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification		Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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