FAIRCHILD SEMICONDUCTOR®

May 2009

Ultrafast Rectifier

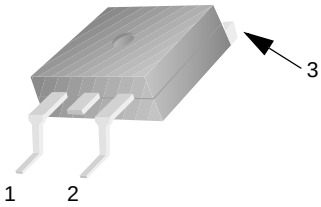
FFD20UP20S

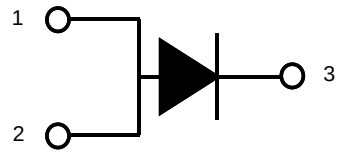
Features

- Ultrafast with soft recovery, trr <45ns
- Reverse Voltage, V_{RRM}=200V
- Forward Voltage < 1.05V @ T_C =100°C
- RoHS compliant

Applications

- Power switching circuits
- Output rectifiers
- Freewheeling diodes
- Switching mode power supply





1, 2 ANODE 3. CATHODE (FLANGE)

Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{RRM}	Peak Repetitive Reverse Voltage	200	V
$I_{F(AV)}$	Average Rectified Forward Current @ T_C = 123°C	20	A
I_{FSM}	Non-repetitive Peak Surge Current 60Hz Single Half-Sine Wave	200	A
T_J, T_{STG}	Operating and Storage Temperature Range	-65 to +150	°C

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Maximum Thermal Resistance, Junction to Case	1.9	°C/W

Package Marking and Ordering Information

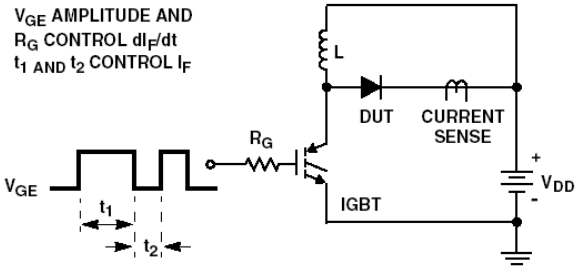
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
F20UP20S	FFD20UP20S	D-PAK	13” Dia	-	2500

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

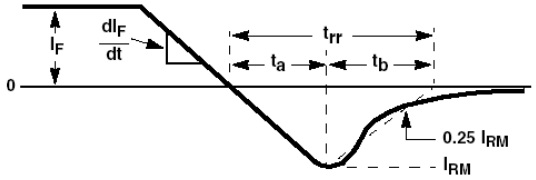
Symbol	Parameter		Min.	Typ.	Max.	Units
V_{FM}*	Maximum Instantaneous Forward Voltage I_F = 20A I_F = 20A I_F = 30A	 $T_C = 25^oC$ $T_C = 100^oC$ $T_C = 25^oC$	 - - -	 0.94 0.84 1.00	 1.15 1.05 -	V
I_{RM}*	Maximum Instantaneous Reverse Current @ rated V_R	$T_C = 25^oC$ $T_C = 100^oC$	- -	- -	100 500	μA
t_{rr}	Reverse Recovery Time (I_F = 20A, di/dt = 200A/μs)		-	22	45	ns
W_{AVL}	Avalanche Energy (L = 40mH)		20	-	-	mJ

* Pulse Test: Pulse Width = 300μs, Duty Cycle = 2%

*

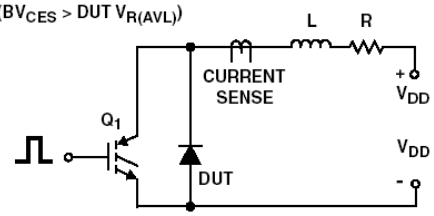


t_{rr} TEST CIRCUIT

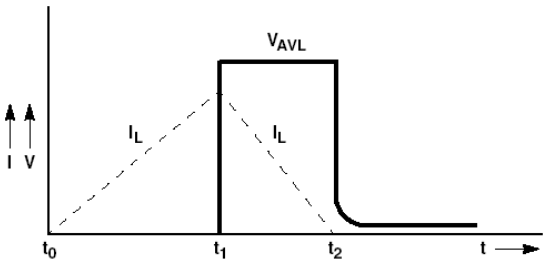


t_{rr} WAVEFORMS AND DEFINITIONS

I_{MAX} = 1A
L = 40mH
R < 0.1Ω
$E_{AVL} = 1/2LI^2 [V_{R(AVL)}/(V_{R(AVL)} - V_{DD})]$
Q_1 = IGBT (BV_{CES} > DUT $V_{R(AVL)}$)



AVALANCHE ENERGY TEST CIRCUIT



AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

Test Circuit and Waveforms

Typical Performance Characteristics

Figure 1. Typical Forward Voltage Drop vs. Forward Current

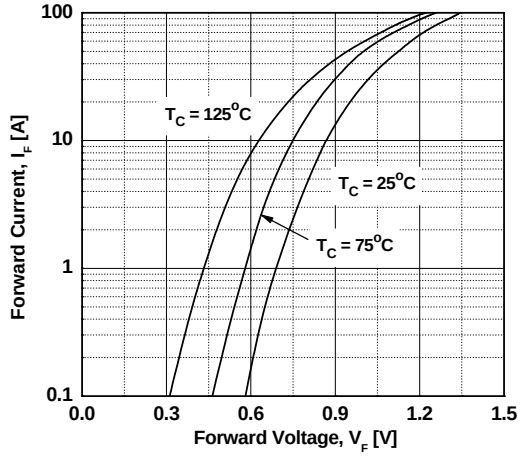


Figure 2. Typical Reverse Current vs. Reverse Voltage

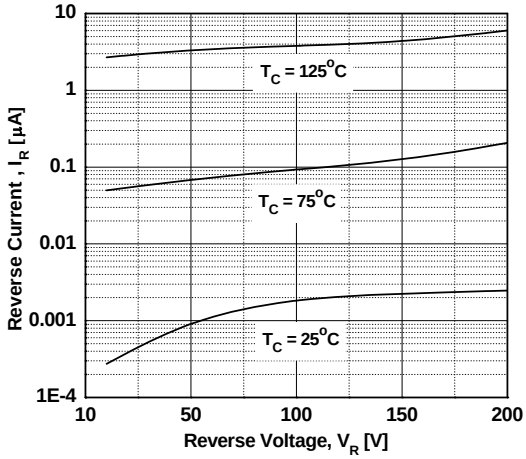


Figure 3.Typical Junction Capacitance

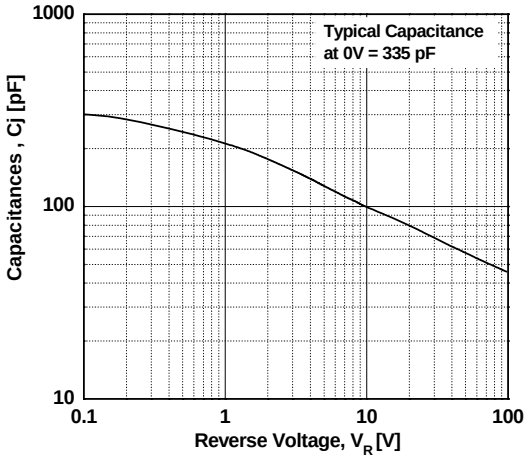


Figure 4. Typical Reverse Recovery Time vs. di/dt

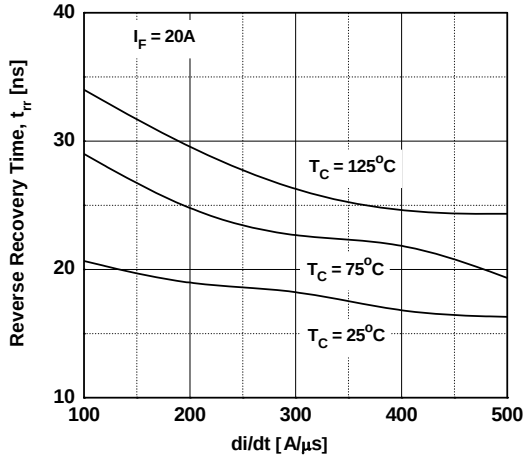


Figure 5. Typical Reverse Recovery Current vs. di/dt

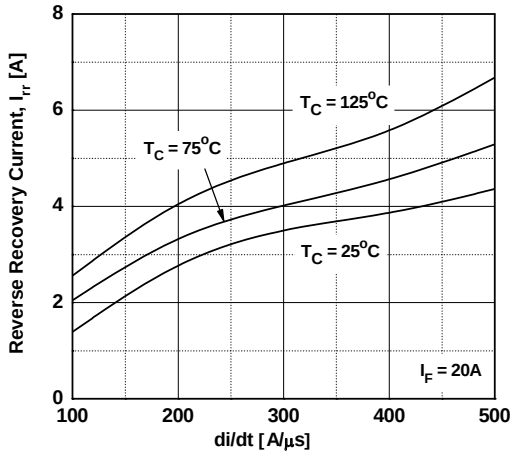
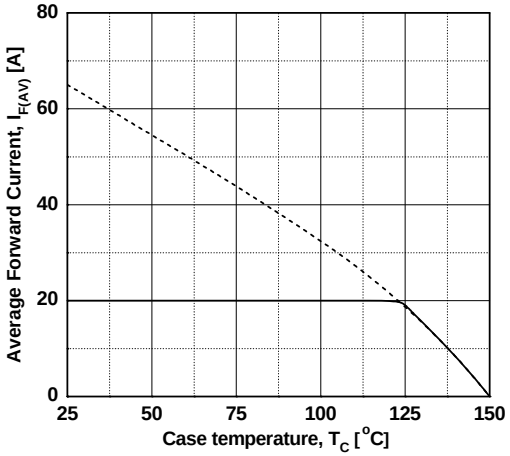
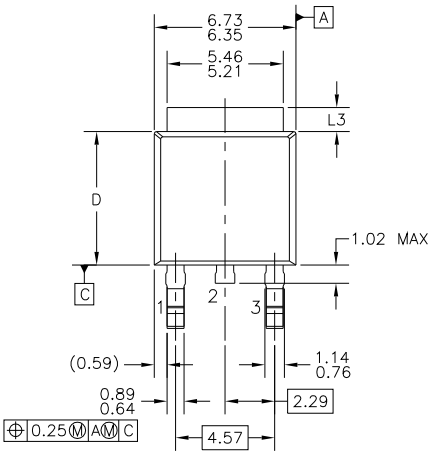


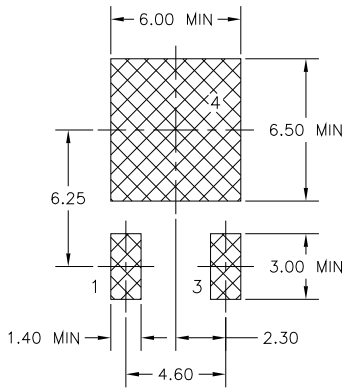
Figure 6. Forward Current Derating Curve



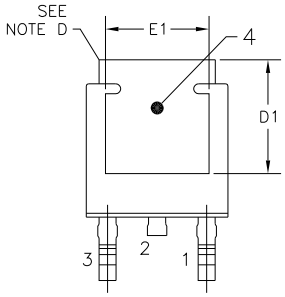
Mechanical Dimensions

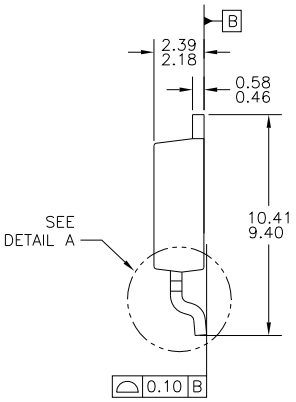
D-PAK

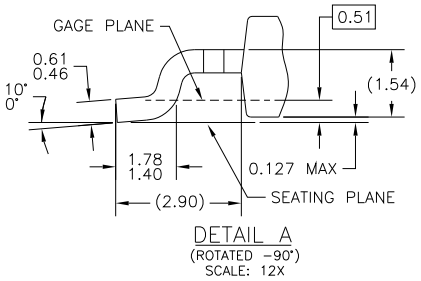




LAND PATTERN RECOMMENDATION







DETAIL A
(ROTATED −90°)
SCALE: 12X

NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.

B) THIS PACKAGE CONFORMS TO JEDEC, TO−252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.

C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.

E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION AA	OPTION AB
L3	0.89−1.27	1.52−2.03
D	5.97−6.22	5.33−5.59
E1	4.32 MIN	3.81 MIN
D1	5.21 MIN	4.57 MIN

F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Dimensions in Millimeters

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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