FAIRCHILD SEMICONDUCTOR®

December 2007

# 74ABT374
# Octal D-Type Flip-Flop with 3-STATE Outputs

## Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- 3-STATE outputs for bus-oriented applications
- Output sink capability of 64mA, source capability of 32mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50pF and 250pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High-impedance, glitch-free bus loading during entire power up and power down cycle
- Nondestructive, hot-insertion capability

## General Description

The ABT374 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

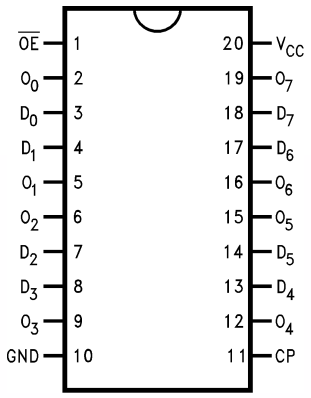
## Ordering Information

| Order Number | Package Number | Package Description |
|---|---|---|
| 74ABT374CSC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74ABT374CSJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74ABT374CMSA | MSA20 | 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide |
| 74ABT374CMTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

## Connection Diagram




## Pin Descriptions

| Pin Names | Description |
|---|---|
| $D_0$–$D_7$ | Data Inputs |
| CP | Clock Pulse Input (Active Rising Edge) |
| $\overline{OE}$ | 3-STATE Output Enable Input (Active LOW) |
| $O_0$–$O_7$ | 3-STATE Outputs |

## Functional Description

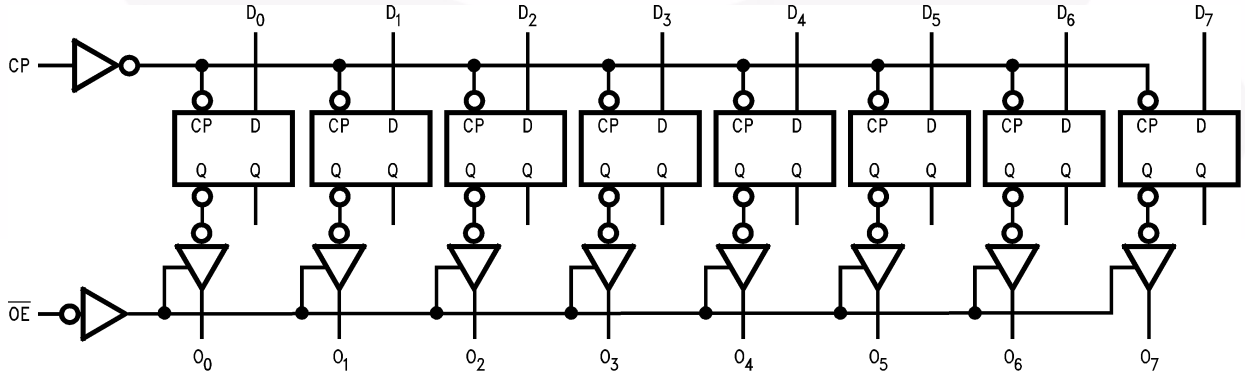
The ABT374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs are in a high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

## Function Table

| Inputs | | | Internal | Outputs | |
|---|---|---|---|---|---|
| $\overline{OE}$ | CP | D | Q | O | Function |
| H | H | L | NC | Z | Hold |
| H | H | H | NC | Z | Hold |
| H | ↗ | L | L | Z | Load |
| H | ↗ | H | H | Z | Load |
| L | ↗ | L | L | L | Data Available |
| L | ↗ | H | H | H | Data Available |
| L | H | L | NC | NC | No Change in Data |
| L | H | H | NC | NC | No Change in Data |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

## Logic Diagram




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|---|---|---|
| $T_{STG}$ | Storage Temperature | –65°C to +150°C |
| $T_A$ | Ambient Temperature Under Bias | –55°C to +125°C |
| $T_J$ | Junction Temperature Under Bias | –55°C to +150°C |
| $V_{CC}$ | $V_{CC}$ Pin Potential to Ground Pin | –0.5V to +7.0V |
| $V_{IN}$ | Input Voltage(1) | –0.5V to +7.0V |
| $I_{IN}$ | Input Current(1) | –30mA to +5.0mA |
| $V_O$ | Voltage Applied to Any Output | |
| | Disabled or Power-Off State | –0.5V to 5.5V |
| | HIGH State | –0.5V to $V_{CC}$ |
| | Current Applied to Output in LOW State (Max.) | twice the rated $I_{OL}$ (mA) |
| | DC Latchup Source Current Across Common Operating Range | |
| | $\overline{OE}$ Pin | –150mA |
| | Other Pins | –500mA |
| | Over Voltage Latchup (I/O) | 10V |

**Note:**

1. Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Rating |
|---|---|---|
| $T_A$ | Free Air Ambient Temperature | –40°C to +85°C |
| $V_{CC}$ | Supply Voltage | +4.5V to +5.5V |
| $\Delta V / \Delta t$ | Minimum Input Edge Rate | |
| | Data Input | 50mV/ns |
| | Enable Input | 20mV/ns |
| | Clock Input | 100mV/ns |

## DC Electrical Characteristics

| Symbol | Parameter | | $V_{CC}$ | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | | Recognized HIGH Signal | 2.0 | | | V |
| $V_{IL}$ | Input LOW Voltage | | | Recognized LOW Signal | | | 0.8 | V |
| $V_{CD}$ | Input Clamp Diode Voltage | | Min. | $I_{IN}$ = –18mA | | | –1.2 | V |
| $V_{OH}$ | Output HIGH Voltage | | Min. | $I_{OH}$ = –3mA | 2.5 | | | V |
| | | | | $I_{OH}$ = –32mA | 2.0 | | | |
| $V_{OL}$ | Output LOW Voltage | | Min. | $I_{OL}$ = 64mA | | | 0.55 | V |
| $I_{IH}$ | Input HIGH Current | | Max. | $V_{IN}$ = 2.7V(3) | | | 1 | µA |
| | | | | $V_{IN}$ = $V_{CC}$ | | | 1 | |
| $I_{BVI}$ | Input HIGH Current Breakdown Test | | Max. | $V_{IN}$ = 7.0V | | | 7 | µA |
| $I_{IL}$ | Input LOW Current | | Max. | $V_{IN}$ = 0.5V(3) | | | –1 | µA |
| | | | | $V_{IN}$ = 0.0V | | | –1 | |
| $V_{ID}$ | Input Leakage Test | | 0.0 | $I_{ID}$ = 1.9µA, All Other Pins Grounded | 4.75 | | | V |
| $I_{OZH}$ | Output Leakage Current | | 0–5.5V | $V_{OUT}$ = 2.7V, $\overline{OE}$ = 2.0V | | | 10 | µA |
| $I_{OZL}$ | Output Leakage Current | | 0–5.5V | $V_{OUT}$ = 0.5V, $\overline{OE}$ = 2.0V | | | –10 | µA |
| $I_{OS}$ | Output Short-Circuit Current | | Max. | $V_{OUT}$ = 0.0V | –100 | | –275 | mA |
| $I_{CEX}$ | Output HIGH Leakage Current | | Max. | $V_{OUT}$ = $V_{CC}$ | | | 50 | µA |
| $I_{ZZ}$ | Bus Drainage Test | | 0.0 | $V_{OUT}$ = 5.5V, All Others $V_{CC}$ or GND | | | 100 | µA |
| $I_{CCH}$ | Power Supply Current | | Max. | All Outputs HIGH | | | 50 | µA |
| $I_{CCL}$ | Power Supply Current | | Max. | All Outputs LOW | | | 30 | mA |
| $I_{CCZ}$ | Power Supply Current | | Max. | $\overline{OE}$ = $V_{CC}$, All Others at $V_{CC}$ or GND | | | 50 | µA |
| $I_{CCT}$ | Additional $I_{CC}$/Input | Outputs Enabled | Max. | $V_I$ = $V_{CC}$ – 2.1V | | | 2.5 | mA |
| | | Outputs 3-STATE | | Enable Input $V_I$ = $V_{CC}$ – 2.1V | | | 2.5 | mA |
| | | Outputs 3-STATE | | Data Input $V_I$ = $V_{CC}$ – 2.1V, All Others at $V_{CC}$ or GND | | | 2.5 | mA |
| $I_{CCD}$ | Dynamic $I_{CC}$ No Load(4) | | Max. | Outputs OPEN, $\overline{OE}$ = GND(2), One-Bit Toggling, 50% Duty Cycle | | | 0.30 | mA/ MHz |

**Notes:**

2. For 8-bit toggling, $I_{CCD}$ < 0.8mA/MHz.
3. Guaranteed, but not tested.

## DC Electrical Characteristics

SOIC package.

| Symbol | Parameter | $V_{CC}$ | Conditions $C_L = 50pF$, $R_L = 500\Omega$ | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 5.0 | $T_A = 25°C$[4] | | 0.5 | 0.8 | V |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | 5.0 | $T_A = 25°C$[4] | –1.3 | –0.9 | | V |
| $V_{OHV}$ | Minimum HIGH Level Dynamic Output Voltage | 5.0 | $T_A = 25°C$[5] | 2.5 | 3.0 | | V |
| $V_{IHD}$ | Minimum HIGH Level Dynamic Input Voltage | 5.0 | $T_A = 25°C$[6] | 2.0 | 1.6 | | V |
| $V_{ILD}$ | Maximum LOW Level Dynamic Input Voltage | 5.0 | $T_A = 25°C$[6] | | 1.3 | 0.8 | V |

**Notes:**

4. Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at Low. Guaranteed, but not tested.
5. Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.
6. Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold ($V_{ILD}$), 0V to threshold ($V_{IHD}$). Guaranteed, but not tested.

## AC Electrical Characteristics

SOIC and SSOP package.

| Symbol | Parameter | $T_A = +25°C$, $V_{CC} = +5V$, $C_L = 50pF$ | | | $T_A = –55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50pF$ | | $T_A = –40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50pF$ | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $f_{MAX}$ | Maximum Clock Frequency | 150 | 200 | | 150 | | 150 | | MHz |
| $t_{PLH}$ | Propagation Delay | 2.0 | 3.2 | 5.0 | 1.4 | 6.6 | 2.0 | 5.0 | ns |
| $t_{PHL}$ | CP to $O_n$ | 2.0 | 3.3 | 5.0 | 2.0 | 7.6 | 2.0 | 5.0 | |
| $t_{PZH}$ | Output Enable Time | 1.5 | 3.1 | 5.3 | 0.8 | 5.7 | 1.5 | 5.3 | ns |
| $t_{PZL}$ | | 1.5 | 3.1 | 5.3 | 1.5 | 7.2 | 1.5 | 5.3 | |
| $t_{PHZ}$ | Output Disable Time | 1.5 | 3.6 | 5.4 | 1.3 | 7.2 | 1.5 | 5.4 | ns |
| $t_{PLZ}$ | | 1.5 | 3.4 | 5.4 | 1.0 | 7.0 | 1.5 | 5.4 | |

## AC Operating Requirements

| Symbol | Parameter | $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$ | | $T_A = –55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50pF$ | | $T_A = –40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50pF$ | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_S(H)$ | Setup Time, HIGH or LOW $D_n$ to CP | 1.5 | | 2.5 | | 1.0 | | ns |
| $t_S(L)$ | | 1.5 | | 2.5 | | 1.5 | | |
| $t_H(H)$ | Hold Time, HIGH or LOW $D_n$ to CP | 1.0 | | 2.5 | | 1.0 | | ns |
| $t_H(L)$ | | 1.0 | | 2.5 | | 1.0 | | |
| $t_W(H)$ | Pulse Width, CP HIGH or LOW | 3.0 | | 3.3 | | 3.0 | | ns |
| $t_W(L)$ | | 3.0 | | 3.3 | | 3.0 | | |

## Extended AC Electrical Characteristics

SOIC package.

| Symbol | Parameter | $T_A = –40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50pF$, 8 Outputs Switching[7] | | $T_A = –40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250pF$[8] | | $T_A = –40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250pF$, 8 Outputs Switching[9] | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay CP to $O_n$ | 1.5 | 5.7 | 2.0 | 7.8 | 2.0 | 10.0 | ns |
| $t_{PHL}$ | | 1.5 | 5.7 | 2.0 | 7.8 | 2.0 | 10.0 | |
| $t_{PZH}$ | Output Enable Time | 1.5 | 6.2 | 2.0 | 8.0 | 2.0 | 10.5 | ns |
| $t_{PZL}$ | | 1.5 | 6.2 | 2.0 | 8.0 | 2.0 | 10.5 | |
| $t_{PHZ}$ | Output Disable Time | 1.0 | 5.5 | [10] | | [10] | | ns |
| $t_{PZL}$ | | 1.0 | 5.5 | | | | | |

**Notes:**

7. This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).
8. This specification is guaranteed but not tested. The limits represent propagation delay with 250pF load capacitors in place of the 50pF load capacitors in the standard AC load. This specification pertains to single output switching only.
9. This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250pF load capacitors in place of the 50pF load capacitors in the standard AC load.
10. The 3-STATE delay Time is dominated by the RC network (500Ω, 250pF) on the output and has been excluded from the datasheet.

## Skew[15]

SOIC package.

| Symbol | Parameter | $T_A = -40°C$ to $+85°C$<br>$V_{CC} = 4.5V–5.5V$<br>$C_L = 50$ pF<br>8 Outputs Switching[11]<br>Max. | $T_A = -40°C$ to $+85°C$<br>$V_{CC} = 4.5V–5.5V$<br>$C_L = 250$ pF<br>8 Outputs Switching[12]<br>Max. | Units |
|---|---|---|---|---|
| $t_{OSHL}$[13] | Pin to Pin Skew, HL Transitions | 1.0 | 1.8 | ns |
| $t_{OSLH}$[13] | Pin to Pin Skew, LH Transitions | 1.0 | 1.8 | ns |
| $t_{PS}$[12] | Duty Cycle, LH–HL Skew | 1.8 | 4.3 | ns |
| $t_{OST}$[13] | Pin to Pin Skew, LH/HL Transitions | 2.0 | 4.3 | ns |
| $t_{PV}$[14] | Device to Device Skew, LH/HL Transitions | 2.5 | 4.6 | ns |

**Notes:**

11. This specification is guaranteed but not tested. The limits represent propagation delays with 250pF load capacitors in place of the 50pF load capacitors in the standard AC load.
12. This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.
13. Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW ($t_{OSHL}$), LOW-to-HIGH ($t_{OSLH}$), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW ($t_{OST}$). This specification is guaranteed but not tested.
14. Propagation delay variation for a given set of conditions (i.e., temperature and $V_{CC}$) from device to device. This specification is guaranteed but not tested.
15. This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

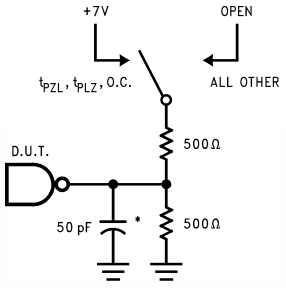
## Capacitance

| Symbol | Parameter | Conditions<br>$T_A = 25°C$ | Typ. | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC} = 0V$ | 5.0 | pF |
| $C_{OUT}$[16] | Output Capacitance | $V_{CC} = 5.0V$ | 9.0 | pF |

**Note:**

16. $C_{OUT}$ is measured at frequency f = 1MHz, per MIL-STD-883, Method 3012.

## AC Loading




*Includes jig and probe capacitance

**Figure 1. Standard AC Test Load**

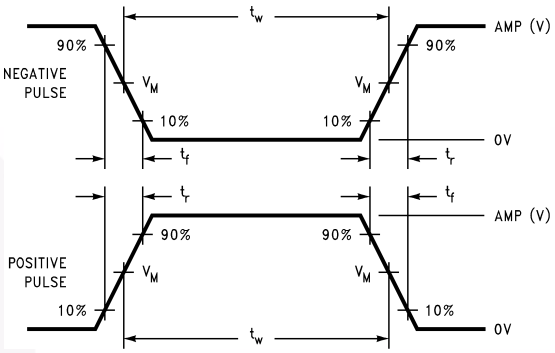



**Figure 2. $V_M$ = 1.5V**

**Input Pulse Requirements**

| Amplitude | Rep. Rate | $t_w$ | $t_r$ | $t_f$ |
|---|---|---|---|---|
| 3.0V | 1 MHz | 500ns | 2.5ns | 2.5ns |

**Figure 3. Test Input Signal Requirements**

## AC Waveforms

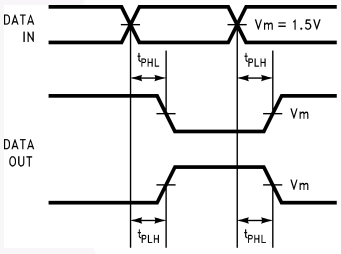



**Figure 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**

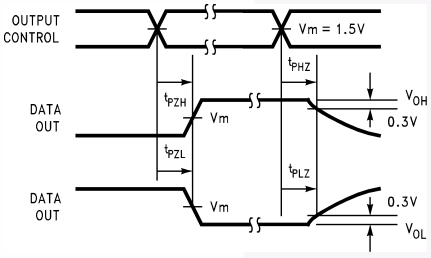



**Figure 6. 3-STATE Output HIGH and LOW Enable and Disable Times**

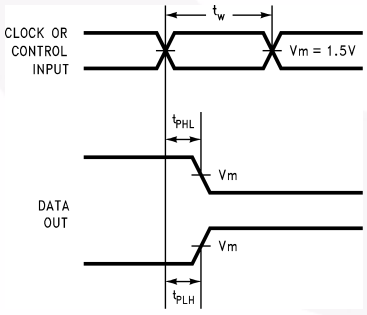



**Figure 5. Propagation Delay, Pulse Width Waveforms**

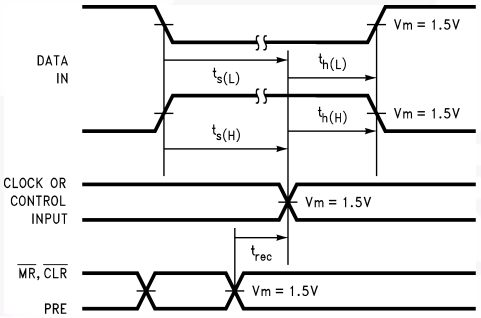



**Figure 7. Setup Time, Hold Time and Recovery Time Waveforms**

## Physical Dimensions

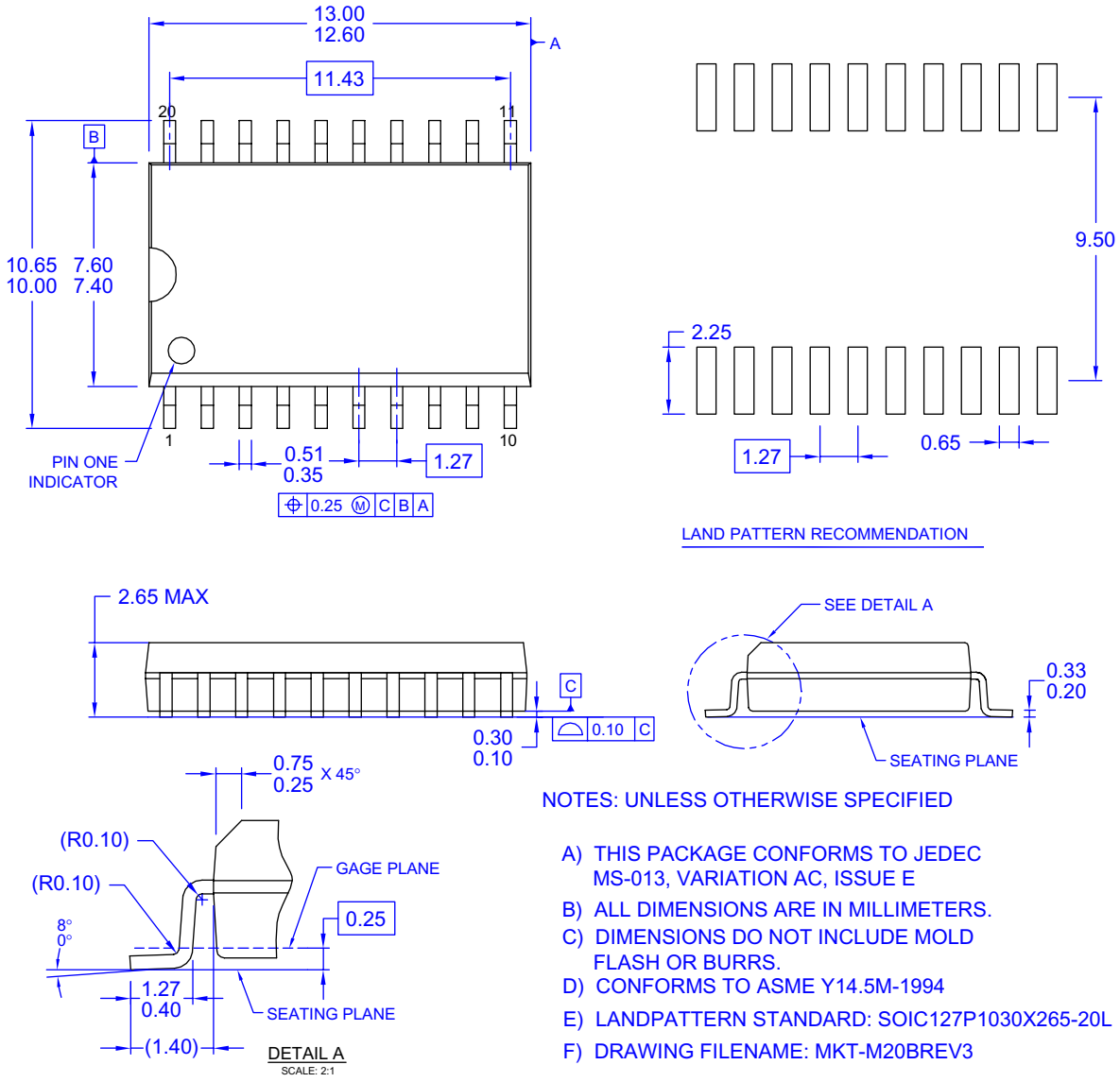



**Figure 8. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide**

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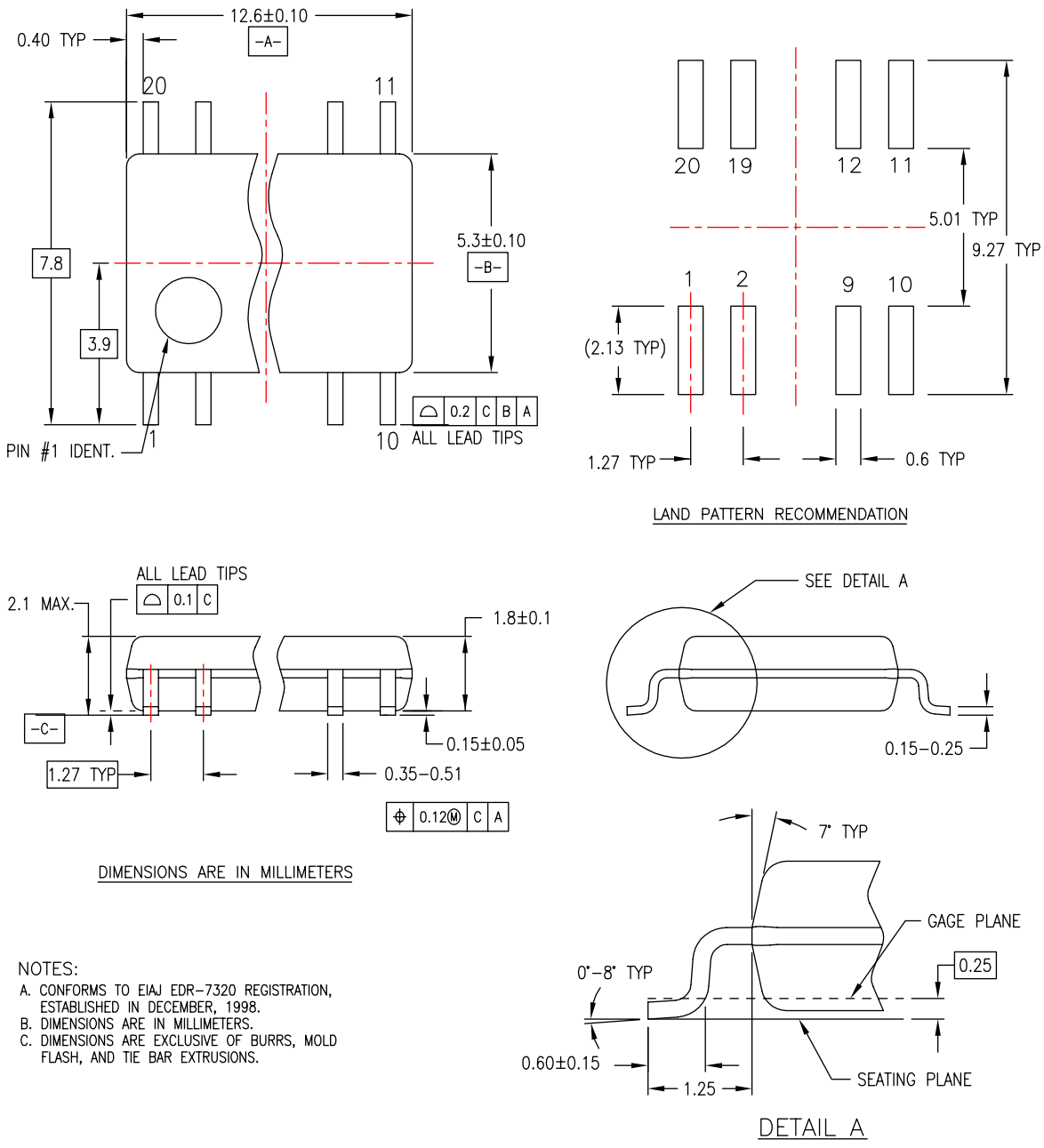
## Physical Dimensions (Continued)




NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

**Figure 9. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**

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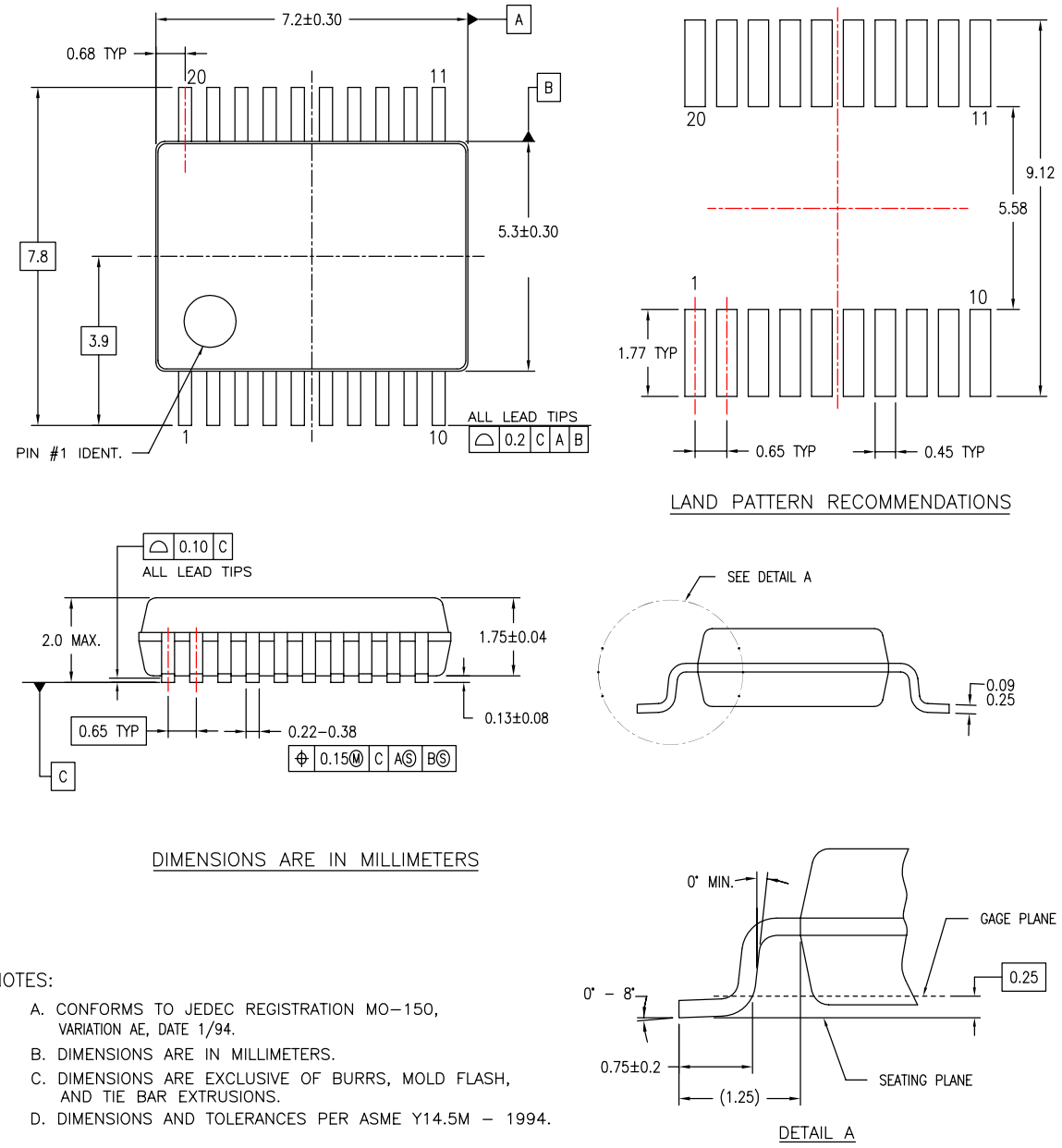
## Physical Dimensions (Continued)




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–150, VARIATION AE, DATE 1/94.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M – 1994.

MSA20REVB

**Figure 10. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide**

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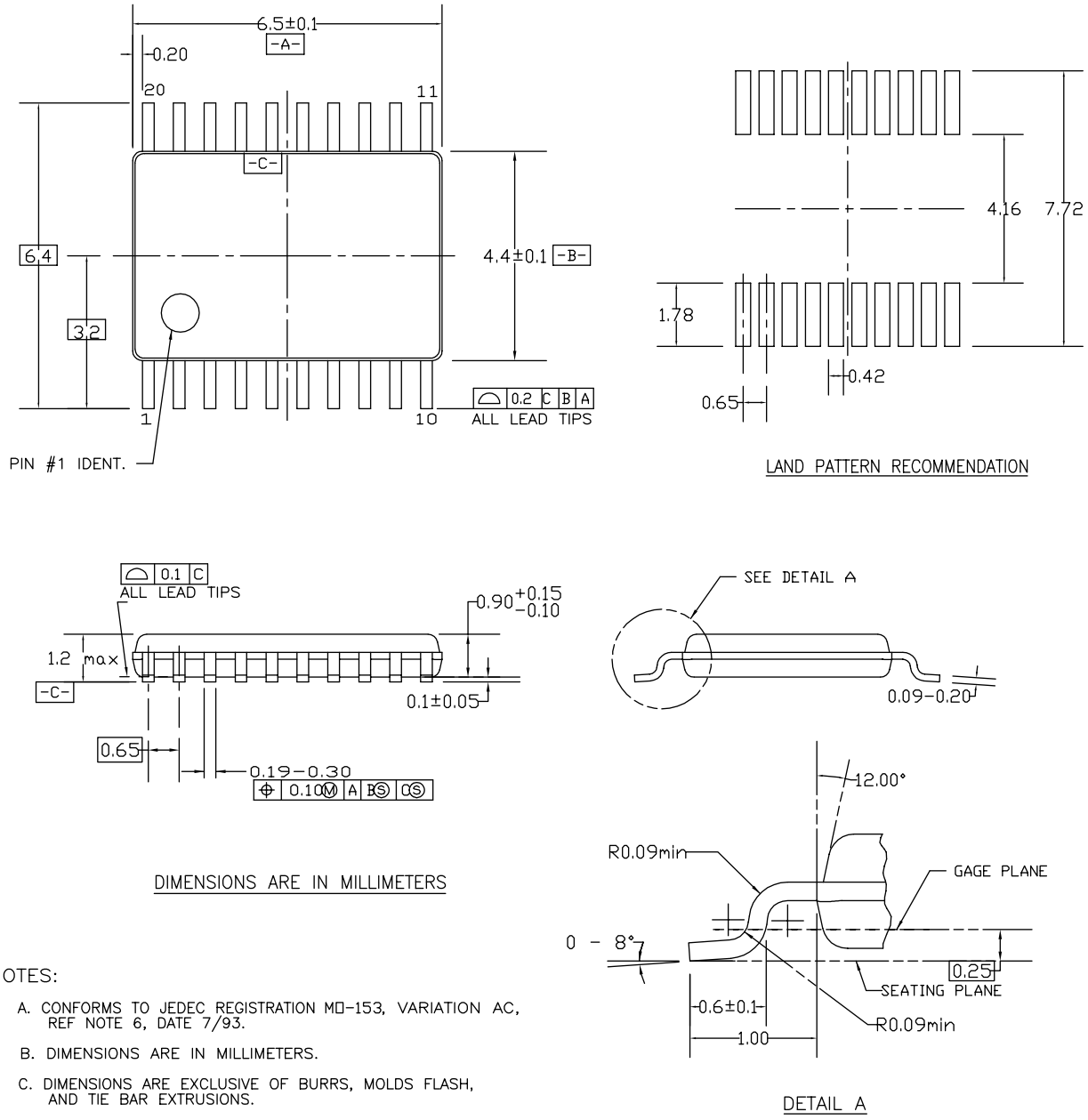
## Physical Dimensions (Continued)




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

**Figure 11. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**

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