

March 1994 Revised May 2005

# 74ABT16374 16-Bit D-Type Flip-Flop with 3-STATE Outputs

#### **General Description**

The ABT16374 contains sixteen non-inverting D-type flipflops with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable  $\overline{(\text{OE})}$  are common to each byte and can be shorted together for full 16-bit operation.

#### **Features**

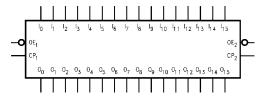
- Separate control logic for each byte
- 16-bit version of the ABT374
- Edge-triggered D-type inputs
- Buffered Positive edge-triggered clock
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Guaranteed latch-up protection

### **Ordering Code:**

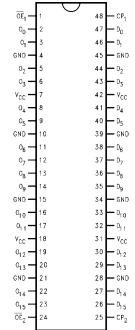
Order Number	Package Number	Package Description				
74ABT16374CSSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide				
74ABT16374CMTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide				

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### **Logic Symbol**



# **Connection Diagram**



#### **Pin Descriptions**

Pin Name	Description			
ŌĒn	3-STATE Output Enable Input (Active LOW)			
CP <sub>n</sub>	Clock Pulse Input (Active Rising Edge)			
D <sub>0</sub> -D <sub>15</sub>	Data Inputs			
O <sub>0</sub> -O <sub>15</sub>	3-STATE Outputs			

## **Functional Description**

The ABT16374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CPn) transition. With the Output Enable  $(\overline{OE}_n)$  LOW, the contents of the flip-flops are available at the outputs. When  $\overline{\text{OE}}_n$  is HIGH, the outputs go to the high impedance state. Operation of the OE<sub>n</sub> input does not affect the state of the flip-flops.

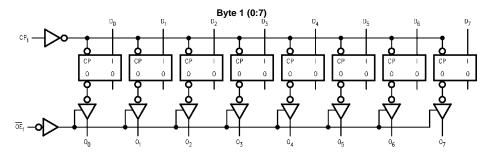
#### **Truth Tables**

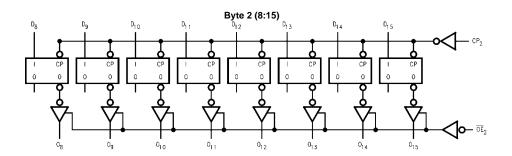
	Inputs		Outputs
CP <sub>1</sub>	OE <sub>1</sub>	D <sub>0</sub> -D <sub>7</sub>	O <sub>0</sub> -O <sub>7</sub>
\	L	Н	Н
~	L	L	L
L	L	Х	(Previous)
Х	Н	Х	Z

	Inputs	Outputs	
CP <sub>2</sub>	O <sub>8</sub> -O <sub>15</sub>		
~	L	Н	Н
~	L	L	L
L	L	Χ	(Previous)
X	Н	Χ	Z

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial Z = High Impedance

### **Logic Diagrams**





-40°C to +85°C

+4.5V to +5.5V

50 mV/ns

20 mV/ns

100mV/ns

### **Absolute Maximum Ratings**(Note 1)

**Recommended Operating Conditions** 

Free Air Ambient Temperature

Minimum Input Edge Rate ( $\Delta V/\Delta t$ )

Supply Voltage

Data Input

Enable Input

Clock Input

-65°C to +150°C Storage Temperature

-55°C to +125°C Ambient Temperature under Bias Junction Temperature under Bias  $-55^{\circ}C$  to  $+150^{\circ}C$ 

V<sub>CC</sub> Pin Potential to Ground Pin -0.5V to +7.0V

Input Voltage (Note 2) -0.5V to +7.0VInput Current (Note 2) -30 mA to +5.0 mA

Voltage Applied to Any Output

in the Disabled or

Power-Off State -0.5V to 5.5Vin the HIGH State -0.5V to  $V_{CC}$ 

Current Applied to Output

in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

DC Latchup Source Current:

OE Pin -350 mA

(Across Comm Operating Range)

Other Pins -500 mA

Over Voltage Latchup (I/O)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.  $10V\quad \text{Note 2: } \text{Either voltage limit or current limit is sufficient to protect inputs.}$ 

## **DC Electrical Characteristics**

Symbol	Param	eter	Min	Тур	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Vo	oltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage		2.5			V	Min	I <sub>OH</sub> = -3 mA
			2.0			V	Min	I <sub>OH</sub> = -32 mA
V <sub>OL</sub>	Output LOW Voltage				0.55	V	Min	I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current				1	μА	Max	V <sub>IN</sub> = 2.7V (Note 3)
					1	μΛ	IVIAX	$V_{IN} = V_{CC}$
I <sub>BVI</sub>	Input HIGH Current B	reakdown Test			7	μА	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current				-1	μΑ Мах	V <sub>IN</sub> = 0.5V (Note 3)	
					-1	,	IVICA	$V_{IN} = 0.0V$
$V_{ID}$	Input Leakage Test		4.75			V 0.0 I <sub>II</sub>	I <sub>ID</sub> = 1.9 μA	
								All Other Pins Grounded
I <sub>OZH</sub>	Output Leakage Curre	ent			10	μА	0-5.5V	$V_{OUT} = 2.7V; \overline{OE} = 2.0V$
l <sub>OZL</sub>	Output Leakage Curre	ent			-10	μА	0-5.5V	V <sub>OUT</sub> = 0.5V; <del>OE</del> = 2.0V
los	Output Short-Circuit (	Current	-100		-275	mA	Max	V <sub>OUT</sub> = 0.0V
I <sub>CEX</sub>	Output HIGH Leakage	e Current			50	μА	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>ZZ</sub>	Bus Drainage Test				100	μА	0.0	$V_{OUT} = 5.5V$ ; All Others $V_{CC}$ or GND
I <sub>CCH</sub>	Power Supply Curren	t			2.0	mA	Max	All Outputs HIGH
I <sub>CCL</sub>	Power Supply Curren	t			62	mA	Max	All Outputs LOW
I <sub>CCZ</sub>	Power Supply Curren	t			2.0	mA	Max	OE = V <sub>CC</sub> ; All Others at V <sub>CC</sub> or GND
I <sub>CCT</sub>	Additional I <sub>CC</sub> /Input	Outputs Enabled			2.5	mA		V <sub>I</sub> = V <sub>CC</sub> - 2.1V
		Outputs 3-STATE			2.5	mA	Max	Enable Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V
		Outputs 3-STATE			2.5	mA		Data Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V
								All Others at V <sub>CC</sub> or GND
I <sub>CCD</sub>	Dynamic I <sub>CC</sub>	No Load				mA/		Outputs Open
	(Note 3)				0.30	MHz	Max	OE = GND, (Note 4)
							One Bit Toggling, 50% Duty Cycle	

Note 3: Guaranteed, but not tested.

Note 4: For 8-bit toggling,  $I_{CCD} < 0.8 \ mA/MHz.$ 

### **AC Electrical Characteristics**

(SSOP Package)

Symbol	Parameter		$T_A = +25$ °C $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$			$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50 \text{ pF}$		
		Min	Тур	Max	Min	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	150			150		MHz	
t <sub>PLH</sub>	Propagation Delay	1.8		6.2	1.8	6.2	ns	
t <sub>PHL</sub>	CP to O <sub>n</sub>	1.8		5.9	1.8	5.9	115	
t <sub>PZH</sub>	Output Enable Time	1.2		5.6	1.2	5.6	20	
t <sub>PZL</sub>		1.6		5.3	1.6	5.3	ns	
t <sub>PHZ</sub>	Output Disable Time	2.2		7.1	2.2	7.1	ns	
t <sub>PLZ</sub>		2.2		6.6	2.2	6.6	115	

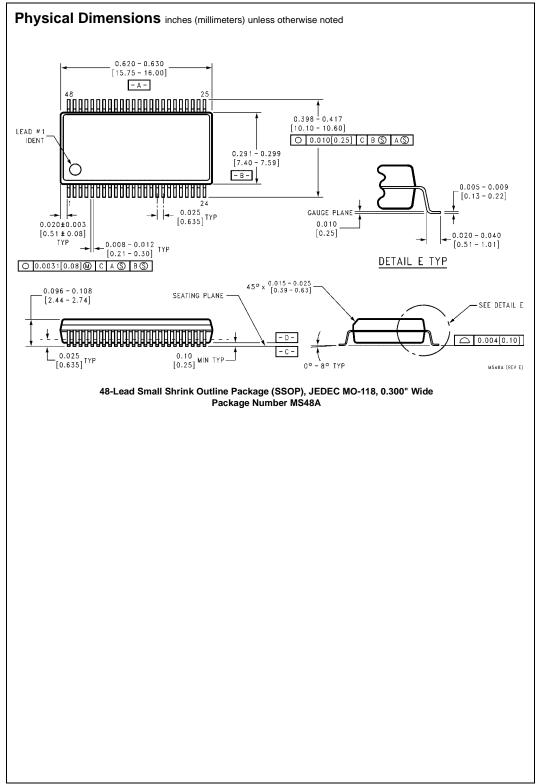
# **AC Operating Requirements**

Symbol	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50 \text{ pF}$		Units	
		Min	Max	Min	Max		
t <sub>S</sub> (H)	Setup Time, HIGH	1.1		1.1		20	
t <sub>S</sub> (L)	or LOW D <sub>n</sub> to CP	1.1		1.1		ns	
t <sub>H</sub> (H)	Hold Time, HIGH	1.3		1.3			
t <sub>H</sub> (L)	or LOW D <sub>n</sub> to CP	1.3		1.3		ns	
t <sub>W</sub> (H)	Pulse Width, CP	3.0		3.0			
t <sub>W</sub> (L)	HIGH or LOW	3.0		3.0		ns	

# Capacitance

Symbol	Parameter	Тур	Units	Conditions (T <sub>A</sub> = 25°C)
C <sub>IN</sub>	Input Capacitance	5.0	pF	V <sub>CC</sub> = 0V
C <sub>OUT</sub> (Note 5)	Output Capacitance	11.0	pF	V <sub>CC</sub> = 5.0V

Note 5: C<sub>OUT</sub> is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.



### Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 12.50±0.10 0.40 TYP -B-10±0,10 89 9.20 B.10 50. O.2 C B A ALL LEAD TIPS PIN #1 IDENT LAND PATTERN RECOMMENDATION O.1 C SEE DETAIL A 0.90+0.15 0.09-0.20 0.10±0.05 0.50 0.17-0.27 ♦ 0.13\( \old{\text{0}} \) A B\( \old{\text{S}} \) C\( \old{\text{S}} \) 12.00' TOP & BOTTOM DIMENSIONS ARE IN MILLIMETERS GAGE PLANE 0.25 NOTES A. CONFORMS TO JEDEC REGISTRATION MC-153, VARIATION ED, DATE 4/97. B. DIMENSIONS ARE IN MILLIMETERS. SEATING PLANE 0.60±0.10 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982. DETAIL A MTD48REVC

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

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