# **Power MOSFET**

# 30 V, 94 A, Single N-Channel, SOIC-8 FL

#### **Features**

- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These are Pb-Free Devices

#### **Applications**

- VCORE Applications
- DC-DC Converters
- Low Side Switching

#### MAXIMUM RATINGS (T, I=25°C unless otherwise stated)

R	Symbol	Value	Unit		
Drain-to-Source Voltage			$V_{DSS}$	30	V
Gate-to-Source Voltage			$V_{GS}$	±20	V
Continuous Drain		T <sub>A</sub> = 25°C	I <sub>D</sub>	18	Α
Current R <sub>θJA</sub> (Note 1)		T <sub>A</sub> = 85°C	1	13	
Power Dissipa- tion R <sub>θJA</sub> (Note 1)		T <sub>A</sub> = 25°C	P <sub>D</sub>	2.35	W
Continuous Drain Current R <sub>0JA</sub>		T <sub>A</sub> = 25°C	I <sub>D</sub>	11	Α
(Note 2)	Steady State	T <sub>A</sub> = 85°C	1	8.0	
Power Dissipa- tion R <sub>θJA</sub> (Note 2)	State	T <sub>A</sub> = 25°C	P <sub>D</sub>	0.91	W
Continuous Drain Current R <sub>BJC</sub>		T <sub>C</sub> = 25°C	I <sub>D</sub>	94	Α
(Note 1)		T <sub>C</sub> = 85°C		68	
Power Dissipation R <sub>θJC</sub> (Note 1)		T <sub>C</sub> = 25°C	$P_D$	62.5	W
Pulsed Drain Cur- rent	T <sub>A</sub> = 25°C, t <sub>p</sub> = 10 μs		I <sub>DM</sub>	140	Α
Current limited by package	T <sub>A</sub> = 25°C		I <sub>DmaxPkg</sub>	140	Α
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C
Source Current (Body Diode)			I <sub>S</sub>	62.5	Α
Drain to Source			dV/dt	10	V/ns
Single Pulse Drain-to-Source Avalanche Energy $T_J$ = 25°C, $V_{DD}$ = 50 V, $V_{GS}$ = 10 V, $I_L$ = 30 $A_{pk}$ , $L$ = 1.0 mH, $R_G$ = 25 $\Omega$			E <sub>AS</sub>	450	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T <sub>L</sub>	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

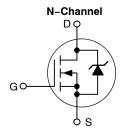
- Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
   Surface-mounted on FR4 board using the minimum recommended pad size.



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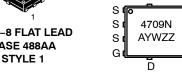
#### http://onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> Typ	I <sub>D</sub> Max	
30 V	2.85 mΩ @ 10 V	94 A	
00 V	4.0 mΩ @ 4.5 V		





## **MARKING DIAGRAM & PIN ASSIGNMENT** D



4709N = Specific Device Code = Assembly Location

= Year W = Work Week ZZ = Lot Traceability

## **ORDERING INFORMATION**

Device		Package	Shipping <sup>†</sup>		
	NTMFS4709NT1G	SOIC-8 FL (Pb-Free)	1500 / Tape & Reel		
	NTMFS4709NT3G	SOIC-8 FL (Pb-Free)	5000 / Tape & Reel		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### THERMAL RESISTANCE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{ hetaJC}$	2.0	°C/W
Junction-to-Ambient - Steady State (Note 3)	$R_{ hetaJA}$	53.2	
Junction-to-Ambient - Steady State (Note 4)	$R_{ hetaJA}$	137.8	

## **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS				_		_	_
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T				5.6		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V,	T <sub>J</sub> = 25°C			1.0	μΑ
		$V_{DS} = 24 \text{ V}$	T <sub>J</sub> = 125°C			10	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V	' <sub>GS</sub> = ±20 V			±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}$ , I	D = 250 μA	1.0		3.0	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				5.6		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 11.5 V	I <sub>D</sub> = 30 A		2.8		
			I <sub>D</sub> = 15 A		2.8		
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A		2.85	3.6	mΩ
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 30 A		4.0	5.5	
			I <sub>D</sub> = 15 A		4.0		
Forward Transconductance	9FS	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A			41		S
CHARGES AND CAPACITANCES							
Input Capacitance	C <sub>ISS</sub>				2370		
Output Capacitance	C <sub>OSS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 12 V			1240		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>				305		
Total Gate Charge	Q <sub>G(TOT)</sub>				20		
Threshold Gate Charge	Q <sub>G(TH)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 15 V;			2.4		]
Gate-to-Source Charge	$Q_{GS}$	I <sub>D</sub> = 3	30 Å		4.5		nC
Gate-to-Drain Charge	$Q_{GD}$				11		
Total Gate Charge	Q <sub>G(TOT)</sub>				48		
Threshold Gate Charge	Q <sub>G(TH)</sub>	$V_{GS} = 11.5 \text{ V}, V_{DS} = 15 \text{ V};$ $I_{D} = 30 \text{ A}$			4.0		nC
Gate-to-Source Charge	$Q_{GS}$				6.5		
Gate-to-Drain Charge	$Q_{GD}$				10.6		
SWITCHING CHARACTERISTICS (Note 6)							
Turn-On Delay Time	t <sub>d(ON)</sub>				16		
Rise Time	t <sub>r</sub>	$V_{GS}$ = 4.5 V, $V_{DS}$ = 15 V, $I_{D}$ = 30 A, $R_{G}$ = 3.0 $\Omega$			173		
Turn-Off Delay Time	t <sub>d(OFF)</sub>				20		ns
Fall Time	t <sub>f</sub>				105		

<sup>5.</sup> Pulse Test: pulse width  $\pm\,300~\mu\text{s},$  duty cycle  $\pm\,2\%$ 

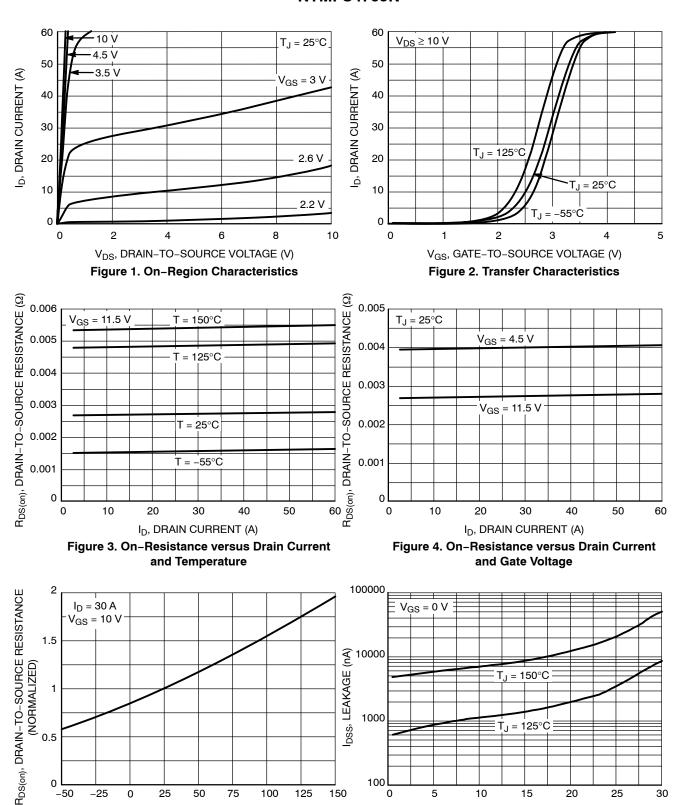
Surface-mounted on FR4 board using 1 sq in pad, 1 oz Cu.
 Surface-mounted on FR4 board using the minimum recommended pad size.

<sup>6.</sup> Switching characteristics are independent of operating junction temperatures.

# **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
SWITCHING CHARACTERISTICS (Note	e 6)					-	
Turn-On Delay Time	t <sub>d(ON)</sub>	$V_{GS} = 11.5 \text{ V}, V_{DS} = 15 \text{ V}, \\ I_{D} = 30 \text{ A}, R_{G} = 3.0 \Omega$			8.5		
Rise Time	t <sub>r</sub>				87		
Turn-Off Delay Time	t <sub>d(OFF)</sub>	I <sub>D</sub> = 30 A, I	$R_{\rm G} = 3.0  \Omega$		31.5		ns
Fall Time	t <sub>f</sub>	1			8.5		1
DRAIN-SOURCE DIODE CHARACTER	RISTICS						
Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 20 A	T <sub>J</sub> = 25°C		0.75	1.0	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 50 A	T <sub>J</sub> = 25°C		0.85		
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 20 A	T <sub>J</sub> = 125°C		0.7		
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V},$ $d_{IS}/d_{t} = 100 \text{ A/}\mu\text{s},$ $I_{S} = 25 \text{ A}$			48		ns
Charge Time	ta				23		
Discharge Time	t <sub>b</sub>				25		
Reverse Recovery Charge	Q <sub>RR</sub>				55		nC
Package Parasitic Values	•					•	•
Gate Resistance	$R_{G}$	T <sub>A</sub> = 25°C			0.65		Ω

<sup>5.</sup> Pulse Test: pulse width  $\pm 300~\mu s$ , duty cycle  $\pm 2\%$ 6. Switching characteristics are independent of operating junction temperatures.



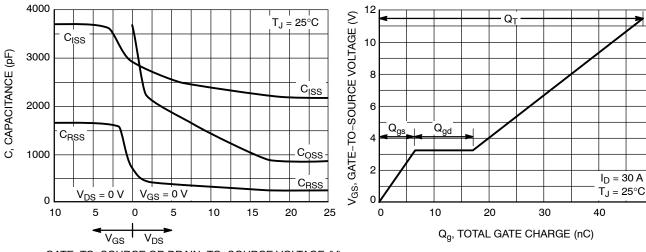
T<sub>J</sub>, TEMPERATURE (°C)

Figure 5. On–Resistance Variation with
Temperature

V<sub>DS</sub>, DRAIN-TO-SOURCE VOLTAGE (V)

Figure 6. Drain-to-Source Leakage Current

versus Voltage



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (V)

Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

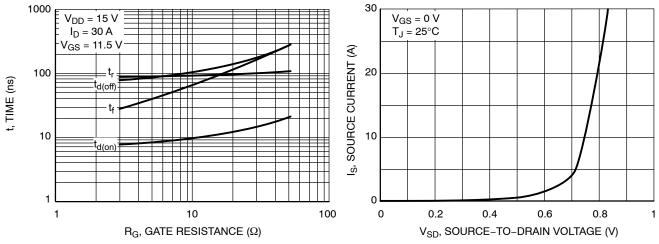


Figure 9. Resistive Switching Time Variation versus Gate Resistance

Figure 10. Diode Forward Voltage versus Current

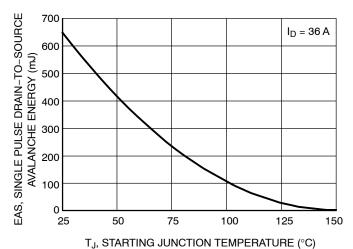
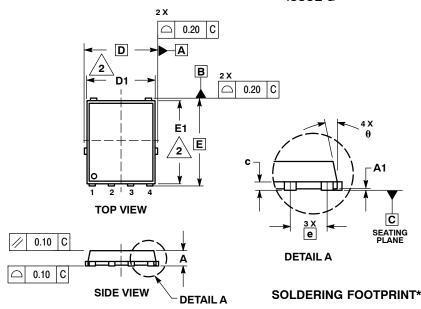


Figure 11. Maximum Avalanche Energy versus

## PACKAGE DIMENSIONS





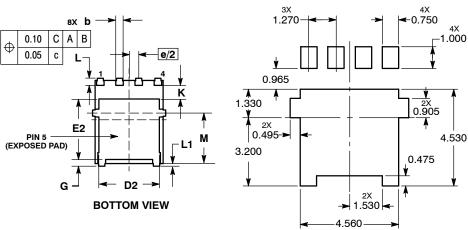
#### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETER. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE

	MILLIMETERS					
DIM	MIN	NOM	MAX			
Α	0.90	1.00	1.10			
A1	0.00		0.05			
b	0.33	0.41	0.51			
С	0.23	0.28	0.33			
D		5.15 BSC				
D1	4.50	4.90	5.10			
D2	3.50		4.22			
E		6.15 BSC				
E1	5.50	5.80	6.10			
E2	3.45		4.30			
е		1.27 BSC	;			
G	0.51	0.61	0.71			
K	1.20	1.35	1.50			
L	0.51	0.61	0.71			
L1	0.05	0.17	0.20			
М	3.00	3.40	3.80			
θ	0 °		12 °			

- STYLE 1: PIN 1. SOURCE 2. SOURCE

  - 3. SOURCE GATE
  - 5. DRAIN



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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