



FDS6898AZ_F085

Dual N-Channel Logic Level PWM Optimized PowerTrench® MOSFET

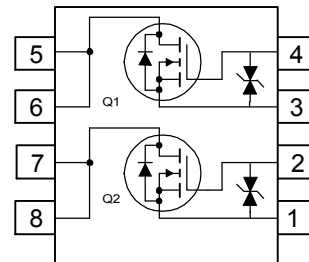
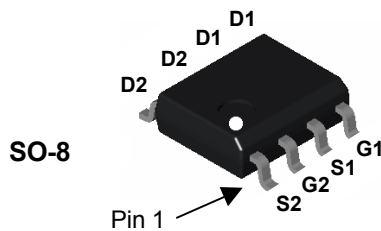
General Description

These N-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- 9.4 A, 20 V $R_{DS(ON)} = 14 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
 $R_{DS(ON)} = 18 \text{ m}\Omega @ V_{GS} = 2.5 \text{ V}$
- Low gate charge (16 nC typical)
- ESD protection diode (note 3)
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability
- Qualified to AEC Q101
- RoHS Compliant



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Rated	Units
V _{DSS}	Drain-Source Voltage	20	V
V _{GSS}	Gate-Source Voltage	± 12	V
I _D	Drain Current – Continuous (Note 1a)	9.4	A
	– Pulsed	38	
P _D	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6898AZ	FDS6898AZ_F085	13"	12mm	2500 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		21		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 16 V, V _{GS} = 0 V			1	μA
I _{GSSF}	Gate–Body Leakage, Forward	V _{GS} = 12 V, V _{DS} = 0 V			10	μA
I _{GSSR}	Gate–Body Leakage, Reverse	V _{GS} = –12 V, V _{DS} = 0 V			–10	μA

On Characteristics (Note 2)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.5	1	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		–3.5		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 4.5 V, I _D = 9.4 A V _{GS} = 2.5 V, I _D = 8.3 A V _{GS} = 4.5 V, I _D = 9.4 A, T _J = 125°C		10 13 14	14 18 21	mΩ
I _{D(on)}	On–State Drain Current	V _{GS} = 4.5 V, V _{DS} = 5 V	19			A
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 9.4 A		47		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 10 V, V _{GS} = 0 V, f = 1.0 MHz		1821		pF
C _{oss}	Output Capacitance			440		pF
C _{rss}	Reverse Transfer Capacitance			208		pF

Switching Characteristics (Note 2)

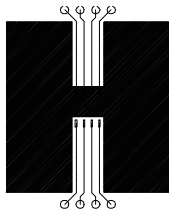
t _{d(on)}	Turn–On Delay Time	V _{DD} = 10 V, I _D = 1 A, V _{GS} = 4.5 V, R _{GEN} = 6 Ω		10	20	ns
t _r	Turn–On Rise Time			15	27	ns
t _{d(off)}	Turn–Off Delay Time			34	55	ns
t _f	Turn–Off Fall Time			16	29	ns
Q _g	Total Gate Charge		V _{DS} = 10 V, I _D = 9.4 A, V _{GS} = 4.5 V		16	23
Q _{gs}	Gate–Source Charge			3		nC
Q _{gd}	Gate–Drain Charge			4		nC

Drain–Source Diode Characteristics and Maximum Ratings

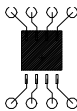
I _S	Maximum Continuous Drain–Source Diode Forward Current				1.3	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.3 A (Note 2)		0.7	1.2	V

Notes:

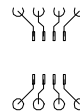
- R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a) 78°C/W when mounted on a 0.5in² pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in² pad of 2 oz copper



c) 135°C/W when mounted on a minimum mounting pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied

Typical Characteristics

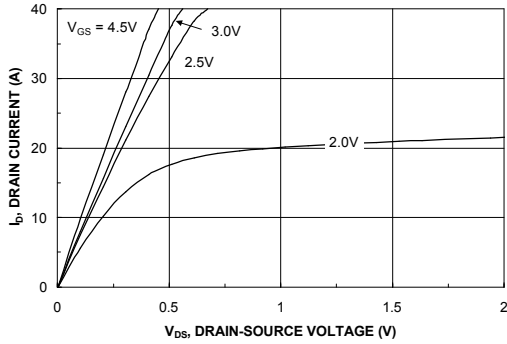


Figure 1. On-Region Characteristics.

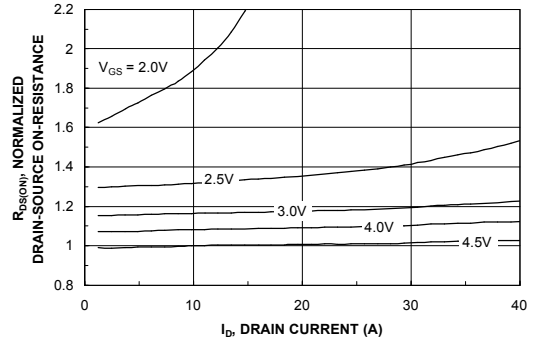


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

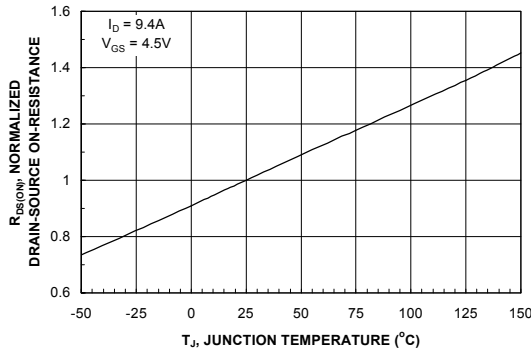


Figure 3. On-Resistance Variation with Temperature.

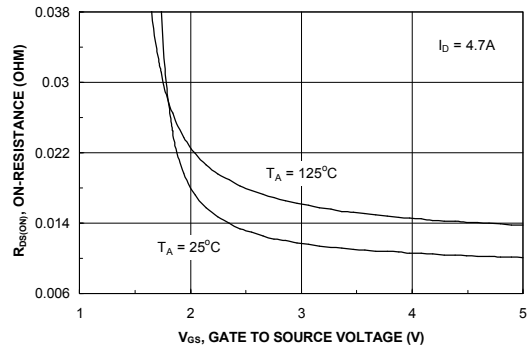


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

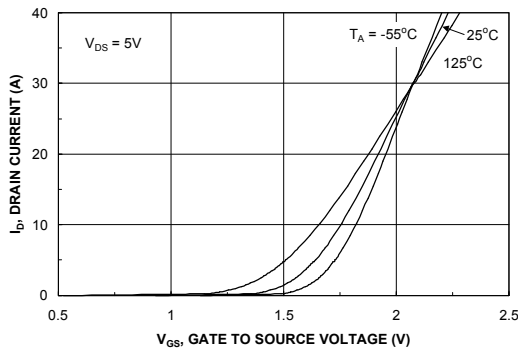


Figure 5. Transfer Characteristics.

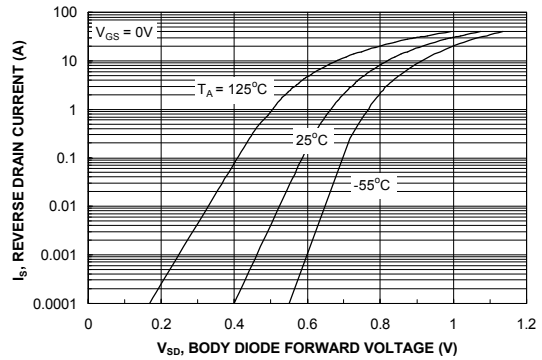


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

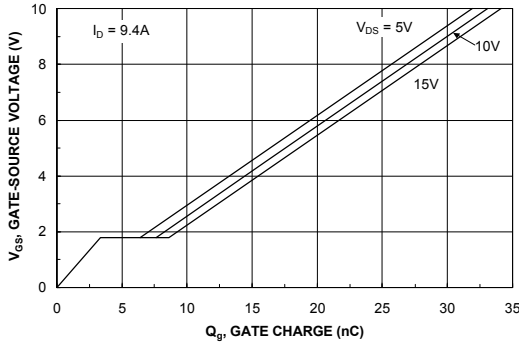


Figure 7. Gate Charge Characteristics.

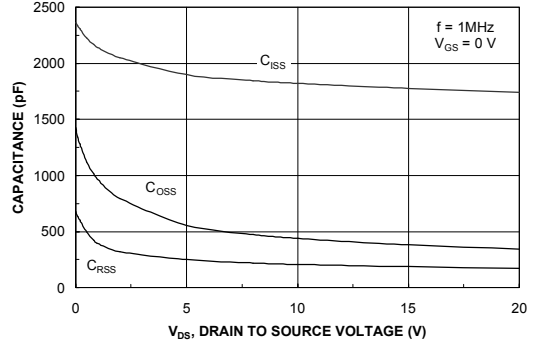


Figure 8. Capacitance Characteristics.

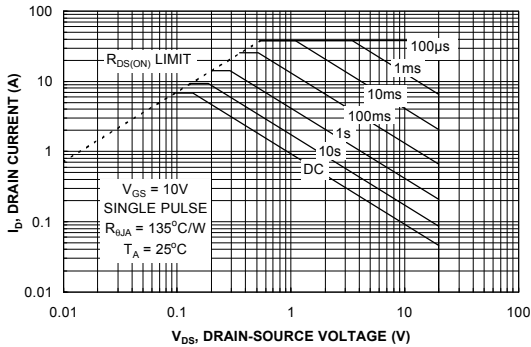


Figure 9. Maximum Safe Operating Area.

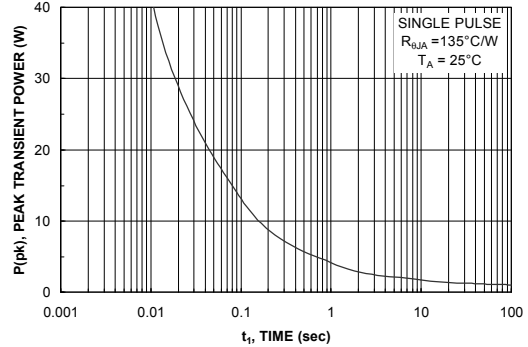


Figure 10. Single Pulse Maximum Power Dissipation.

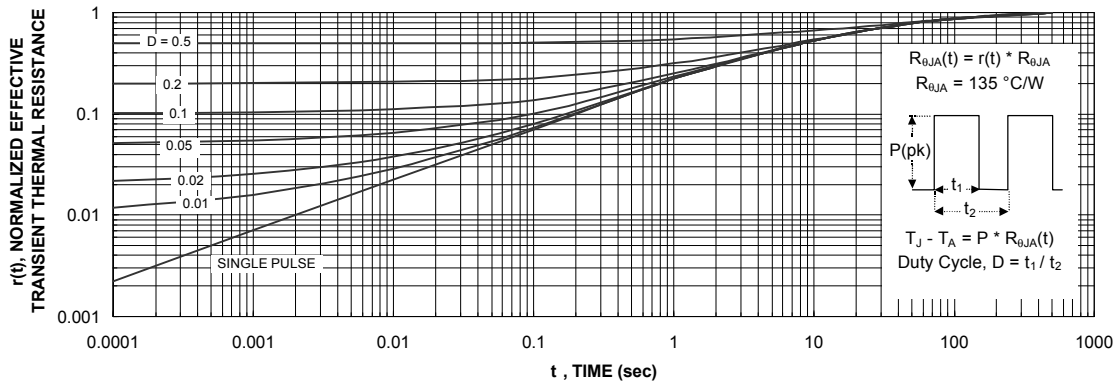






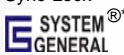
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.



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