October 2010

UniFET-II™

FDP12N50NZ / FDPF12N50NZ

N-Channel MOSFET

500V, 11.5A, 0.52Ω

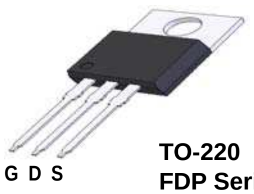
Features

- $R_{DS(on)}$ = 0.46Ω (Typ.) @ V_{GS} = 10V, I_D = 5.75A
- Low gate charge (Typ. 23nC)
- Low C_{rss} (Typ. 14pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant

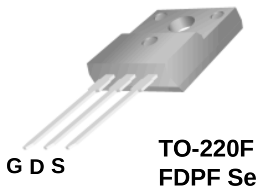
Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

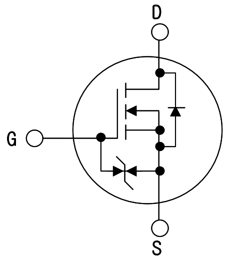
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



TO-220
FDP Series



TO-220F
FDPF Series
(potted)



MOSFET Maximum Ratings $T_C = 25^oC$ unless otherwise noted*

Symbol	Parameter		FDP12N50NZ	FDPF12N50NZ	Units
V_{DSS}	Drain to Source Voltage		500		V
V_{GSS}	Gate to Source Voltage		±25		V
I_D	Drain Current	- Continuous ($T_C = 25^oC$)	11.5	11.5*	A
		- Continuous ($T_C = 100^oC$)	6.9	6.9*	
I_{DM}	Drain Current	- Pulsed (Note 1)	46	46*	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	560		mJ
I_{AR}	Avalanche Current	(Note 1)	11.5		A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	17		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5		V/ns
P_D	Power Dissipation	($T_C = 25^oC$)	170	42	W
		- Derate above 25^oC	1.37	0.33	W/^{o}C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		^{o}C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300		^{o}C

*Dran current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FDP12N50NZ	FDPF12N50NZ	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.73	3.0	^{o}C/W
$R_{\theta CS}$	Thermal Resistance, Case to Sink Typ	0.5	-	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP12N50NZ	FDP12N50NZ	TO-220	-	-	50
FDPF12N50NZ	FDPF12N50NZ	TO-220F	-	-	50

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$, $T_J = 25^oC$	500	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$, Referenced to 25^oC	-	0.5	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500V$, $V_{GS} = 0V$	-	-	1	µA
		$V_{DS} = 400V$, $T_C = 125^oC$	-	-	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm25V$, $V_{DS} = 0V$	-	-	±10	µA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10V$, $I_D = 5.75A$	-	0.46	0.52	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20V$, $I_D = 5.75A$	-	12	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz	-	945	1235	pF
C_{oss}	Output Capacitance		-	155	205	pF
C_{rss}	Reverse Transfer Capacitance		-	14	20	pF
Q_g	Total Gate Charge at 10V	$V_{DS} = 400V$, $I_D = 11.5A$ $V_{GS} = 10V$	-	23	30	nC
Q_{gs}	Gate to Source Gate Charge		-	5.5	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	9.6	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250V$, $I_D = 11.5A$ $R_G = 25\Omega$	-	20	50	ns
t_r	Turn-On Rise Time		-	50	110	ns
$t_{d(off)}$	Turn-Off Delay Time		-	60	130	ns
t_f	Turn-Off Fall Time		-	45	100	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	11.5	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	46	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V$, $I_{SD} = 11.5A$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V$, $I_{SD} = 11.5A$ $dI_F/dt = 100A/\mu s$	-	315	-	ns
Q_{rr}	Reverse Recovery Charge		-	2.0	-	µC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L = 8.5mH$, $I_{AS} = 11.5A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25°C$
3. $I_{SD} \leq 11.5A$, $di/dt \leq 200A/\mu s$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25°C$
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

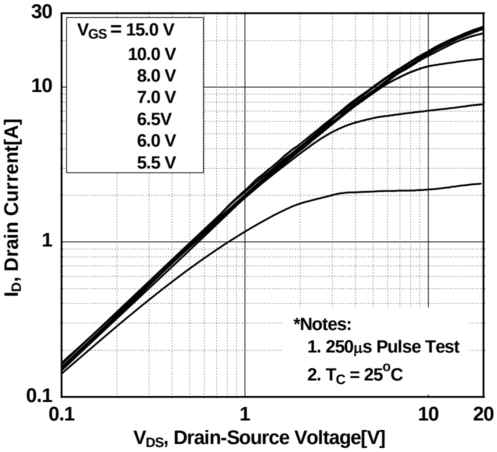


Figure 2. Transfer Characteristics

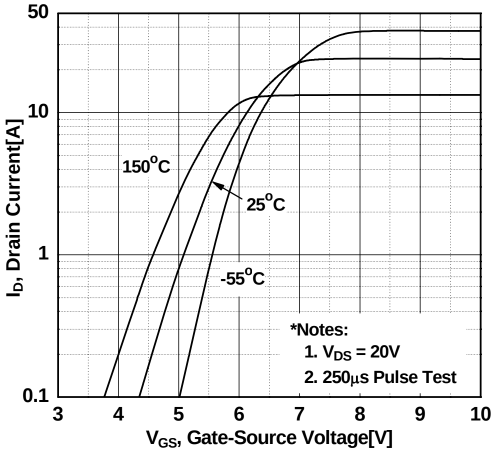


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

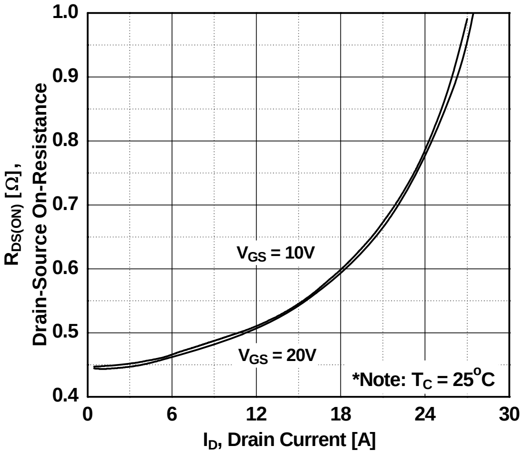


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

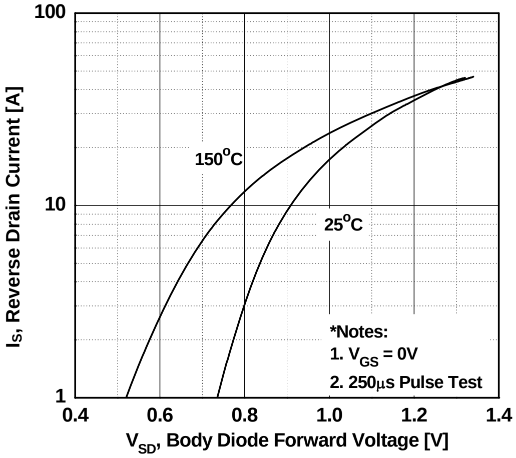


Figure 5. Capacitance Characteristics

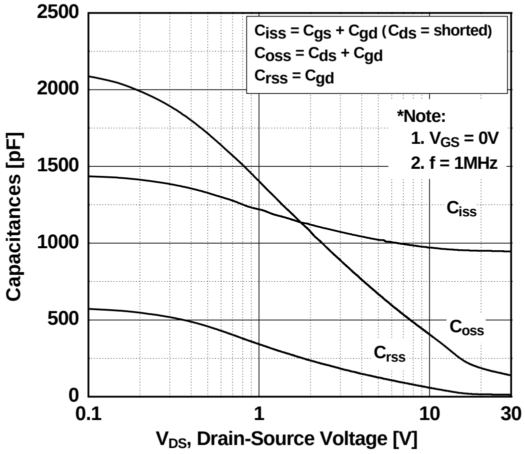
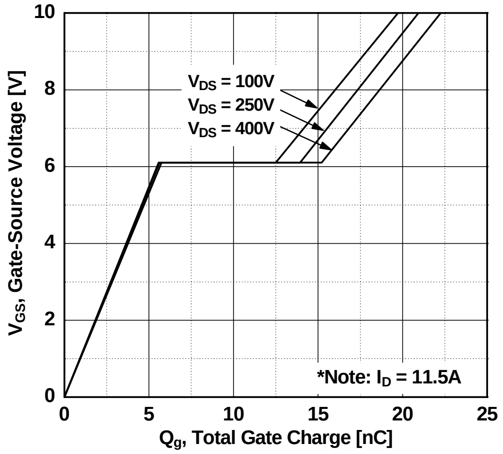


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

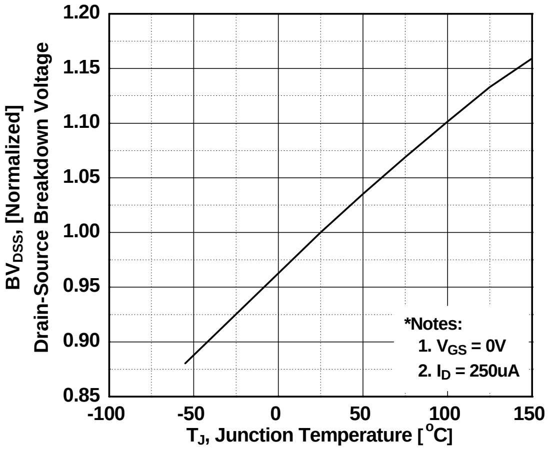


Figure 8. On-Resistance Variation vs. Temperature

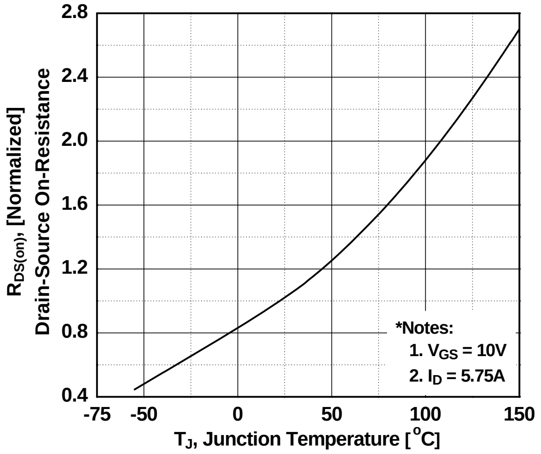


Figure 9. Maximum Safe Operating Area - FDPF12N50NZ

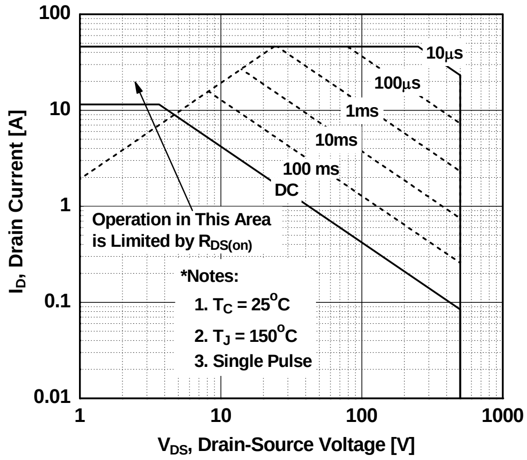


Figure 10.Maximum Safe Operating Area - FDP12N50NZ

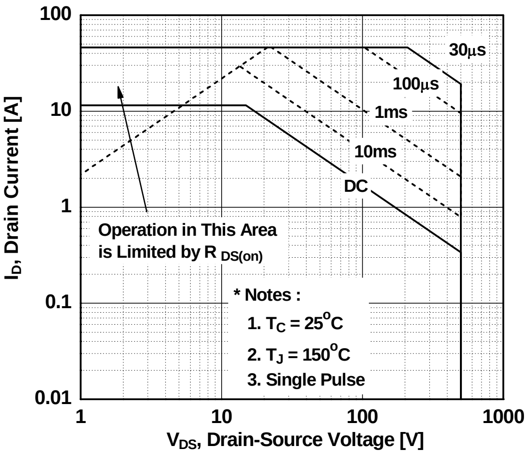
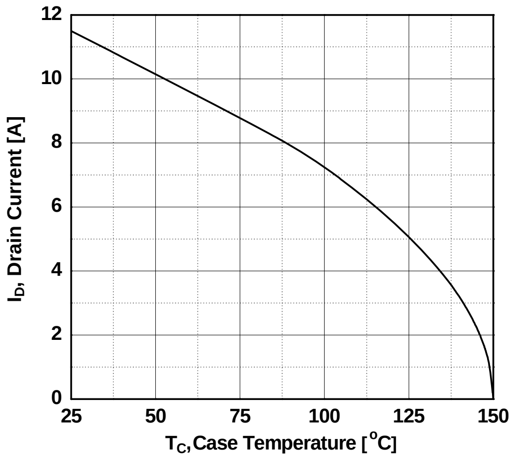


Figure 11. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve - FDP12N50NZ

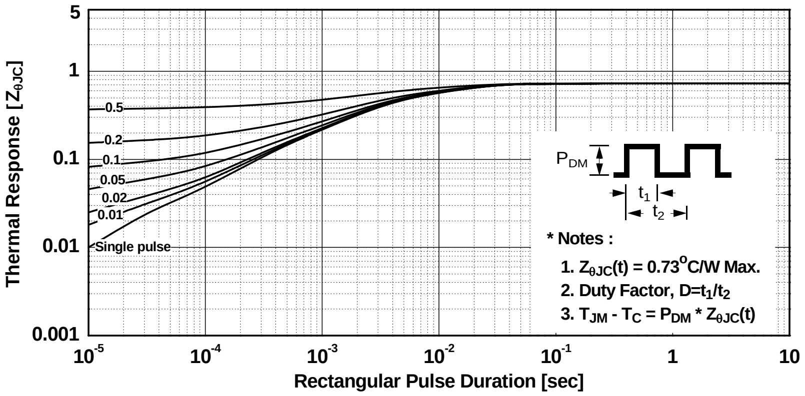
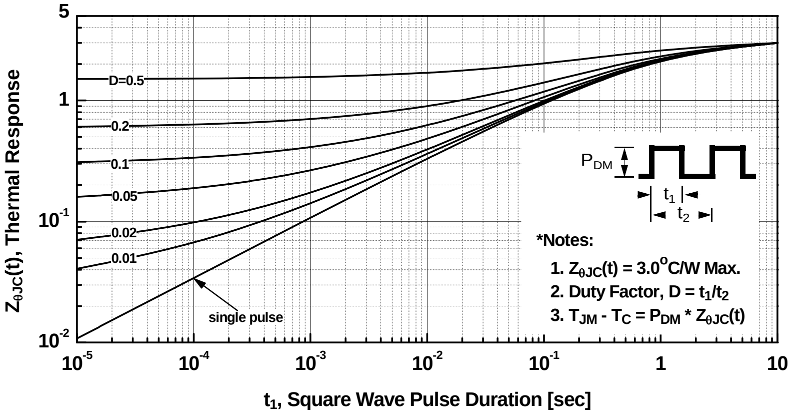
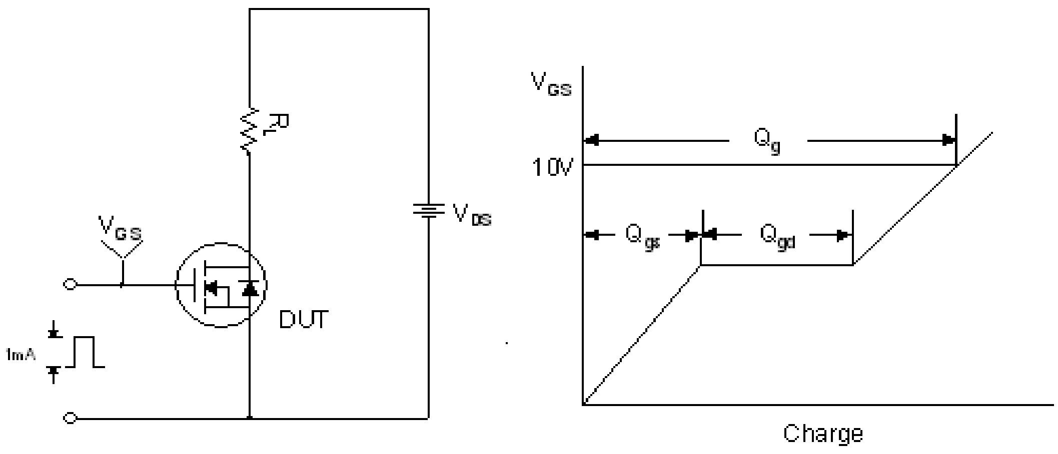


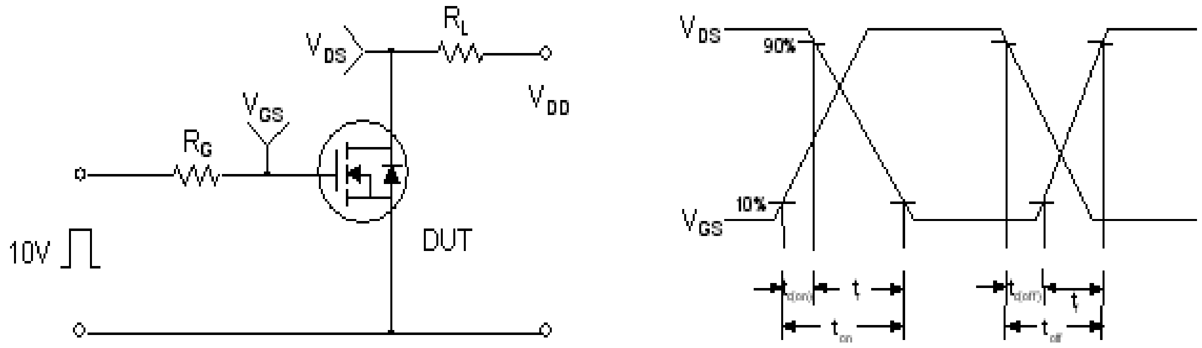
Figure 13. Transient Thermal Response Curve - FDPF12N50NZ



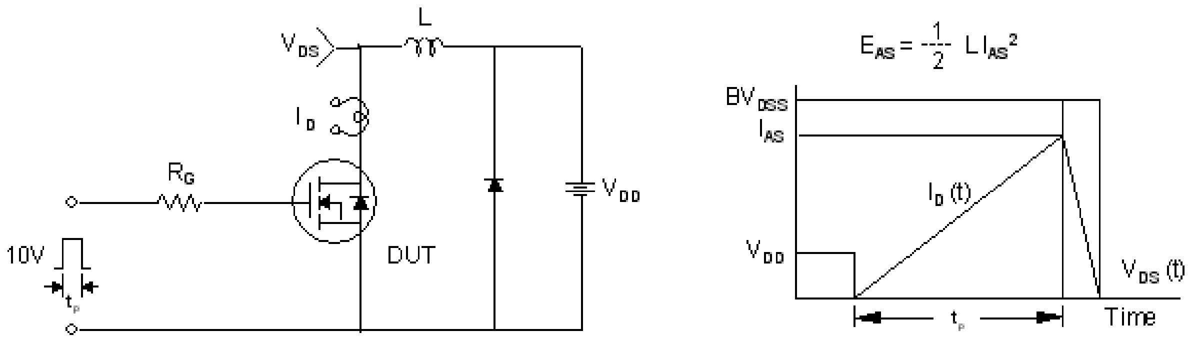
Gate Charge Test Circuit & Waveform



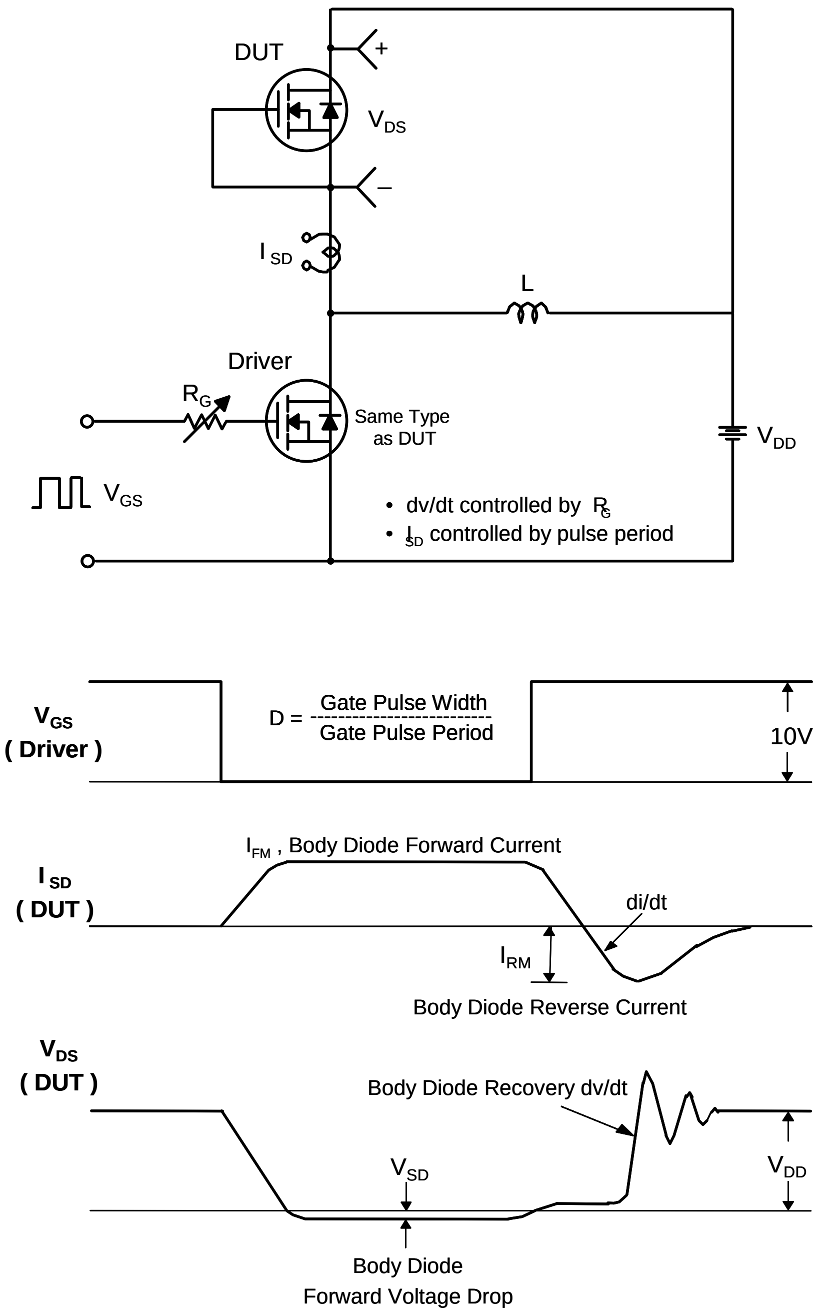
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

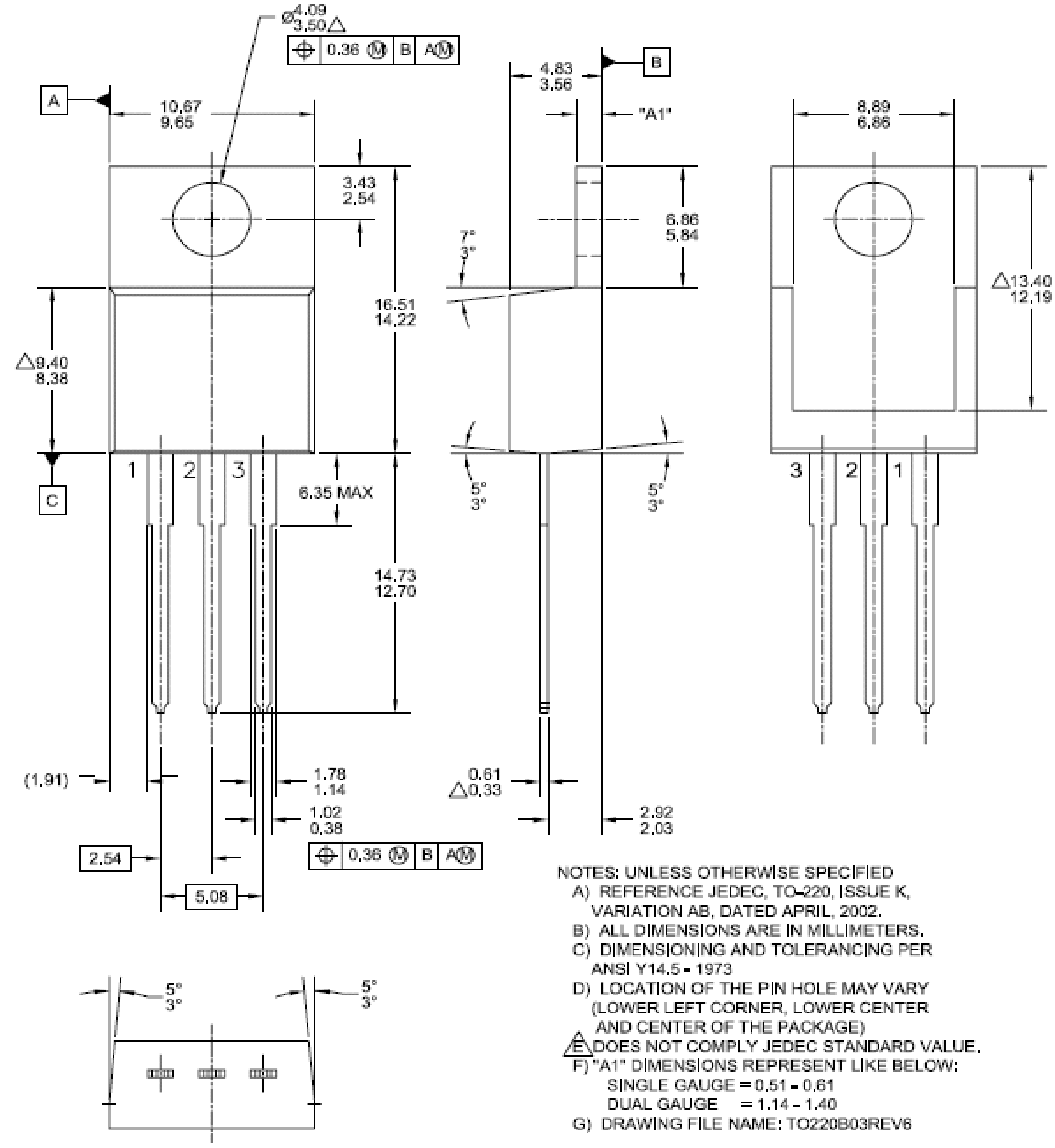


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

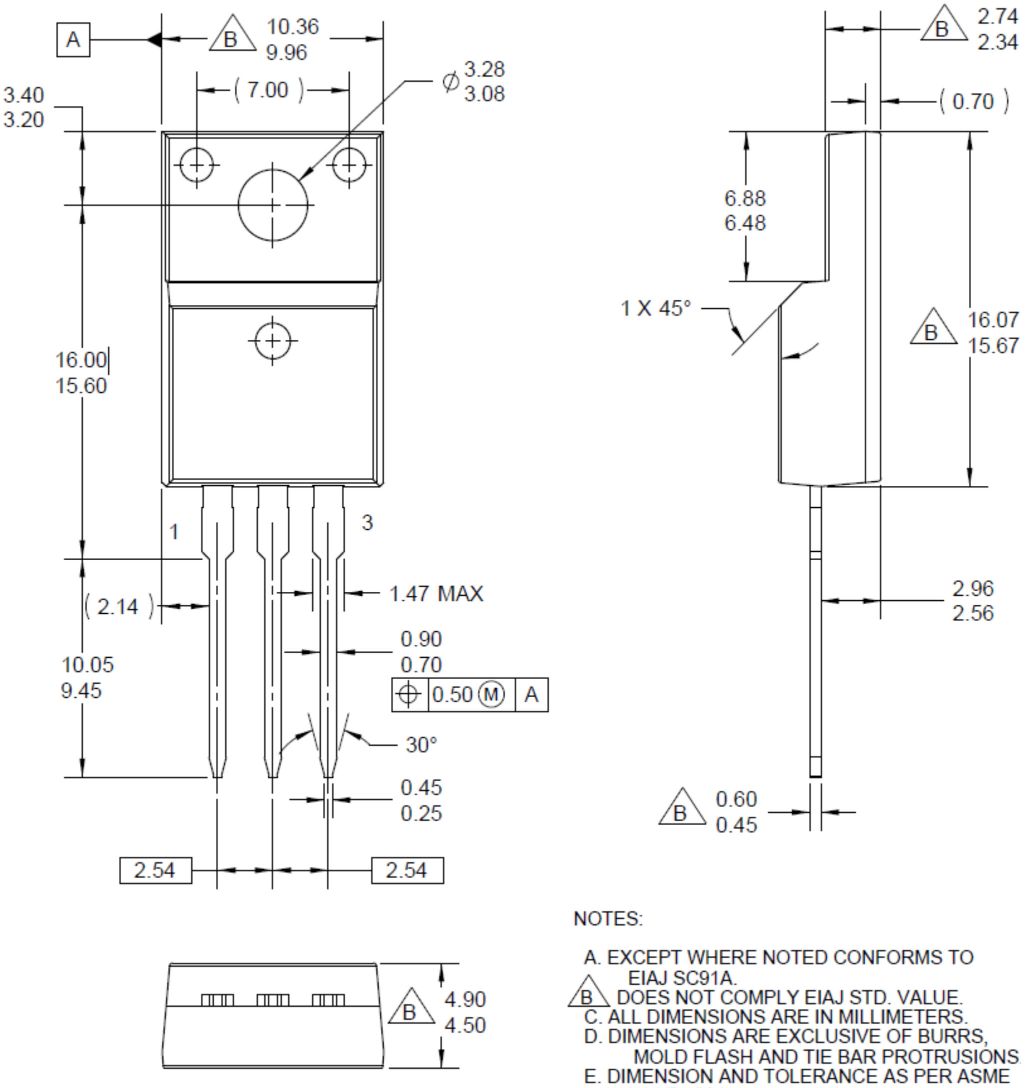
TO-220



NOTES: UNLESS OTHERWISE SPECIFIED
- A) REFERENCE JEDEC, TO-220, ISSUE K, VARIATION AB, DATED APRIL, 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1973
- D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
- E) DOES NOT COMPLY JEDEC STANDARD VALUE.
- F) "A1" DIMENSIONS REPRESENT LIKE BELOW:
  - SINGLE GAUGE = 0.51 - 0.61
  - DUAL GAUGE = 1.14 - 1.40
- G) DRAWING FILE NAME: TO220B03REV6

Package Dimensions (Continued)

TO-220F



NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.

B DOES NOT COMPLY EIAJ STD. VALUE.

C. ALL DIMENSIONS ARE IN MILLIMETERS.

D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS

E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.

F. DRAWING FILE NAME: TO220M03REV1

* Front/Back Side Isolation Voltage : 2500V

Dimensions in Millimeters

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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