

# FDMS8888

## N-Channel PowerTrench® MOSFET

30 V, 21 A, 9.5 mΩ

### Features

- Max  $r_{DS(on)}$  = 9.5 mΩ at  $V_{GS} = 10$  V,  $I_D = 13.5$  A
- Max  $r_{DS(on)}$  = 14.5 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 10.9$  A
- Advanced Package and Silicon combination for low  $r_{DS(on)}$  and high efficiency
- MSL1 robust package design
- RoHS Compliant

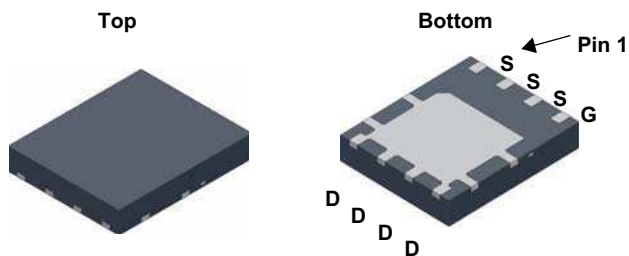


### General Description

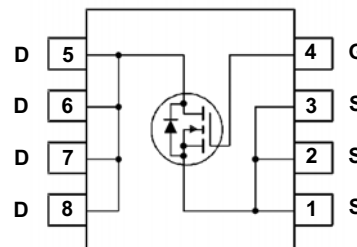
The FDMS8888 has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance.

### Applications

- Synchronous Buck for Notebook Vcore and Server
- Notebook Battery Pack
- Load Switch



Power 56



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$	21	A
	-Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	51	
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	13.5	
	-Pulsed	80	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	54	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	42	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.3	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
8888	FDMS8888	Power 56	13 "	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^{\circ}\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^{\circ}\text{C}$		19		mV/ $^{\circ}\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	1.2	1.9	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^{\circ}\text{C}$		-7		mV/ $^{\circ}\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 13.5\text{ A}$		8	9.5	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 10.9\text{ A}$		11	14.5	
		$V_{GS} = 10\text{ V}$ , $I_D = 13.5\text{ A}$ , $T_J = 125\text{ }^{\circ}\text{C}$		12	14.5	
$g_{FS}$	Forward Transconductance	$V_{DD} = 10\text{ V}$ , $I_D = 13.5\text{ A}$		78		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		1195	1585	pF
$C_{oss}$	Output Capacitance			234	315	pF
$C_{rss}$	Reverse Transfer Capacitance			161	245	pF
$R_g$	Gate Resistance			0.9	2.5	$\Omega$

**Switching Characteristics**

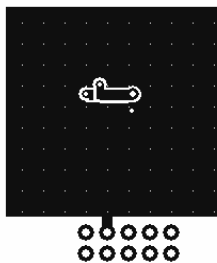
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 13.5\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		9	18	ns
$t_r$	Rise Time			6	12	ns
$t_{d(off)}$	Turn-Off Delay Time			23	27	ns
$t_f$	Fall Time			4	10	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$	$V_{DD} = 15\text{ V}$ , $I_D = 13.5\text{ A}$	23	33	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to }5\text{ V}$		13	18	nC
$Q_{gs}$	Gate to Source Charge			3.5		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			5.1		nC

**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2.1\text{ A}$ (Note 2)		0.74	1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = 13.5\text{ A}$ (Note 2)		0.84	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 13.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		20	32	ns
$Q_{rr}$	Reverse Recovery Charge			8	16	nC

**NOTES:**

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 50  $^{\circ}\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 125  $^{\circ}\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.  
3. Starting  $T_J = 25\text{ }^{\circ}\text{C}$ ,  $L = 0.3\text{ mH}$ ,  $I_{AS} = 19\text{ A}$ ,  $V_{DD} = 27\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

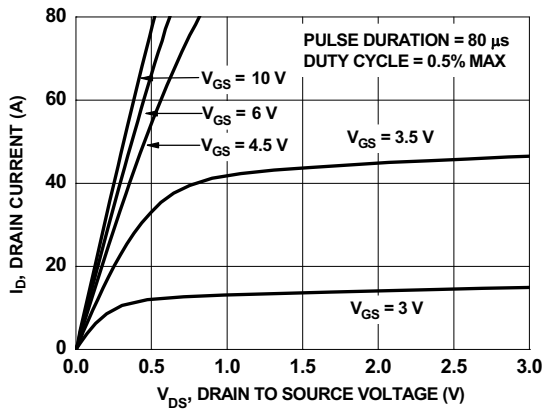


Figure 1. On Region Characteristics

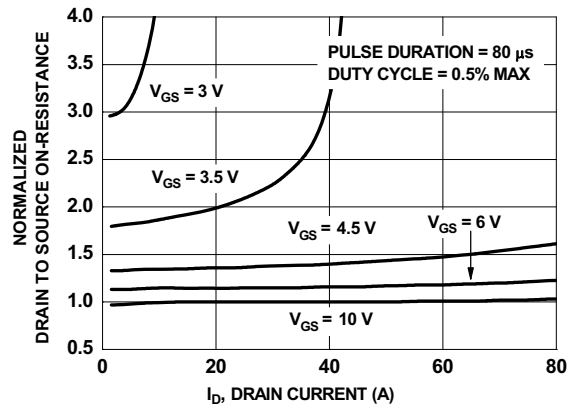


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

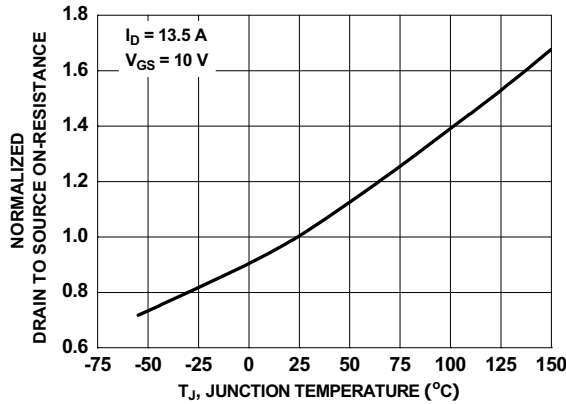


Figure 3. Normalized On Resistance vs Junction Temperature

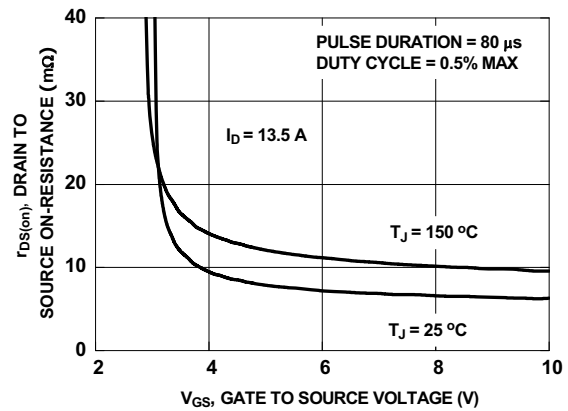


Figure 4. On-Resistance vs Gate to Source Voltage

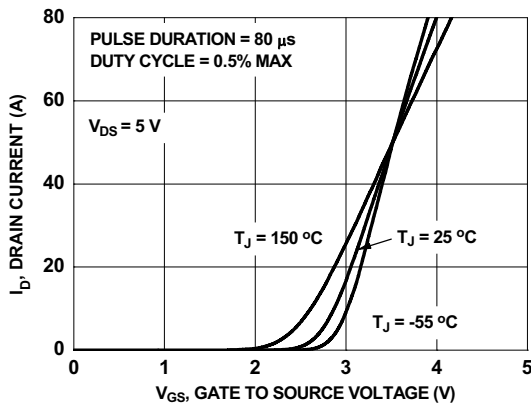


Figure 5. Transfer Characteristics

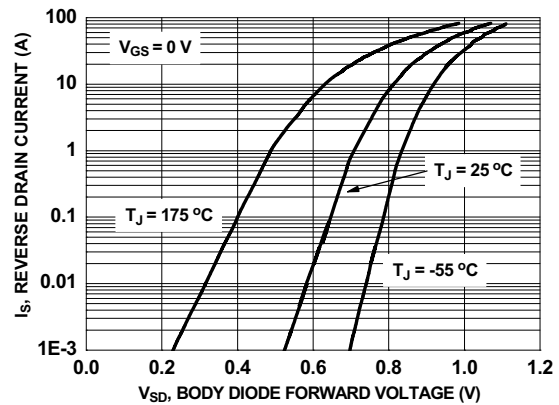


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

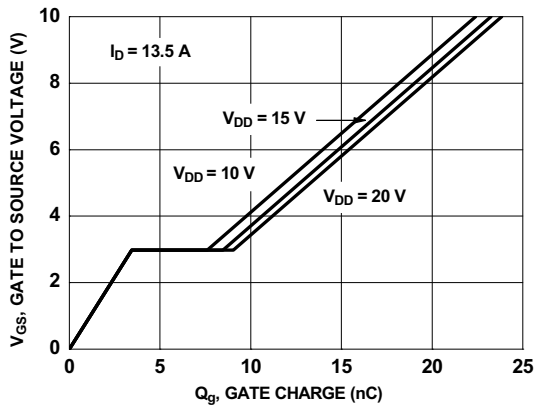


Figure 7. Gate Charge Characteristics

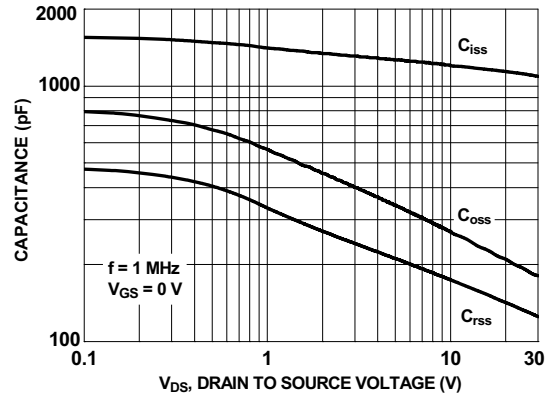


Figure 8. Capacitance vs Drain to Source Voltage

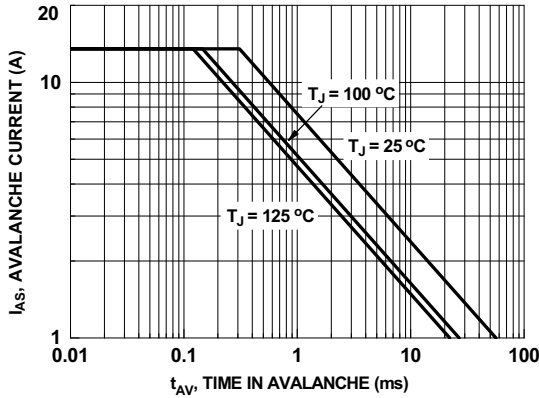


Figure 9. Unclamped Inductive Switching Capability

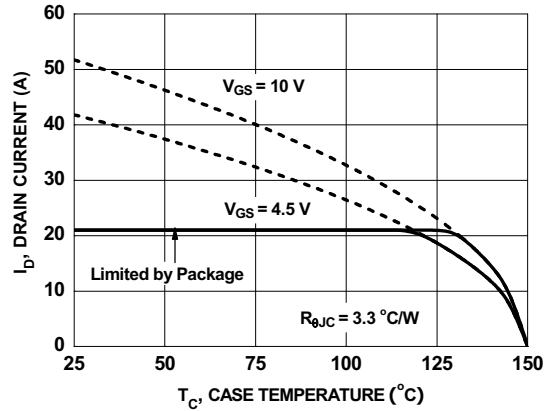


Figure 10. Maximum Continuous Drain Current vs Case Temperature

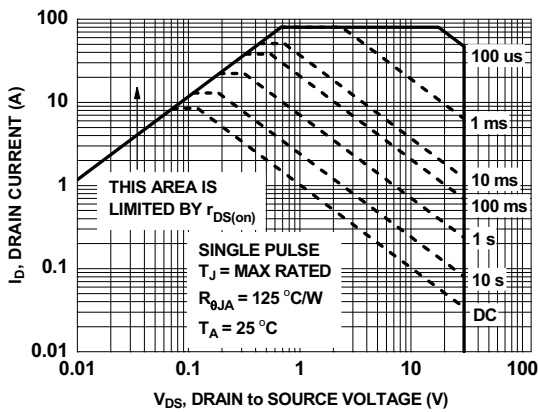


Figure 11. Forward Bias Safe Operating Area

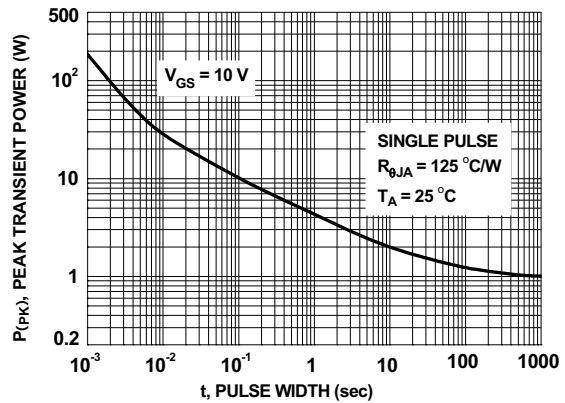


Figure 12. Single Pulse Maximum Power Dissipation

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

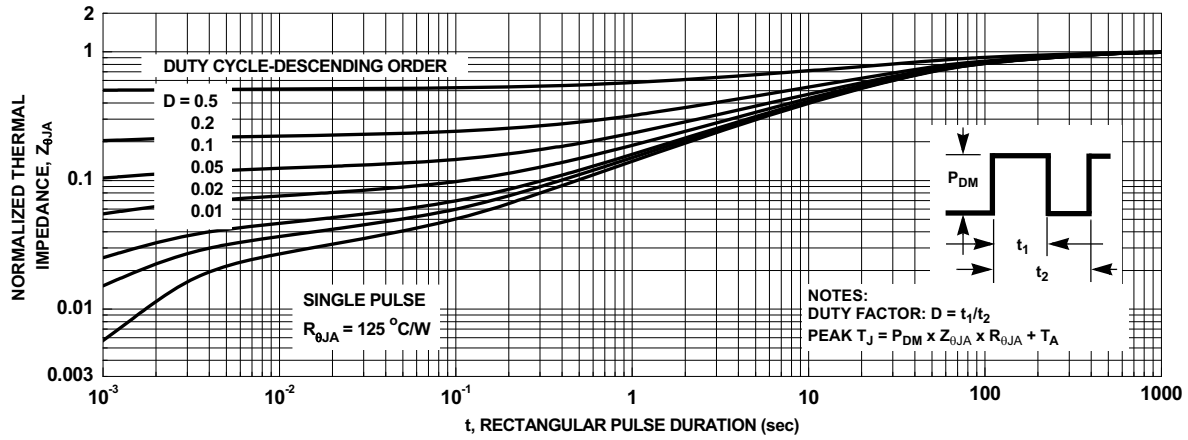
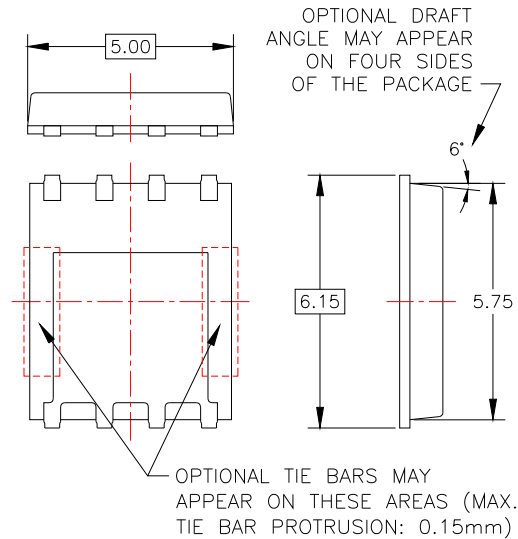
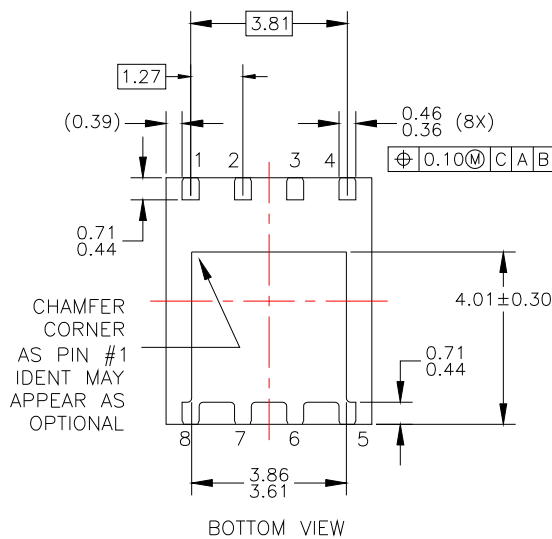
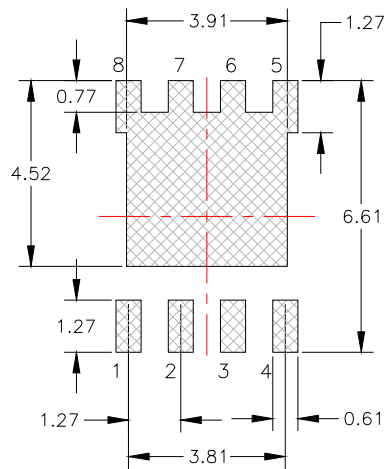
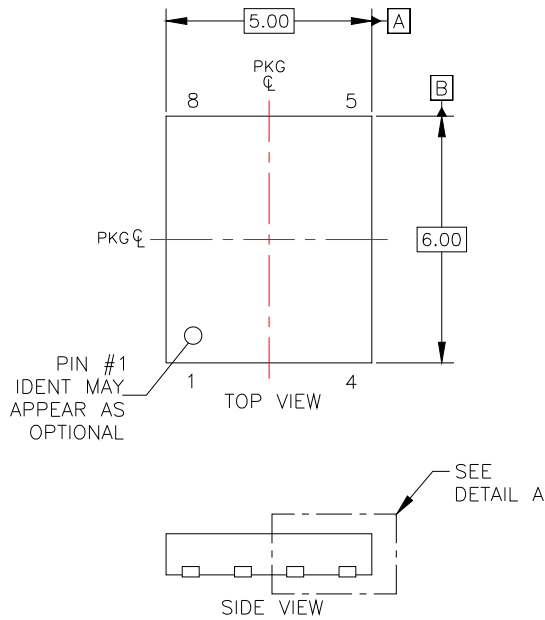


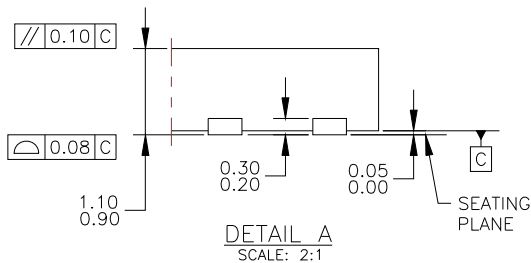
Figure 13. Junction-to-Ambient Transient Thermal Response Curve

# Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED




- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.





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Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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