

# FDMC7570S

## N-Channel Power Trench® SyncFET™ 25 V, 40 A, 2 mΩ

### Features

- Max  $r_{DS(on)}$  = 2 mΩ at  $V_{GS} = 10$  V,  $I_D = 27$  A
- Max  $r_{DS(on)}$  = 2.9 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 21.5$  A
- Advanced Package and Combination for low  $r_{DS(on)}$  and high efficiency
- SyncFET Schottky Body Diode
- 100% UIL Tested
- RoHS Compliant

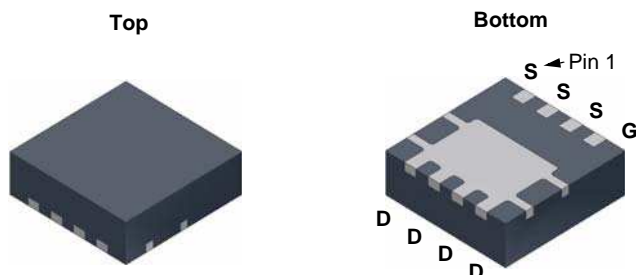


### General Description

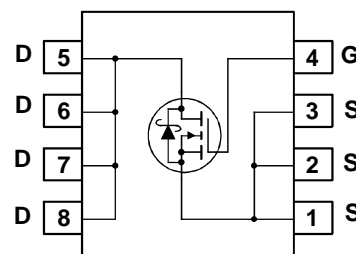
The FDMC7570S has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

### Applications

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/ GPU low side switch
- Networking Point of Load low side switch
- Telecom secondary side rectification



Power 33



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	25	V
$V_{GS}$	Gate to Source Voltage (Note 4)	±20	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25$ °C	40	A
	-Continuous (Silicon limited) $T_C = 25$ °C	132	
	-Continuous $T_A = 25$ °C (Note 1a)	27	
	-Pulsed	120	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	144	mJ
$P_D$	Power Dissipation $T_C = 25$ °C	59	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC7570S	FDMC7570S	Power 33	13 "	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^{\circ}\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$ , referenced to $25\text{ }^{\circ}\text{C}$		21		mV/ $^{\circ}\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$			500	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current, Forward	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 1\text{ mA}$	1.2	1.7	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 10\text{ mA}$ , referenced to $25\text{ }^{\circ}\text{C}$		-4		mV/ $^{\circ}\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 27\text{ A}$		1.6	2	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 21.5\text{ A}$		2.4	2.9	
		$V_{GS} = 10\text{ V}$ , $I_D = 27\text{ A}$ , $T_J = 125\text{ }^{\circ}\text{C}$		2.2	2.8	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 27\text{ A}$		154		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 13\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		3315	4410	pF
$C_{oss}$	Output Capacitance			1010	1345	pF
$C_{rss}$	Reverse Transfer Capacitance			168	255	pF
$R_g$	Gate Resistance			1.2	2.1	$\Omega$

**Switching Characteristics**

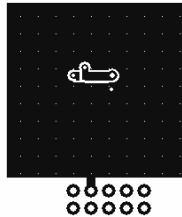
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 13\text{ V}$ , $I_D = 27\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		14	26	ns
$t_r$	Rise Time			6.8	14	ns
$t_{d(off)}$	Turn-Off Delay Time			34	55	ns
$t_f$	Fall Time			4.5	10	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$	$V_{DD} = 13\text{ V}$ $I_D = 27\text{ A}$	49	68	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$		22	31	nC
$Q_{gs}$	Gate to Source Gate Charge			10.8		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			5.5		nC

**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 27\text{ A}$ (Note 2)		0.78	1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = 2\text{ A}$ (Note 2)		0.43	0.8	
$t_{rr}$	Reverse Recovery Time	$I_F = 27\text{ A}$ , $di/dt = 300\text{ A}/\mu\text{s}$		30	48	ns
$Q_{rr}$	Reverse Recovery Charge			29	46	nC

**Notes:**

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $53\text{ }^{\circ}\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper.



b.  $125\text{ }^{\circ}\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width  $< 300\text{ }\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3.  $E_{AS}$  of  $144\text{ mJ}$  is based on starting  $T_J = 25\text{ }^{\circ}\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = 17\text{ A}$ ,  $V_{DD} = 23\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.3\text{ mH}$ ,  $I_{AS} = 25\text{ A}$

4. As an N-ch device, the negative Vgs rating is for lower duty cycle pulse occurrence only. No continuous rating is implied.

## Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

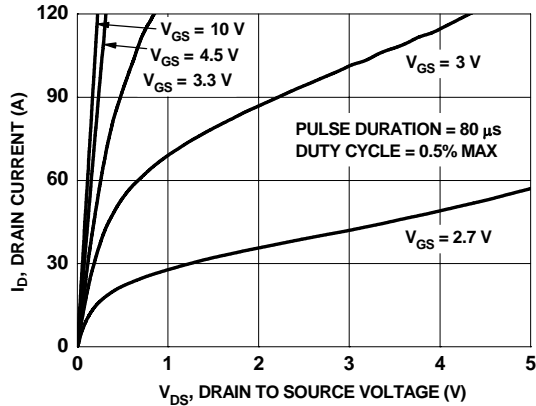


Figure 1. On-Region Characteristics

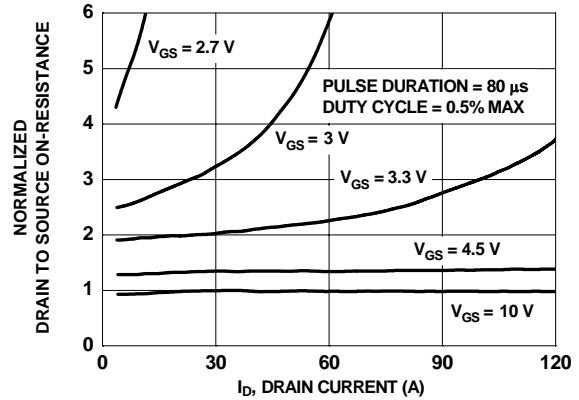


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

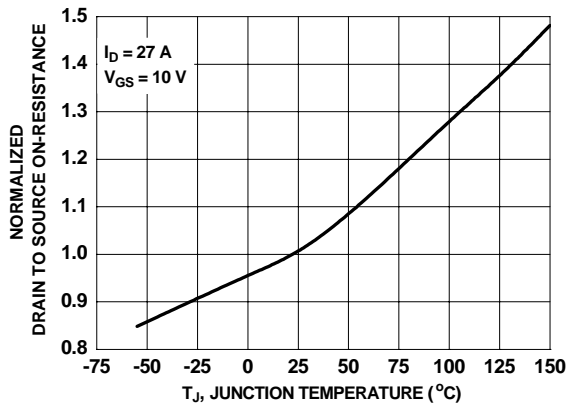


Figure 3. Normalized On-Resistance vs Junction Temperature

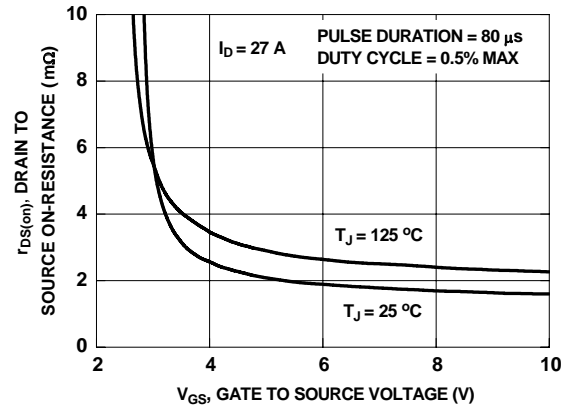


Figure 4. On-Resistance vs Gate to Source Voltage

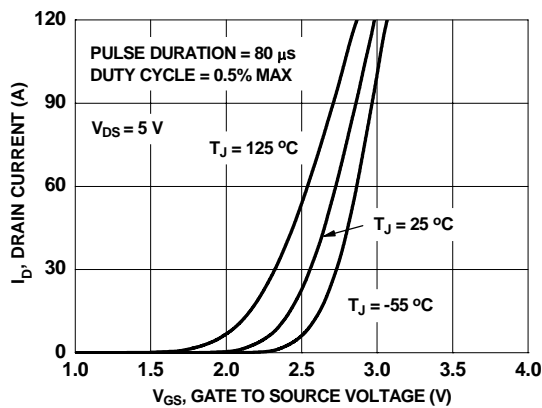


Figure 5. Transfer Characteristics

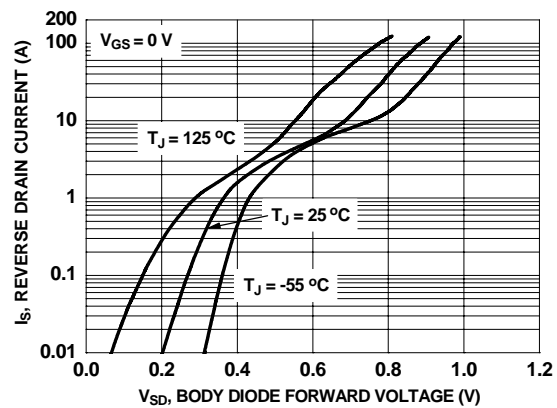


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

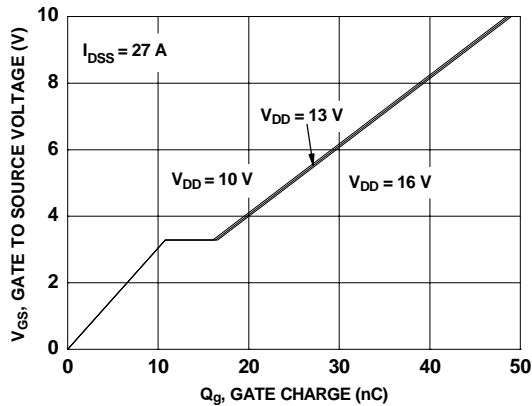


Figure 7. Gate Charge Characteristics

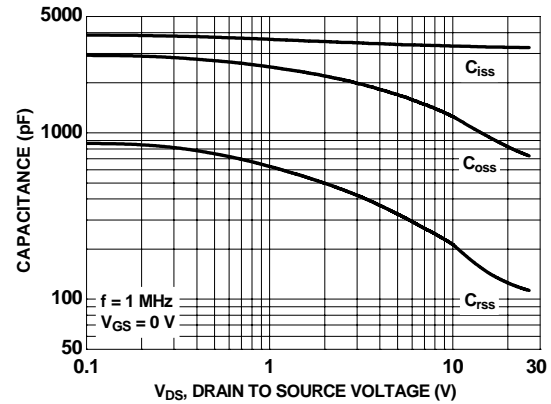


Figure 8. Capacitance vs Drain to Source Voltage

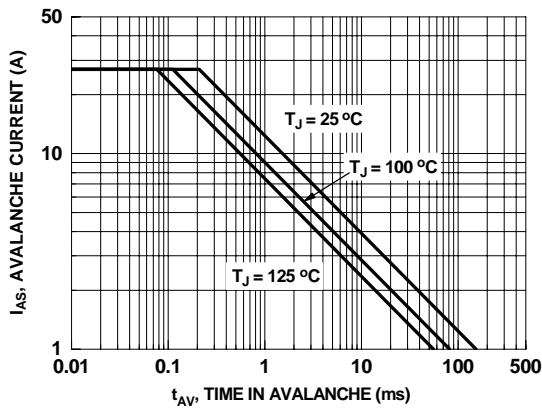


Figure 9. Unclamped Inductive Switching Capability

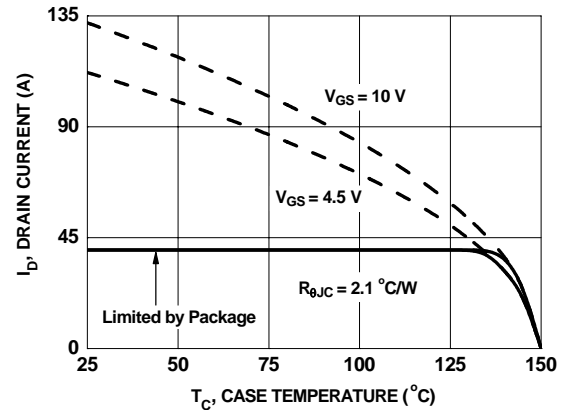


Figure 10. Maximum Continuous Drain Current vs Case Temperature

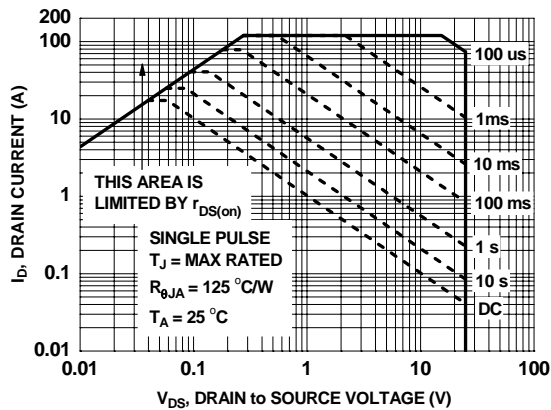


Figure 11. Forward Bias Safe Operating Area

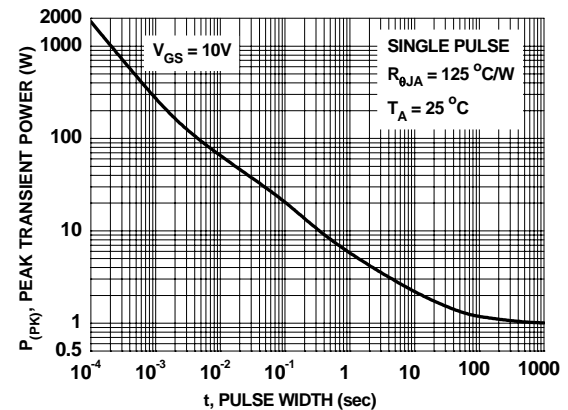
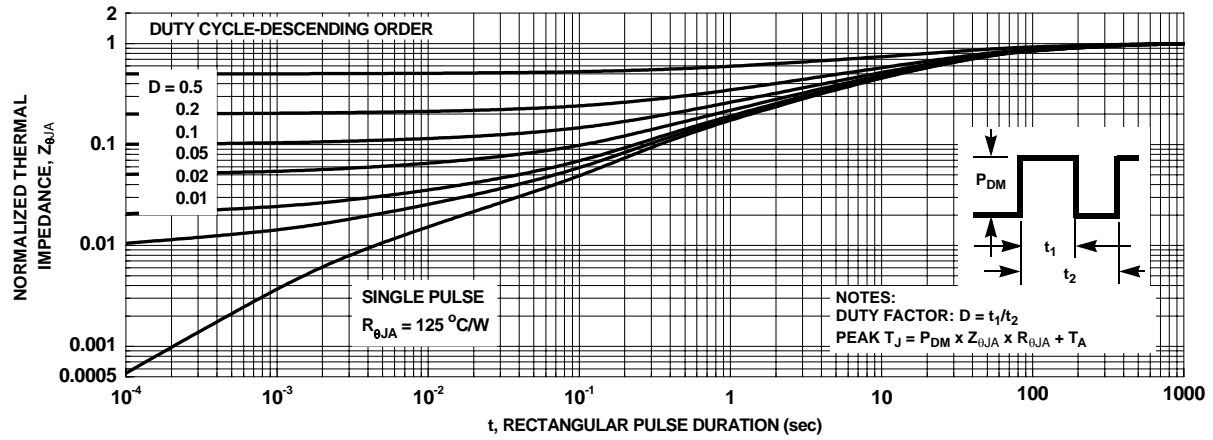


Figure 12. Single Pulse Maximum Power Dissipation

**Typical Characteristics**  $T_J = 25\text{ }^{\circ}\text{C}$  unless otherwise noted



## Typical Characteristics (continued)

### SyncFET Schottky body diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMC7570S.

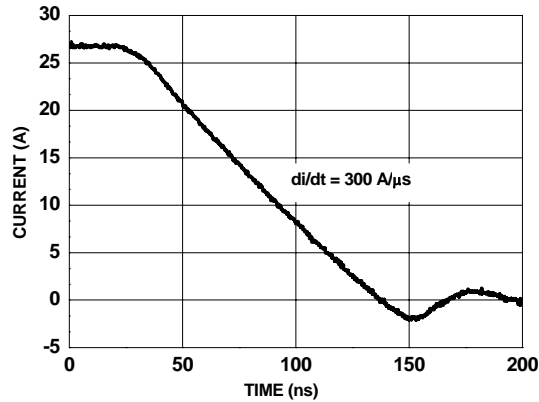


Figure 14. FDMC7570S SyncFET body diode reverse recovery characteristic

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

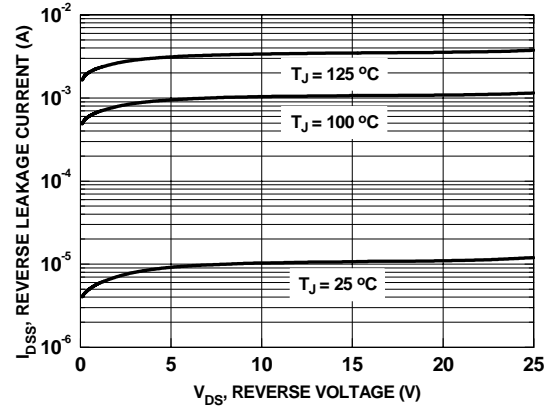
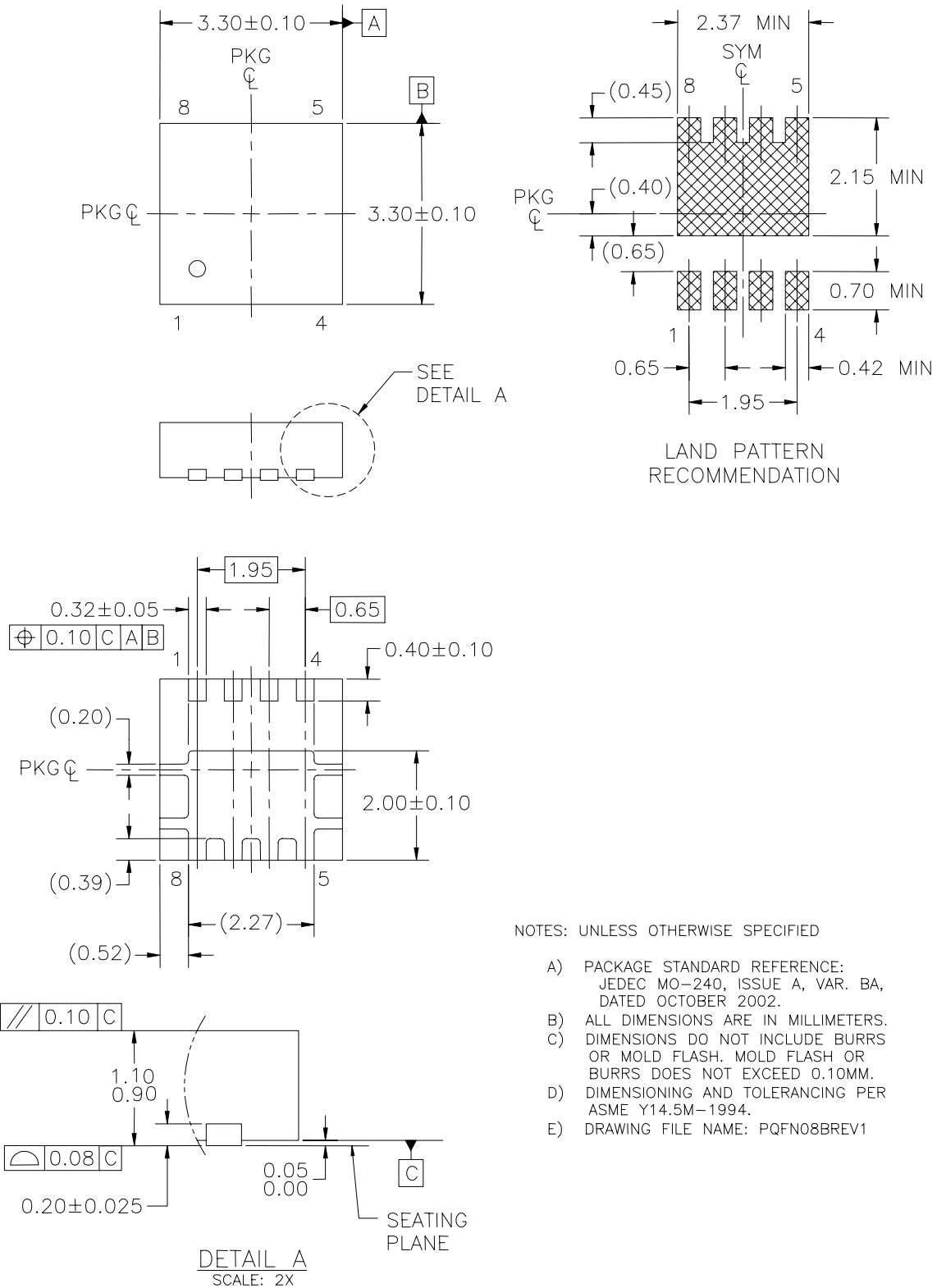


Figure 15. SyncFET body diode reverse leakage versus drain-source voltage

## Dimensional Outline and Pad Layout



PQFN08BREV1



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Rev. I45