

# FDG6306P

## P-Channel 2.5V Specified PowerTrench<sup>®</sup> MOSFET

### General Description

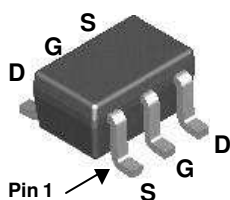
This PChannel 2.5V specified MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications with a wide range of gate drive voltage (2.5V – 12V).

### Applications

- Battery management
- Load switch

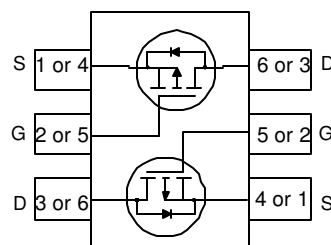
### Features

- –0.6 A, –20 V.  $R_{DS(ON)} = 420\text{ m}\Omega$  @  $V_{GS} = -4.5\text{ V}$   
 $R_{DS(ON)} = 630\text{ m}\Omega$  @  $V_{GS} = -2.5\text{ V}$
- Low gate charge
- High performance trench technology for extremely low  $R_{DS(ON)}$
- Compact industry standard SC70-6 surface mount package



**SC70-6**

The pinouts are symmetrical; pin 1 and pin 4 are interchangeable.



### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	–20	V
$V_{GSS}$	Gate-Source Voltage	$\pm 12$	V
$I_D$	Drain Current – Continuous (Note 1)	–0.6	A
	– Pulsed	–2.0	
$P_D$	Power Dissipation for Single Operation (Note 1)	0.3	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	–55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	415	$^\circ\text{C/W}$
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### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.06	FDG6306P	7"	8mm	3000 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	–20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$		–14		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			–1	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage, Forward	$V_{GS} = -12\text{ V}, V_{DS} = 0\text{ V}$			–100	nA
$I_{GSSR}$	Gate–Body Leakage, Reverse	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$			100	nA

**On Characteristics** (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	–0.6	–1.2	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$		3		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -4.5\text{ V}, I_D = -0.6\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -0.5\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -0.6\text{ A}, T_J = 125^\circ\text{C}$		300 470 400	420 630 700	M $\Omega$
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	–2			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -0.6\text{ A}$		1.8		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		114		pF
$C_{oss}$	Output Capacitance			24		pF
$C_{rss}$	Reverse Transfer Capacitance			9		pF

**Switching Characteristics** (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$		5.5	11	ns
$t_r$	Turn–On Rise Time			14	25	ns
$t_{d(off)}$	Turn–Off Delay Time			6	12	ns
$t_f$	Turn–Off Fall Time			1.7	3.4	ns
$Q_g$	Total Gate Charge	$V_{DS} = -10\text{ V}, I_D = -0.6\text{ A},$ $V_{GS} = -4.5\text{ V}$		1.4	2.0	nC
$Q_{gs}$	Gate–Source Charge			0.3		nC
$Q_{gd}$	Gate–Drain Charge			0.4		nC

**Drain–Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain–Source Diode Forward Current				–0.25	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -0.25\text{ A}$ (Note 2)		–0.77	–1.2	V

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.  $R_{\theta JA} = 415^\circ\text{C/W}$  when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

## Typical Characteristics

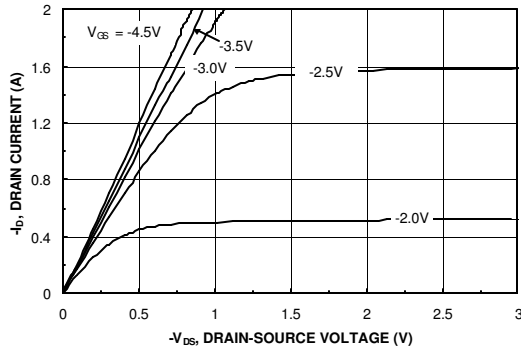


Figure 1. On-Region Characteristics.

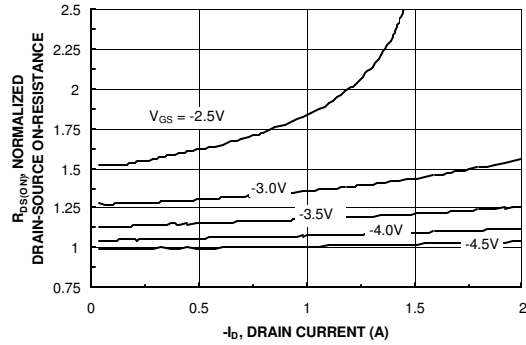


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

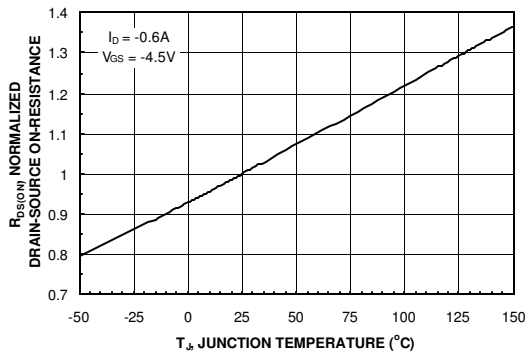


Figure 3. On-Resistance Variation with Temperature.

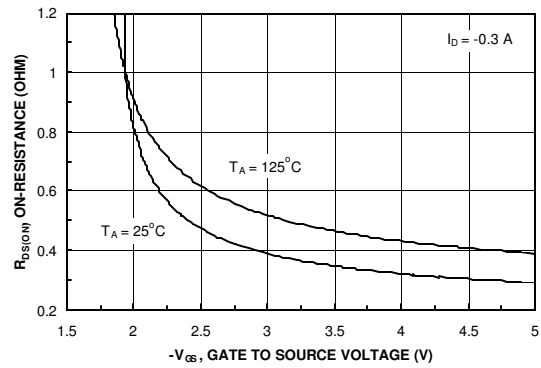


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

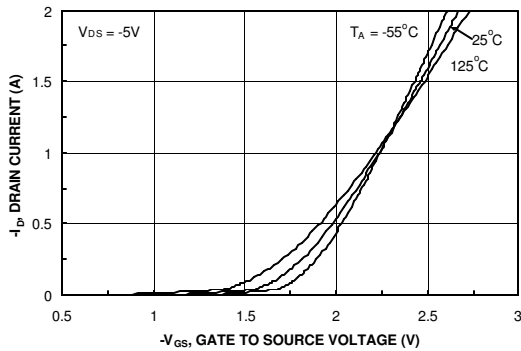


Figure 5. Transfer Characteristics.

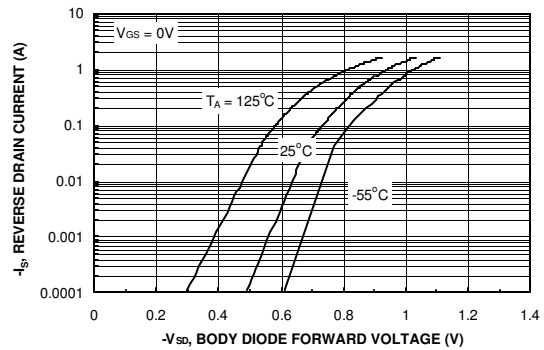


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics

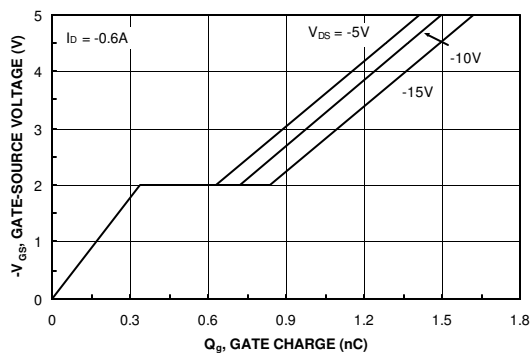


Figure 7. Gate Charge Characteristics.

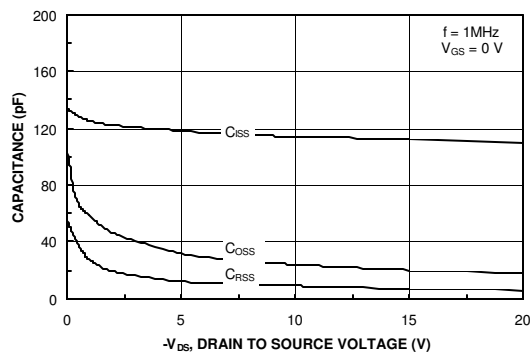


Figure 8. Capacitance Characteristics.

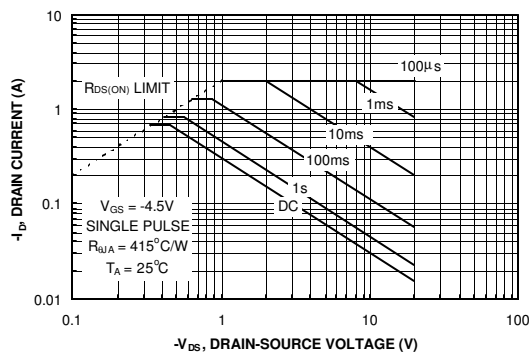


Figure 9. Maximum Safe Operating Area.

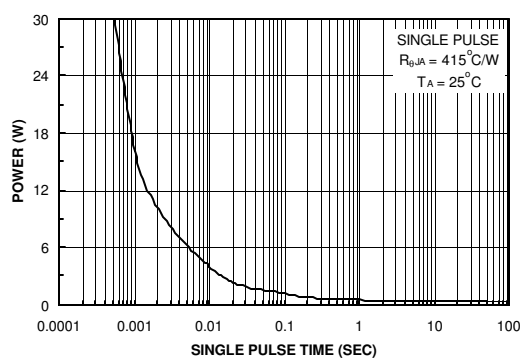


Figure 10. Single Pulse Maximum Power Dissipation.

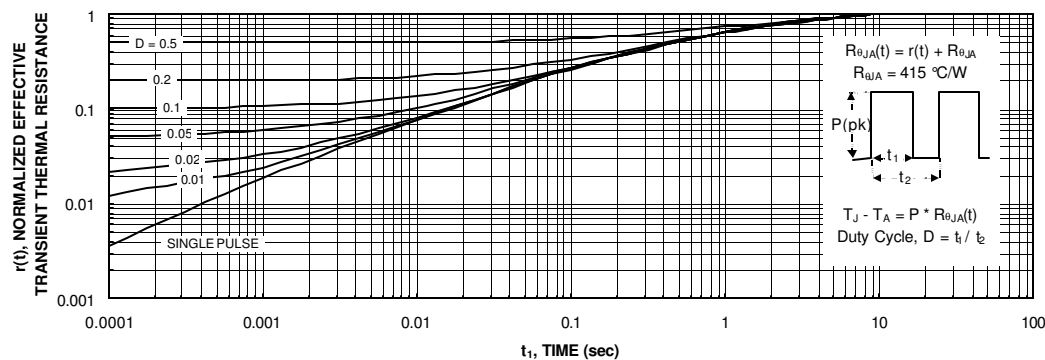


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1.  
Transient thermal response will change depending on the circuit board design.

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DOME™	ISOPLANAR™	Quiet Series™	
E <sup>2</sup> CMOS™	MICROWIRE™	SILENT SWITCHER®	
EnSigna™	OPTOLOGIC™	SMART START™	
FACT™	OPTOPLANAR™	SuperSOT™-3	
FACT Quiet Series™	PACMAN™	SuperSOT™-6	
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