FAIRCHILD
SEMICONDUCTOR™

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FDG313N

Digital FET, N-Channel

General Description

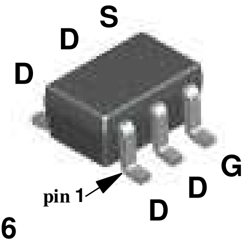
This N-Channel enhancement mode field effect transistor is produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistor and small signal MOSFET.

Applications

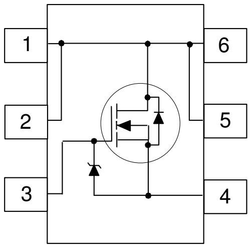
- Load switch
- Battery protection
- Power management

Features

- 0.95 A, 25 V. $R_{DS(on)} = 0.45\ \Omega$ @ $V_{GS} = 4.5$ V
  $R_{DS(on)} = 0.60\ \Omega$ @ $V_{GS} = 2.7$ V.
- Low gate charge (1.64 nC typical)
- Very low level gate drive requirements allowing direct operation in 3V circuits ($V_{GS(th)} < 1.5$V).
- Gate-Source Zener for ESD ruggedness (>6kV Human Body Model).
- Compact industry standard SC70-6 surface mount package.



SC70-6



Absolute Maximum Ratings

$T_A = 25°C$ unless otherwise noted

Symbol	Parameter		FDG313N	Units
V_{DSS}	Drain-Source Voltage		25	V
V_{GSS}	Gate-Source Voltage		± 8	V
I_D	Drain Current - Continuous	(Note 1a)	0.95	A
	- Pulsed		2	
P_D	Power Dissipation for Single Operation	(Note 1a)	0.75	W
		(Note 1b)	0.55	
		(Note 1c)	0.48	
T_J, T_{stg}	Operating and Storage Junction Temperature Range		-55 to +150	°C
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm)		6	kV

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1c)	260	°C/W

Package Outlines and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.13	FDG313N	7”	8mm	3000 units

DMOS Electrical Characteristics

$T_A = 25°C$ unless otherwise noted

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ µA	25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25°C		30		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 20$ V, $V_{GS} = 0$ V			1	µA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = 8$ V, $V_{DS} = 0$ V			100	nA

On Characteristics (Note 2)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ µA	0.65	0.8	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25°C		-2		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5$ V, $I_D = 0.5$ A $V_{GS} = 4.5$ V, $I_D = 0.5$ A @ 125°C $V_{GS} = 2.7$ V, $I_D = 0.2$ A		0.35 0.53 0.45	0.45 0.76 0.6	Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5$ V, $V_{DS} = 5$ V	0.5			A
g_{FS}	Forward Transconductance	$V_{DS} = 5$ V, $I_D = 0.5$ A		1.5		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	$V_{DS} = 10$ V, $V_{GS} = 0$ V, f = 1.0 MHz		50		pF
C_{oss}	Output Capacitance			28		pF
C_{rss}	Reverse Transfer Capacitance			9		pF

Switching Characteristics (Note 2)

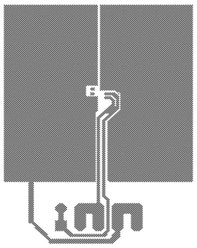
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 6$ V, $I_D = 0.5$ A, $V_{GS} = 4.5$ V, $R_{GEN} = 50$ Ω		3	6	ns
t_r	Turn-On Rise Time			8.5	18	ns
$t_{d(off)}$	Turn-Off Delay Time			17	30	ns
t_f	Turn-Off Fall Time			13	25	ns
Q_g	Total Gate Charge	$V_{DS} = 5$ V, $I_D = 0.95$ A, $V_{GS} = 4.5$ V		1.64	2.3	nC
Q_{gs}	Gate-Source Charge			0.38		nC
Q_{gd}	Gate-Drain Charge			0.45		nC

Drain-Source Diode Characteristics and Maximum Ratings

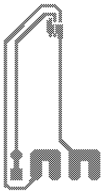
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_S	Maximum Continuous Drain-Source Diode Forward Current				0.6	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 0.6$ A (Note 2)		0.8	1.2	V

Notes:

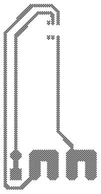
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 170°C/W when mounted on a 1 in^2 pad of 2oz copper.



b) 225°C/W when mounted on a half of package sized 2oz. copper.



c) 260°C/W when mounted on a minimum pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

Typical Characteristics

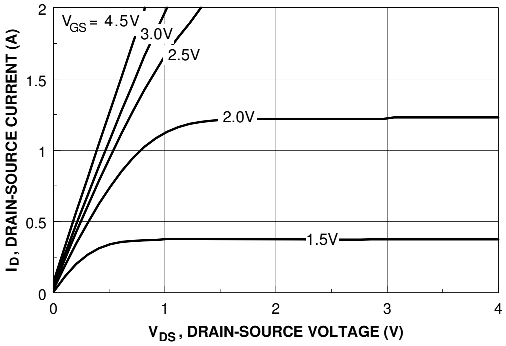


Figure 1. On-Region Characteristics.

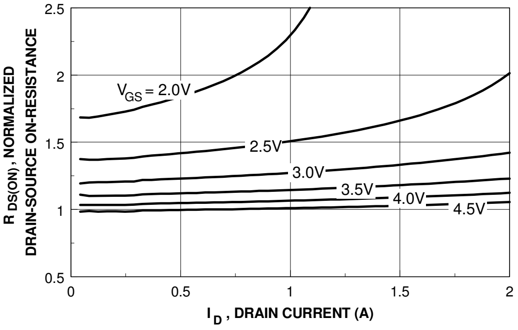


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

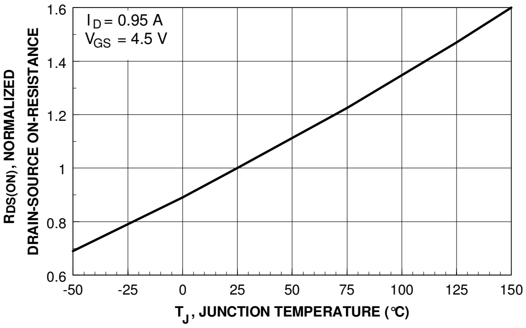


Figure 3. On-Resistance Variation with Temperature.

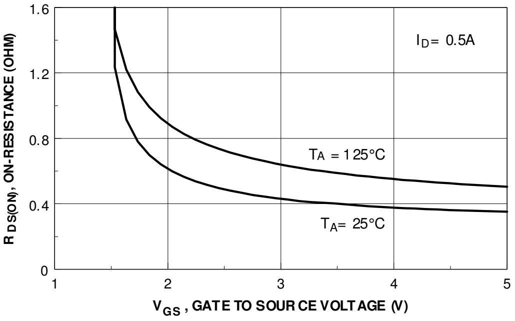


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

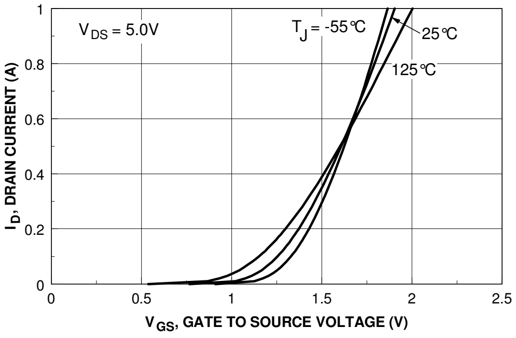


Figure 5. Transfer Characteristics.

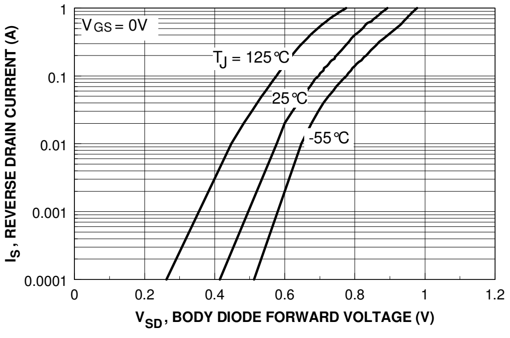


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

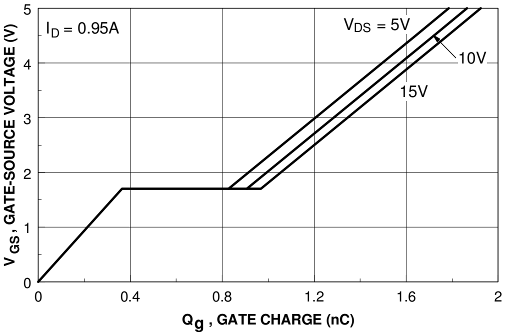


Figure 7. Gate-Charge Characteristics.

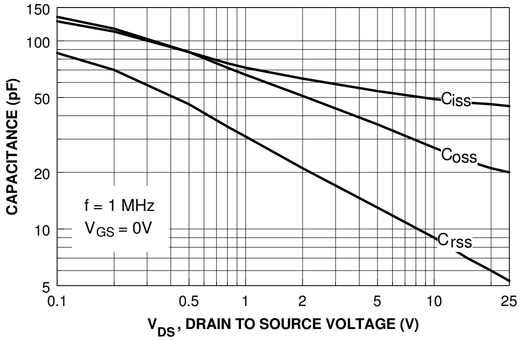


Figure 8. Capacitance Characteristics.

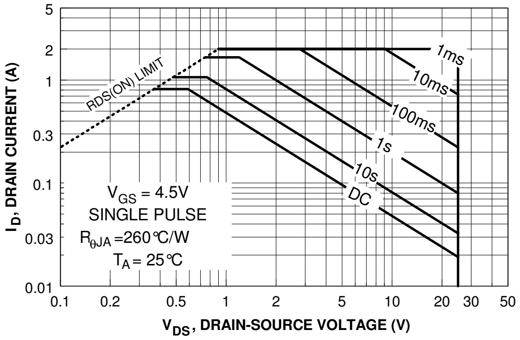


Figure 9. Maximum Safe Operating Area.

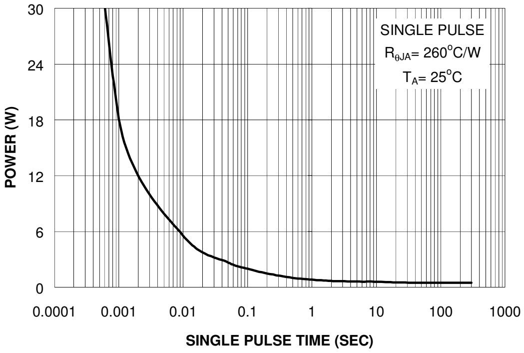


Figure 10. Single Pulse Maximum Power Dissipation.

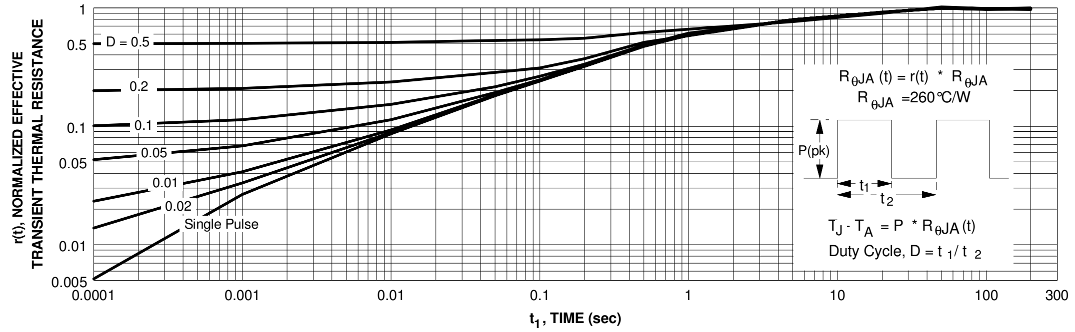


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient themal response will change depending on the circuit board design.

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