

FDFMA3N109

Integrated N-Channel PowerTrench® MOSFET and Schottky Diode

General Description

This device is designed specifically as a single package solution for a boost topology in cellular handset and other ultra-portable applications. It features a MOSFET with low input capacitance, total gate charge and onstate resistance, and an independently connected schottky diode with low forward voltage and reverse leakage current to maximize boost efficiency.

The MicroFET 2x2 package offers exceptional thermal performance for its physical size and is well suited to switching and linear mode applications.

Features

MOSFET:

• 2.9 A, 30 V $R_{DS(ON)}$ = 123 $m\Omega$ @ V_{GS} = 4.5 V

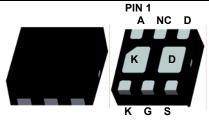
 $R_{DS(ON)}$ = 140 m Ω @ V_{GS} = 3.0 V

 $R_{DS(ON)} = 163 \text{ m}\Omega @ V_{GS} = 2.5 \text{ V}$

Schottky:

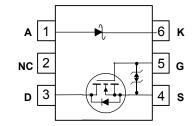
- V_F < 0.46 V @ 500mA
- Low profile 0.8 mm maximum in the new package MicroFET 2x2 mm
- HBM ESD protection level = 1.8kV typical (Note 3)
- RoHS Compliant





MicroFET 2x2





Symbol	Parameter	Ratings	Units	
V _{DS}	Drain-Source Voltage		30	V
V _{GS}	Gate-Source Voltage	±12	V	
I _D	Drain Current – Continuous (T _C = 25°C, V _{GS} = 4.5V)		2.9	
	- Continuous ($T_C = 25^{\circ}C$, $V_{GS} = 2.5V$)		2.7	Α
	– Pulsed		10	
P _D	Power Dissipation for Single Operation	(Note 1a)	1.5	W
	Power Dissipation for Single Operation	(Note 1b)	0.65	VV
T_J, T_{STG}	Operating and Storage Temperature		-55 to +150	°C
V_{RRM}	Schottky Repetitive Peak Reverse Voltage		28	V
Io	Schottky Average Forward Current		1	Α

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient	(Note 1a)	83	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	193	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1c)	101	C/VV
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1d)	228	

Package Marking and Ordering Information

	J : : : : :			
Device Marking	Device	Reel Size	Tape width	Quantity
109	FDFMA3N109	7"	8mm	3000 units

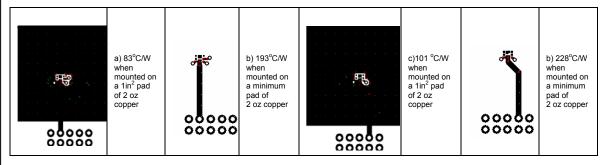
Symbol	Parameter	Test Con	ditions	Min	Тур	Max	Units
Off Char	acteristics	1			I	I	
BV _{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0 V$, $I_D =$	250 μΑ	30			V
ΔBV _{DSS} ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, Refere			25		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS}	; = 0 V			1	μА
I _{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 12 \text{ V}, V_{DS}$; = 0 V			±10	μА
On Char	acteristics	•					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D =$	250 μΑ	0.4	1.0	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250 \mu A$, Refere	enced to 25°C		-3		mV/°C
		$V_{GS} = 4.5V, I_D = 2.9$	9A		75	123	
		$V_{GS} = 3.0V, I_{D} = 2.7A$			84	140	
R _{DS(on)}	Static Drain–Source	$V_{GS} = 2.5V, I_D = 2.5$			92	163	mΩ
-(- /	On–Resistance	$V_{GS} = 4.5V, I_D = 2.9A, T_C = 85^{\circ}C$			95	166	- -
		$V_{GS} = 3.0V, I_D = 2.7A, T_C = 150^{\circ}C$ $V_{GS} = 2.5V, I_D = 2.5A, T_C = 150^{\circ}C$			138 150	203 268	
Dumanaia	Charactaristics	V _{GS} - 2.5V, I _D - 2.5	DA, 1c - 150 C		150	200	
C _{iss}	Input Capacitance	V 45V V	0.17	1	190	220	pF
Coss	Output Capacitance	$V_{DS} = 15 \text{ V}, V_{GS}$ f = 1.0 MHz	$_{\rm S}$ = 0 V,		30	40	рF
	<u>' '</u>	1 - 1.0 MITZ					
C _{rss}	Reverse Transfer Capacitance Gate Resistance	V _{GS} = 0 V, f =	1 O MU-7		20 4.6	30	pF Ω
		V GS - O V, I -	1.0 IVII 12		4.0		52
	g Characteristics (Note 2)	V _{DD} = 15 V, I _D =	. 1 A			40	
t _{d(on)}	Turn-On Delay Time	$V_{GS} = 15 \text{ V}, I_D = 15 \text{ V}$,		6	12	ns
t _r	Turn-On Rise Time	VGS - 4.5 V, NGEN - 0 12			8	16	ns
t _{d(off)}	Turn–Off Delay Time	_			12	21	ns
t _f	Turn–Off Fall Time				2	4	ns
Q _g	Total Gate Charge	$V_{DS} = 15 \text{ V}, \qquad I_{D} = 2.9 \text{ A},$ $V_{GS} = 4.5 \text{ V}$			2.4	3.0	nC
Q _{gs}	Gate–Source Charge				0.35		nC
Q _{gd}	Gate-Drain Charge				0.75		nC
Drain-Sc	urce Diode Characteristics						
Is	Maximum Continuous Drain-Source	e Diode Forward Cur	rent			2.9	Α
V_{SD}	Drain–Source Diode Forward	I _S = 2.0 A			0.9	1.2	V
	Voltage	I _S = 1.1 A			8.0	1.2	
t _{rr}	Diode Reverse Recovery Time	$I_F = 2.9 \text{ A},$			10		ns
Q _{rr}	Diode Reverse Recovery Charge	dI _F /dt = 100 A/μs			2		nC
Schottky	Diode Characteristics						
I_R	Reverse Leakage	V _R = 28 V	$T_J = 25^{\circ}C$		10	100	μΑ
ית		VK 20 V	T _J = 85°C		0.07	4.7	mA
V _F	Forward Voltage	I _F = 1 A	T _J = 25°C		0.50	0.57	V
• 15		173	T _J = 85°C		0.49	0.60	
V_{F}	Forward Voltage	I _F = 500 mA	T _J = 25°C		0.40	0.46	V
•		1 '	T _J = 85°C	1	0.36	0.43	

Electrical Characteristics

T_A = 25°C unless otherwise noted

Notes:

- 1. R_{0,JA} is determined with the device mounted on a 1 in² oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0,JC} is guaranteed by design while R_{0,JA} is determined by the user's board design.
 - (a) MOSFET R_{0JA} = 83°C/W when mounted on a 1in² pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB
 - (b) MOSFET $R_{\theta JA}$ = 193°C/W when mounted on a minimum pad of 2 oz copper
 - (c) Schottky $R_{\theta JA}$ = 101°C/W when mounted on a 1in² pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB
 - (d) Schottky $R_{\theta JA}$ = 228°C/W when mounted on a minimum pad of 2 oz copper



Scale 1:1 on letter size paper

- **2.** Pulse Test: Pulse Width < 300μ s, Duty Cycle < 2.0%
- 3: The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics

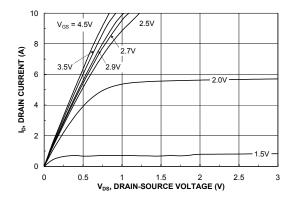


Figure 1. On-Region Characteristics.

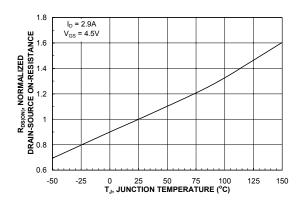


Figure 3. On-Resistance Variation with Temperature.

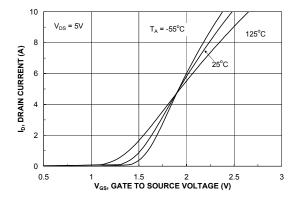


Figure 5. Transfer Characteristics.

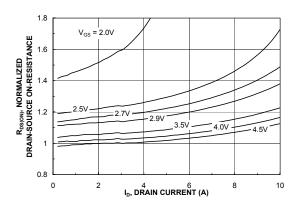


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

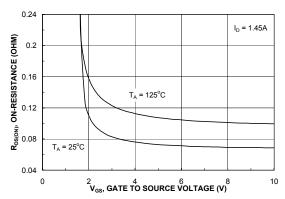


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

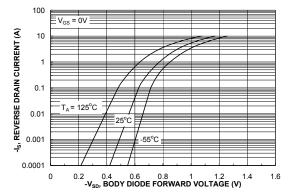
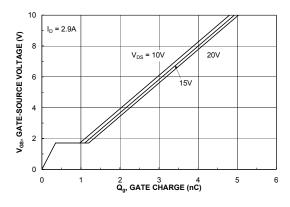


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics



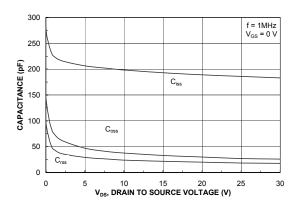
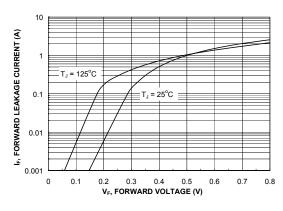


Figure 7. Gate Charge Characteristics.





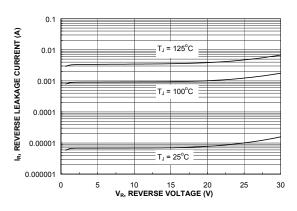


Figure 9. Schottky Diode Forward Voltage.

Figure 10. Schottky Diode Reverse Current.

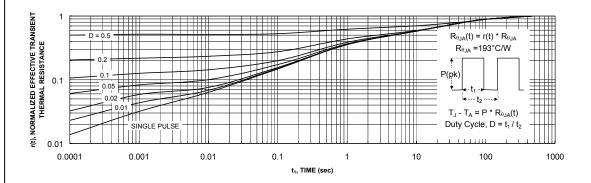


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.





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