FAIRCHILD SEMICONDUCTOR®

May 2011

FDD6685

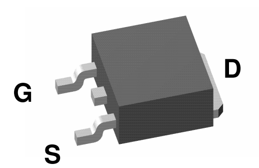
30V P-Channel PowerTrench® MOSFET

General Description

This P-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gave drive voltage ratings (4.5V – 25V).

Features

- –40 A, –30 V. $R_{DS(ON)}$ = 20 mΩ @ V_{GS} = –10 V
  $R_{DS(ON)}$ = 30 mΩ @ V_{GS} = –4.5 V
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability
- Qualified to AEC Q101



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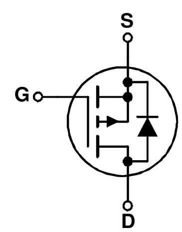


Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		–30	V
V_{GSS}	Gate-Source Voltage		±25	V
I_D	Continuous Drain Current @T_C=25°C	(Note 3)	–40	A
	@T_A=25°C	(Note 1a)	–11	
	Pulsed, PW ≤ 100µs	(Note 1b)	–100	
P_D	Power Dissipation for Single Operation	(Note 1)	52	W
		(Note 1a)	3.8	
		(Note 1b)	1.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	2.9	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	96	°C/W

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at http://www.aecouncil.com/
Reliability data can be found at: http://www.fairchildsemi.com/products/discrete/reliability/index.html.
All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
FDD6685	FDD6685	13"	12mm	2500 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 4)						
E_{AS}	Single Pulse Drain-Source Avalanche Energy	I_D = –11 A		42		mJ
I_{AS}	Maximum Drain-Source Avalanche Current			–11		A
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 µA	–30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C		–24		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –24 V, V_{GS} = 0 V			–1	µA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±25V, V_{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 µA	–1	–1.8	–3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C		5		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –10 V, I_D = –11 A V_{GS} = –4.5 V, I_D = –9 A V_{GS} = –10 V, I_D = –11 A, T_J=125°C		14 21 20	20 30	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = –10 V, V_{DS} = –5 V	–20			A
g_{FS}	Forward Transconductance	V_{DS} = –5 V, I_D = –11 A		26		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –15 V, V_{GS} = 0 V, f = 1.0 MHz		1715		pF
C_{oss}	Output Capacitance			440		pF
C_{rss}	Reverse Transfer Capacitance			225		pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz		3.6		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –15 V, I_D = –1 A, V_{GS} = –10 V, R_{GEN} = 6 Ω		17	31	ns
t_r	Turn–On Rise Time			11	21	ns
$t_{d(off)}$	Turn–Off Delay Time			43	68	ns
t_f	Turn–Off Fall Time			21	34	ns
Q_g	Total Gate Charge	V_{DS} = –15V, I_D = –11 A, V_{GS} = –5 V		17	24	nC
Q_{gs}	Gate–Source Charge			9		nC
Q_{gd}	Gate–Drain Charge			4		nC
Drain–Source Diode Characteristics and Maximum Ratings						
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –3.2 A (Note 2)		–0.8	–1.2	V
Trr	Diode Reverse Recovery Time	IF = –11 A, diF/dt = 100 A/µs		26		ns
Qrr	Diode Reverse Recovery Charge			13		nC

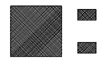
Electrical Characteristics

$T_A = 25°C$ unless otherwise noted

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) $R_{\theta JA} = 40°C/W$ when mounted on a $1in^2$ pad of 2 oz copper



b) $R_{\theta JA} = 96°C/W$ when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

3. Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$ where P_D is maximum power dissipation at $T_C = 25°C$ and $R_{DS(on)}$ is at $T_{J(max)}$ and $V_{GS} = 10V$.

4. Starting $T_J = 25°C$, $L = 0.69mH$, $I_{AS} = -11A$

Typical Characteristics

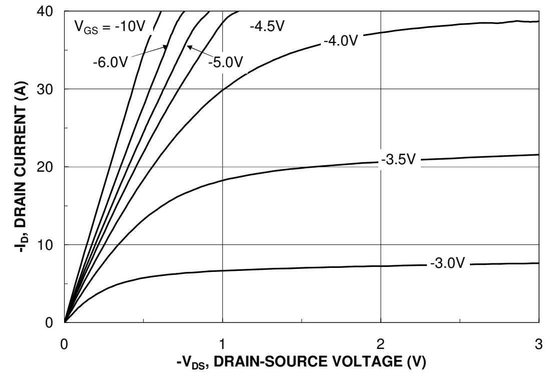


Figure 1. On-Region Characteristics.

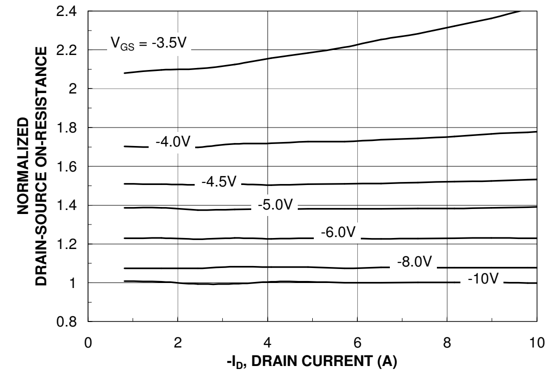


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

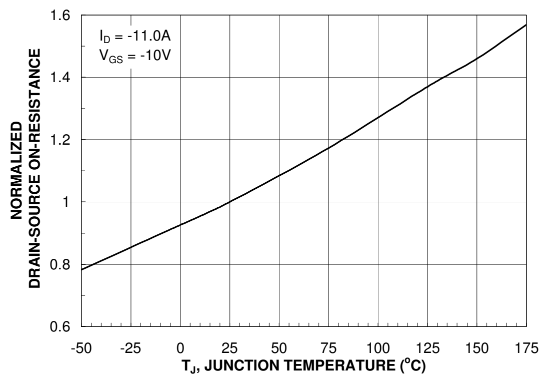


Figure 3. On-Resistance Variation with Temperature.

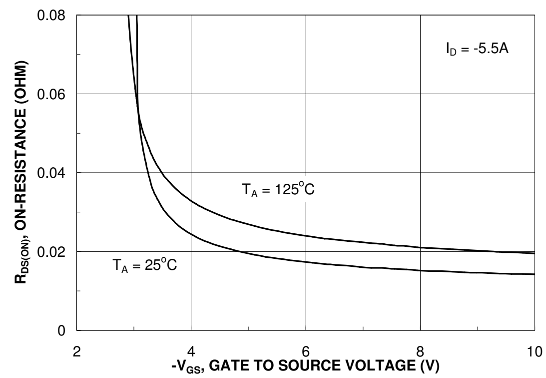


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

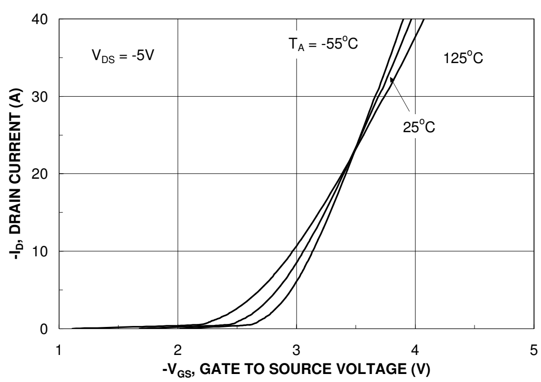


Figure 5. Transfer Characteristics.

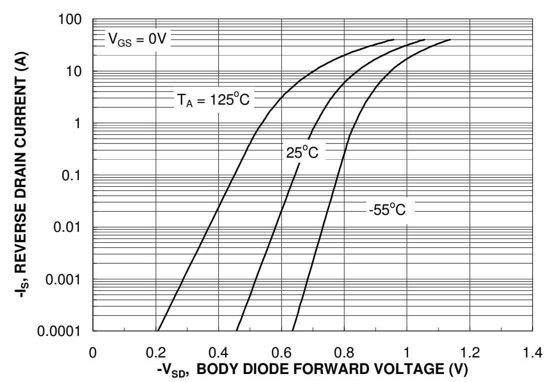


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

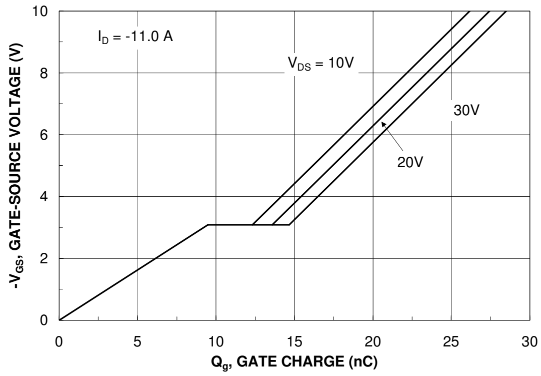


Figure 7. Gate Charge Characteristics.

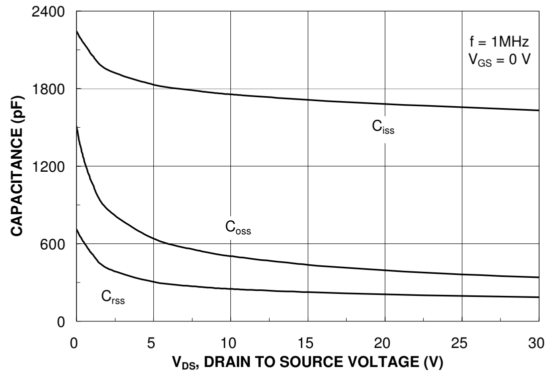


Figure 8. Capacitance Characteristics.

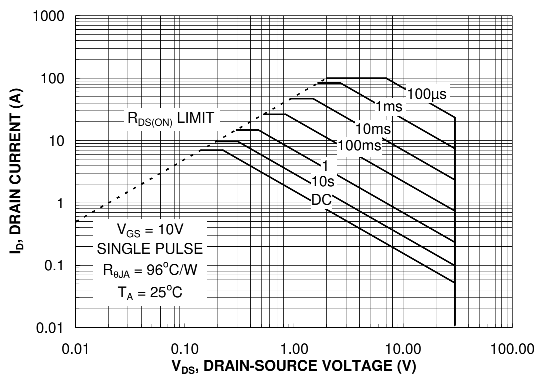


Figure 9. Maximum Safe Operating Area.

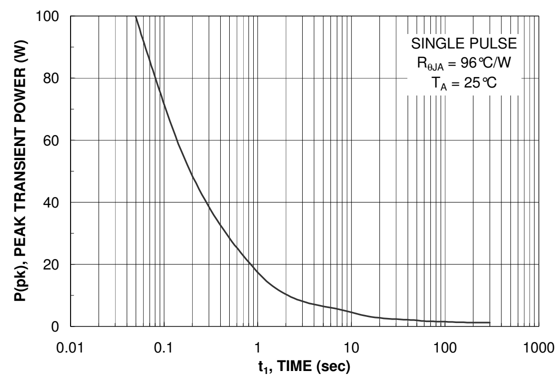


Figure 10. Single Pulse Maximum Power Dissipation.

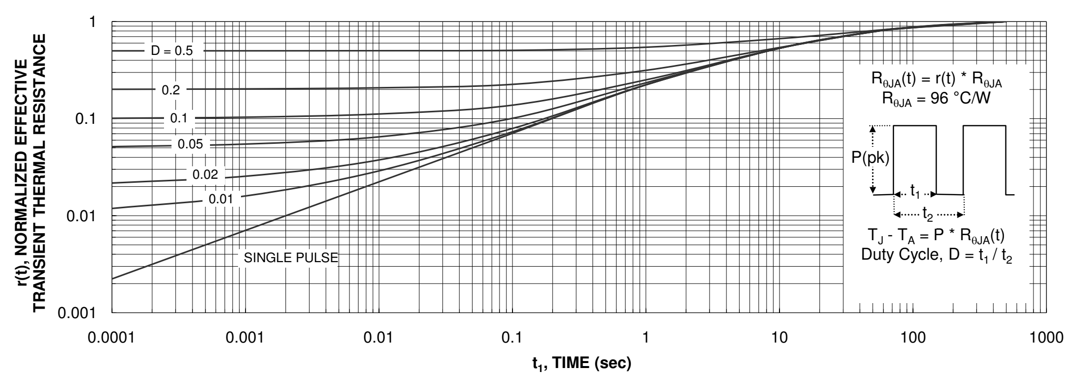


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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Rev. I54