

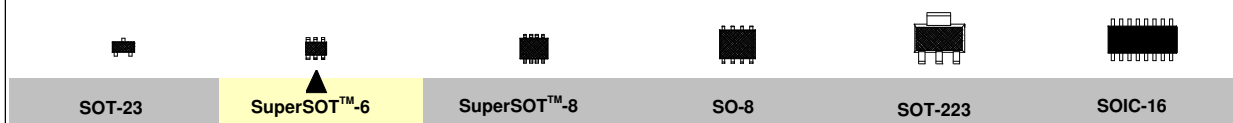
## FDC6304P Digital FET, Dual P-Channel

### General Description

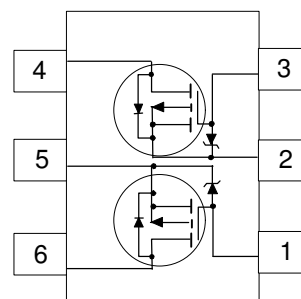
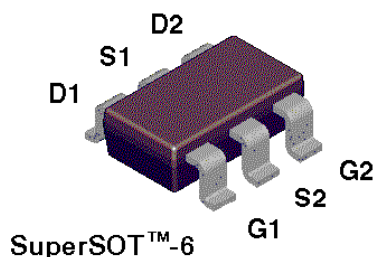
These P-Channel enhancement mode field effect transistor are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is tailored to minimize on-state resistance at low gate drive conditions. This device is designed especially for application in battery power applications such as notebook computers and cellular phones. This device has excellent on-state resistance even at gate drive voltages as low as 2.5 volts.

### Features

- -25 V, -0.46 A continuous, -1.0 A Peak.  
 $R_{DS(ON)} = 1.5 \Omega @ V_{GS} = -2.7 V$   
 $R_{DS(ON)} = 1.1 \Omega @ V_{GS} = -4.5 V.$
- Very low level gate drive requirements allowing direct operation in 3V circuits.  $V_{GS(th)} < 1.5 V.$
- Gate-Source Zener for ESD ruggedness.  
 >6kV Human Body Model.



Mark: .304



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless other wise noted

Symbol	Parameter	FDC6304P	Units
$V_{DSS}$	Drain-Source Voltage	-25	V
$V_{GSS}$	Gate-Source Voltage	-8	V
$I_D$	Drain Current - Continuous	-0.46	A
	- Pulsed	-1	
$P_D$	Maximum Power Dissipation (Note 1a)	0.9	W
	(Note 1b)	0.7	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm)	6.0	kV

### THERMAL CHARACTERISTICS

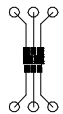
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	140	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	60	$^\circ\text{C/W}$

# Electrical Characteristics (T<sub>A</sub> = 25 °C unless otherwise noted )

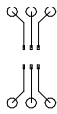
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-25			V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	I <sub>D</sub> = -250 μA, Referenced to 25 °C		-22		mV / °C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V T <sub>J</sub> = 55 °C			-1	μA
					-10	μA
I <sub>GSS</sub>	Gate - Body Leakage Current	V <sub>GS</sub> = -8 V, V <sub>DS</sub> = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Temp. Coefficient	I <sub>D</sub> = -250 μA, Referenced to 25 °C		2.1		mV / °C
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-0.65	-0.86	-1.5	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = -2.7 V, I <sub>D</sub> = -0.25 A		1.22	1.5	Ω
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -0.5 A		0.87	1.1	
		T <sub>J</sub> = 125 °C		1.21	2	
I <sub>D(ON)</sub>	On-State Drain Current	V <sub>GS</sub> = -2.7 V, V <sub>DS</sub> = -5 V	-0.5			A
		V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -5 V	-1			
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = -5 V, I <sub>D</sub> = -0.5 A		0.8		S
DYNAMIC CHARACTERISTICS						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		62		pF
C <sub>oss</sub>	Output Capacitance			35		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			9.5		pF
SWITCHING CHARACTERISTICS (Note 2)						
t <sub>D(on)</sub>	Turn - On Delay Time	V <sub>DD</sub> = -6 V, I <sub>D</sub> = -0.5 A, V <sub>GS</sub> = -4.5 V, R <sub>GEN</sub> = 50 Ω		7	20	ns
t <sub>r</sub>	Turn - On Rise Time			8	20	ns
t <sub>D(off)</sub>	Turn - Off Delay Time			55	110	ns
t <sub>f</sub>	Turn - Off Fall Time			35	70	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = -5 V, I <sub>D</sub> = -0.25 A, V <sub>GS</sub> = -4.5 V		1.1	1.5	nC
Q <sub>gs</sub>	Gate-Source Charge			0.32		nC
Q <sub>gd</sub>	Gate-Drain Charge			0.28		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				-0.5	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -0.5 A (Note 2)		-0.88	-1.2	V

Notes:

1. R<sub>JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>JA</sub> is guaranteed by design while R<sub>JA</sub> is determined by the user's board design.



a. 140°C/W on a 0.125 in² pad of 2oz copper.



b. 180°C/W on a 0.005 in² pad of 2oz copper.

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

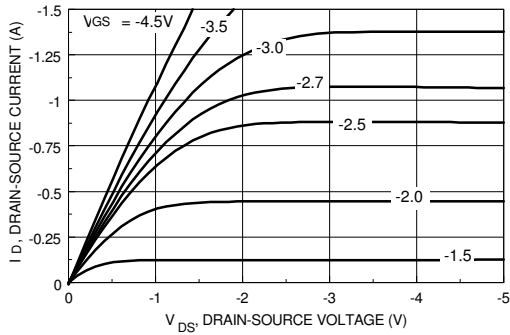


Figure 1. On-Region Characteristics.

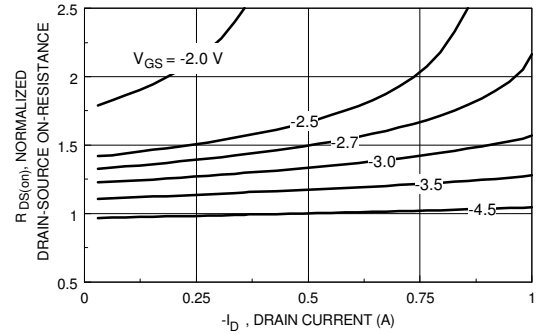


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

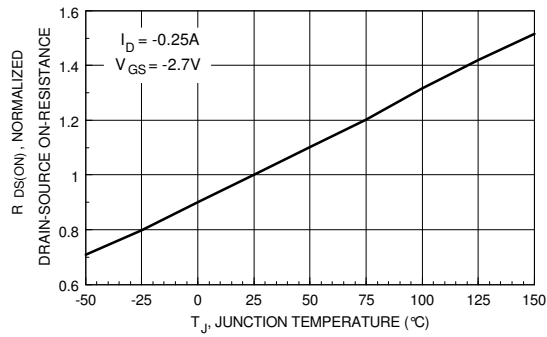


Figure 3. On-Resistance Variation with Temperature.

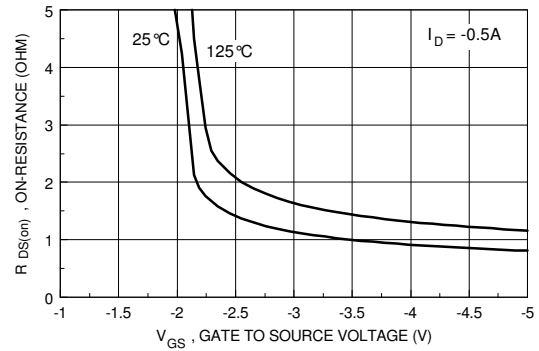


Figure 4. On Resistance Variation with Gate-To- Source Voltage.

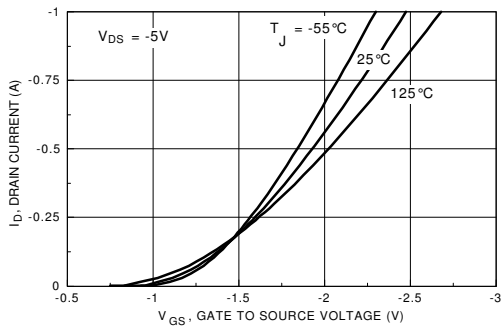


Figure 5. Transfer Characteristics.

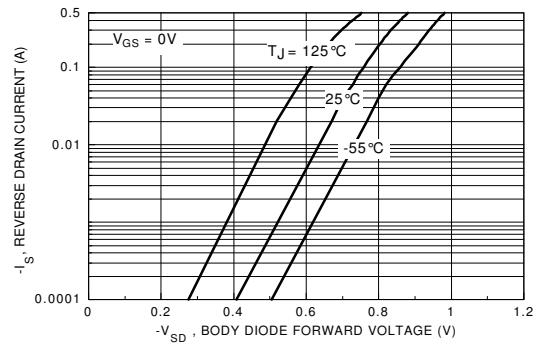


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Electrical And Thermal Characteristics

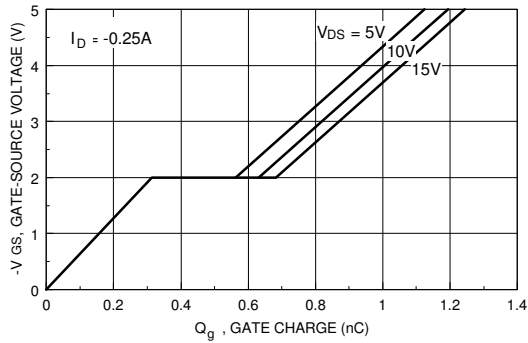


Figure 7. Gate Charge Characteristics.

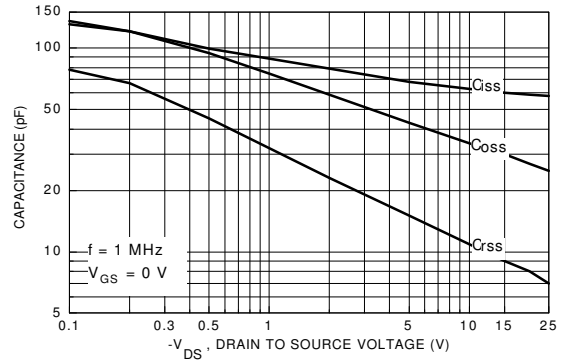


Figure 8. Capacitance Characteristics.

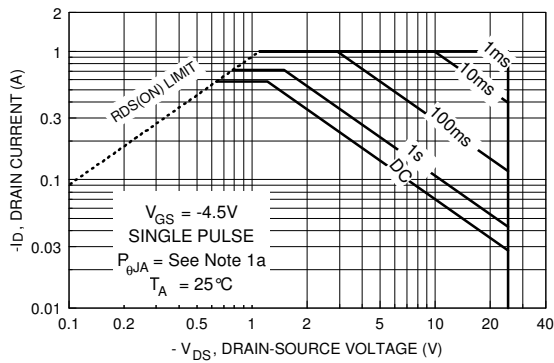


Figure 9. Maximum Safe Operating Area.

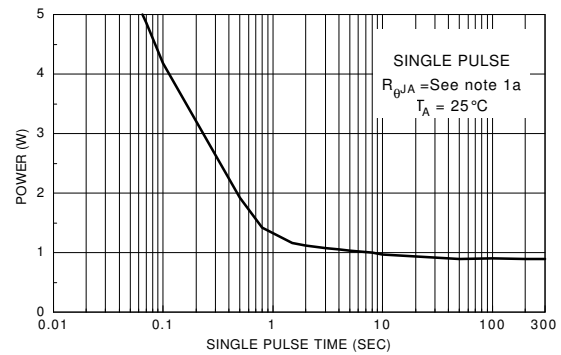


Figure 10. Single Pulse Maximum Power Dissipation.

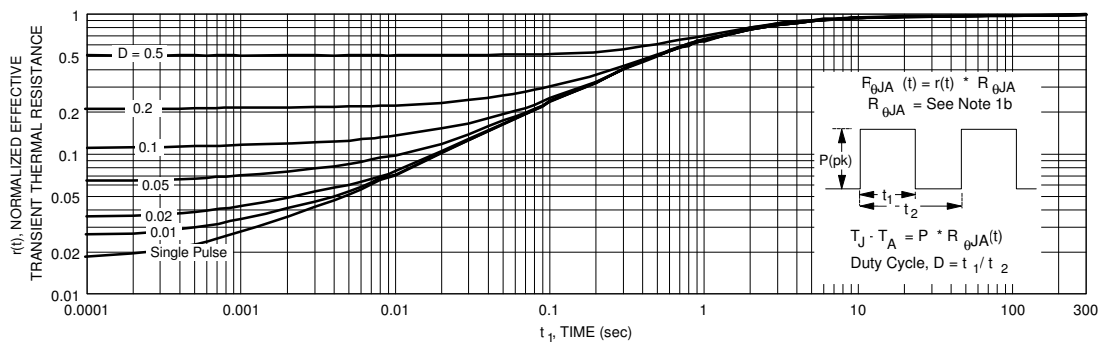


Figure 11. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.

## TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE <sub>x</sub> <sup>™</sup>	FAST <sup>®</sup>	OPTOLOGIC <sup>™</sup>	SMART START <sup>™</sup>	VCX <sup>™</sup>
Bottomless <sup>™</sup>	FAST <sub>r</sub> <sup>™</sup>	OPTOPLANAR <sup>™</sup>	STAR*POWER <sup>™</sup>	
CoolFET <sup>™</sup>	FRFET <sup>™</sup>	PACMAN <sup>™</sup>	Stealth <sup>™</sup>	
CROSSVOLT <sup>™</sup>	GlobalOptoisolator <sup>™</sup>	POP <sup>™</sup>	SuperSOT <sup>™</sup> -3	
DenseTrench <sup>™</sup>	GTO <sup>™</sup>	Power247 <sup>™</sup>	SuperSOT <sup>™</sup> -6	
DOME <sup>™</sup>	HiSeC <sup>™</sup>	PowerTrench <sup>®</sup>	SuperSOT <sup>™</sup> -8	
EcoSPARK <sup>™</sup>	ISOPLANAR <sup>™</sup>	QFET <sup>™</sup>	SyncFET <sup>™</sup>	
E <sup>2</sup> CMOS <sup>™</sup>	LittleFET <sup>™</sup>	QS <sup>™</sup>	TinyLogic <sup>™</sup>	
EnSigna <sup>™</sup>	MicroFET <sup>™</sup>	QT Optoelectronics <sup>™</sup>	TruTranslation <sup>™</sup>	
FACT <sup>™</sup>	MicroPak <sup>™</sup>	Quiet Series <sup>™</sup>	UHC <sup>™</sup>	
FACT Quiet Series <sup>™</sup>	MICROWIRE <sup>™</sup>	SILENT SWITCHER <sup>®</sup>	UltraFET <sup>®</sup>	

STAR\*POWER is used under license

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.