FAN5009

Dual Bootstrapped 12V MOSFET Driver

Features

- Drives N-channel High-Side and Low-Side MOSFETs in a synchronous buck configuration
- 12V High-Side and 12V Low-Side Drive
- Internal Adaptive "Shoot-Through" Protection
- Integrated Bootstrap Diode for High-Side Drive
- Fast rise and fall times
- Switching Frequency Up to 500kHz
- $\overline{OD}$ input for Output Disable – allows for synchronization with PWM controller
- SOIC-8 Package
- Available in low thermal resistance MLP package

Applications

- Multi-phase VRM/VRD regulators for Microprocessor Power
- High Current/High Frequency DC/DC Converters
- High Power Modular Supplies

General Description

The FAN5009 is a dual, high frequency MOSFET driver, specifically designed to drive N-Channel power MOSFETs in a synchronous-rectified buck converter. These drivers, combined with a Fairchild Multi-Phase PWM controller and power MOSFETs, form a complete core voltage regulator solution for advanced microprocessors.

The FAN5009 drives the upper and lower MOSFET gates of a synchronous buck regulator to $12V_{GS}$. The upper gate drive includes an integrated boot diode and requires only an external bootstrap capacitor (C_{BOOT}). The output drivers in the FAN5009 have the capacity to efficiently switch power MOSFETs at frequencies up to 500kHz. The circuit's adaptive shoot-through protection prevents the MOSFETs from conducting simultaneously.

The FAN5009 is rated for operation from 0°C to +85°C and is available in low profile SOIC-8 or MLP packages.

Typical Application

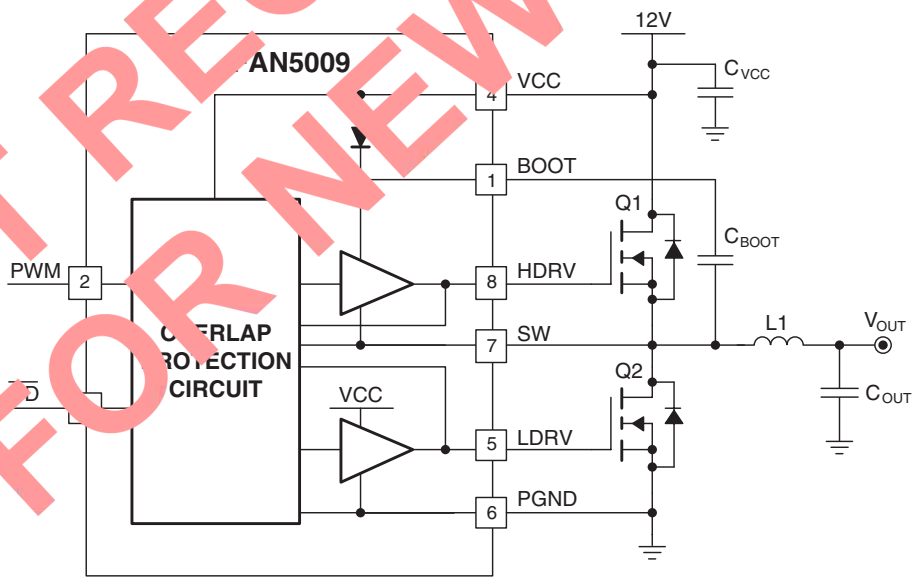
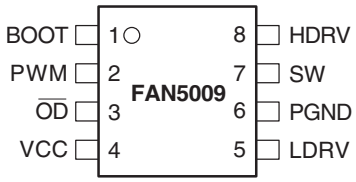
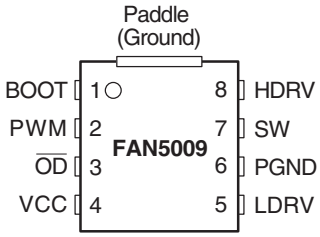


Figure 1. Typical Application.

Pin Configuration



FAN5009M 8-pin SO-8 package

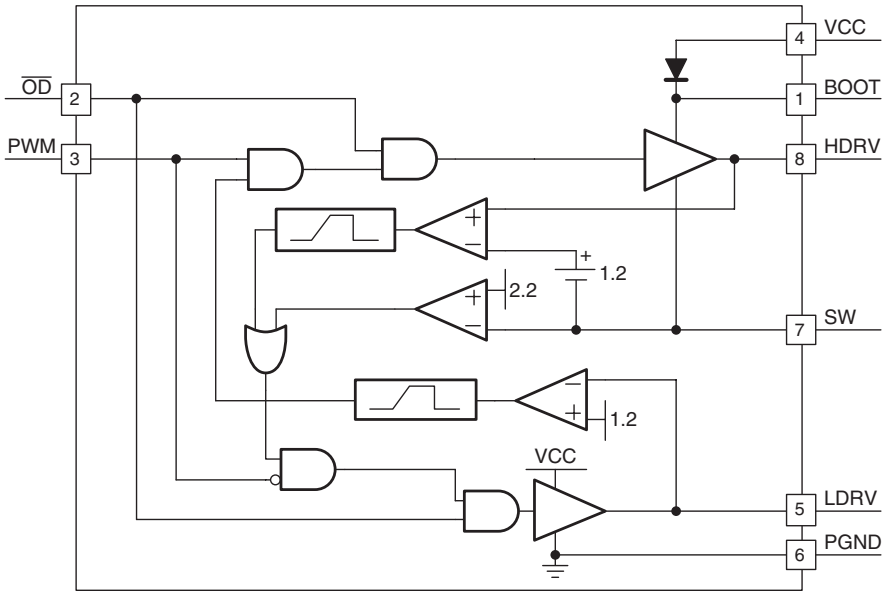


FAN5009MP 8-pin MLP package
(Paddle should be connected to ground or left floating)

Pin Definitions

Pin #	Pin Name	Pin Function Description
1	BOOT	**Bootstrap Supply Input.** Provides voltage supply to high-side MOSFET driver. Connect to bootstrap capacitor. See Applications Section.
2	PWM	**PWM Signal Input.** This pin accepts a logic-level PWM signal from the controller.
3	$\overline{OD}$	**Output Disable.** When low, this pin disables FET switching (HDRV and LDRV are held low).
4	VCC	**Power Input**. +12V chip bias power. Bypass with a 1µF ceramic capacitor.
5	LDRV	**Low Side Gate Drive Output.** Connect to the gate of low-side power MOSFET(s).
6	PGND	**Power ground.** Connect directly to source of low-side MOSFET(s).
7	SW	**Switch Node Input**. Connect as shown in Figure 1. SW provides return for high-side bootstrapped driver and acts as a sense point for the adaptive shoot-thru protection.
8	HDRV	**High Side Gate Drive Output** – Connect to the gate of high-side power MOSFET(s).

Functional Block Diagram



Absolute Maximum Ratings

Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually, not in combination. Unless otherwise specified, voltages are referenced to PGND.

Parameter		Min.	Max.	Units
VCC to PGND		–0.3	15	V
PWM and $\overline{OD}$ pins		–0.3	5.5	V
SW to PGND	Continuous	–1	15	V
	Transient (t=100nsec, F≤500kHz)	–5(1)	25	V
BOOT to SW		–0.3	15	V
BOOT to PGND	Continuous	–0.3	30	V
	Transient (t=100nsec, F≤500kHz)		33(1)	V
HDRV		V_{SW}–1	V_{BOOT}+0.3	V
LDRV	Continuous	–0.5	V_{CC}+0.3	V
	Transient (t=200nsec)	–2(1)		V

Notes:

1. For transient derating beyond the levels indicated, refer to the graphs on page 7.

Thermal Information

Parameter	Min.	Typ.	Max.	Units
Junction Temperature (T_J)	0		150	°C
Storage Temperature	–65		150	°C
Lead Soldering Temperature, 10 seconds			300	°C
Vapor Phase, 60 seconds			215	°C
Infrared, 15 seconds			220	°C
Power Dissipation (P_D) T_A = 25°C			715	mW
Thermal Resistance, SO8 – Junction to Case θ_{JC}		40		°C/W
Thermal Resistance, SO8 – Junction to Ambient θ_{JA}		140		°C/W
Thermal Resistance, MLP – Junction to Paddle θ_{JC}		4		°C/W

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCC	VCC to PGND	10	12	13.5	V
Ambient Temperature (T_A)		0		85	°C
Junction Temperature (T_J)		0		125	°C

Electrical Specifications

V_{CC} = 12V, and T_A = 25°C using circuit in Figure 2 unless otherwise noted. The • denotes specifications which apply over the full operating temperature range.

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Input Supply							
VCC Voltage Range	V_{CC}		•	6.4	12	13.5	V
VCC Current	I_{CC}	$\overline{OD}$ = 0V	•		3.5	8	mA
Bootstrap Diode							
Continuous Forward Current	$I_{F(AVG)}$		•			25	mA
Reverse Breakdown Voltage	V_R		•	15			V
Reverse Recovery Time[2]	t_{RR}				10		ns
Forward Voltage[2]	V_F	I_F = 10mA			0.8	0.95	V
$\overline{OD}$ Input							
Input High Voltage	$V_{IH\ (\overline{OD})}$		•	2.5			V
Input Low Voltage	$V_{IL\ (\overline{OD})}$		•			0.8	V
Input Current	$I_{\overline{OD}}$	$\overline{OD}$ = 3.0V	•	–300		+300	nA
Propagation Delay[2]	$t_{pdl(\overline{OD})}$	See Figure 3			30	40	ns
	$t_{pdh(\overline{OD})}$				30	45	ns
PWM Input							
Input High Voltage	$V_{IH(PWM)}$		•	3.5			V
Input Low Voltage	$V_{IL(PWM)}$		•			0.8	V
Input Current	$I_{IL(PWM)}$		•	-1		+1	µA
High-Side Driver							
Output Resistance, Sourcing Current	R_{HUP}	V_{BOOT}–V_{SW} = 12V			3.8	4.4	Ω
Output Resistance, Sinking Current	R_{HDN}	V_{BOOT}–V_{SW} = 12V			1.4	1.8	Ω
Transition Times[2,4]	$t_{R(HDRV)}$	See Figure 2			40	55	ns
	$t_{F(HDRV)}$				20	30	ns
Propagation Delay[2,3]	$t_{pdh(HDRV)}$	See Figure 2, and 4			50	65	ns
	$t_{pdl(HDRV)}$				25	40	ns

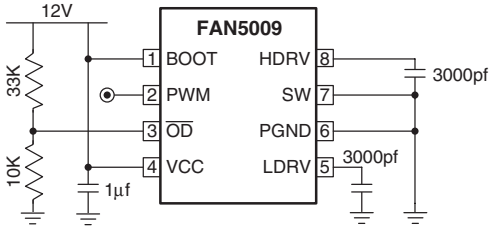


Figure 2. Test Circuit