



# FAN21SV06 — TinyBuck™

## 6A, 24V Single-Input Integrated Synchronous Buck Regulator with Synchronization Capability

### Features

- Single-Supply Operation with 6A Output Current
- Over 94% Efficiency
- Fully Synchronous Operation with Integrated Schottky Diode on Low-Side MOSFET Boosts Efficiency
- Single Supply Device for  $V_{IN} > 6.5V - 24V$
- Programmable Frequency Operation (200-600KHz)
- Externally Synchronizable Clock with Master/Slave Provisions
- Wide Input Range with Dual Supply: 3.0V to 24V
- Output Voltage Range: 0.8V to 80% $V_{IN}$
- Power-Good Signal
- Accepts Ceramic Capacitors on Output
- External Compensation for Flexible Design
- Starts Up on Pre-Bias Outputs
- Integrated Bootstrap Diode
- Programmable Over-Current Protection
- Under-Voltage, Over-Voltage, and Thermal-Shutdown Protections
- 5x6mm, 25-pin, 3-pad MLP

### Applications

- Servers & Telecom
- Graphics Cards & Displays
- High-End Computing Systems
- Set-Top Boxes & Game Consoles
- Point-of-Load Regulation

### Description

The FAN210SV06 TinyBuck™ is a highly efficient, small-footprint, programmable-frequency, 6A integrated synchronous buck regulator.

FAN21SV06 contains both synchronous MOSFETs and a controller/driver with optimized interconnects in one package, which enables designers to solve high-current requirements in a small area with minimal external components, thereby saving cost. On-board internal 5V regulator enables single-supply operation for input voltages  $>6.5V$ .

The FAN21SV06 can be configured to drive multiple slave devices OR synchronize to an external system clock. In slave mode, FAN21SV06 may be set up to be free-running in the absence of a master clock signal.

External compensation, programmable switching frequency, and current-limit features allow for design optimization and flexibility. High-frequency operation allows for all ceramic solutions.

Fairchild's advanced BiCMOS power process combined with low- $R_{DS(ON)}$  internal MOSFETs and a thermally efficient MLP package provide the ability to dissipate high power in a small package. Integration helps to minimize critical inductances making layout simpler and more efficient compared to discrete solutions.

Output over-voltage, under-voltage, over-current and thermal-shutdown protections help protect the device from damage during fault conditions. FAN21SV06 prevents pre-biased output discharge during startup in point-of-load applications.

### Related Resources

- [TinyCalc™ Calculator Design Tool](#)
- [AN-6033 — FAN21SV06 Design Guide](#)
- [AN-8022 — TinyCalc™ Calculator](#)

### Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN21SV06MPX	-10°C to 85°C	Molded Leadless Package (MLP) 5x6mm	Tape and Reel
FAN21SV06EMPX	-40°C to 85°C	Molded Leadless Package (MLP) 5x6mm	Tape and Reel

## Typical Application Diagram

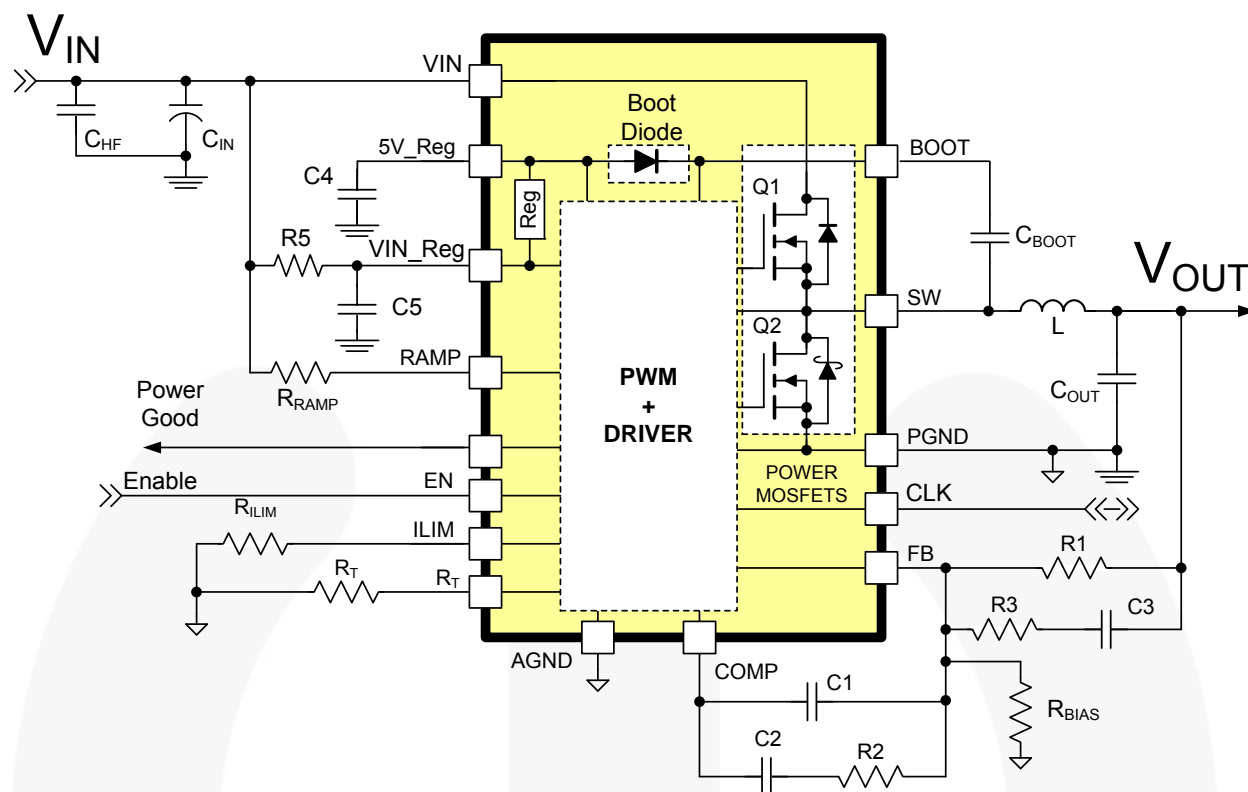


Figure 1. Typical Application, Master,  $V_{IN}=6.5V$  to 24V

## Block Diagram

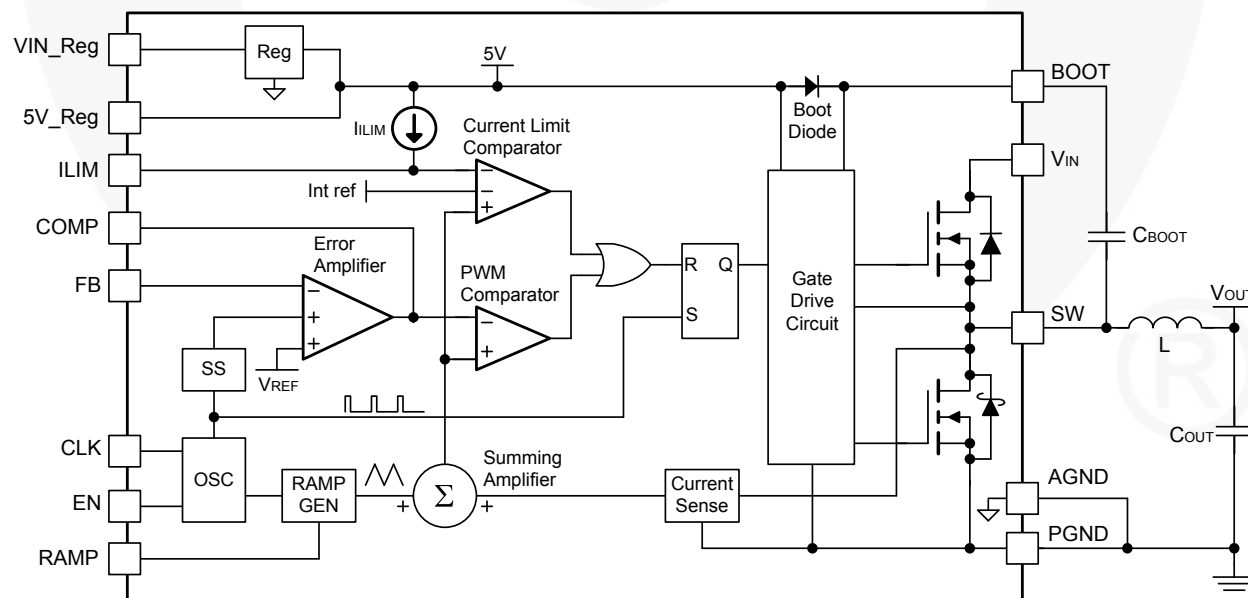


Figure 2. Block Diagram

## Pin Configuration

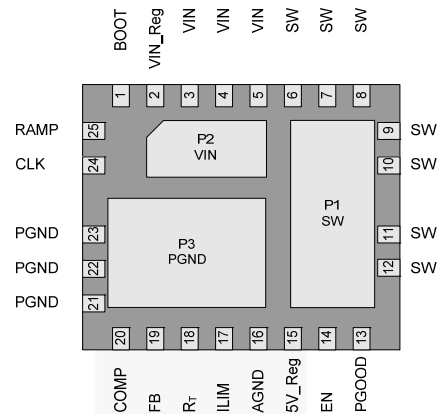


Figure 3. MLP 5x6mm Pin Configuration (Bottom View)

## Pad / Pin Definitions

Pad / Pin	Name	Description
P1, 6-12	SW	<b>Switching Node.</b> Junction of high-side and low-side MOSFETs.
P2, 3-5	VIN	<b>Power Input Voltage.</b> Supply voltage for the converter.
P3, 21-23	PGND	<b>Power Ground.</b> Power return and Q2 source.
1	BOOT	<b>High-Side Drive BOOT Voltage.</b> Connect through capacitor ( $C_{BOOT}$ ) to SW. The IC has an internal synchronous bootstrap diode to recharge the capacitor on this pin to 5V.
2	VIN_Reg	<b>Regulator Input Voltage.</b> Input voltage to the internal regulator. Connect to input voltage >6.5V with 1 $\mu$ F bypass capacitor at the pin.
13	PGOOD	<b>Power-Good.</b> An open-drain output that pulls LOW when the voltage on the FB pin is outside the limits specified in the electrical specs. PGOOD does not assert HIGH until the fault latch is enabled.
14	EN	<b>ENABLE.</b> Enables operation when pulled to logic HIGH or left open. Toggling EN resets the regulator after a latched-fault condition. This input has an internal pull-up. When a latched fault occurs, EN is discharged by a current sink.
15	5V_Reg	<b>5V Regulator Output.</b> Internal regulator output that provides power for the IC's logic and analog circuitry. This pin should be connected to AGND through a >2.2 $\mu$ F X5R/X7R capacitor.
16	AGND	<b>Analog Ground.</b> The signal ground for the IC. All internal control voltages are referred to this pin. Tie this pin to the ground island/plane through the lowest impedance connection.
17	ILIM	<b>Current Limit.</b> A resistor ( $R_{ILIM}$ ) from this pin to AGND can be used to program the current-limit trip threshold lower than the internal default setting.
18	$R_T$	<b>Oscillator Frequency and Master/Slave Set.</b> Connecting a resistor ( $R_T$ ) to AGND sets the oscillator frequency and configures the CLK pin as an output (master). Tying this pin to 5V_Reg through a resistor configures the CLK signal as an input (slave) and establishes the free-running oscillator frequency.
19	FB	<b>Output Voltage Feedback.</b> Connect through a resistor divider to the output voltage.
20	COMP	<b>Compensation.</b> Error amplifier output. Connect the external compensation network between this pin and FB.
24	CLK	<b>Clock.</b> Bi-directional signal pin, depending on master/slave configuration. When configured as a master, this pin represents the clock output that connects directly to the slave(s) for synchronizing with 180° phase shift.
25	RAMP	<b>Ramp Amplitude.</b> A resistor ( $R_{RAMP}$ ) connected from this pin to VIN sets the internal ramp amplitude and also provides voltage feedforward functionality.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter	Conditions	Min.	Max.	Units
V <sub>IN</sub> , V <sub>IN_Reg</sub> to AGND	AGND=PGND		28	V
5V_Reg to AGND	AGND=PGND		6	V
BOOT to PGND			35	V
BOOT to SW		-0.5	6.0	V
SW to PGND	Continuous	-0.5	24.0	V
	Transient (t < 20ns, f ≤ 600KHz)	-5	30	V
All other pins		-0.3	6.0	V
ESD	Human Body Model, JESD22-A114	1.5		kV
	Charged Device Model, JESD22-C101	2.5		

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
f <sub>SW</sub>	Switching Frequency		200	500	600	KHz
V <sub>IN</sub> , V <sub>IN_Reg</sub>	Supply Voltage for Power and Bias	V <sub>IN</sub> to PGND	3.0		24.0	V
		V <sub>IN_Reg</sub> to AGND	6.5		24.0	V
T <sub>A</sub>	Ambient Temperature	FAN21SV06MX	-10		+85	°C
		FAN21SV06EMX	-40		+85	°C
T <sub>J</sub>	Junction Temperature				+125	°C

## Thermal Information

Symbol	Parameter		Min.	Typ.	Max.	Units
T <sub>STG</sub>	Storage Temperature		-65		+150	°C
T <sub>L</sub>	Lead Soldering Temperature, 30sec				+300	°C
θ <sub>JC</sub>	Thermal Resistance: Junction-to-Case	P1 (Q2)		4		°C/W
		P2 (Q1)		7		°C/W
		P3		4		°C/W
θ <sub>J-PCB</sub>	Thermal Resistance: Junction-to-Mounting Surface <sup>(1)</sup>			35 <sup>(1)</sup>		°C/W
P <sub>D</sub>	Total Power Dissipation in the package, T <sub>A</sub> =25°C <sup>(1)</sup>				2.8	W

### Note:

1. Typical thermal resistance when mounted on a four-layer, two-ounce PCB, as shown in Figure 37. Actual results are dependent upon mounting method and surface related to the design.

## Electrical Characteristics

Recommended operating conditions, using the circuit in Figure 1, with  $V_{IN}$ ,  $V_{IN\_Reg}=12V$ , unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supplies					
Operating Current (VIN+VIN_Reg)	V <sub>IN</sub> =12V, 5V_Reg open, CLK open, f <sub>SW</sub> =500KHz, No Load		22	30	mA
VIN_Reg Operating Current	EN=High, 5V_Reg open, CLK open, f <sub>SW</sub> =500KHz		11		mA
VIN_Reg Quiescent Current	EN=High, FB=0.9V		4	5	mA
VIN_Reg Standby Current	EN=0, V <sub>IN</sub> =12V			1	mA
5V_Reg Output Voltage	Internal V <sub>CC</sub> Regulator, No Load (6.5V <VIN_Reg<24V)	4.7	5.0	5.3	V
5V_Reg Max Current Load	VIN_Reg=12V)			5	mA
VIN_Reg UVLO Threshold	Rising V <sub>IN</sub> , V <sub>IN</sub> =VIN_Reg		5.6	6.3	V
	Falling V <sub>IN</sub> , V <sub>IN</sub> =VIN_Reg			5	V
Reference					
Reference Voltage measured at FB (See Figure 4 for Temperature Coefficient)	FAN21SV06M, 25°C	794	800	806	mV
	FAN21SV06EM, 25°C	795	800	805	mV
Oscillator					
Frequency	R <sub>T</sub> =50kΩ to GND (Master Mode)	255	300	345	KHz
	R <sub>T</sub> =24kΩ to GND (Master Mode)	540	600	660	KHz
Frequency in Slave Mode compared to Master Mode	R <sub>T</sub> =24 kΩ to 50kΩ to 5V_Reg (Slave Mode)	-15		+15	%
Minimum On-Time <sup>(2)</sup>			40	65	ns
Duty Cycle	V <sub>IN</sub> =6.5V, f <sub>SW</sub> =600KHz		80	85	%
Ramp Amplitude, Peak-to-Peak <sup>(2)</sup>	16V <sub>IN</sub> , 1.8V <sub>OUT</sub> , R <sub>T</sub> =30kΩ, R <sub>RAMP</sub> =200kΩ		0.5		V
Minimum Off-Time <sup>(2)</sup>			100	150	ns
Synchronization					
CLK Output Pulse Width	Master (R <sub>T</sub> to GND)	70	85	100	ns
CLK Output Sink Current	Master, V <sub>CLK</sub> =0.4V	0.25		0.35	mA
CLK Output Source Current	Master, V <sub>CLK</sub> =2V	-2.5		-2.0	mA
CLK Input Pulse Width	Slave: V <sub>CLK</sub> ≥ 2V	50			ns
CLK Input Source Current	Slave: V <sub>CLK</sub> =1V	-230	-200	-170	μA
CLK Input Threshold, Rising	Slave	1.73	1.83	1.93	V
Soft-Start					
V <sub>OUT</sub> to Regulation (T <sub>0.8</sub> )	Frequency=500KHz		2.5		ms
Fault Enable/SSOK (T <sub>1.0</sub> )			3.1		ms
Error Amplifier					
DC Gain <sup>(2)</sup>	VIN_Reg > 6.5V	80	85		dB
Gain Bandwidth Product <sup>(2)</sup>		12	15		MHz
Output Voltage Swing (V <sub>COMP</sub> )		0.4		4.0	V
Output Current, Sourcing	5V_Reg=5V, V <sub>COMP</sub> =2.2V	1.5	2.2	2.5	mA
Output Current, Sinking	5V_Reg=5V, V <sub>COMP</sub> =1.2V	0.8	1.2	1.5	mA
FB Bias Current	V <sub>FB</sub> =0.8V, 25°C	-850	-650	-450	nA

### Note:

2. Specifications guaranteed by design and characterization; not production tested.

**Electrical Characteristics** (Continued)

Recommended operating conditions using the circuit in Figure 1 with  $V_{IN}$ ,  $V_{IN\_Reg}=12V$ , unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
<b>Control Functions</b>					
EN Threshold, Rising			1.35	2.00	V
EN Hysteresis			250		mV
EN Pull-Up Current	$V_{IN\_Reg} > 6.5V$	-8	-6	-4	$\mu A$
EN Discharge Current	Auto-Restart Mode, $V_{IN\_Reg} > 6.5V$		1		$\mu A$
FB OK Drive Resistance			800	1000	$K\Omega$
PGOOD LOW Threshold	$FB < V_{REF}$ , 2 Consecutive Clock Cycles <sup>(3)</sup>	-14.5	-11.0	-8.0	$\%V_{REF}$
	$FB > V_{REF}$ , 2 Consecutive Clock Cycles <sup>(3)</sup>	+6.5	+10.0	+13.5	$\%V_{REF}$
PGOOD Low Voltage	$I_{OUT} \leq 2mA$			0.4	V
PGOOD Leakage Current	$V_{PGOOD}=5V$		0.2	1.0	$\mu A$
<b>Protection and Shutdown</b>					
Current Limit	$R_{ILIM}$ open, $f_{sw}=500KHz$ , $V_{OUT}=1.8V$ , $R_{ramp}=200k\Omega$ , 16 Consecutive Clock Cycles <sup>(3)</sup>	7	9	11	A
$I_{LIM}$ Current	$V_{IN\_Reg} > 6.5V$ , $25^{\circ}C$	-11	-10	-9	$\mu A$
Over-Temperature Shutdown	Internal Temperature		155		$^{\circ}C$
Over-Temperature Hysteresis			30		$^{\circ}C$
Over-Voltage Threshold	2 Consecutive Clock Cycles <sup>(3)</sup>	110	115	120	$\%V_{OUT}$
Under-Voltage Shutdown	16 Consecutive Clock Cycles <sup>(3)</sup>	68	73	78	$\%V_{OUT}$
Fault-Discharge Threshold	Measured at FB pin		250		mV
Fault-Discharge Hysteresis	Measured at FB pin ( $V_{FB} \sim 500mV$ )		250		mV

**Note:**

3. Delay times are not tested in production. Guaranteed by design.

## Typical Characteristics

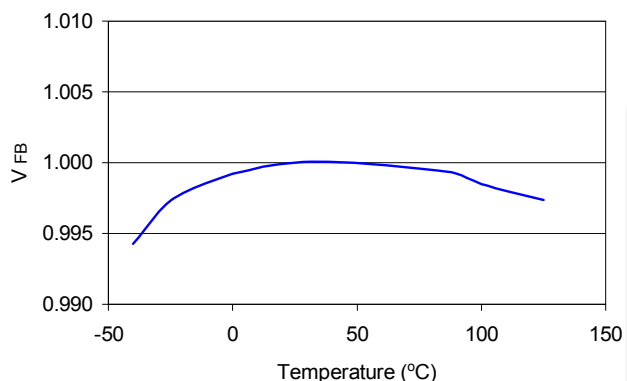


Figure 4. Reference Voltage ( $V_{FB}$ ) vs. Temperature, Normalized

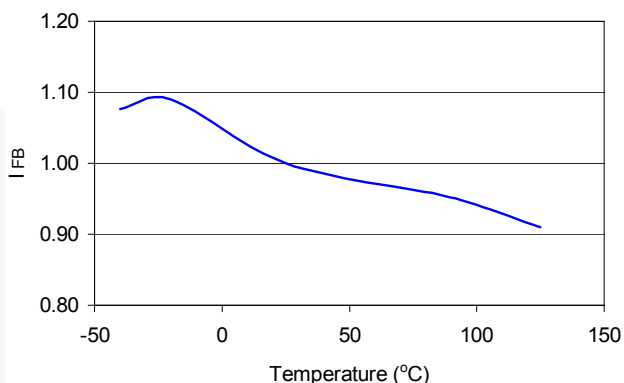


Figure 5. Reference Bias Current ( $I_{FB}$ ) vs. Temperature, Normalized

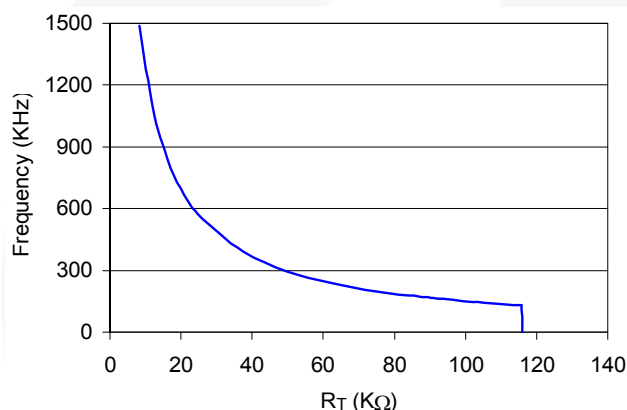


Figure 6. Frequency vs.  $R_T$  (Master)

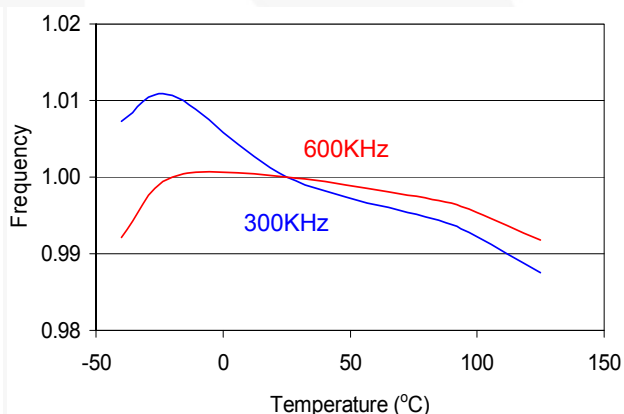


Figure 7. Frequency vs. Temperature, Normalized

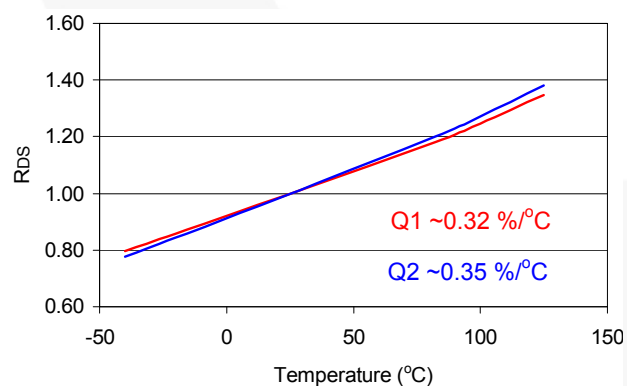


Figure 8.  $R_{DS}$  vs. Temperature, Normalized ( $5V_{Reg}=V_{GS}=5V$ )

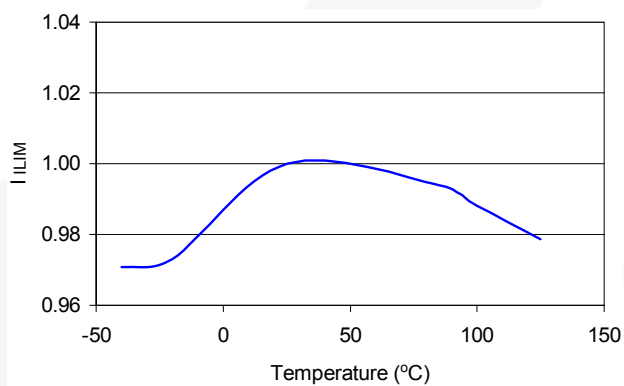
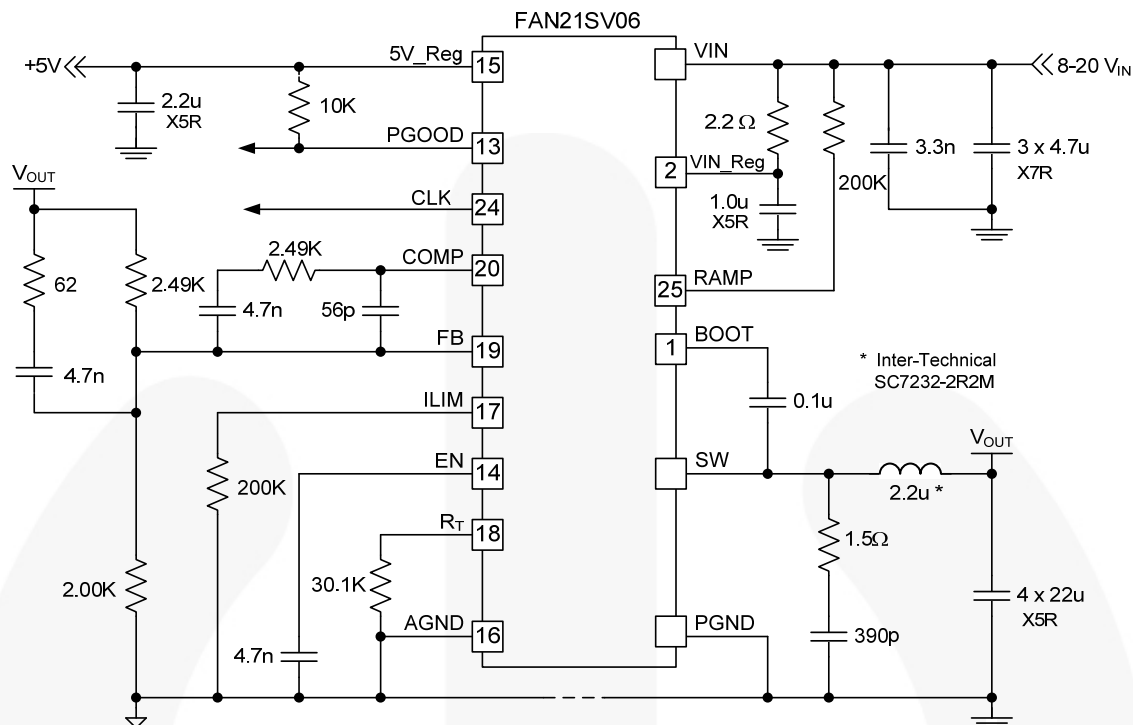
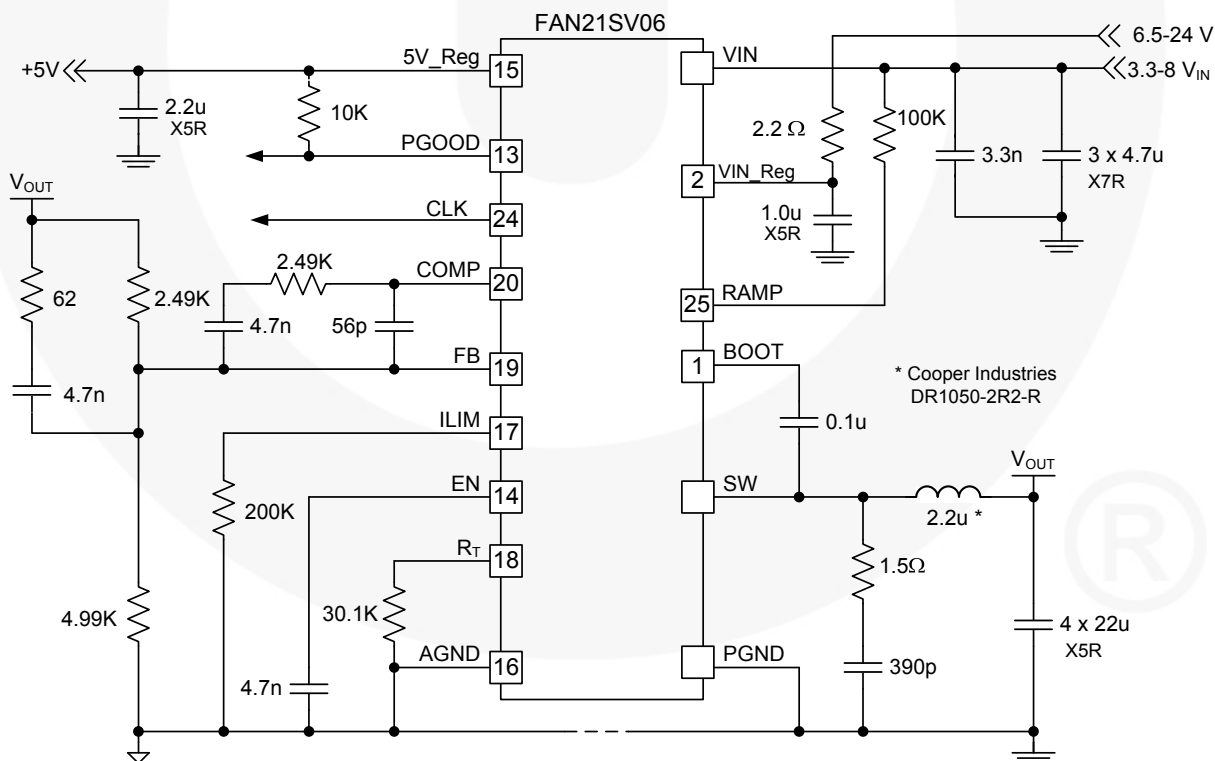


Figure 9.  $I_{LIM}$  Current ( $I_{LIM}$ ) vs. Temperature, Normalized

## Application Circuit

Figure 10. Single-Supply Application Circuit: 1.8V<sub>OUT</sub>, 500KHz, MasterFigure 11. Dual-Supply Application Circuit : 1.2V<sub>OUT</sub>, 600KHz, Master 3.3V – 8V Input



## Typical Performance Characteristics

Typical operating characteristics using the circuit shown in Figure 10, unless otherwise specified.

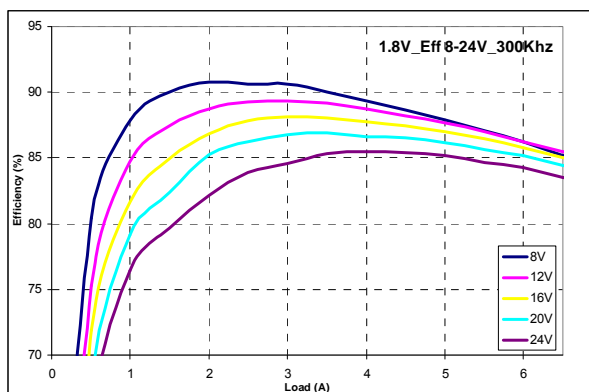


Figure 12. 1.8 V<sub>OUT</sub> Efficiency Over V<sub>IN</sub> vs. Load

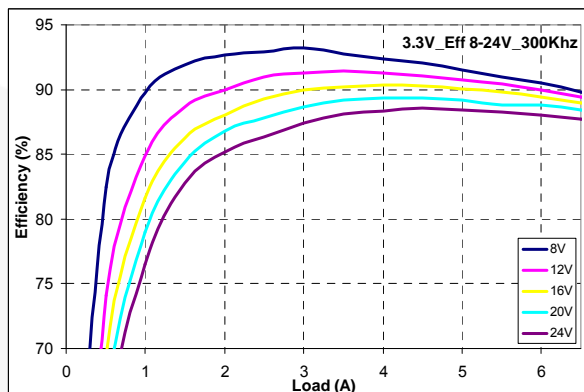


Figure 13. 3.3 V<sub>OUT</sub> Efficiency vs. Load  
(Circuit Value Changes)

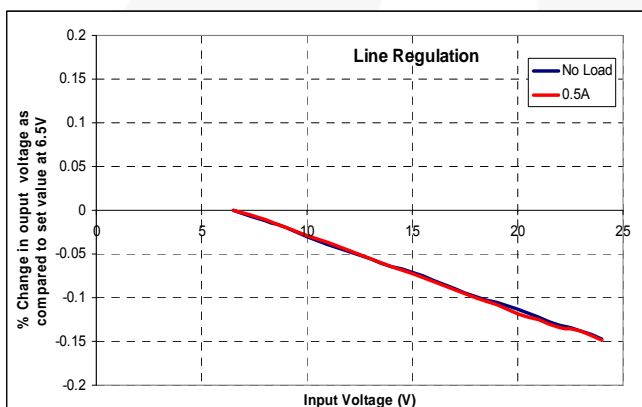


Figure 14. 1.8 V<sub>OUT</sub> Line Regulation

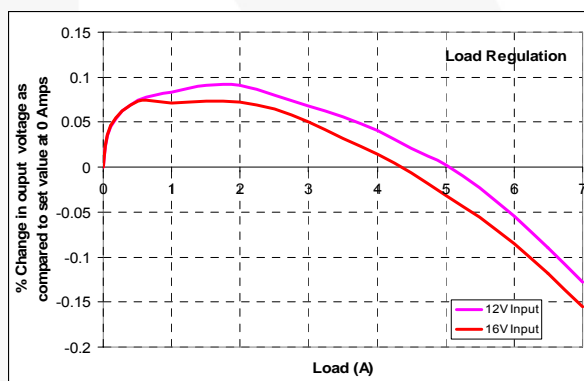


Figure 15. 1.8 V<sub>OUT</sub> Load Regulation

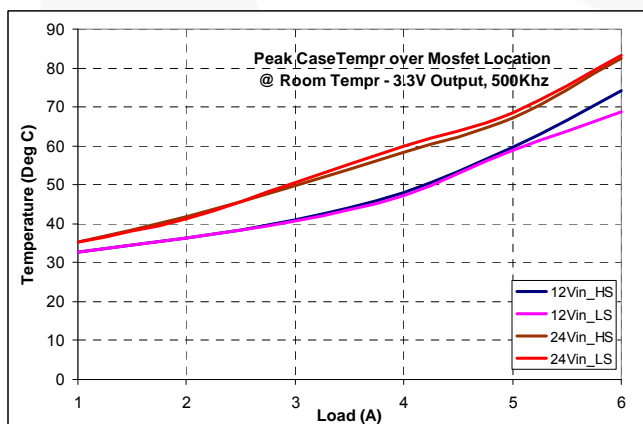


Figure 16. Peak Case Temp over MOSFET Locations  
3.3V Output, 12V and 24V Input (500KHz)

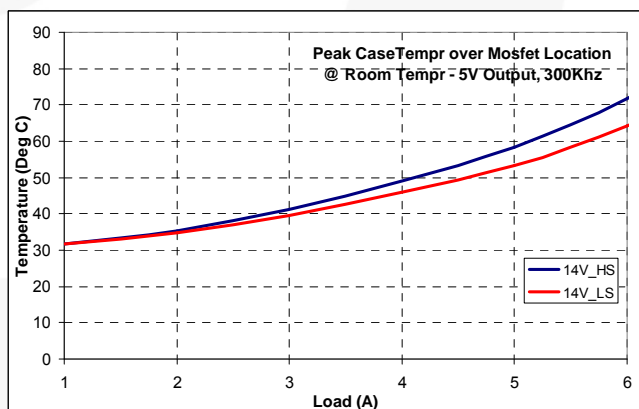


Figure 17. Peak Case Temp. Over MOSFET Locations  
5V Output (300KHz)

## Typical Performance Characteristics (Continued)

Typical operating characteristics using the circuit shown in Figure 10.  $V_{IN}=12V$ , unless otherwise specified.

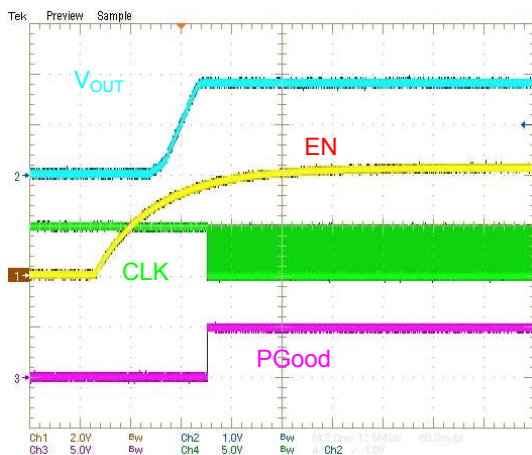


Figure 18. CLK and  $V_{OUT}$  at Startup

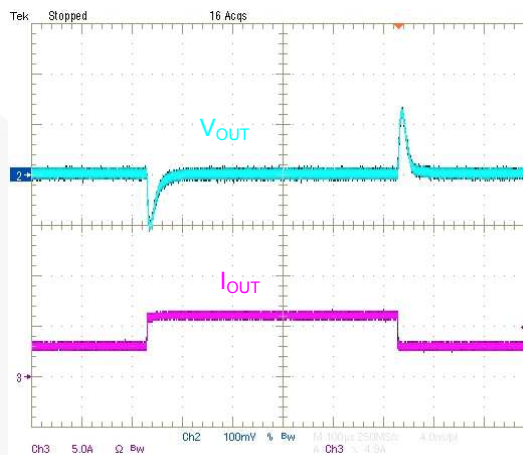


Figure 19. Transient Response, 3-6A Load

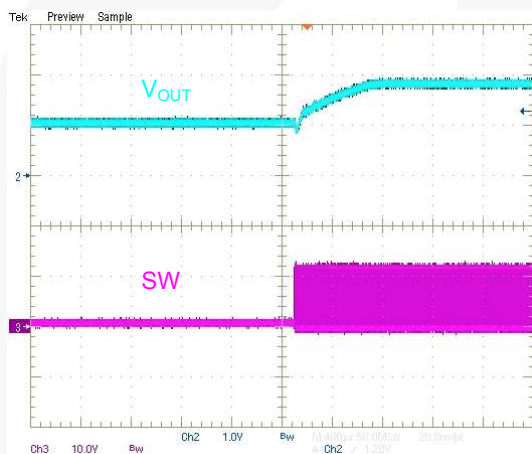


Figure 20. Startup on Pre-Bias

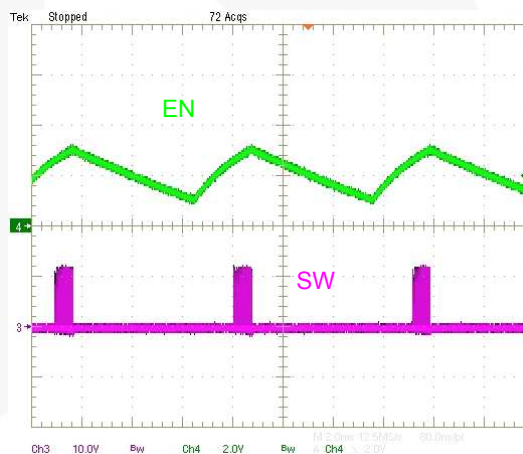


Figure 21. Restart on Fault

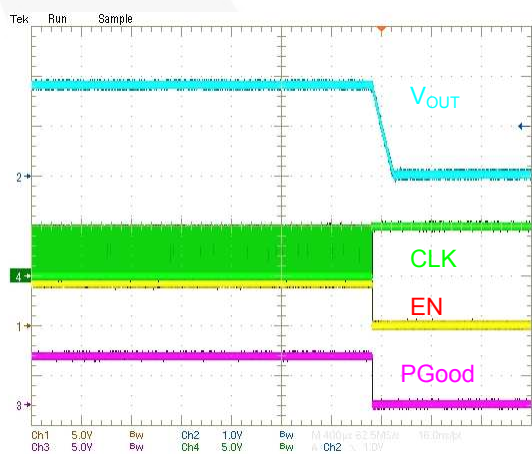


Figure 22. Shutdown, 1A Load

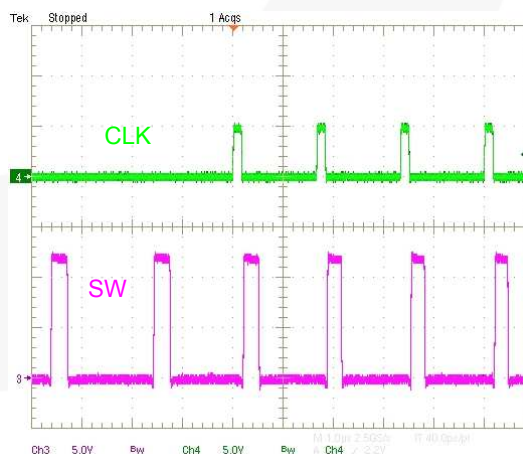


Figure 23. Slave (500KHz Free-Run to 600KHz Synchronization)

## Typical Performance Characteristics (Continued)

Typical operating characteristics using the circuit shown in Figure 10, unless otherwise specified.

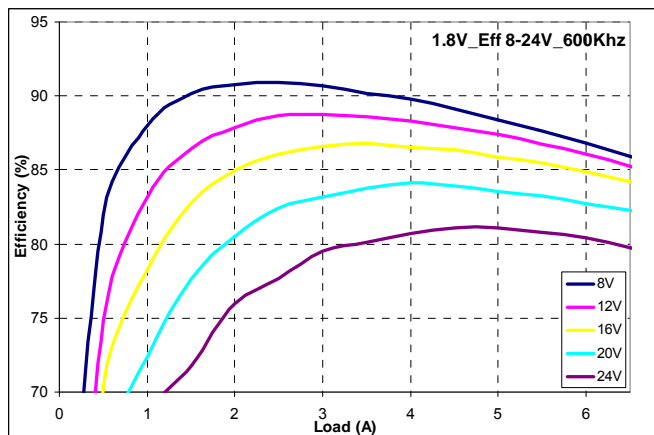


Figure 24. 1.8 V<sub>OUT</sub> Efficiency 600KHz

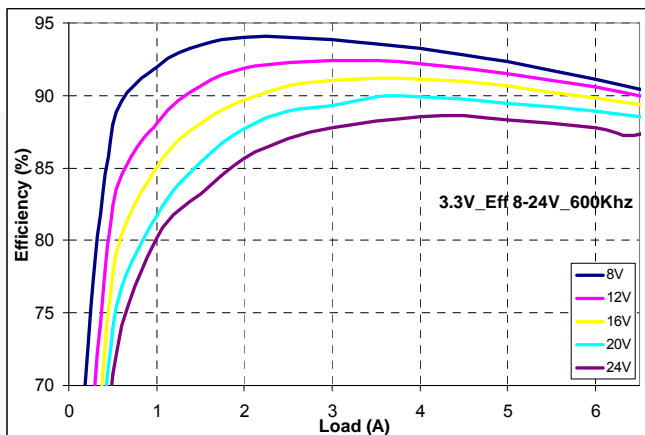


Figure 25. 3.3 V<sub>OUT</sub> Efficiency 600KHz

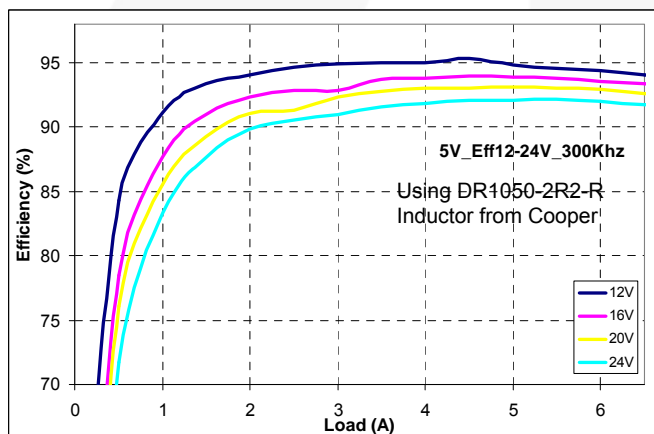


Figure 26. 5 V<sub>OUT</sub> Efficiency 300KHz  
(Circuit Values Change)

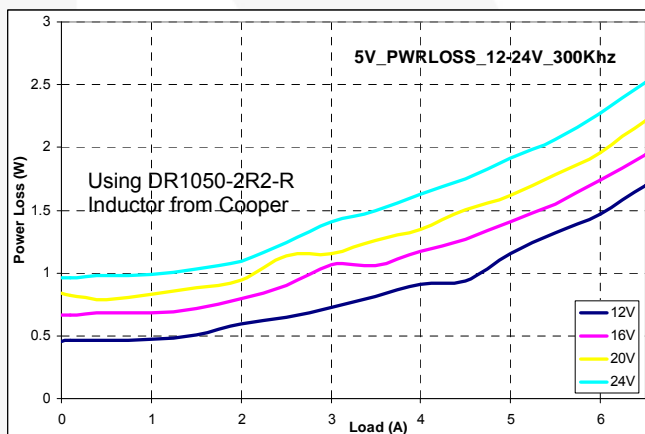


Figure 27. Device Power Loss (5 V<sub>OUT</sub>, 300KHz)  
(Circuit Values Change)

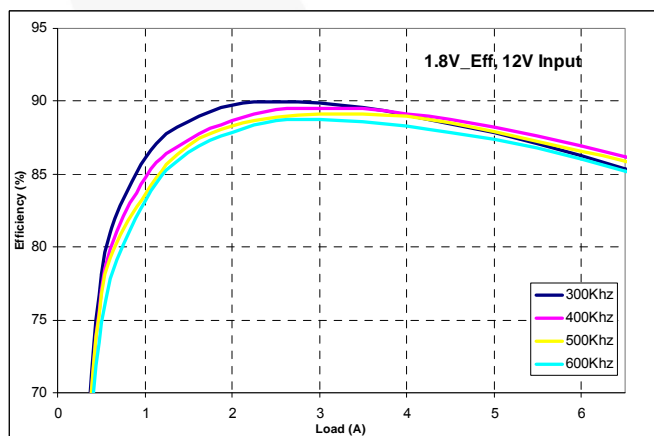


Figure 28. 1.8 V<sub>OUT</sub> Efficiency Over  $f_{SW}$   
(Circuit Values Change)

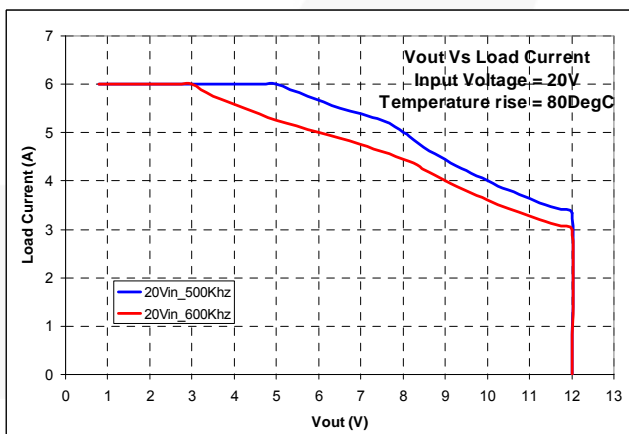


Figure 29. Typical Output Operating Area Based on  
Thermal Limitations (Circuit Values Change)

## Circuit Operation

### PWM Generation

Refer to Figure 2 for the PWM control mechanism. FAN21SV06 uses the summing-mode method of control to generate the PWM pulses. An amplified current-sense signal is summed with an internally generated ramp and the combined signal is compared with the output of the error amplifier to generate the pulse width to drive the high-side MOSFET. Sensed current from the previous cycle is used to modulate the output of the summing block. The output of the summing block is also compared against a voltage threshold set by the  $R_{LIM}$  resistor to limit the inductor current on a cycle-by-cycle basis. The controller facilitates external compensation for enhanced flexibility.

### Initialization

Once  $V_{IN\_Reg}$  voltage exceeds the UVLO threshold and EN is HIGH, the IC checks for an open or shorted FB pin before releasing the internal soft-start ramp (SS).

If R1 is open (Figure 1), error amplifier output (COMP) is forced LOW and no pulses are generated. After the SS ramp times out (T1.0), an under-voltage fault occurs.

If the parallel combination of R1 and  $R_{BIAS}$  is  $\leq 1k\Omega$ , the internal SS ramp is not released and the regulator does not start.

### Internal Regulator

FAN21SV06 facilitates single-supply operation for input voltages  $>6.5V$ . At startup, the output of the internal regulator tracks the input voltage and comes into regulation (5V) when  $V_{IN\_Reg}$  exceeds the UVLO threshold. The EN pin is released at the same time. The output voltage of the internal regulator (5V\_Reg) is set to 5V. The internal regulator supplies power to all the control circuits including the drivers.

For applications with  $V_{IN} < 6.5V$ , FAN21SV06 can be used if  $V_{IN\_Reg}$  is provided with a separate low-power source  $>6.5V$ .  $V_{IN\_Reg}$  supply should come up after  $V_{IN}$  during dual-supply operation. The  $V_{IN\_Reg}$  pin should always be decoupled with at least  $1\mu F$  ceramic capacitor (see Figure 11).

Since  $V_{CC}$  is used to drive the internal MOSFET gates, high peak currents are present on the 5V\_Reg pin. Connect a  $\geq 2.2\mu F$  X5R or X7R decoupling capacitor between the 5V\_Reg pin and PGND.

In addition to supplying power for the control circuits internally, 5V\_Reg output can be used as a reference voltage for other applications requiring low noise reference voltage. 5V\_Reg is capable of sourcing up to 5mA of output current.

When EN is pulled LOW externally, 5V\_Reg output is still present but the IC is in standby mode with no switching.

### Soft-Start

FAN21SV06 uses an internal digital soft-start circuit to slowly ramp up the output voltage and limit inrush current during startup. When 5V\_Reg is in regulation and EN is high, the circuit releases SS and enables the PWM regulator. Soft-start time is a function of switching frequency (number of clock cycles).

Once internal SS ramp has charged to 0.8V (T0.8), the output voltage is in regulation. Until SS ramp reaches 1.0V (T1.0), only over-current-protection circuit is active during soft-start and all other output protections are inhibited.

In dual-supply operation mode, it is necessary to apply  $V_{IN}$  before  $V_{IN\_Reg}$  reaches its UVLO threshold to avoid skipping the soft-start cycle.

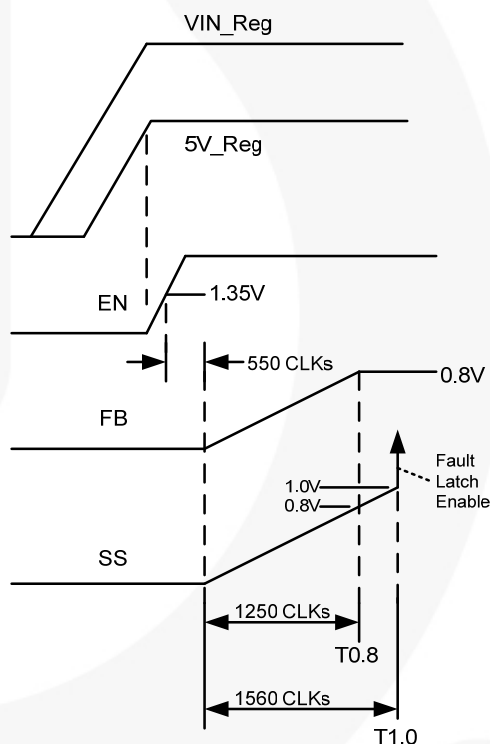


Figure 30. Typical Soft-Start Timing Diagram

$V_{IN\_Reg}$  UVLO or toggling the EN pin discharges the SS and resets the IC.

### Startup on Pre-Bias

The regulator does not allow the low-side MOSFET to operate in full synchronous mode until SS reaches 95% of  $V_{REF}$  ( $\sim 0.76V$ ). This enables the regulator to startup on a pre-biased output and ensures that output is not discharged during the soft-start cycle.

## Protections

The converter output is monitored and protected against extreme overload, short-circuit, over-voltage, and under-voltage conditions.

### Under-Voltage Protection

If FB remains below the under-voltage threshold for 16 consecutive clock cycles, the fault latch is set and the converter shuts down. This fault is prevented from setting the fault latch during soft-start.

### Over-Voltage Protection

If FB exceeds  $115\% \cdot V_{REF}$  for two consecutive clock cycles, the fault latch is set and shutdown occurs.

A shorted high-side MOSFET condition is detected when SW voltage exceeds  $\sim 0.7V$  while the low-side MOSFET is fully enhanced. The fault latch is set immediately upon detection.

These two fault conditions are allowed to set the fault latch at any time, including during soft-start.

### Over-Temperature Protection

The chip incorporates an over-temperature-protection circuit that sets the fault latch when a die temperature of about  $155^{\circ}C$  is reached. The IC is allowed to restart when the die temperature falls below  $125^{\circ}C$ .

### EN / Auto-Restart

After a fault, EN pin is discharged with  $1\mu A$  current pull down to a  $1.1V$  threshold before the internal  $800k\Omega$  pull up is restored. A new soft-start cycle begins when EN charges above  $1.35V$ .

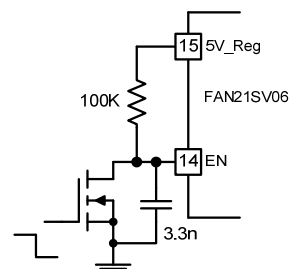
Depending on the external circuit, the FAN21SV06 can be configured to remain latched off or automatically restart after a fault, as listed in Table 1.

**Table 1. Fault / Restart Configurations**

EN pin	Controller / Restart State
Pull to GND	Standby
Connected to 5V_Reg	No restart – latched OFF
Open	Immediate restart after fault
Cap to GND	New soft-start cycle after: EN is HIGH (Auto Restart Mode)

With EN left open, restart is immediate.

If auto-restart is not desired, tie the EN pin high with a logic gate to keep the  $1\mu A$  current sink from discharging EN to  $1.1V$ . Figure 31 shows one method to pull up EN to  $V_{CC}$  for a latch configuration.



**Figure 31. Enable Control with Latch Option**

### Power Good (PGOOD) Signal

PGOOD is an open-drain output that asserts LOW when  $V_{OUT}$  is out of regulation, as measured at the FB pin. The thresholds are specified in the Electrical Specifications section. PGOOD does not assert HIGH until soft start is complete (T1.0).

## Application Information

### Setting the Output Voltage

The output voltage of the regulator can be set from  $0.8V$  to  $\sim 80\%$  of  $V_{IN}$  by an external resistor divider ( $R1$  and  $R_{BIAS}$  in Figure 1). For output voltages  $> 3.3V$ , output current rating may need to be de-rated depending on the ambient temperature, power dissipated in the package and the PCB layout. (Refer to Thermal Information table and Figure 29.)

The internal reference is set to  $0.8V$  with  $650nA$  sourced from the FB pin to ensure that the regulator does not start if the pin is left open.

The external resistor divider is calculated using:

$$\frac{0.8V}{R_{BIAS}} = \frac{V_{OUT} - 0.8V}{R1} + 650nA \quad (1)$$

Connect  $R_{BIAS}$  between FB and AGND.

### Setting the Clock Frequency

Oscillator frequency is determined by a resistor,  $R_T$ , that is connected between the ( $R_T$ )pin and AGND (Master Mode) or 5V\_Reg (Slave Mode):

$$f_{(KHz)} = \frac{10^6}{(65 \cdot R_T) + 135} \quad (2)$$

where  $R_T$  is expressed in  $k\Omega$ .

$$R_{T(K\Omega)} = \frac{(10^6 / f) - 135}{65} \quad (3)$$

where frequency ( $f$ ) is expressed in KHz. In slave mode, the switching frequency is about 10% slower for the same  $R_T$ .

The regulator does not start if  $R_T$  is open in Master mode.

## Calculating the Inductor Value

Typically the inductor value is chosen based on ripple current ( $\Delta I_L$ ) which is chosen between 10 to 35% of the maximum DC load. Regulator designs that require fast transient response use a higher ripple-current setting while regulator designs that require higher efficiency keep ripple current on the low side and operate at a lower switching frequency.

$$\Delta I_L = \frac{V_{OUT} \cdot (1-D)}{L \cdot f} \quad (4)$$

where  $f$  is the oscillator frequency, and

$$L = \frac{V_{OUT} \cdot (1-D)}{\Delta I_L \cdot f} \quad (5)$$

## Setting the Ramp-Resistor Value

As a starting point, set the internal ramp amplitude ( $\Delta V_{RAMP}$ ) to 0.5V.  $R_{RAMP}$  is approximately:

$$R_{RAMP}(K\Omega) = \frac{(V_{IN} - 1.8) \cdot V_{OUT}}{18 \times 10^{-6} \cdot V_{IN} \cdot f} - 2 \quad (6)$$

where frequency ( $f$ ) is expressed in KHz.

Refer to [AN-6033 — FAN21SV06 Design Guide](#) to determine the optimal  $R_{RAMP}$  value.

## Setting the Current Limit

There are two levels of current-limit thresholds in FAN21SV06. The first level of protection is through an internal default limit set at the factory to provide cycle-by-cycle current limit and prevent output current beyond normal usage levels. The second level of protection is a flexible one to be set externally by the user. Current-limit protection is enabled whenever the lower of the two thresholds is reached. The FAN21SV06 uses its internal low-side MOSFET as the current-sensing element. The current-limit threshold voltage ( $V_{ILIM}$ ) is compared to the voltage drop across the low-side MOSFET, sampled at the end of each PWM off-time/cycle. The internal default threshold ( $I_{LIM}$  open) is temperature compensated.

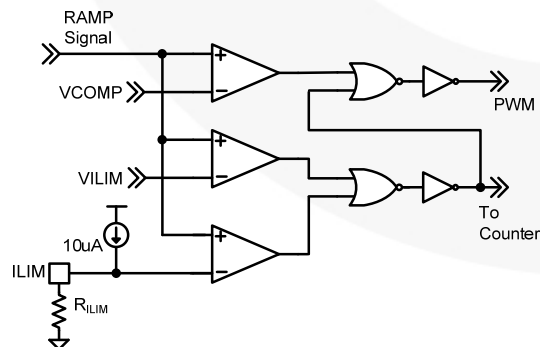


Figure 32. ILIM Network

The 10 $\mu$ A current sourced from the ILIM pin can be used to establish a lower, temperature-dependent, current-limit threshold by connecting an external resistor ( $R_{ILIM}$ ) to AGND:

$$R_{ILIM}(K\Omega) = 95 + 5 \cdot I_{OUT} \cdot K_T \cdot K1 + \frac{V_{OUT} \cdot 3.33 \cdot 10^6}{R_{RAMP} \cdot f_{SW}} \quad (7)$$

where:

$I$ =desired current-limit set point in Amps,  
 $K_T$ =the normalized temperature coefficient of the low-side MOSFET (Q2) from Figure 8.

$K1$ =Overload co-efficient (use 1.2 to 1.4)

$V_{OUT}$ =Set output voltage

$R_{RAMP}$ =Ramp resistor used, in k $\Omega$

$f_{SW}$ =Selected switching frequency, in KHz.

After 16 consecutive pulse-by-pulse current-limit cycles, the fault latch is set and the regulator shuts down. Cycling VIN\_Reg or EN restores operation after a normal soft-start cycle (refer to Auto-Restart section).

The over-current protection fault latch is active during the soft-start cycle. Use a 1% resistor for  $R_{ILIM}$ . For a given  $R_{RAMP}$  and  $R_{ILIM}$  setting, the current-limit point varies slightly in an inverse relationship to  $V_{IN}$ . In case  $R_{ILIM}$  is not connected, the IC uses the internal default current-limit threshold.

## Loop Compensation

The control loop is compensated using a feedback network around the error amplifier. Figure 33 shows a complete Type-3 compensation network. Type-2 compensation eliminates R3 and C3.

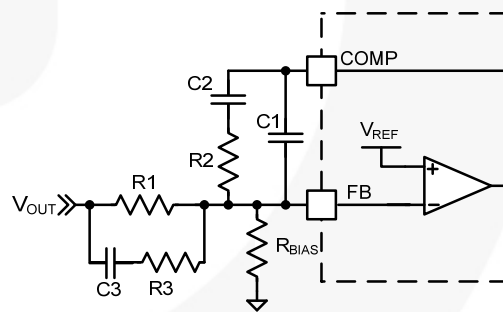


Figure 33. Compensation Network

Since the FAN21SV06 employs summing current-mode architecture, Type-2 compensation can be used for many applications. For applications that require wide loop bandwidth and/or use very low-ESR output capacitors, Type-3 compensation may be required.

$R_{RAMP}$  provides feedforward compensation for changes in  $V_{IN}$ . With a fixed  $R_{RAMP}$  value, the modulator gain increases as  $V_{IN}$  is reduced, which could make it difficult to compensate the loop. For low-input-voltage-range designs (3V to 8V),  $R_{RAMP}$  and the compensation component values are going to be different as compared to designs with  $V_{IN}$  between 8V and 24V.



## Master/Slave Configuration

When first enabled, the IC determines if it is configured as a master or slave for synchronization, depending on how  $R_T$  is connected.

**Table 2. Master / Slave Configuration**

$R_T$ to:	Master / Slave	CLK Pin
GND	Master	Output
5V_Reg	Slave, free-running	Input

Slaves free-run in the absence of an external clock signal input when  $R_T$  is connected to 5V\_Reg, allowing regulation to be maintained. It is not recommended to leave  $R_T$  open when running in slave mode to avoid noise pick up on the clock pin.

Slave free-running frequency should be set at least 25% lower than the incoming synchronizing pulse frequency. Maximum synchronizing clock frequency is recommended to be below 600KHz.

## Synchronization

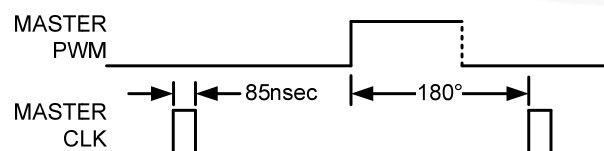
The synchronization method employed by the FAN21SV06 also provides the following features for maximum flexibility.

- Synchronization to an external system clock
- Multiple FAN21SV06s can be synchronized to a single master or system clock
- Independently programmable phase adjustment for one or multiple slaves
- Free-running capability in the absence of system clock or, if the master is disabled/faulted, the slaves can continue to regulate at a lower frequency

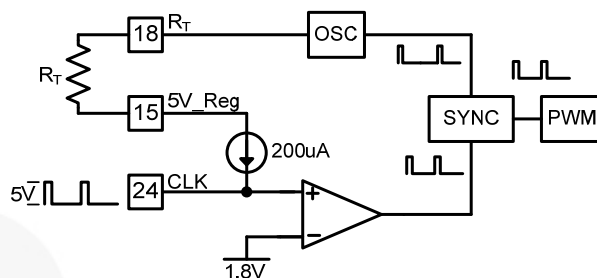
The FAN21SV06 master outputs an 85ns-wide clock (CLK) signal, delayed 180° from its leading PWM edge. This feature allows out-of-phase operation for the slaves, thereby reducing the input capacitance requirements when more than one converter is operating on the same input supply. The leading SW-node edge is delayed ~40ns from the rising PWM signal.

On a slave, synchronization is rising-edge triggered. The CLK input pin has a 1.8V threshold and a 200 $\mu$ A current source pull-up.

In Master mode, the clock signals go out after power-good signal asserts high. Likewise, in Slave mode synchronization to an external clock signal occurs after the power-good signal goes high. Until then, the converter operates in free-run mode.

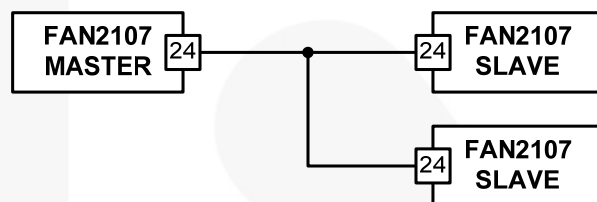


**Figure 34. Synchronization Timing Diagram**



**Figure 35. Slave-CLK-Input Block Diagram**

One or more slaves can be connected directly to a master or system clock to achieve a 180° phase shift.



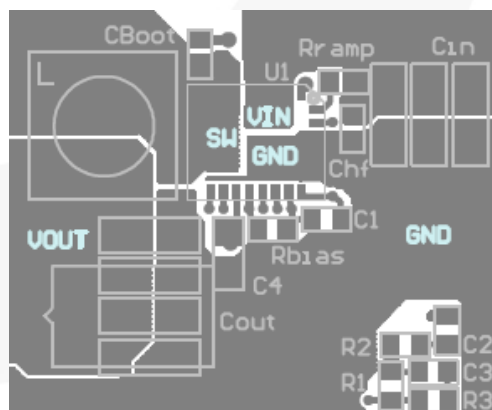
**Figure 36. Slaves with 180° Phase Shift**

Since the synchronizing circuit utilizes a narrow reset pulse, the actual phase delay is slightly more than 180°.

The FAN21SV06 is not intended for use in single-output, multi-phase regulator applications.

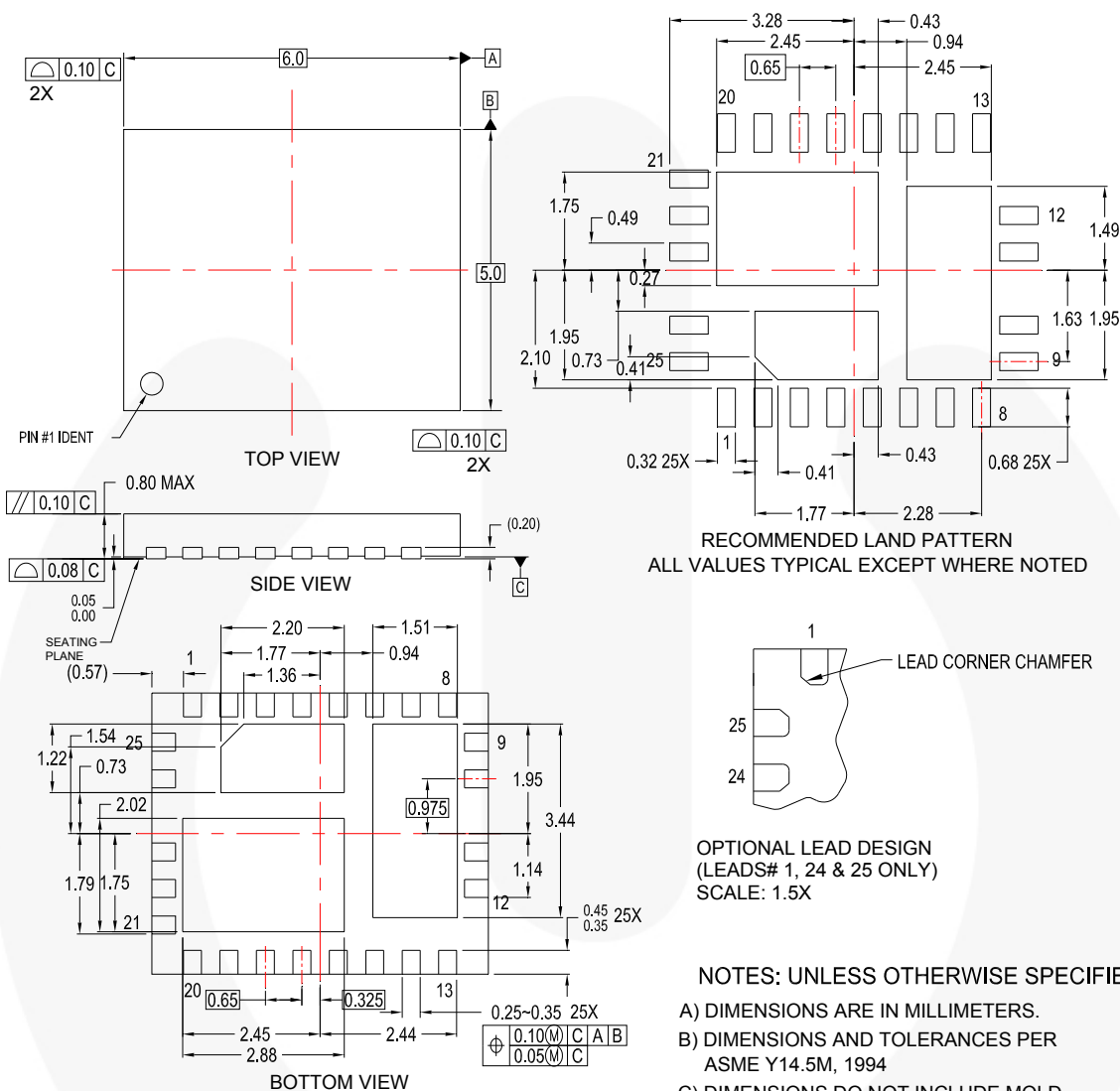
## PCB Layout

Good PCB layout and careful attention to temperature rise is essential for reliable operation of the regulator. Four-layer PCB with 2-ounce copper on the top and bottom side and thermal vias connecting the layers is recommended. Keep power traces wide and short to minimize losses and ringing. Do not connect AGND to PGND below the IC. Connect AGND pin to PGND at the output OR to the PGND plane.



**Figure 37. Recommended PCB Layout**

## Physical Dimensions



**Figure 38. 5x6mm Molded Leadless Package (MLP)**

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