FAIRCHILD SEMICONDUCTOR®

February 2008

74VHC164
8-Bit Serial-In, Parallel-Out Shift Register

Features

- High Speed: f_{MAX} = 175MHz at V_{CC} = 5V
- Low power dissipation: I_{CC} = 4µA (max.) at T_A = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min.)
- Power down protection provided on all inputs
- Low noise: V_{OLP} = 0.8V (max.)
- Pin and function compatible with 74HC164

General Description

The VHC164 is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHC164 is a high-speed 8-Bit Serial-In/Parallel-Out Shift Register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock. An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

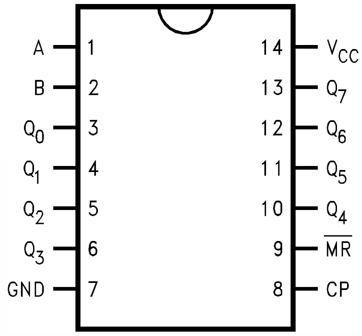
Ordering Information

Order Number	Package Number	Package Description
74VHC164M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC164SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC164MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC164N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Pin Description

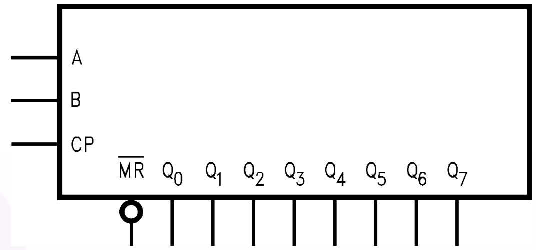
Pin Names	Description
A, B	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$	Master Reset Input (Active LOW)
Q_0–Q_7	Outputs

Functional Description

The VHC164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active High Enable for data entry through the other input. An unused input must be tied HIGH.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs (A • B) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

Logic Symbol



Function Table

Operating Mode	Inputs			Outputs	
	$\overline{MR}$	A	B	Q_0	Q_1–Q_7
Reset (Clear)	L	X	X	L	L–L
Shift	H	L	L	L	Q_0–Q_6
	H	L	H	L	Q_0–Q_6
	H	H	L	L	Q_0–Q_6
	H	H	H	H	Q_0–Q_6

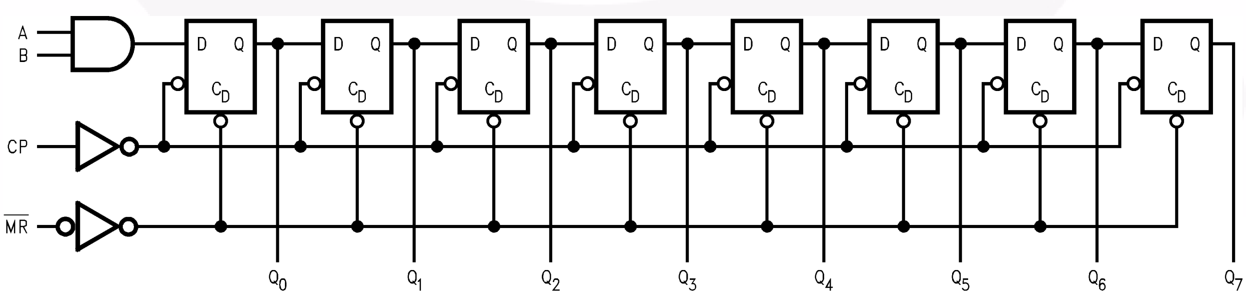
H = HIGH Voltage Levels

L = LOW Voltage Levels

X = Immaterial

Q = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_{IN}	DC Input Voltage	–0.5V to +7.0V
V_{OUT}	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_{IK}	Input Diode Current	–20mA
I_{OK}	Output Diode Current	±20mA
I_{OUT}	DC Output Current	±25mA
I_{CC}	DC V_{CC} / GND Current	±75mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions[1]

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0V to 5.5V
V_{IN}	Input Voltage	0V to +5.5V
V_{OUT}	Output Voltage	0V to V_{CC}
T_{OPR}	Operating Temperature	–40°C to +85°C
t_r, t_f	Input Rise and Fall Time, V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	 0ns/V ~ 100ns/V 0ns/V ~ 20ns/V

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions		$T_A = 25°C$			$T_A = –40°C$ to +85°C		Units
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	2.0			1.50			1.50		V
		3.0–5.5			0.7 x V_{CC}			0.7 x V_{CC}		
V_{IL}	LOW Level Input Voltage	2.0					0.50		0.50	V
		3.0–5.5					0.3 x V_{CC}		0.3 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = –50μA$	1.9	2.0		1.9		V
		3.0			2.9	3.0		2.9		
		4.5			4.4	4.5		4.4		
		3.0		$I_{OH} = –4mA$	2.58			2.48		
		4.5		$I_{OH} = –8mA$	3.94			3.80		
V_{OL}	LOW Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50μA$		0.0	0.1		0.1	V
		3.0				0.0	0.1		0.1	
		4.5				0.0	0.1		0.1	
		3.0		$I_{OL} = 4mA$			0.36		0.44	
		4.5		$I_{OL} = 8mA$			0.36		0.44	
I_{IN}	Input Leakage Current	0–5.5	V_{IN} = 5.5V or GND				±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND				4.0		40.0	μA

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25°C$		Units
				Typ.	Limits	
V_{OLP}(2)	Quiet Output Maximum Dynamic V_{OL}	5.0	$C_L = 50pF$	0.5	0.8	V
V_{OLV}(2)	Quiet Output Minimum Dynamic V_{OL}	5.0	$C_L = 50pF$	–0.5	–0.8	V
V_{IHD}(2)	Minimum HIGH Level Dynamic Input Voltage	5.0	$C_L = 50pF$		3.5	V
V_{ILD}(2)	Maximum LOW Level Dynamic Input Voltage	5.0	$C_L = 50pF$		1.5	V

Note:

2. Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units
				Min.	Typ.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	3.3 ± 0.3	$C_L = 15pF, R_L = 1k\Omega$	80	125		65		MHz
			$C_L = 50pF, R_L = 1k\Omega$	50	75		45		
		5.0 ± 0.5	$C_L = 15pF, R_L = 1k\Omega$	125	175		105		
			$C_L = 50pF, R_L = 1k\Omega$	85	115		75		
t_{PLH}, t_{PHL}	Propagation Delay Time (CP–Q_n)	3.3 ± 0.3	$C_L = 15pF, R_L = 1k\Omega$		8.4	12.8	1.0	15.0	ns
			$C_L = 50pF, R_L = 1k\Omega$		10.9	16.3	1.0	18.5	
		5.0 ± 0.5	$C_L = 15pF, R_L = 1k\Omega$		5.8	9.0	1.0	10.5	
			$C_L = 50pF, R_L = 1k\Omega$		7.3	11.0	1.0	12.5	
t_{PHL}	Propagation Delay Time ($\overline{MR}$–Q_n)	3.3 ± 0.3	$C_L = 15pF, R_L = 1k\Omega$		8.3	12.8	1.0	15.0	ns
			$C_L = 50pF, R_L = 1k\Omega$		10.8	16.3	1.0	18.5	
		5.0 ± 0.5	$C_L = 15pF, R_L = 1k\Omega$		5.2	8.6	1.0	10.0	
			$C_L = 50pF, R_L = 1k\Omega$		6.7	10.6	1.0	12.0	
C_{IN}	Input Capacitance		V_{CC} = Open		4	10		10	pF
C_{PD}	Power Dissipation Capacitance		(3)		76				pF

Note:

3. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I_{CC} (opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$.

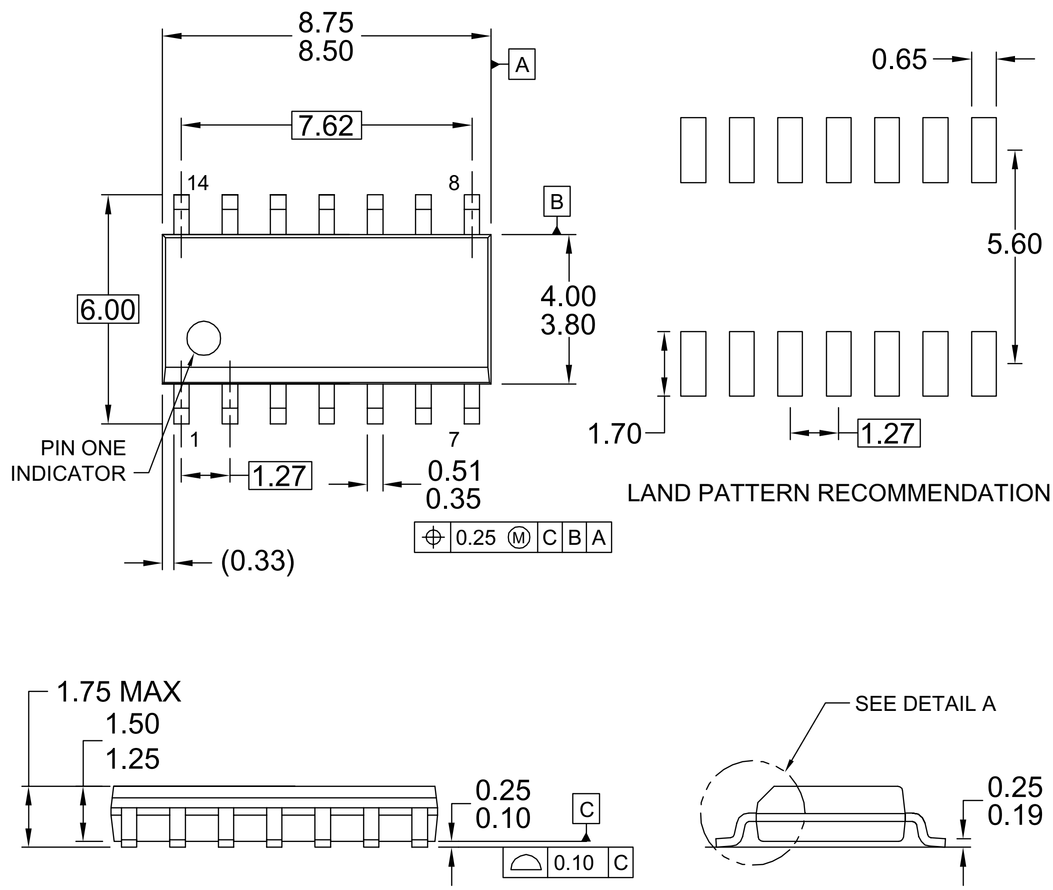
AC Operating Requirements

Symbol	Parameter	V_{CC} (V)(4)	$T_A = 25°C$		$T_A = -40°C$ to $+85°C$	Units
			Typ.	Guaranteed Minimum		
t_W(L), t_W(H)	Minimum Pulse Width (CP)	3.3		5.0	5.0	ns
		5.0		5.0	5.0	
t_W(L)	Minimum Pulse Width ($\overline{MR}$)	3.3		5.0	5.0	ns
		5.0		5.0	5.0	
t_S	Minimum Setup Time	3.3		5.0	6.0	ns
		5.0		4.5	4.5	
t_H	Minimum Hold Time	3.3		0.0	0.0	ns
		5.0		1.0	1.0	
t_{REC}	Minimum Removal Time ($\overline{MR}$)	3.3		2.5	2.5	ns
		5.0		2.5	2.5	

Note:

4. V_{CC} is 3.3 ± 0.3V or 5.0 ± 0.5V

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X145-14M
E) DRAWING CONFORMS TO ASME Y14.5M-1994
F) DRAWING FILE NAME: M14AREV13

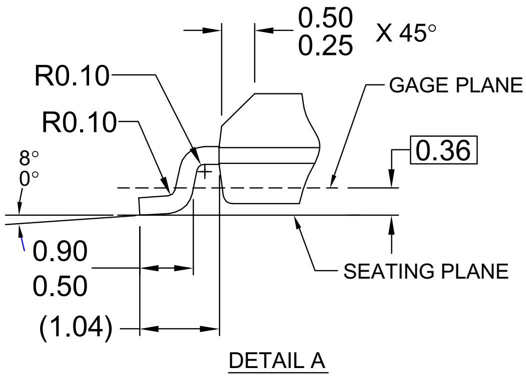


Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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Physical Dimensions (Continued)

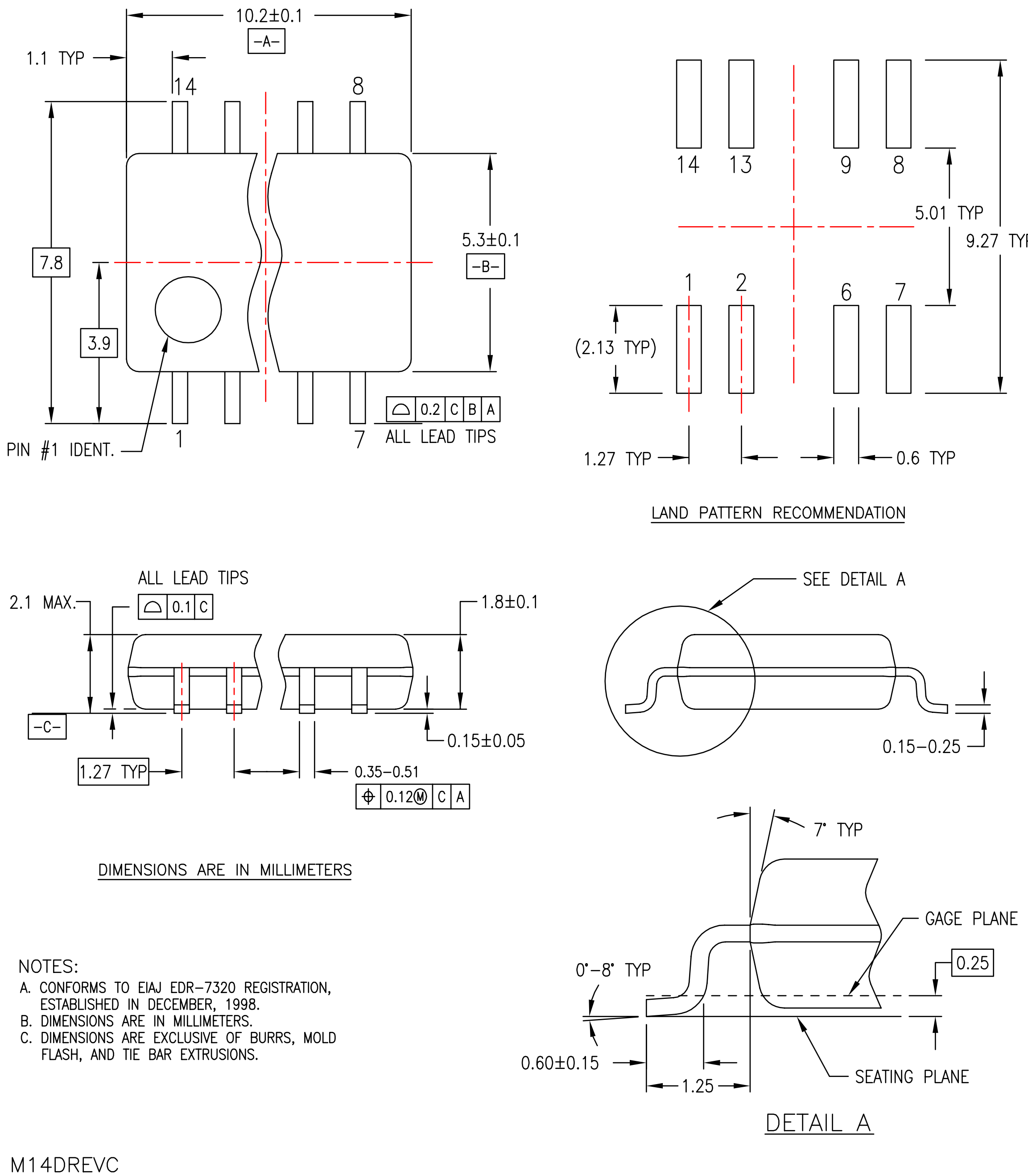

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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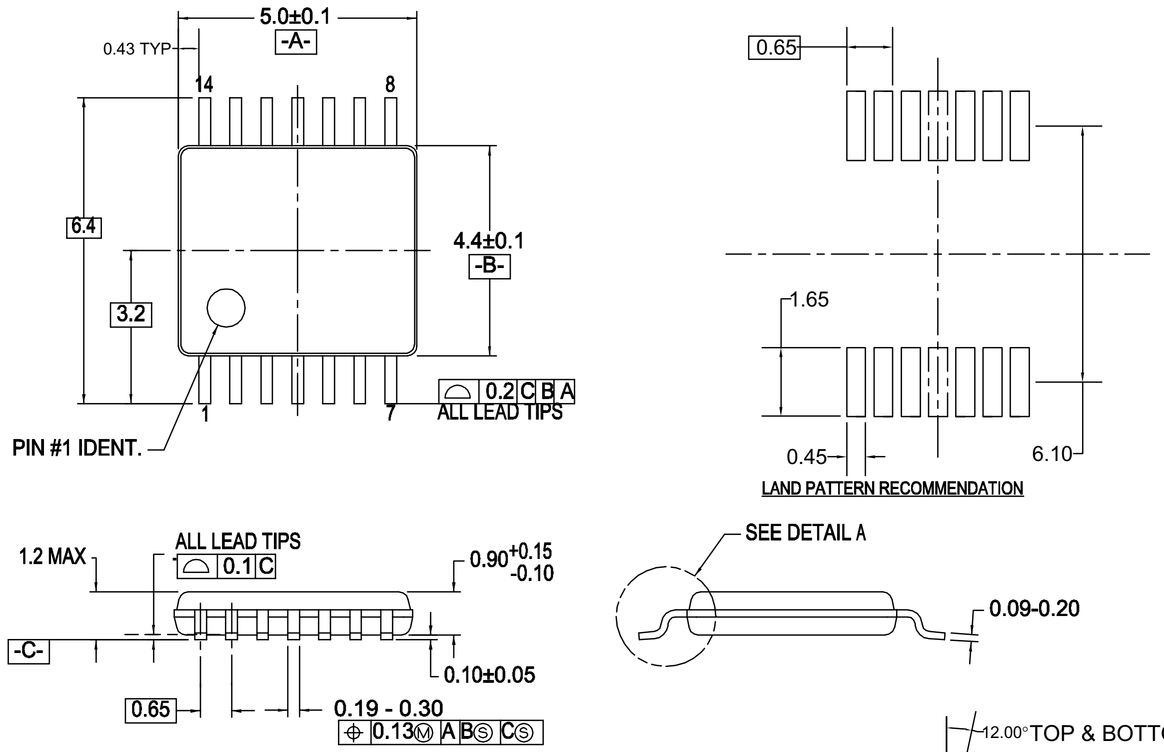
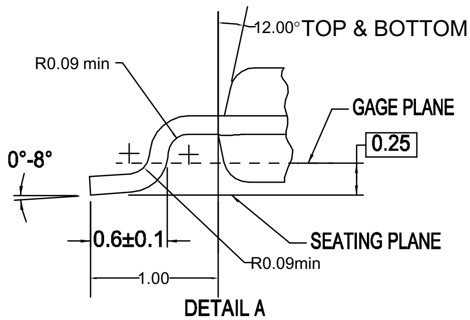
Physical Dimensions (Continued)





NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
E. LANDPATTERN STANDARD: SOP65P640X110-14M
F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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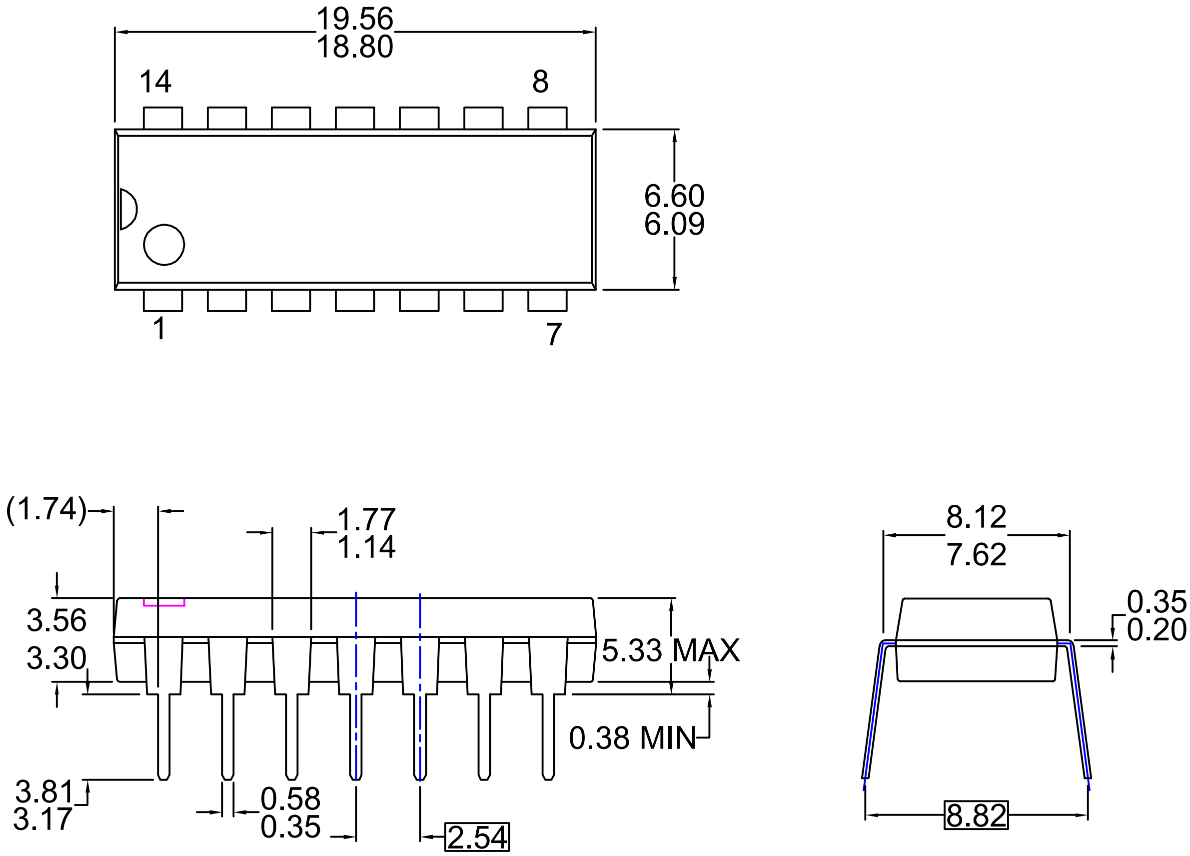
Physical Dimensions (Continued)



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THIS PACKAGE CONFORMS TO

A) JEDEC MS-001 VARIATION BA

B) ALL DIMENSIONS ARE IN MILLIMETERS.

DIMENSIONS ARE EXCLUSIVE OF BURRS,

C) MOLD FLASH, AND TIE BAR EXTRUSIONS.

D) DIMENSIONS AND TOLERANCES PER ASME Y14.5-1994

E) DRAWING FILE NAME: MKT-N14AREV7

Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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