

# 74LVX125

## Low Voltage Quad Buffer with 3-STATE Outputs

### Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

### General Description

The LVX125 contains four independent non-inverting buffers with 3-STATE outputs. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

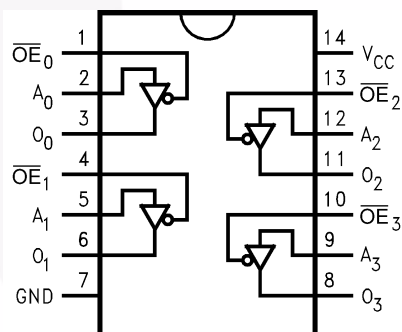
### Ordering Information

Order Number	Package Number	Package Description
74LVX125M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LVX125SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVX125MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

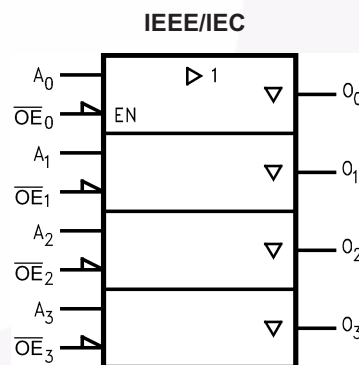
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

### Connection Diagram



### Logic Symbol



### Pin Description

Pin Names	Description
$A_n$	Inputs
$\overline{OE}_n$	Output Enable Inputs
$O_n$	Outputs

### Truth Table

Inputs		Output
$\overline{OE}_n$	$A_n$	$O_n$
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level

L = LOW Voltage Level

Z = High Impedance

X = Immaterial

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	−0.5V to +7.0V
$I_{IK}$	DC Input Diode Current, $V_I = -0.5V$	−20mA
$V_I$	DC Input Voltage	−0.5V to 7V
$I_{OK}$	DC Output Diode Current $V_O = -0.5V$	−20mA
	$V_O = V_{CC} + 0.5V$	+20mA
$V_O$	DC Output Voltage	−0.5V to $V_{CC} + 0.5V$
$I_O$	DC Output Source or Sink Current	±25mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	±50mA
$T_{STG}$	Storage Temperature	−65°C to +150°C
P	Power Dissipation	180mW

## Recommended Operating Conditions<sup>(1)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	2.0V to 3.6V
$V_I$	Input Voltage	0V to 5.5V
$V_O$	Output Voltage	0V to $V_{CC}$
$T_A$	Operating Temperature	−40°C to +85°C
$\Delta t / \Delta V$	Input Rise and Fall Time	0ns/V to 100ns/V

### Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	Conditions	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V <sub>IH</sub>	HIGH Level Input Voltage	2.0		1.5			1.5		V
		3.0		2.0			2.0		
		3.6		2.4			2.4		
V <sub>IL</sub>	LOW Level Input Voltage	2.0				0.5		0.5	V
		3.0				0.8		0.8	
		3.6				0.8		0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	2.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -50μA	1.9	2.0		1.9		V
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -50μA	2.9	3.0		2.9		
			V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -4mA	2.58			2.48		
V <sub>OL</sub>	LOW Level Output Voltage	2.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 50μA		0.0	0.1		0.1	V
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 50μA		0.0	0.1		0.1	
			V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 4mA			0.36		0.44	
I <sub>OZ</sub>	3-STATE Output Off-State Current	3.6	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , V <sub>OUT</sub> = V <sub>CC</sub> or GND			±0.25		±2.5	μA
I <sub>IN</sub>	Input Leakage Current	3.6	V <sub>IN</sub> = 5.5V or GND			±0.1		±1.0	μA
I <sub>CC</sub>	Quiescent Supply Current	3.6	V <sub>IN</sub> = V <sub>CC</sub> or GND			4.0		40.0	μA

Noise Characteristics<sup>(2)</sup>

Symbol	Parameter	V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	T <sub>A</sub> = 25°C		Units
				Typ.	Limit	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	50	0.3	0.8	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	50	-0.3	-0.8	V
V <sub>IHD</sub>	Minimum HIGH Level Dynamic Input Voltage	3.3	50		2.0	V
V <sub>ILD</sub>	Maximum LOW Level Dynamic Input Voltage	3.3	50		0.8	V

## Note:

2. Input t<sub>r</sub> = t<sub>f</sub> = 3ns

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time, Data to Output	2.7	C <sub>L</sub> = 15pF		5.8	10.1	1.0	13.5	ns
			C <sub>L</sub> = 50pF		8.3	13.6	1.0	17.0	
		3.3 ± 0.3	C <sub>L</sub> = 15pF		4.4	6.2	1.0	8.5	
			C <sub>L</sub> = 50pF		6.9	9.7	1.0	12.0	
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time	2.7	C <sub>L</sub> = 15pF, R <sub>L</sub> = 1kΩ		5.3	9.3	1.0	12.5	ns
			C <sub>L</sub> = 50pF, R <sub>L</sub> = 1kΩ		7.8	12.8	1.0	16.0	
		3.3 ± 0.3	C <sub>L</sub> = 15pF, R <sub>L</sub> = 1kΩ		4.0	5.6	1.0	7.5	
			C <sub>L</sub> = 50pF, R <sub>L</sub> = 1kΩ		6.5	9.1	1.0	11.0	
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	2.7	C <sub>L</sub> = 50pF, R <sub>L</sub> = 1kΩ		10.0	15.7	1.0	19.0	ns
		3.3 ± 0.3	C <sub>L</sub> = 50pF, R <sub>L</sub> = 1kΩ		8.3	11.2	1.0	13.0	
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew <sup>(3)</sup>	2.7	C <sub>L</sub> = 50pF			1.5		1.5	ns
		3.3				1.5		1.5	

## Note:

3. Parameter guaranteed by design  $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

## Capacitance

Symbol	Parameter	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units
		Min.	Typ.	Max.	Min.	Max.	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance <sup>(4)</sup>		14				pF

## Note:

4. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:  $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} \times I_{CC}}{4 \text{ (per bit)}}$

## Physical Dimensions

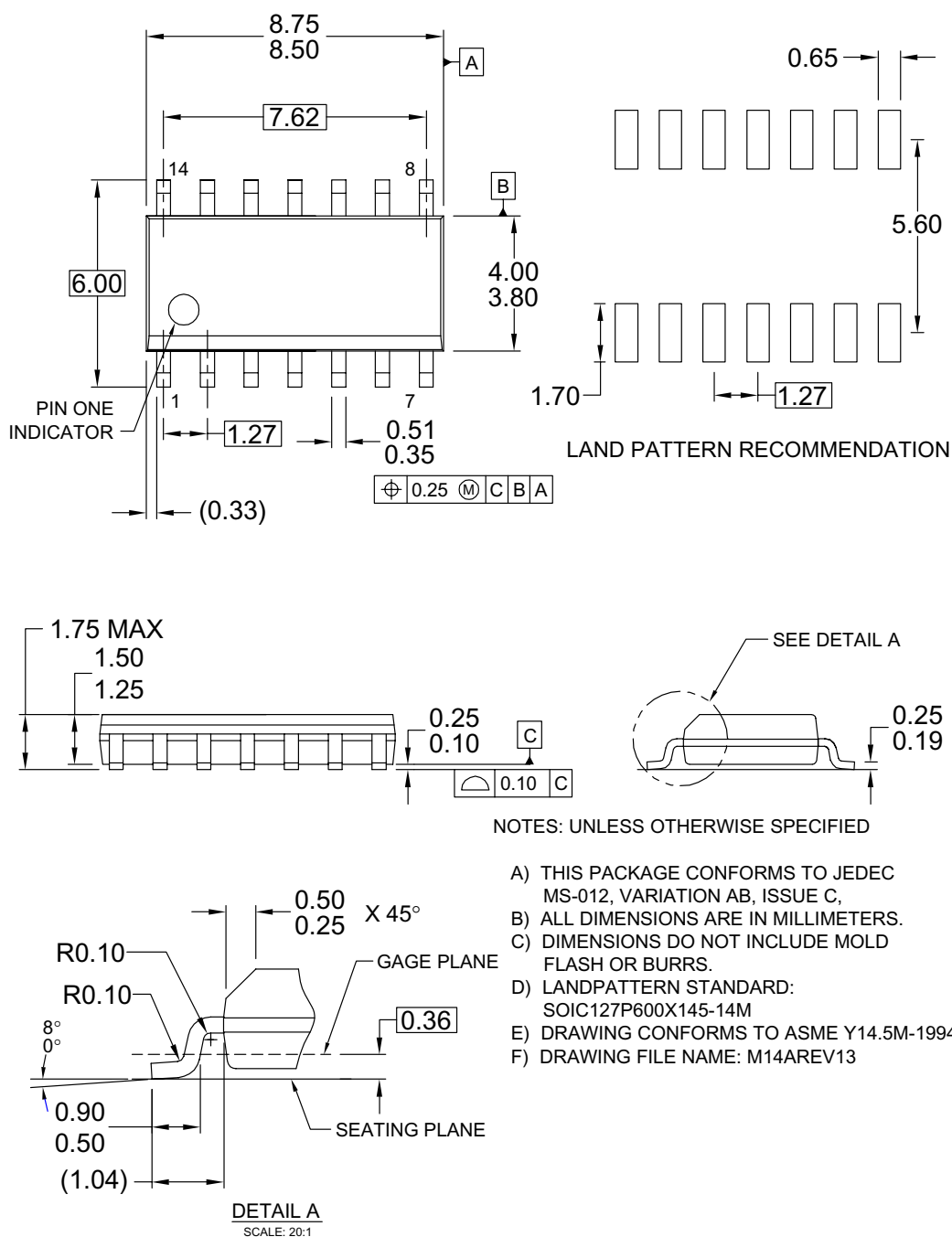


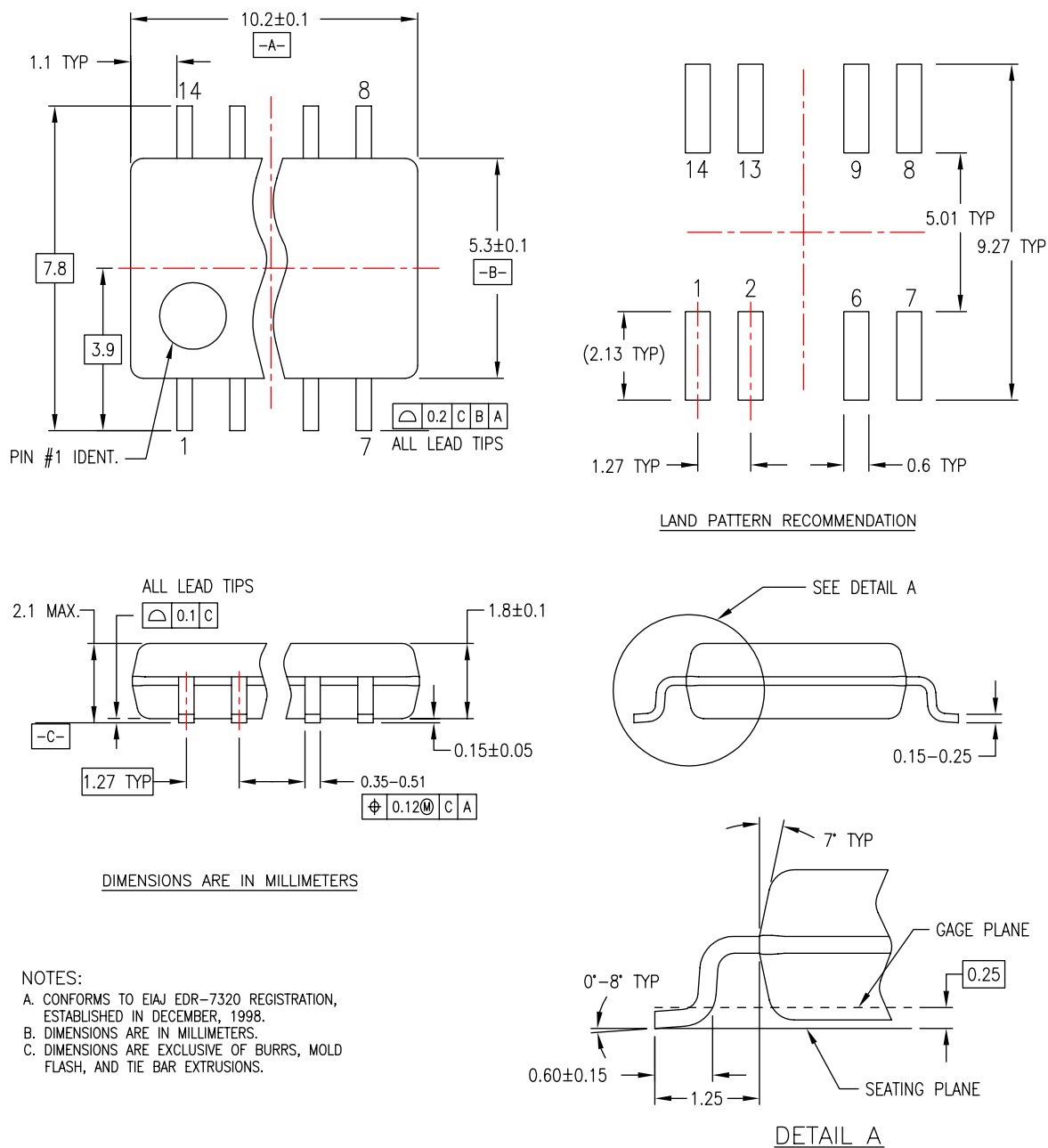
Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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## Physical Dimensions (Continued)



M14DREVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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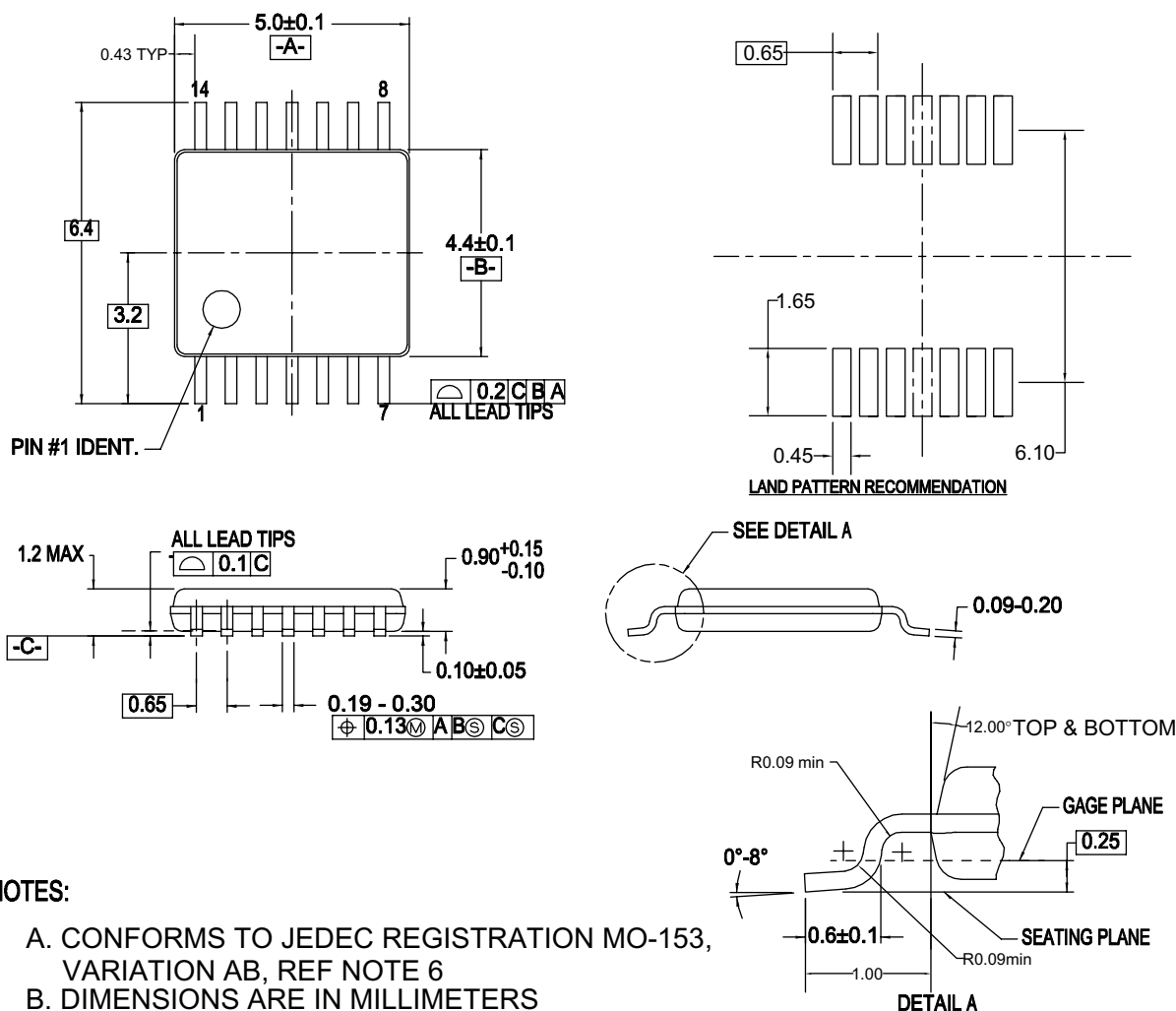


Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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

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