January 2008

74LVTH125
Low Voltage Quad Buffer with 3-STATE Outputs

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink –32mA/+64mA
- Functionally compatible with the 74 series 125
- Latch-up performance exceeds 500mA
- ESD performance:
  - Human-body model > 2000V
  - Machine model > 200V
  - Charged-device model > 1000V

General Description

The LVTH125 contains four independent non-inverting buffers with 3-STATE outputs.

These buffers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH125 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

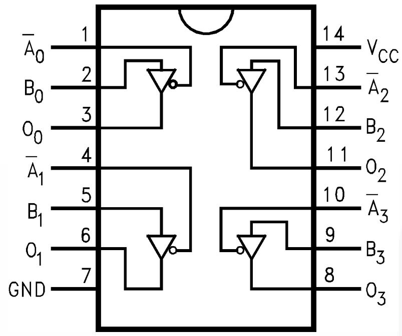
Ordering Information

Order Number	Package Number	Package Description
74LVTH125M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LVTH125SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVTH125MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

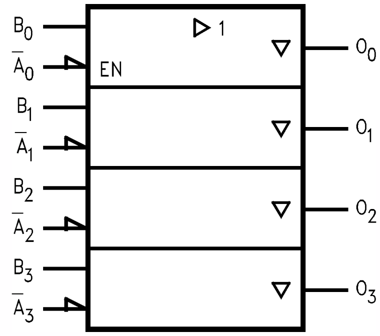
All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Symbol

IEEE/IEC



Pin Description

Pin Names	Description
$\overline{A}_n$, B_n	Inputs
O_n	3-STATE Outputs

Truth Table

Inputs		Output
$\overline{A}_n$	B_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +4.6V
V_I	DC Input Voltage	–0.5V to +7.0V
V_O	DC Output Voltage Output in 3-STATE	–0.5V to +7.0V
	Output in HIGH or LOW State[1]	–0.5V to +7.0V
I_{IK}	DC Input Diode Current, V_I < GND	–50mA
I_{OK}	DC Output Diode Current, V_O < GND	–50mA
I_O	DC Output Current, $V_O > V_{CC}$ Output at HIGH State	64mA
	Output at LOW State	128mA
I_{CC}	DC Supply Current per Supply Pin	±64mA
I_{GND}	DC Ground Current per Ground Pin	±128mA
T_{STG}	Storage Temperature	–65°C to +150°C

Note:

1. I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH-Level Output Current		–32	mA
I_{OL}	LOW-Level Output Current		64	mA
T_A	Free-Air Operating Temperature	–40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = –40°C to +85°C			Units
				Min.	Typ.[2]	Max.	
V_{IK}	Input Clamp Diode Voltage	2.7	I_I = –18mA			–1.2	V
V_{IH}	Input HIGH Voltage	2.7–3.6	$V_O \leq$ 0.1V or	2.0			V
V_{IL}	Input LOW Voltage	2.7–3.6	$V_O \geq V_{CC}$ – 0.1V			0.8	V
V_{OH}	Output HIGH Voltage	2.7–3.6	I_{OH} = –100µA	V_{CC} – 0.2			V
		2.7	I_{OH} = –8mA	2.4			
		3.0	I_{OH} = –32mA	2.0			
V_{OL}	Output LOW Voltage	2.7	I_{OL} = 100µA			0.2	V
			I_{OL} = 24mA			0.5	
		3.0	I_{OL} = 16mA			0.4	
			I_{OL} = 32mA			0.5	
			I_{OL} = 64mA			0.55	
$I_{I(HOLD)}$	Bushold Input Minimum Drive	3.0	V_I = 0.8V	75			µA
			V_I = 2.0V	–75			
$I_{I(OD)}$	Bushold Input Over-Drive Current to Change State	3.0	[3]	500			µA
			[4]	–500			
I_I	Input Current	3.6	V_I = 5.5V			10	µA
	Control Pins	3.6	V_I = 0V or V_{CC}			±1	
	Data Pins	3.6	V_I = 0V			–5	
			$V_I = V_{CC}$			1	
I_{OFF}	Power Off Leakage Current	0	0V $\leq V_I$ or $V_O \leq$ 5.5V			±100	µA
$I_{PU/PD}$	Power up/down 3-STATE Output Current	0–1.5	V_O = 0.5V to 3.0V, V_I = GND or V_{CC}			±100	µA
I_{OZL}	3-STATE Output Leakage Current	3.6	V_O = 0.5V			–5	µA
I_{OZH}	3-STATE Output Leakage Current	3.6	V_O = 3.0V			5	µA
$I_{OZH}+$	3-STATE Output Leakage Current	3.6	$V_{CC} < V_O \leq$ 5.5V			10	µA
I_{CCH}	Power Supply Current	3.6	Outputs HIGH			0.19	mA
I_{CCL}	Power Supply Current	3.6	Outputs LOW			5	mA
I_{CCZ}	Power Supply Current	3.6	Outputs Disabled			0.19	mA
$I_{CCZ}+$	Power Supply Current	3.6	$V_{CC} \leq V_O \leq$ 5.5V, Outputs Disabled			0.19	mA
ΔI_{CC}	Increase in Power Supply Current[5]	3.6	One Input at V_{CC} – 0.6V, Other Inputs at V_{CC} or GND			0.2	mA

Notes:

2. All typical values are at V_{CC} = 3.3V, T_A = 25°C.
3. An external driver must source at least the specified current to switch from LOW-to-HIGH.
4. An external driver must sink at least the specified current to switch from HIGH-to-LOW.
5. This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics(6)

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25°C$			Units
			$C_L = 50$ pF, $R_L = 500\Omega$	Min.	Typ.	Max.	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	(7)		0.8		V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	(7)		–0.8		V

Notes:

6. Characterized in SOIC package. Guaranteed parameter, but not tested.
7. Max number of outputs defined as (n). n–1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter	$T_A = –40°C$ to $+85°C$, $C_L = 50pF$, $R_L = 500\Omega$					Units
		$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
		Min.	Typ.(8)	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, Data to Output	1.0		3.5	1.0	4.5	ns
t_{PHL}		1.0		3.9	1.0	4.9	
t_{PZH}	Output Enable Time	1.0		4.0	1.0	5.5	ns
t_{PZL}		1.1		4.0	1.1	5.4	
t_{PHZ}	Output Disable Time	1.5		4.5	1.5	5.7	ns
t_{PLZ}		1.3		4.5	1.3	4.0	
t_{OSHL}, t_{OSLH}	Output to Output Skew(9)			1.0		1.0	ns

Notes:

8. All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.
9. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

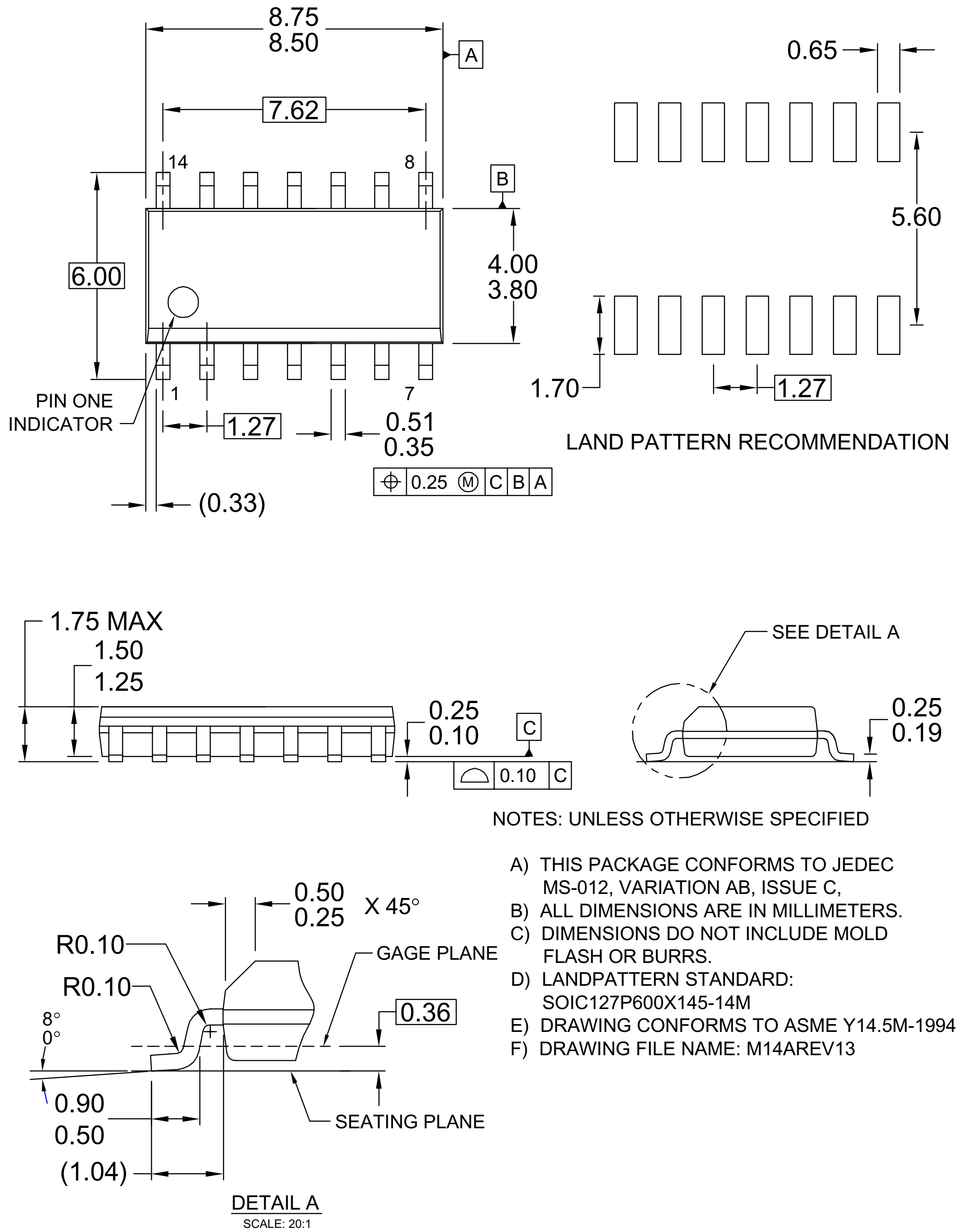
Capacitance(10)

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}	4	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}	8	pF

Note:

10. Capacitance is measured at frequency f = 1MHz, per MIL-STD-883B, Method 3012.

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X145-14M
E) DRAWING CONFORMS TO ASME Y14.5M-1994
F) DRAWING FILE NAME: M14AREV13

Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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Physical Dimensions (Continued)

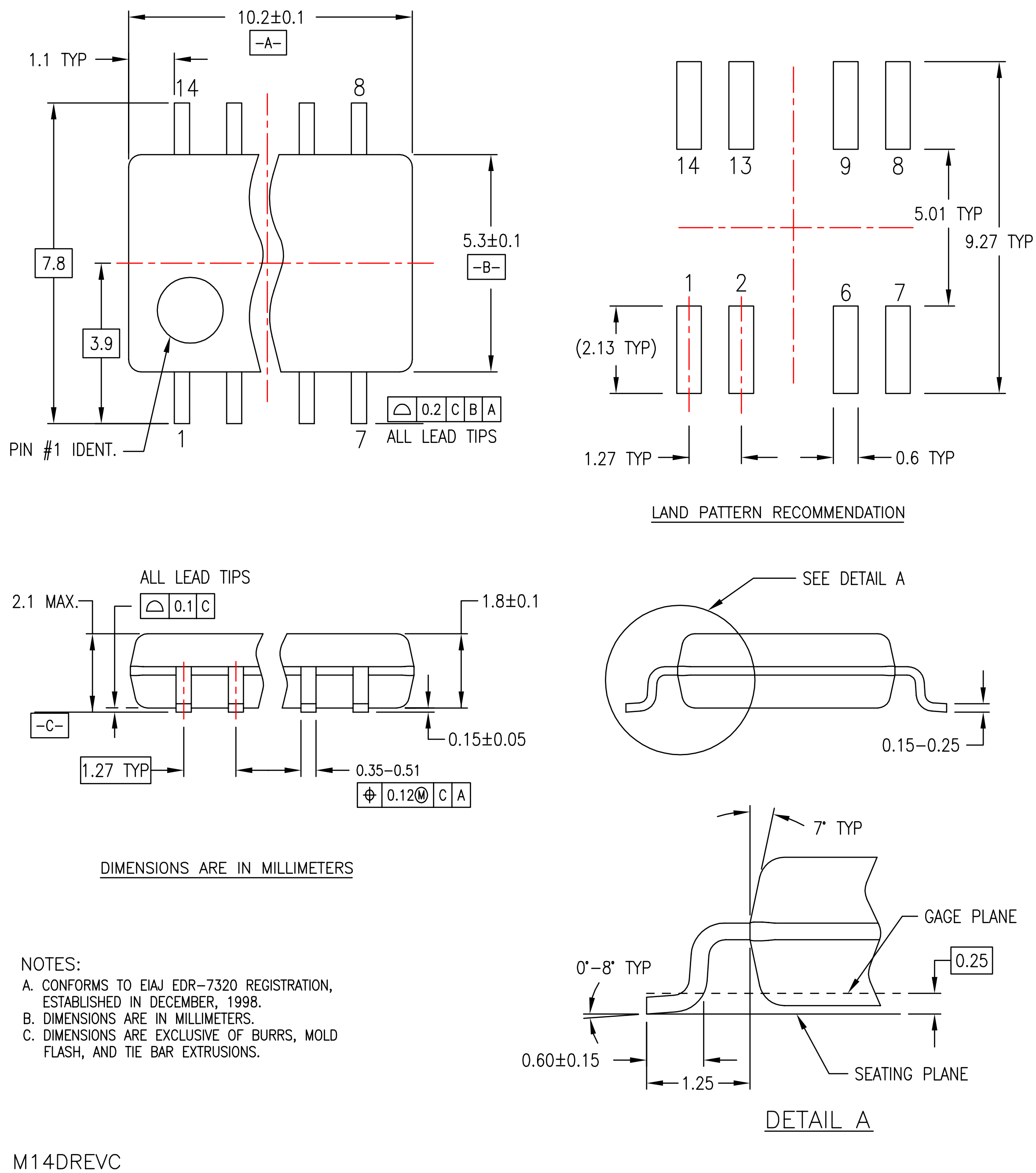

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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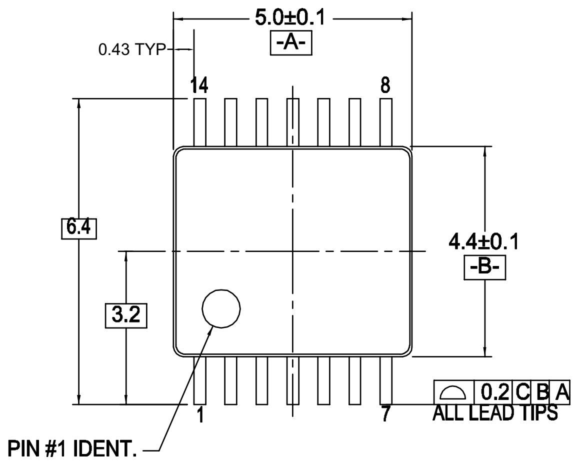
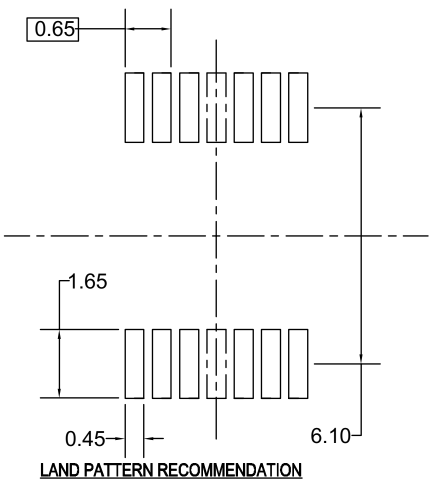
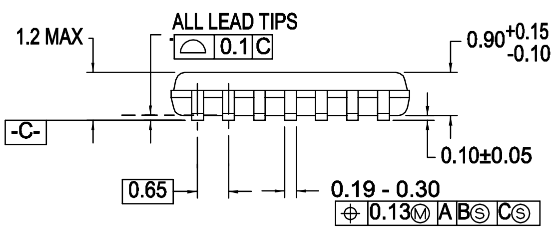
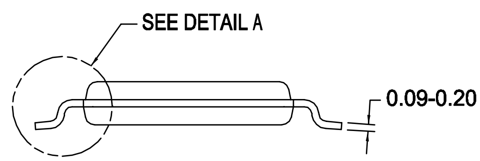
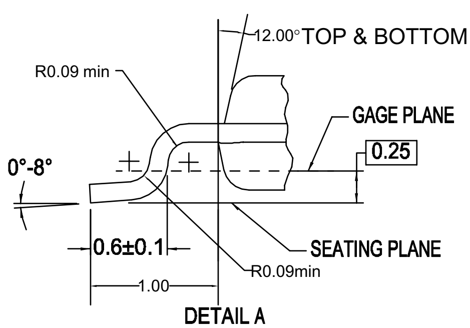
Physical Dimensions (Continued)











NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
E. LANDPATTERN STANDARD: SOP65P640X110-14M
F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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