

February 1994 Revised May 2005

74LCX16240

Low Voltage 16-Bit Inverting Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The LCX16240 contains sixteen inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The LCX16240 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capacity of interfacing to a 5V signal environment

The LCX16240 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- \blacksquare 2.3V to 3.6V $\rm V_{CC}$ specifications provided
- \blacksquare 4.5 ns t_{PD} max (V $_{CC}$ = 3.3V), 20 μA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ±24 mA output drive (V_{CC} = 3.0V)
- Implements proprietary noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:

Human body model > 2000V

Machine model > 200V

Note 1: To ensure the high-impedance state during power up or down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

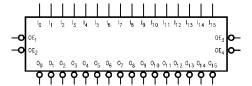
Order Number	Package Number	Package Description
74LCX16240MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LCX16240MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Logic Symbol



Pin Descriptions

Pin Names Description			
OE n	Output Enable Inputs (Active LOW)		
I ₀ -I ₁₅	Inputs		
$\overline{O}_0 - \overline{O}_{15}$	Outputs		

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Truth Tables

Inp	uts	Outputs
OE ₁	I ₀ -I ₃	$\overline{O}_0 - \overline{O}_3$
L	L	Н
L	Н	L
Н	X	Z

Inp	uts	Outputs
OE₃	I ₈ –I ₁₁	0 ₈ -0 ₁₁
L	L	Н
L	Н	L
Н	Z	Z

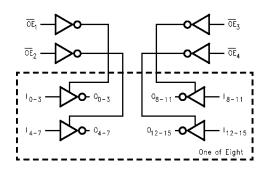
Inp	uts	Outputs
ŌE₂	I ₄ –I ₇	$\overline{O}_4 - \overline{O}_7$
L	L	Н
L	Н	L
Н	X	Z

Inp	uts	Outputs
ŌE₄	I ₁₂ –I ₁₅	\overline{O}_{12} – \overline{O}_{15}
L	L	Н
L	Н	L
Н	Z	Z

Functional Description

The LCX16240 contains sixteen inverting buffers with 3-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The 3-STATE outputs are controlled by an Output Enable $(\overline{\mbox{OE}}_n)$ input for each nibble. When \overline{OE}_n is LOW, the outputs are in 2-state mode. When $\overline{\rm OE}_{\rm n}$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagram



H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings(Note 2) Parameter Value Units Symbol Conditions ٧ Supply Voltage -0.5 to +7.0 V_{CC} DC Input Voltage ٧ -0.5 to +7.0 V_{I} DC Output Voltage -0.5 to +7.0 Output in 3-STATE -0.5 to $V_{CC} + 0.5$ Output in HIGH or LOW State (Note 3) DC Input Diode Current -50 $V_I < GND$ mΑ V_O < GND DC Output Diode Current -50 I_{OK} mΑ +50 $V_O > V_{CC}$ DC Output Source/Sink Current ±50 mΑ I_{CC} DC Supply Current per Supply Pin ±100 mΑ DC Ground Current per Ground Pin ±100 I_{GND}

-65 to +150

Recommended Operating Conditions (Note 4)

Symbol	Parameter		Min	Max	Units
V _{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	V
VI	Input Voltage		0	5.5	V
Vo	Output Voltage	HIGH or LOW State	0	V _{CC}	V
		3-STATE	0	5.5	V
I _{OH} /I _{OL}	Output Current	$V_{CC} = 3.0V - 3.6V$		±24	
		$V_{CC} = 2.7V - 3.0V$		±12	mA
		$V_{CC} = 2.3V - 2.7V$		±8	
T _A	Free-Air Operating Temperature		-40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, V _{IN} = 0.8V–2.0V, V _{CC} = 3.0V		0	10	ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Storage Temperature

 $\mathsf{T}_{\mathsf{STG}}$

Note 4: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{cc}	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units
Syllibol		Conditions	(V)	Min	Max	Units
/ _{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 - 3.6	2.0		· ·
/ _{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 - 3.6		0.8	ľ
/ _{ОН}	HIGH Level Output Voltage	I _{OH} = -100 μA	2.3 - 3.6	V _{CC} - 0.2		V
		I _{OH} = -8 mA	2.3	1.8		
		I _{OH} = -12 mA	2.7	2.2		
		I _{OH} = -18 mA	3.0	2.4		
		I _{OH} = -24 mA	3.0	2.2		
/ _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.3 - 3.6		0.2	
		I _{OL} = 8 mA	2.3		0.6	
		I _{OL} = 12 mA	2.7		0.4	V
		I _{OL} = 16 mA	3.0		0.4	
		I _{OL} = 24 mA	3.0		0.55	
ı	Input Leakage Current	$0 \le V_1 \le 5.5V$	2.3 - 3.6		±5.0	μА
OZ	3-STATE Output Leakage	$0 \le V_O \le 5.5V$	2.3 - 3.6		±5.0	
		$V_I = V_{IH}$ or V_{IL}				μА
OFF	Power-Off Leakage Current	V _I or V _O = 5.5V	0		10	μА

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC}	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units
- Cy2C.	1 4.4	oon annone	(V)	Min	Max	•
Icc	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 3.6		20	μА
		$3.6V \le V_I$, $V_O \le 5.5V$ (Note 5)	2.3 – 3.6		±20	μΑ
ΔI_{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} -0.6V	2.3 - 3.6		500	μА

Note 5: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

		$T_A = -40$ °C to $+85$ °C, $R_L = 500 \Omega$						
Symbol		$V_{CC} = 3.3V \pm 0.3V$ $C_L = 50 \text{ pF}$		V _{CC} = 2.7V C _L = 50 pF		V_{CC} = 2.5 \pm 0.2V C_L = 30 pF		Units
	Parameter							
İ		Min	Max	Min	Max	Min	Max	
t _{PHL}	Propagation Delay	1.0	4.5	1.0	5.3	1.0	5.4	ns
t _{PLH}	Data to Output	1.0	4.5	1.0	5.3	1.0	5.4	
t _{PZL}	Output Enable Time	1.0	5.4	1.0	6.0	1.0	7.0	20
t _{PZH}		1.0	5.4	1.0	6.0	1.0	7.0	ns
t _{PLZ}	Output Disable Time	1.0	5.3	1.0	5.4	1.0	6.4	20
t_{PHZ}		1.0	5.3	1.0	5.4	1.0	6.4	ns
toshl	Output to Output Skew (Note 6)		1.0					ns
t _{OSLH}			1.0					115

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C	°C Unit	
Syllibol	Farameter	Conditions	(V)	Typical	Onit	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	3.3	0.8	V	
		$C_L = 30pF$, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	0.6	v v	
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	3.3	-0.8	V	
		$C_L = 30pF, V_{IH} = 2.5V, V_{IL} = 0V$	2.5	-0.6	\	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	$V_{CC} = Open, V_I = 0V \text{ or } V_{CC}$	7	pF
C _{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_{I} = 0V$ or V_{CC} , $f = 10$ MHz	20	pF

AC LOADING and WAVEFORMS Generic for LCX Family

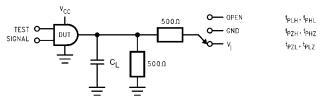
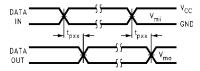
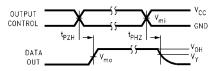


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

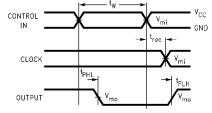
Test	Switch	
t _{PLH} , t _{PHL}	Open	
t _{PZL} , t _{PLZ}	6V at V_{CC} = 3.3 ± 0.3V V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V	
t _{PZH} ,t _{PHZ}	GND	



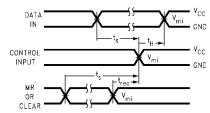
Waveform for Inverting and Non-Inverting Functions



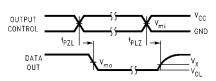
3-STATE Output High Enable and Disable Times for Logic



Propagation Delay. Pulse Width and \mathbf{t}_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

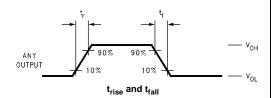
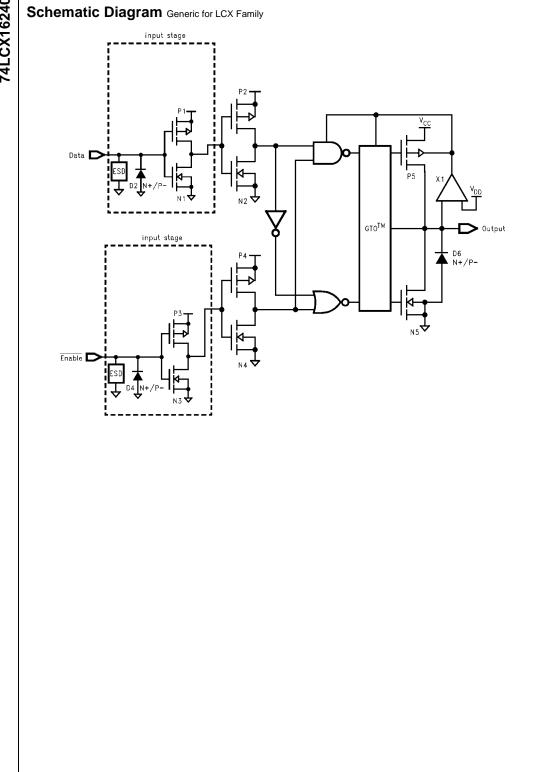
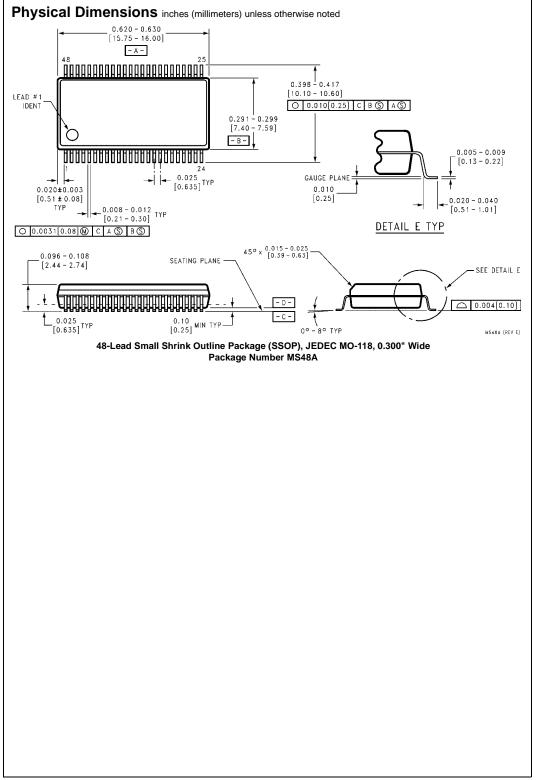


FIGURE 2. Waveforms (Input Characteristics; f =1MHz, $t_r = t_f = 3ns$)

Symbol	V _{CC}			
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V	
V _{mi}	1.5V	1.5V	V _{CC} /2	
V _{mo}	1.5V	1.5V	V _{CC} /2	
V _x	V _{OL} + 0.3V	V _{OL} + 0.3V	V _{OL} + 0.15V	
V _y	V _{OH} – 0.3V	V _{OH} – 0.3V	V _{OH} – 0.15V	





Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 12.50±0.10 0.40 TYP -B-99. 9.20 8.10 50. O.2 C B A ALL LEAD TIPS PIN #1 IDENT 0.50 LAND PATTERN RECOMMENDATION 0.1 C SEE DETAIL A 0.90+0.15 ALL LEAD TIPS 0.09-0.20 0.10±0.05 0.17-0.27 0.50 ♦ 0.13@ A BS CS 12.00' TOP & BOTTOM DIMENSIONS ARE IN MILLIMETERS R0.16 GAGE PLANE 0.25 NOTES: A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ED, DATE 4/97. B. DIMENSIONS ARE IN MILLIMETERS. SEATING PLANE 0.60±0.10 1.00 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982. DETAIL A MTD48REVC

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

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