

**1500 MHz Low Power UltraCMOS™  
Divide-by-4 Prescaler  
Rad hard for Space Applications**

### Features

- DC to 1500 MHz operation
- Fixed divide ratio of 4
- Low-power operation: 6.5 mA typical @ 3 V
- Ultra small package: 8-lead Ceramic SOIC
- Guaranteed 100 Krads(Si) Total Dose Performance
- Superior Single Event Upset Immunity

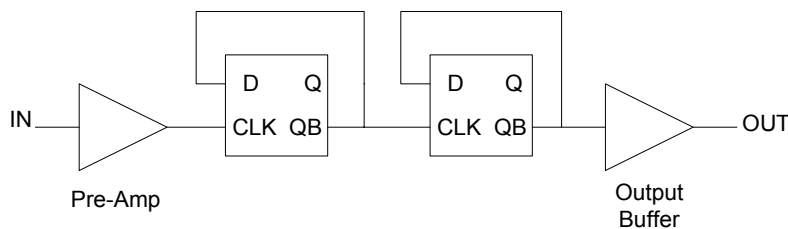
### Product Description

The PE9312 is a high-performance static UltraCMOS™ prescaler with a fixed divide ratio of 4. Its operating frequency range is near DC to 1500 MHz. The PE9312 operates on a nominal 3 V supply and draws only 6.5 mA. It is packaged in a small 8-lead ceramic SOIC and is ideal for frequency scaling and clock generation solutions.

The PE9312 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering excellent RF performance and intrinsic radiation tolerance.

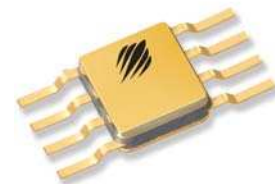
The PE9312 is optimized for commercial space applications. Single Event Latch up (SEL) is physically impossible and Single Event Upset (SEU) is better than  $10^{-9}$  errors per bit / day.

**Figure 1. Functional Diagram**



**Figure 2. Package Type**

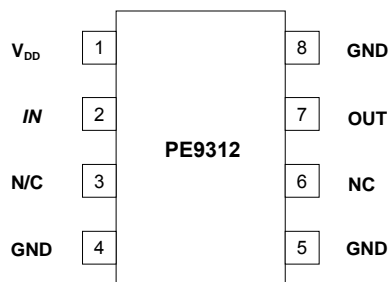
8-lead CSOIC



**Table 1. Electrical Specifications** ( $Z_S = Z_L = 50 \Omega$ )

$V_{DD} = 3.0 \text{ V}$ ,  $-40^\circ \text{ C} \leq T_A \leq 85^\circ \text{ C}$ , unless otherwise specified

Parameter	Conditions	Minimum	Typical	Maximum	Units
Supply Voltage		2.85	3.0	3.15	V
Supply Current			6.5	11	mA
Input Frequency ( $F_{in}$ )		DC		1500	MHz
Input Power ( $P_{in}$ )	$DC < F_{in} < 1000 \text{ MHz}$	-8		+10	dBm
	$1000 < F_{in} < 1500 \text{ MHz}$	0		+10	dBm
Output Power ( $P_{out}$ )	$DC < F_{in} < 1500 \text{ MHz}$	0			dBm

**Figure 3. Pin Configuration**

**Table 2. Pin Descriptions**

Pin No.	Pin Name	Description
1	V <sub>DD</sub>	Power supply pin. Bypassing is required (eg 1000 pF & 100 pF).
2	IN	Input signal pin. Should be coupled with a capacitor (eg 1000 pF).
3	NC	No connection. This pin should be left open.
4	GND	Ground pin. Ground pattern on the board should be as wide as possible to reduce ground impedance.
5	GND	Ground pin.
6	NC	No connection. This pin should be left open.
7	OUT	Divided frequency output pin. This pin should be coupled with a capacitor (eg 1000 pF).
8	GND	Ground Pin.

**Table 3. Absolute Maximum Ratings**

Symbol	Parameter/Conditions	Min	Max	Units
V <sub>DD</sub>	Supply voltage		4.0	V
P <sub>in</sub>	Input Power		15	dBm
V <sub>IN</sub>	Voltage on input	-0.3	V <sub>DD</sub> +0.3	V
T <sub>ST</sub>	Storage temperature range	-65	150	°C
T <sub>OP</sub>	Operating temperature range	-40	85	°C
V <sub>ESD</sub>	ESD voltage (Human Body Model, MIL-STD 883)		1000	V

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage.

### Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

### Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

### Device Functional Considerations

The PE9312 divides an input signal, up to a frequency of 1500 MHz, by a factor of four thereby producing an output frequency at a quarter of the input frequency. To work properly at higher frequency, the input and output signals (pins 2 & 7) must be AC coupled via an external capacitor, as shown in the test circuit in Figure 7. The input may be DC coupled for low frequency operation with care taken to remain within the specified DC input range for the device.

The ground pattern on the board should be made as wide as possible to minimize ground impedance. See Figure 8 for a layout example.

Typical Performance Data:  $V_{DD} = 3.0\text{ V}$

Figure 4. Input Sensitivity

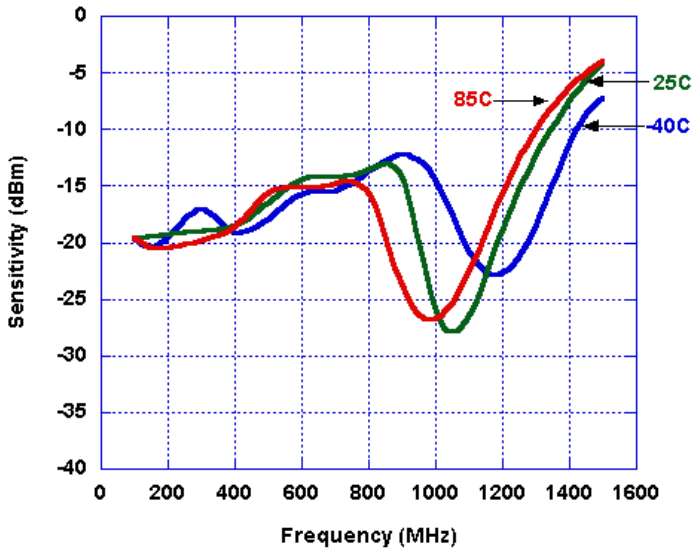


Figure 5. Device Current

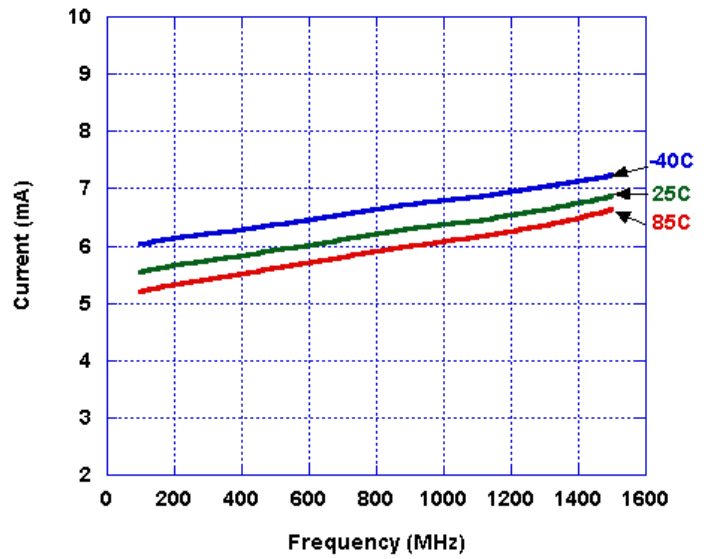
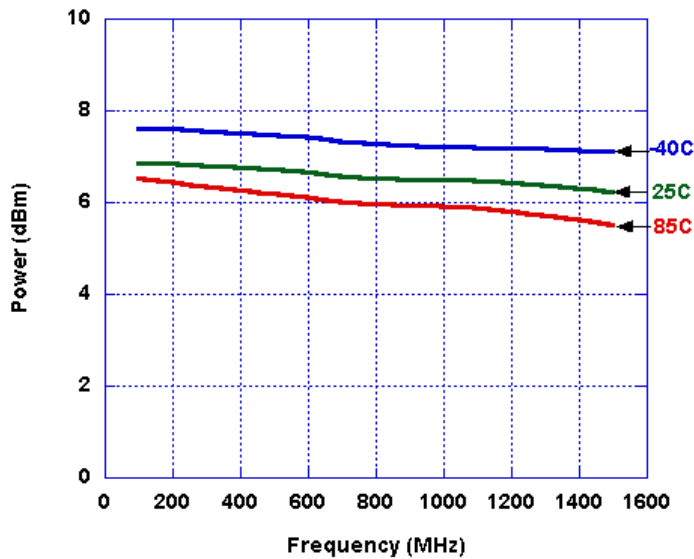
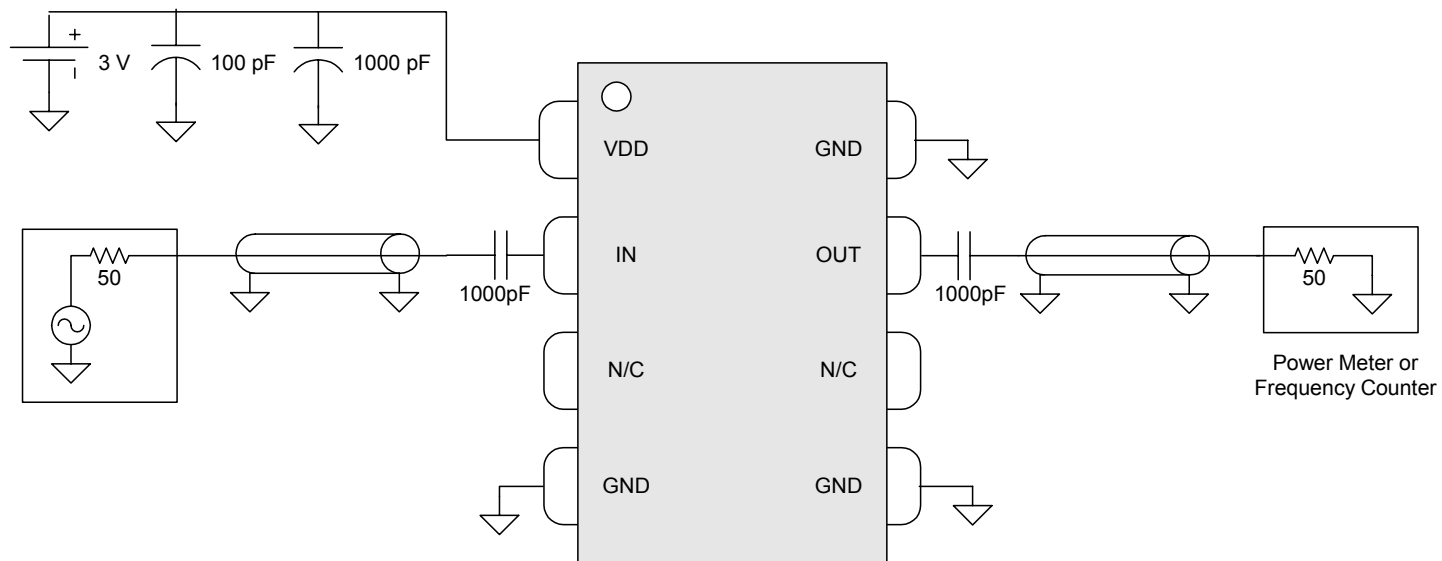


Figure 6. Output Power



**Figure 7. Test Circuit Block Diagram**



## Evaluation Kit Operation

The Ceramic SOIC Prescaler Evaluation Board was designed to help customers evaluate the *PE9312* divide-by-4 prescaler. On this board, the device input (pin 2) is connected to the SMA connector J1 through a 50 Ω transmission line. A series capacitor (C3) provides the necessary DC block for the device input. A value of 1000 pF was used for the evaluation board; other applications may require a different value. It is also possible to place a 0 Ω resistor in this location for very low frequency applications.

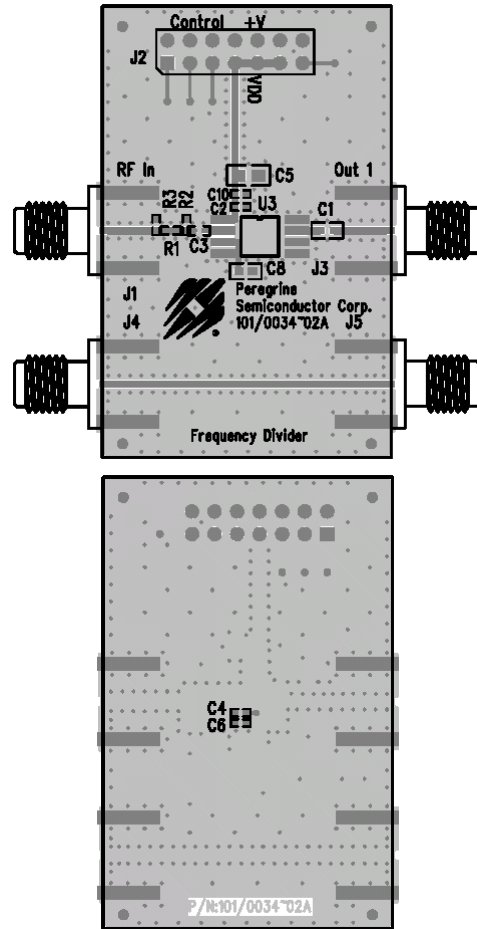
The device output (pin 7) is connected to SMA connector J3 through a 50 Ω transmission line. A series capacitor (C1) provides the necessary DC block for the device output. This capacitor value must be chosen to have a low impedance at the desired output frequency of the device. A value of 1000 pF was chosen for the evaluation board.

The board is constructed of a two-layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide above ground plane model with trace width of 0.030", trace gaps of 0.0061", dielectric thickness of 0.028", metal thickness of 0.0014", and  $\epsilon_r$  of 4.6. Note that the predominate mode of these transmission lines is coplanar waveguide.

J2 provides DC power to the device via pin 1. Two decoupling capacitors (C2=100 pF, C5=1000 pF) are included on this trace. It is the responsibility of the customer to determine proper supply decoupling for their design application.

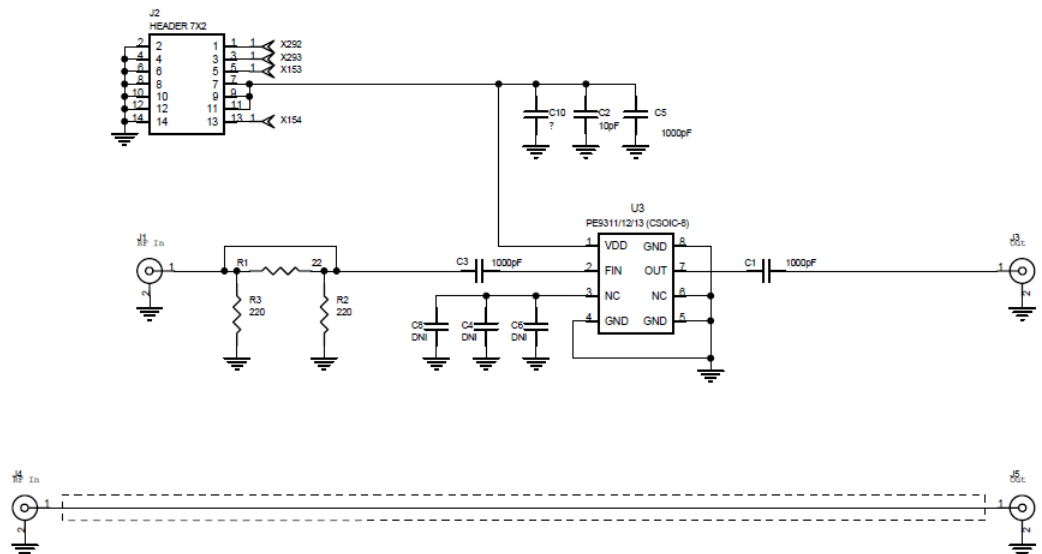
**Figure 8. Evaluation Board Layout**

Peregrine specification 101-0034

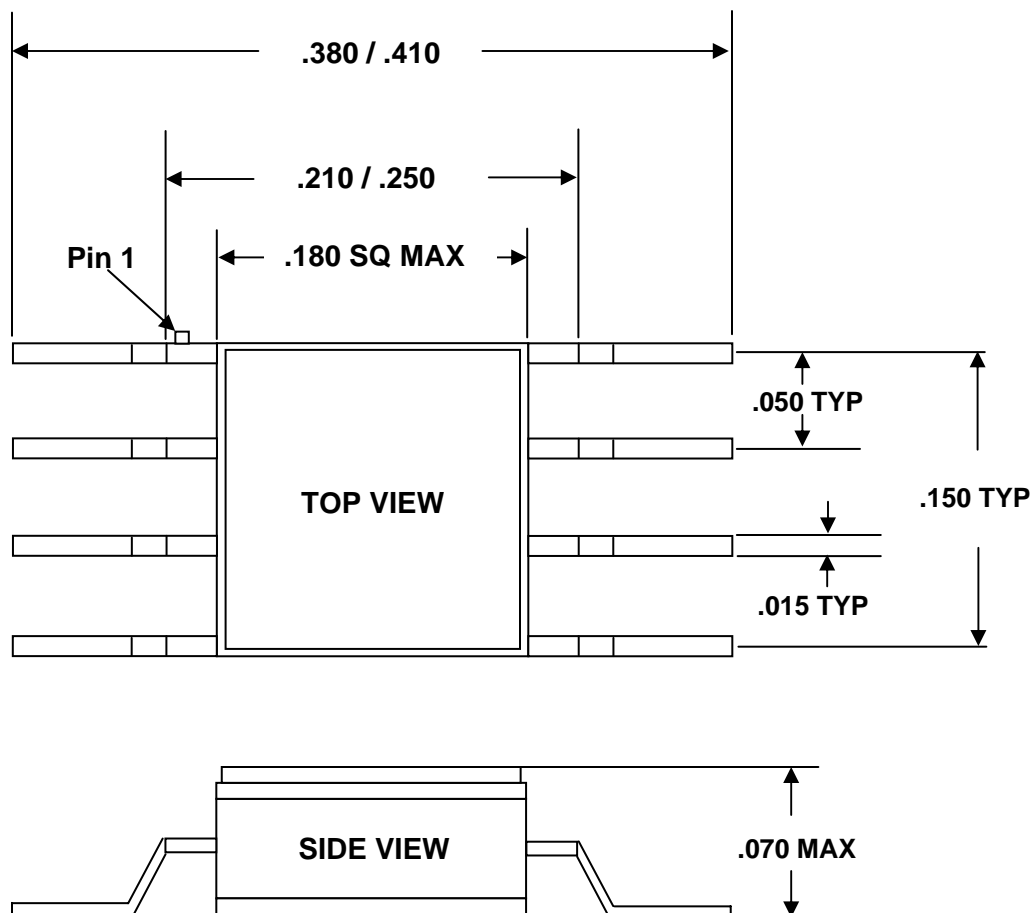


**Figure 9. Evaluation Board Schematic**

Peregrine specification 102-0202



**Figure 10. Package Drawing**  
8-lead CSOIC



**Table 4. Ordering Information**

Order Code	Part Marking	Description	Package	Shipping Method
9312-01	PE9312	PE9312-08CFPG-B Engineering Samples	Gullwing Glass Flatpack	50 / Tray
9312-11	PE9312	PE9312-08CFPG-B Production Units	Gullwing Glass Flatpack	50 / Tray
9312-00	PE9312-EK	PE9312 Evaluation Kit	Evaluation Kit	1 / Box

## Sales Offices

### *The Americas*

#### **Peregrine Semiconductor Corporation**

9380 Carroll Park Drive  
San Diego, CA 92121  
Tel: 858-731-9400  
Fax: 858-731-9499

### *Europe*

#### **Peregrine Semiconductor Europe**

Bâtiment Maine  
13-15 rue des Quatre Vents  
F-92380 Garches, France  
Tel: +33-1-4741-9173  
Fax : +33-1-4741-9173

### **Space and Defense Products**

#### *Americas:*

Tel: 858-731-9453

#### *Europe, Asia Pacific:*

180 Rue Jean de Guiramand  
13852 Aix-En-Provence Cedex 3, France  
Tel: +33-4-4239-3361  
Fax: +33-4-4239-7227

#### **Peregrine Semiconductor, Asia Pacific (APAC)**

Shanghai, 200040, P.R. China  
Tel: +86-21-5836-8276  
Fax: +86-21-5836-7652

#### **Peregrine Semiconductor, Korea**

#B-2607, Kolon Tripolis, 210  
Geumgok-dong, Bundang-gu, Seongnam-si  
Gyeonggi-do, 463-943 South Korea  
Tel: +82-31-728-3939  
Fax: +82-31-728-3940

#### **Peregrine Semiconductor K.K., Japan**

Teikoku Hotel Tower 10B-6  
1-1-1 Uchisaiwai-cho, Chiyoda-ku  
Tokyo 100-0011 Japan  
Tel: +81-3-3502-5211  
Fax: +81-3-3502-5213

For a list of representatives in your area, please refer to our Web site at: [www.psemi.com](http://www.psemi.com)

## Data Sheet Identification

### **Advance Information**

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

### **Preliminary Specification**

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

### **Product Specification**

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

The information in this data sheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this data sheet are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo, and UTSi are registered trademarks and UltraCMOS and HaRP are trademarks of Peregrine Semiconductor Corp.