

For full datasheet, please visit dtc.psemi.com.

Product Description

The PE64904 is a DuNE™-enhanced Digitally Tunable Capacitor (DTC) based on Peregrine's UltraCMOS[®] technology. DTC products provide a monolithically integrated impedance tuning solution for demanding RF applications.

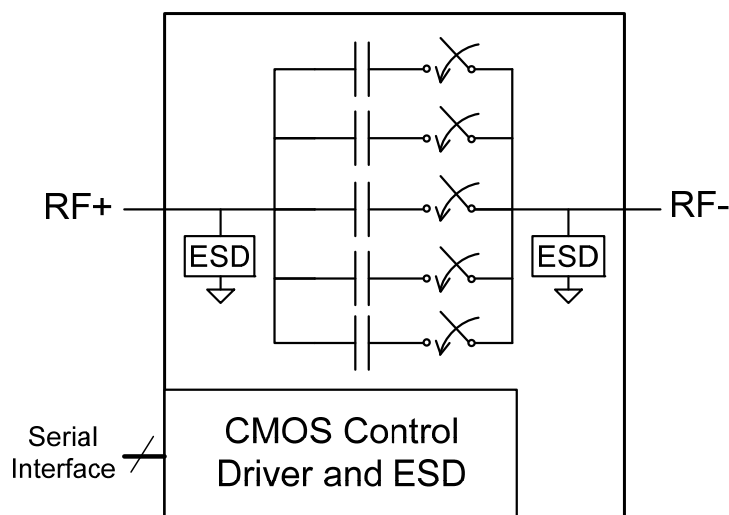
The PE64904 offers high RF power handling and ruggedness, while meeting challenging harmonic and linearity requirements.

This highly versatile product can be used in series or shunt configurations to support a wide variety of tuning circuit topologies.

The device is controlled through the widely supported 3-wire (SPI compatible) interface. All decoding and biasing is integrated on-chip and no external bypassing or filtering components are required.

Peregrine's DuNE™ technology enables excellent linearity and exceptional harmonic performance. DuNE devices deliver performance superior to GaAs devices with the economy and integration of conventional CMOS.

Figure 1. Functional Block Diagram



71-0066-01

Features

- 3-wire (SPI compatible) Serial Interface with built-in bias voltage generation and ESD protection
- DuNE™-enhanced UltraCMOS[®] device
- 5-bit 32-state Digitally Tunable Capacitor
- Series configuration C = 0.60 - 4.60 pF (7.7:1 tuning ratio) in discrete 129 fF steps
- Shunt configuration C = 1.14 - 5.10 pF (4.6:1 tuning ratio) in discrete 129 fF steps
- High RF Power Handling (up to 38 dBm, 30 V_{pk} RF) and High Linearity
- Wide power supply range (2.3 to 3.6V) and low current consumption (typ. 140 μA at 2.6V)
- Excellent 1.5 kV HBM ESD tolerance on all pins
- 2 x 2 x 0.45 mm QFN package
- Applications include:
 - Tunable Filter Networks
 - Tunable Antennas
 - RFID
 - Tunable Matching Networks
 - Phase Shifters
 - Wireless Communications

Figure 2. Package Type

10L 2 x 2 x 0.45 mm QFN package

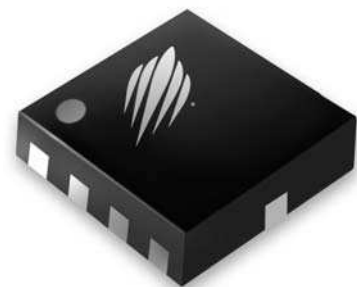


Table 1. Electrical Specifications @ 25°C, V_{DD} = 2.6V

| Parameter | Configuration | Condition | Min | Typ | Max | Unit |
|------------------------------------|---------------|--|------|-------|------|------|
| Operating Frequency Range | Both | | 100 | | 3000 | MHz |
| Minimum Capacitance | Series | State = 00000, 100 MHz (RF+ to RF-) | 0.49 | 0.60 | 0.71 | pF |
| | Shunt | State = 00000, 100 MHz (RF+ to Grounded RF-) | 0.99 | 1.10 | 1.21 | |
| Maximum Capacitance | Series | State = 11111, 100 MHz (RF+ to RF-) | 4.09 | 4.60 | 5.11 | pF |
| | Shunt | State = 11111, 100 MHz (RF+ to Grounded RF-) | 4.59 | 5.10 | 5.61 | |
| Parasitic Capacitance | Series | All States, 100 MHz (RF+ to GND, RF- to GND) | | 0.5 | | pF |
| Tuning Ratio | Series | 100 MHz | | 7.7:1 | | |
| | Shunt | 100 MHz | | 4.6:1 | | |
| Step Size | Both | 5 bits (32 states), constant step size (100 MHz) | | 0.129 | | pF |
| Equivalent Series Resistance | Series | State = 00000 | | 1.40 | | Ω |
| | | State = 11111 | | 1.33 | | |
| Quality Factor (C _{min}) | Shunt | 1GHz | | 35 | | |
| Quality Factor (C _{max}) | Shunt | 1GHz | | 25 | | |
| Harmonics (2fo) | Series | 100 MHz - 3 GHz | | | -36 | dBm |
| Harmonics (3fo) | | 100 MHz - 3 GHz | | | -36 | |

Figure 3. Pin Configuration (Top View)

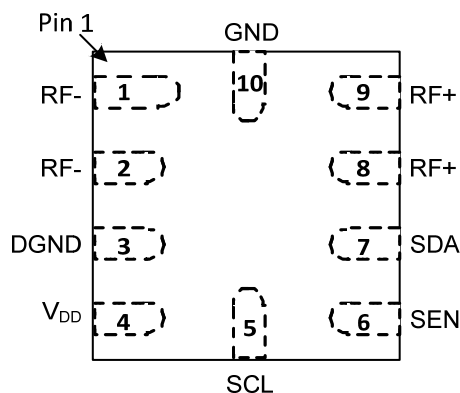


Table 2. Pin Descriptions

| Pin # | Pin Name | Description |
|-------|-----------------|-------------------------------------|
| 1 | RF- | Negative RF Port ¹ |
| 2 | RF- | Negative RF Port ¹ |
| 3 | DGND | Ground |
| 4 | V _{DD} | Power supply pin |
| 5 | SCL | Serial interface Clock input |
| 6 | SEN | Serial Interface Latch Enable Input |
| 7 | SDA | Serial interface Data input |
| 8 | RF+ | Positive RF Port ¹ |
| 9 | RF+ | Positive RF Port ¹ |
| 10 | GND | RF Ground |

Note: 1. Pins 1-2 and 8-9 must be tied together on PCB for optimal performance

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS[®] devices are immune to latch-up.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE64904 in the 10-lead 2 x 2 x 0.45 mm QFN package is MSL1.

Table 3. Operating Ranges

| Parameter | Min | Typ | Max | Units |
|--|-----|-----|----------|------------------------------------|
| V _{DD} Supply Voltage | 2.3 | 2.6 | 3.6 | V |
| I _{DD} Power Supply Current (V _{DD} = 2.6V) | | 140 | 200 | μA |
| V _{IH} Control Voltage High | 1.2 | 1.8 | 3.6 | V |
| V _{IL} Control Voltage Low | 0 | 0 | 0.57 | V |
| Peak Operating RF Voltage @ 100 MHz ¹ RF+ to RF- RF+ and/or RF- to Ground | | | 30 30 | V _{pk} V _{pk} |
| T _{OP} Operating Temperature Range | -40 | | +85 | °C |
| T _{ST} Storage Temperature Range | -65 | | +150 | °C |

Note: 1. De-rated over frequency

Table 4. Absolute Maximum Ratings

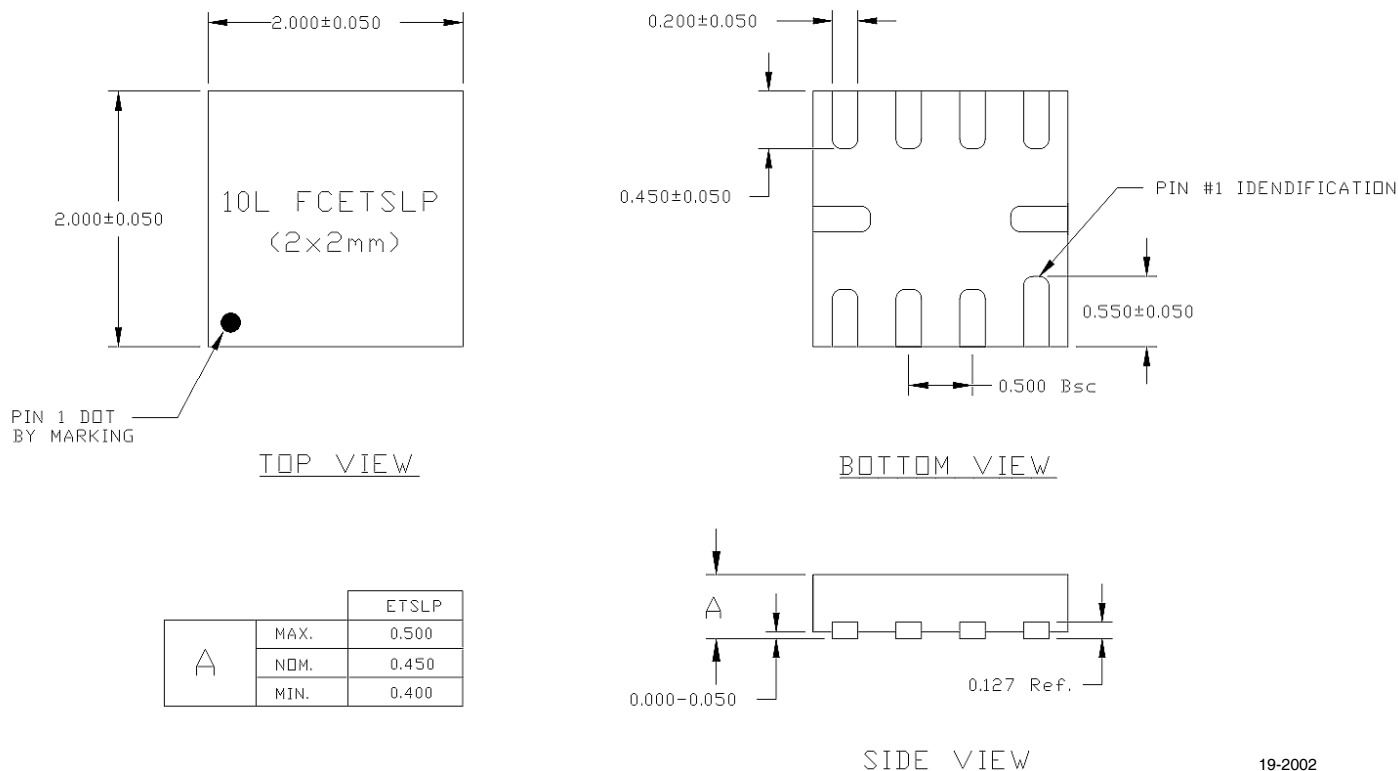
| Symbol | Parameter/Conditions | Min | Max | Units |
|------------------|--|------|------|-------|
| V _{DD} | Power supply voltage | -0.3 | 4.0 | V |
| V _I | Voltage on any DC input | -0.3 | 4.0 | V |
| V _{ESD} | ESD Voltage (HBM, MIL_STD 883 Method 3015.7) | | 1500 | V |

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

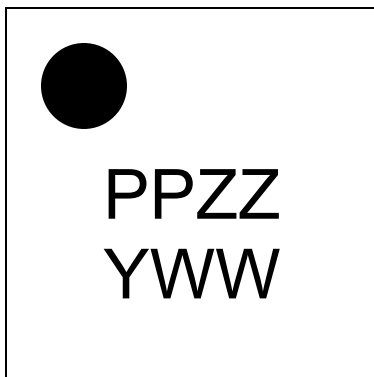
When handling this UltraCMOS[®] device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Figure 4. Package Drawing
10L 2 x 2 x 0.45 mm



19-2002

Figure 5. Marking Specifications

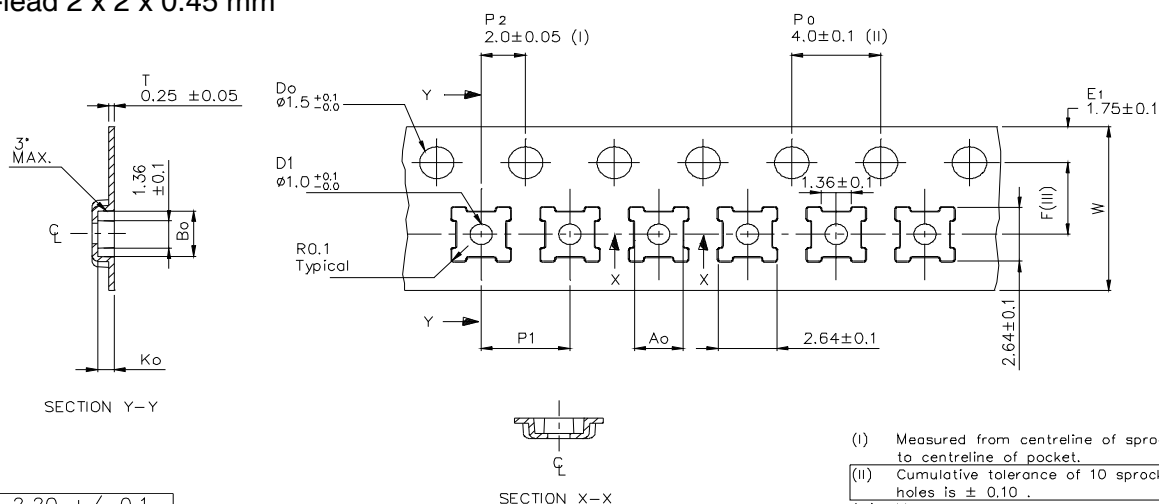


17-0112

| Marking Spec Symbol | Package Marking | Definition |
|---------------------|-----------------|--|
| PP | CG | Part number marking for PE64904 |
| ZZ | 00-99 | Last two digits of lot code |
| Y | 0-9 | Last digit of year, starting from 2009 (0 for 2010, 1 for 2011, etc) |
| WW | 01-53 | Work week |

Figure 24. Tape and Reel Specifications

10-lead 2 x 2 x 0.45 mm

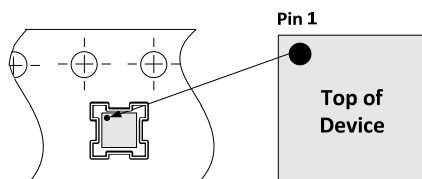


- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is ± 0.10 .
- (III) Measured from centreline of sprocket hole to centreline of pocket.
- (IV) Other material available.

This part shall not contain any banned substance as Sony standard SS-00259

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED.

-----> Tape Feed Direction ----->



Device Orientation in Tape

Table 9. Ordering Information

| Order Code | Package | Description | Shipping Method |
|----------------------------|-----------------------------|-------------------------------|-----------------|
| PE64904MLBA-Z ¹ | 10-lead QFN 2 x 2 x 0.45 mm | Package Part in Tape and Reel | 3000 units/T&R |
| PE64904MLBB-Z ¹ | 10-lead QFN 2 x 2 x 0.45 mm | Package Part in Tape and Reel | 3000 units/T&R |
| EK64904-12 | Evaluation Kit | Evaluation Kit | 1 Set/Box |

Note 1: Unisem (Malaysia) assembly house. Please contact factory for assembly house details.

Sales Contact and Information

For sales and contact information please visit www.psemi.com.

Advance Information: The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice. **Preliminary Specification:** The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product. **Product Specification:** The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

The information in this datasheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this datasheet are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo, UltraCMOS and UTSi are registered trademarks and HaRP, MultiSwitch and DuNE are trademarks of Peregrine Semiconductor Corp. All other trademarks mentioned herein are the property of their respective companies.