Peregrine Semiconductor

Product Brief

PE42674 Flip Chip

SP7T UltraCMOS™ WEDGE Switch 100 – 3000 MHz, +67 dBm IIP3

Figure 1. Functional Diagram

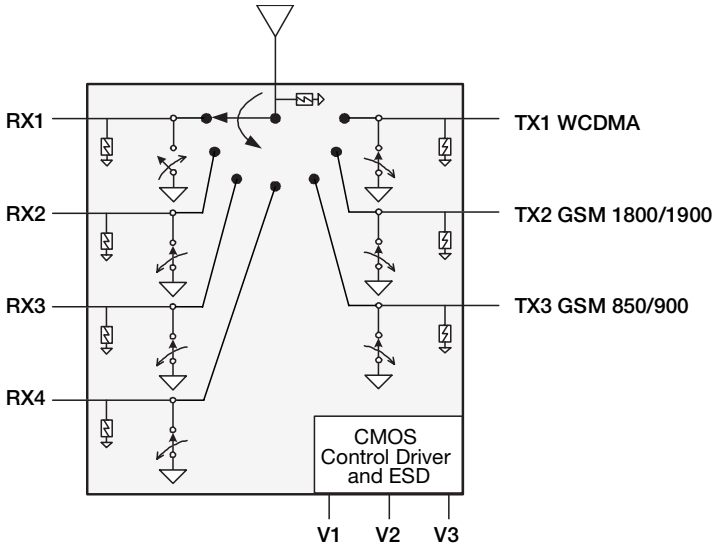


Figure 2. Die Top View

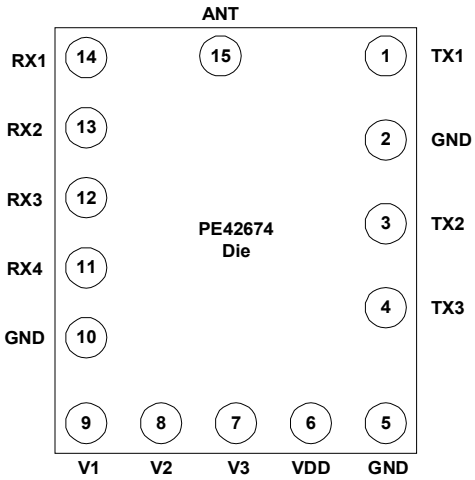
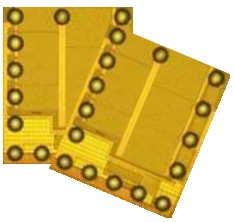


Figure 3. Package Type: Flip Chip



Features

- One WEDGE compliant port (TX1), two GSM/EDGE TX ports, four RX ports
- Three pin CMOS logic control with integral decoder/driver
- Exceptional harmonic performance: $2f_o$ = -85 dBc and $3f_o$ = -79 dBc
- Low TX insertion loss: 0.65 dB at 900 MHz, 0.75 dB at 1900 MHz
- TX – RX Isolation of 38.5 dB at 900 MHz, 31 dB at 1900 MHz
- 1500 V HBM ESD tolerance all ports
- +67 dBm IIP3
- -109 dBm IMD3
- No blocking capacitors required

Product Description

The PE42674 is a HaRP™-enhanced SP7T RF Switch developed on the UltraCMOS™ process technology. This Flip Chip is comprised of three TX and four RX ports and is intended for use in GSM/EDGE/PCS/DCS/ WCDMA handsets. An on-chip CMOS decode logic facilitates three-pin low voltage CMOS control. High ESD tolerance of 1500 V at all ports, no blocking capacitor requirements, and on-chip SAW filter over-voltage protection devices make this the ultimate in integration and ruggedness.

Peregrine's HaRP™ technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS™ process, providing performance superior to GaAs with the economy and integration of conventional CMOS.

Table 1. Target Electrical Specifications @ +25 °C, V_{DD} = 2.75 V

Parameter	Condition	Typ	Units
Insertion loss [1,2]	TX - Ant (850 / 900) TX - Ant (1800 / 1900) TX1 - Ant (1900 / 2200) RX - Ant (850 / 900) RX - Ant (1800 / 1900)	0.65 0.75 0.80 0.90 1.0	dB dB dB dB dB
Return Loss	Port under test in on state	20	dB
Isolation	TX - RX (850 / 900)[2] TX - RX (1800 / 1900)[2] TX - TX (850 / 900) TX - TX (1800 / 1900) TX1 - RX (1900 / 2100)[2] TX - TX1 (850 / 900)[2] TX - TX1 (1800 / 1900)[2]	38.5 31 30.5 25 30 30 25	dB dB dB dB dB dB dB
2nd Harmonic[3]	TX3 850 / 900 MHz, +35 dBm output power, 50 Ω TX2 1800 / 1900 MHz, +33 dBm output power, 50 Ω	-85 -84	dBc dBc
3rd Harmonic[3]	TX3 850 / 900 MHz, +35 dBm output power, 50 Ω TX2 1800 / 1900 MHz, +33 dBm output power, 50 Ω	-79 -76	dBc dBc
WCDMA Band I IMD3	TX1 – Measured in a 50 Ω system at 2.14 GHz at the TX1 port. Input signals are referenced to the ANT port with +20 dBm CW signal at 1.95 GHz and -15 dBm CW signal at 1.76 GHz	-109	dBm
WCDMA Band I IIP3	TX1 – Measured in a 50 Ω system at 2.14 GHz at the TX1 port. Input signals are referenced to the ANT port with +20 dBm CW signal at 1.95 GHz and -15 dBm CW signal at 1.76 GHz	+67	dBm
Switching time	50% of control to (10/90%) RF	2	µs

Notes: 1. The Device was matched with a 0.5pF cap on the ANT trace.
2. All port combinations may not meet typical performance. Limits will be established after device characterization.
3. Pulsed RF input duty cycle of 50% and 4620 µs, measured per 3GPP TS 45.005.

Table 2. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Units
Temperature range	T_{OP}	-40	25	+85	°C
V_{DD} Supply Voltage	V_{DD}	2.5	2.75	3.2	V
I_{DD} Power Supply Current (V_{DD} = 2.75 V)	I_{DD}		13	50	µA
TX input power[4] (VSWR ≤ 3:1) 824-915 MHz	P_{IN}			+35	dBm
TX input power[4] (VSWR ≤ 3:1) 1710-1910 MHz				+33	
RX input power[4] (VSWR =1:1)	P_{IN}			+20	dBm
Control Voltage High[5]	V_{IH}	1.4			V
Control Voltage Low[5]	V_{IL}			0.4	V

Notes: 4. Pulsed RF input duty cycle of 50% and 4620 µs, measured per 3GPP TS 45.005.
5. V_{IH} and V_{IL} values apply to a V_{DD} Supply Voltage range of 2.5-2.95 volts.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any DC input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	+150	°C
P_{IN}(50 Ω)	TX input power (50 Ω)[6,7] 824-915 MHz		+38	dBm
	TX input power (50 Ω)[6,7] 1710-1910 MHz		+36	
	RX input power (50 Ω)[6,7]		+23	
P_{IN} (∞:1)	TX input power (VSWR = (∞:1)[6,7] 824-915 MHz		+35	dBm
	TX input power (VSWR = (∞:1)[6,7] 1710-1910 MHz		+33	
V_{ESD}	ESD Voltage (HBM, MIL_STD 883 Method 3015.7)		1500	V

Notes: 6. Pulsed RF input duty cycle of 50% and 4620 µs, measured per 3GPP TS 45.005.
7. V_{DD} within operating range specified in Table 2.

Part performance is not guaranteed under these conditions. Exposure to absolute maximum conditions for extended periods of time may adversely affect reliability. Stresses in excess of absolute maximum ratings may cause permanent damage.

Table 4. Pin Descriptions

Pin No.	Pin Name	Description
1	TX1[9]	RF I/O - TX1
2	GND[8]	Ground
3	TX2[9]	RF I/O – TX2
4	TX3[9]	RF I/O – TX3
5	GND[8]	Ground
6	V_{DD}[10]	Supply
7	V3[10]	Switch control input, CMOS logic level
8	V2[10]	Switch control input, CMOS logic level
9	V1[10]	Switch control input, CMOS logic level
10	GND[8]	Ground
11	RX4[9]	RF I/O – RX4
12	RX3[9]	RF I/O – RX3
13	RX2[9]	RF I/O – RX2
14	RX1[9]	RF I/O – RX1
15	ANT[9]	RF Common – Antenna

Notes: 8. GND traces should be physically short and connected to ground plane for best performance.
9. Blocking capacitors needed only when non-zero DC voltage present.
10. Application must ensure at least 40 dB of voltage isolation from the RF signal.

Figure 4. Pad Configuration (Top View)

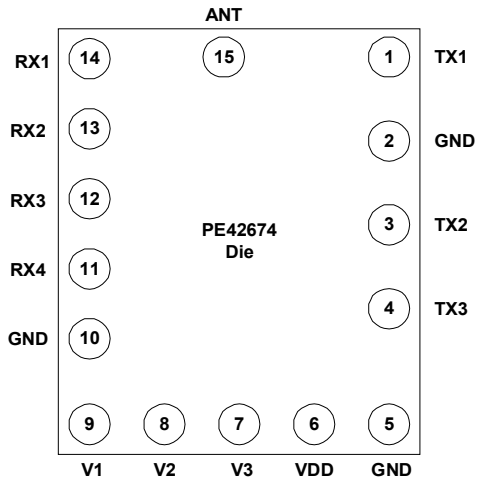


Table 5. Truth Table

Path	V3	V2	V1
RX1 - ANT	0	0	0
RX2 - ANT	0	0	1
RX3 - ANT	0	1	0
RX4 - ANT	0	1	1
TX1 - ANT	1	0	0
TX2 - ANT	1	0	1
TX3 - ANT	1	1	0
All Off	1	1	1

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 6. Ordering Information

Order Code	Description	Package	Shipping Method
PE42674DTI	PE42674-DIE-D	Bumped Wafer on Film Frame	Wafer (Gross Die / Wafer Quantity)
PE42674DBI	PE42674-DIE-304G	Die in Waffle Pack	304 Dice / Waffle Pack
EK-42674-01	PE42674-DIE-1H	Eval Kit	1/ box

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Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

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