

SP6T UltraCMOS™ 2.75 V Switch
100 – 3000 MHz

Figure 1. Functional Diagram

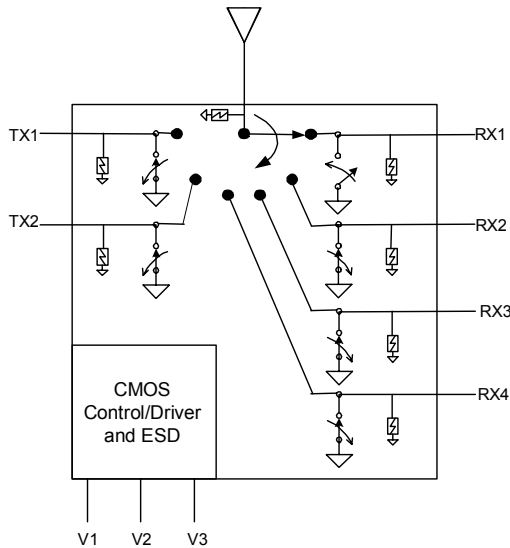
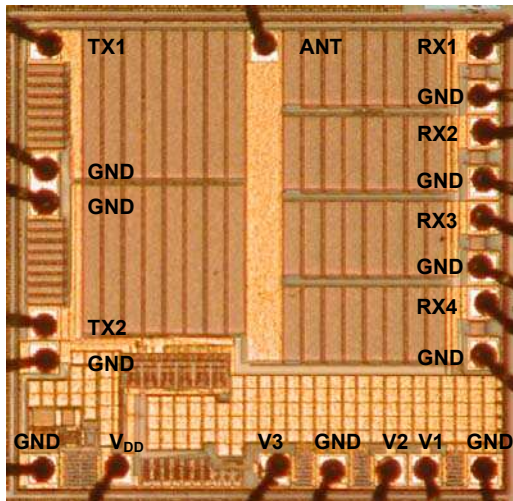


Figure 2. Die Top View



Features

- Three pin CMOS logic control with integral decoder/driver
- Exceptional harmonics performance: $2f_o = -85$ dBc and $3f_o = -83$ dBc
- Low TX insertion loss: 0.55 dB at 900 MHz, 0.65 dB at 1900 MHz
- TX – RX Isolation of 48 dB at 900 MHz, 40 dB at 1900 MHz
- 1500 V HBM ESD tolerance all ports
- 41 dBm P1dB
- No blocking capacitors required

Product Description

The PE42660 is a HaRP™-enhanced SP6T RF Switch developed on the UltraCMOS™ process technology. It addresses the specific design needs of the Quad-Band GSM Handset Antenna Switch Module Market. On-chip CMOS decode logic facilitates three-pin low voltage CMOS control, while high ESD tolerance of 1500 V at all ports, no blocking capacitor requirements, and on-chip SAW filter over-voltage protection devices make this the ultimate in integration and ruggedness.

Peregrine's HaRP™ technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS™ process, providing performance superior to GaAs with the economy and integration of conventional CMOS.

Table 1. Electrical Specifications @ +25 °C, V_{DD} = 2.75 V (Z_S = Z_L = 50 Ω)

Parameter	Conditions	Typical	Units
Operational Frequency		100-3000	MHz
Insertion Loss	ANT - TX - 850 / 900 MHz	0.55	dB
	ANT - TX - 1800 / 1900 MHz	0.65	dB
	ANT - RX - 850 / 900 MHz	0.90	dB
	ANT - RX - 1800 / 1900 MHz	1.00	dB
Isolation	TX - RX - 850 / 900 MHz	48	dB
	TX - RX - 1800 / 1900 MHz	40	dB
	TX - TX - 850 / 900 MHz	29	dB
	TX - TX - 1800 / 1900 MHz	25	dB
Return Loss	850 / 900 MHz	22	dB
	1800 / 1900 MHz	23	
2nd Harmonic ¹	35 dBm TX Input - 850 / 900 MHz	-85	dBc
	33 dBm TX Input - 1800 / 1900 MHz	-84	
3rd Harmonic ¹	35 dBm TX Input - 850 / 900 MHz	-83	dBc
	33 dBm TX Input - 1800 / 1900 MHz	-82	
Switching Time	(10-90%) (90-10%) RF	2	µs

Notes: 1. Pulsed RF input duty cycle of 50% and 4620 µs, measured per 3GPP TS 45.005

Table 2. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Units
Temperature range	T _{OP}	-40		+85	°C
V _{DD} Supply Voltage	V _{DD}	2.65	2.75	2.85	V
I _{DD} Power Supply Current (V _{DD} = 2.75 V)	I _{DD}		13	50	µA
TX input power ² (VSWR ≤ 3:1) 824-915 MHz	P _{IN}			+35	dBm
TX input power ² (VSWR ≤ 3:1) 1710-1910 MHz				+33	
RX input power ² (VSWR ≤ 1:1)	P _{IN}			+20	dBm
Control Voltage High	V _{IH}	0.7 x V _{DD}			V
Control Voltage Low	V _{IL}			0.3 x V _{DD}	V

Note: 2. Assumes RF input period of 4620 µs and duty cycle of 50%.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V _{DD}	Power supply voltage	-0.3	4.0	V
V _I	Voltage on any input	-0.3	V _{DD} + 0.3	V
T _{ST}	Storage temperature range	-65	+150	°C
P _{IN} (50 Ω)	TX input power (50 Ω) ^{3,4} 824-915 MHz		+38	dBm
	TX input power (50 Ω) ^{3,4} 1710-1910 MHz		+36	
	RX input power (50 Ω) ^{3,4}		+23	
P _{IN} (∞:1)	TX input power (VSWR = (∞:1) ^{3,4} 824-915 MHz		+35	dBm
	TX input power (VSWR = (∞:1) ^{3,4} 1710-1910 MHz		+33	
V _{ESD}	ESD Voltage (HBM, MIL_STD 883 Method 3015.7)		1500	V

Note: 3. Assumes RF input period of 4620 µs and duty cycle of 50%.

 4. V_{DD} within operating range specified in Table 2.

Part performance is not guaranteed under these conditions. Exposure to absolute maximum conditions for extended periods of time may adversely affect reliability. Stresses in excess of absolute maximum ratings may cause permanent damage.

Table 4. Pin Descriptions

Pin No.	Pin Name	Description
1	ANT ⁶	RF Common – Antenna
2	TX1 ⁶	RF I/O - TX1
3	GND ⁵	Ground (Requires two bond wires)
4	TX2 ⁶	RF I/O – TX2
5	GND ⁵	Ground
6	GND ⁵	Ground
7	V _{DD}	Supply
8	V3	Switch control input, CMOS logic level
9	GND ⁵	Ground
10	V2	Switch control input, CMOS logic level
11	V1	Switch control input, CMOS logic level
12	GND ⁵	Ground
13	GND ⁵	Ground
14	RX4 ⁶	RF I/O – RX4
15	GND ⁵	Ground
16	RX3 ⁶	RF I/O – RX3
17	GND ⁵	Ground
18	RX2 ⁶	RF I/O – RX2
19	GND ⁵	Ground
20	RX1 ⁶	RF I/O – RX1

Notes: 5. Bond wires should be physically short and connected to ground plane for best performance.

6. Blocking capacitors needed only when non-zero DC voltage present.

Figure 3. Pin Configuration (Top View)

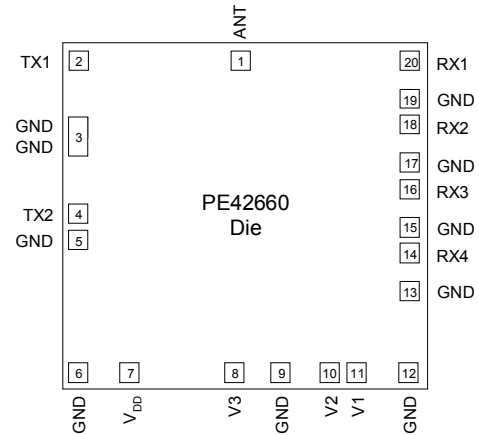


Table 5. Truth Table

Path	V3	V2	V1
ANT – RX1	0	0	0
ANT – RX2	0	0	1
ANT – RX3	0	1	0
ANT – RX4	0	1	1
ANT - TX1	1	0	x
ANT - TX2	1	1	x

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 6. Ordering Information

Order Code	Die ID	Description	Package	Shipping Method
42660-90	C9807_01	PE42660-DIE-D	Film Frame	Wafer (Gross Die / Wafer Quantity)
42660-99	C9807_01	PE42660-DIE-400G	Waffle Pack	400 Dice / Waffle Pack
42660-00	C9807_01	PE42660-DIE-1H	Evaluation Kit	1/ box

Sales Offices

The Americas

Peregrine Semiconductor Corporation

9450 Carroll Park Drive
San Diego, CA 92121
Tel: 858-731-9400
Fax: 858-731-9499

Europe

Peregrine Semiconductor Europe

Bâtiment Maine
13-15 rue des Quatre Vents
F-92380 Garches, France
Tel: +33-1-47-41-91-73
Fax : +33-1-47-41-91-73

Space and Defense Products

Americas:

Tel: 858-731-9453

Europe, Asia Pacific:

180 Rue Jean de Guiramand
13852 Aix-En-Provence Cedex 3, France
Tel: +33(0) 4 4239 3361
Fax: +33(0) 4 4239 7227

North Asia Pacific

Peregrine Semiconductor K.K.

Teikoku Hotel Tower 10B-6
1-1-1 Uchisaiwai-cho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

Peregrine Semiconductor, Korea

#B-2402, Kolon Tripolis, #210
Geumgok-dong, Bundang-gu, Seongnam-si
Gyeonggi-do, 463-480 S. Korea
Tel: +82-31-728-4300
Fax: +82-31-728-4305

South Asia Pacific

Peregrine Semiconductor, China

Shanghai, 200040, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

For a list of representatives in your area, please refer to our Web site at: www.psemi.com

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