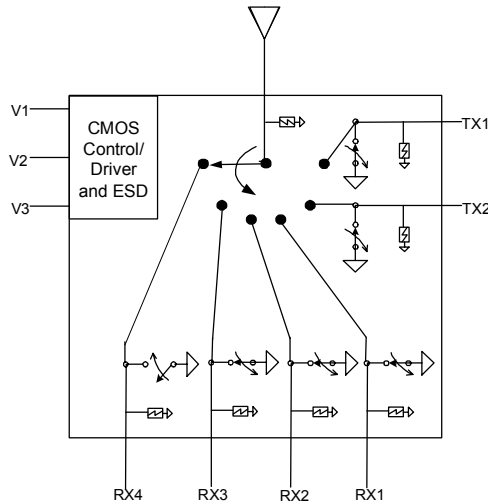


SP6T UltraCMOS™ 2.70 V Switch
100 – 3000 MHz, 50 Ω

Figure 1. Functional Diagram



Features

- Three pin CMOS logic control with integral decoder/driver
- Low TX insertion loss: 0.55 dB at 900 MHz, 0.60 dB at 1900 MHz
- TX – RX Isolation of 38 dB at 900 MHz, 31 dB at 1900 MHz
- Low harmonics: $2f_o = -90$ dBc and $3f_o = -82$ dBc
- 1500 V HBM ESD tolerance all ports
- 41 dBm P1dB, TX paths
- No blocking capacitors required
- RoHS compliant lead-free solder balls

Figure 2. Die Top View

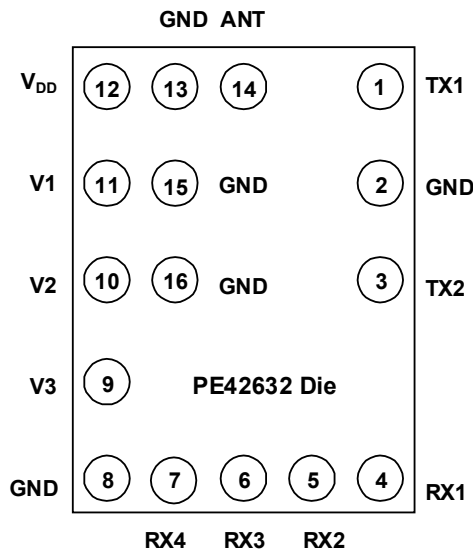
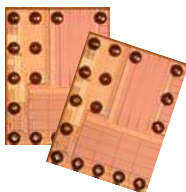


Figure 3. Package Type: Flip Chip



Product Description

The PE42632 is a HaRP™-enhanced SP6T RF Switch developed on the UltraCMOS™ process technology. This 50 Ω switch addresses the specific design needs of the Quad-Band GSM Handset Antenna Switch Module Market. On-chip CMOS decode logic facilitates three-pin low voltage CMOS control. High ESD tolerance of 1500 V at all ports, no blocking capacitor requirements and on-chip SAW filter over-voltage protection devices make this the ultimate in integration and ruggedness.

Peregrine's HaRP™ technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS™ process, providing performance superior to GaAs with the economy and integration of conventional CMOS.

Table 1. Electrical Specifications @ +25 °C, V_{DD} = 2.5 - 2.8 V (Z_S = Z_L = 50 Ω)

| Parameter | Conditions | Typical | Units |
|-----------------------------|-----------------------------------|----------|-------|
| Operational Frequency | | 100-3000 | MHz |
| Insertion Loss ¹ | ANT - TX - 850 / 900 MHz | 0.55 | dB |
| | ANT - TX - 1800 / 1900 MHz | 0.6 | dB |
| | ANT - RX - 850 / 900 MHz | 0.9 | dB |
| | ANT - RX - 1800 / 1900 MHz | 1.15 | dB |
| Isolation | TX - RX - 850 / 900 MHz | 38 | dB |
| | TX - RX - 1800 / 1900 MHz | 31 | dB |
| | TX - TX - 850 / 900 MHz | 31 | dB |
| | TX - TX - 1800 / 1900 MHz | 26 | dB |
| Return Loss | 850 / 900 MHz | 23 | dB |
| | 1800 / 1900 MHz | 22 | dB |
| 2nd Harmonic ^{2,3} | 35 dBm TX Input - 850 / 900 MHz | -90 | dBc |
| | 33 dBm TX Input - 1800 / 1900 MHz | -89 | dBc |
| 3rd Harmonic ^{2,3} | 35 dBm TX Input - 850 / 900 MHz | -82 | dBc |
| | 33 dBm TX Input - 1800 / 1900 MHz | -80 | dBc |
| Switching Time ⁴ | 50% Control Logic to 90% RF | 1 | µs |

- Notes:
1. Insertion loss specified with optimal ANT impedance matching.
 2. Measured in Pulsed Wave Mode.
 3. Assumes RF input duty cycle of 50% and 4620 µs, measured per 3GPP TS 45.005
 4. Power on any port must not exceed +20 dBm during switching event.

Table 2. Operating Ranges

| Parameter | Symbol | Min | Typ | Max | Units |
|---|-----------------|-----------------------|------|-----------------------|-------|
| Temperature range | T _{OP} | -40 | | +85 | °C |
| V _{DD} Supply Voltage | V _{DD} | 2.5 | 2.70 | 2.8 | V |
| I _{DD} Power Supply Current (V _{DD} = 2.75 V) | I _{DD} | | 13 | 20 | µA |
| TX input power ⁵ (VSWR ≤ 3:1) 824-915 MHz | P _{IN} | | | +35 | dBm |
| TX input power ⁵ (VSWR ≤ 3:1) 1710-1910 MHz | | | | +33 | |
| RX input power ⁵ (VSWR = 1:1) | P _{IN} | | | +20 | dBm |
| Control Voltage High | V _{IH} | 0.7 x V _{DD} | | | V |
| Control Voltage Low | V _{IL} | | | 0.3 x V _{DD} | V |

- Note:
5. Assumes RF input period of 4620 µs and duty cycle of 50%.

Table 3. Absolute Maximum Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|------------------------|---|------|----------------------|-------|
| V _{DD} | Power supply voltage | -0.3 | 4.0 | V |
| V _I | Voltage on any DC input | -0.3 | V _{DD} +0.3 | V |
| T _{ST} | Storage temperature range | -65 | +150 | °C |
| T _{OP} | Operating temperature range | -40 | +85 | °C |
| P _{IN} (50 Ω) | TX input power (50 Ω) ^{6,7} 824-915 MHz | | +38 | dBm |
| | TX input power (50 Ω) ^{6,7} 1710-1910 MHz | | +36 | |
| | RX input power (50 Ω) ⁷ | | +23 | |
| P _{IN} (∞ :1) | TX input power (VSWR = (∞ :1) ^{6,7} 824-915 MHz | | +35 | dBm |
| | TX input power (VSWR = (∞ :1) ^{6,7} 1710-1910 MHz | | +33 | dBm |
| V _{ESD} | ESD Voltage (HBM, MIL_STD 883 Method 3015.7) | | 1500 | V |
| | ESD Voltage (MM, JEDEC, JESD22-A114-B) | | 100 | V |

- Notes:
6. Assumes RF input period of 4620 µs and duty cycle of 50%.
 7. V_{DD} within operating range specified in Table 2.

Part performance is not guaranteed under these conditions. Exposure to absolute maximum conditions for extended periods of time may adversely affect reliability. Stresses in excess of absolute maximum ratings may cause permanent damage.

Table 4. Pin Descriptions

| Pin No. | Pin Name | Description |
|---------|------------------|--|
| 1 | TX1 ⁸ | RF I/O – TX1 |
| 2 | GND | TX Ground |
| 3 | TX2 ⁸ | RF I/O – TX2 |
| 4 | RX1 ⁸ | RF I/O – RX1 |
| 5 | RX2 ⁸ | RF I/O – RX2 |
| 6 | RX3 ⁸ | RF I/O – RX3 |
| 7 | RX4 ⁸ | RF I/O – RX4 |
| 8 | GND | RX Ground |
| 9 | V3 | Switch control input, CMOS logic level |
| 10 | V2 | Switch control input, CMOS logic level |
| 11 | V1 | Switch control input, CMOS logic level |
| 12 | V _{DD} | Supply |
| 13 | GND | DC Ground |
| 14 | ANT ⁸ | RF Common - Antenna |
| 15 | GND | DC Ground |
| 16 | GND | DC Ground |

Note: 8. Blocking capacitors needed only when non-zero DC voltage present

Figure 4. Pad Configuration (Top View)

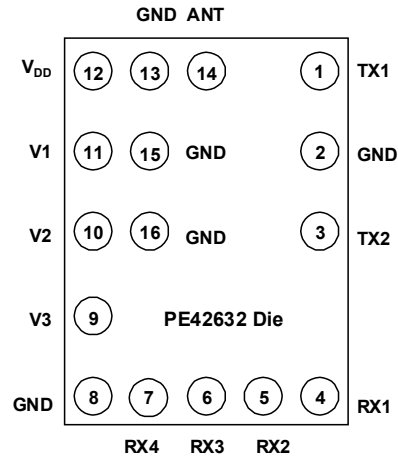


Table 5. Truth Table

| Path | V3 | V2 | V1 |
|-----------|----|----|----|
| ANT - TX1 | 0 | 1 | 1 |
| ANT - TX2 | 0 | 0 | 1 |
| ANT - RX1 | 1 | 1 | 0 |
| ANT - RX2 | 0 | 1 | 0 |
| ANT - RX3 | 1 | 0 | 0 |
| ANT - RX4 | 0 | 0 | 0 |

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 6. Ordering Information

| Order Code | Description | Package | Shipping Method |
|-------------|------------------|----------------------------|------------------------------------|
| PE42632DTI | PE42632-DIE-D | Bumped Wafer on Film Frame | Wafer (Gross Die / Wafer Quantity) |
| PE42632DBI | PE42632-DIE-400G | Die in Waffle Pack | 400 Dice / Waffle Pack |
| EK-42632-01 | PE42632-DIE-1H | Evaluation Kit | 1/ box |

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For a list of representatives in your area, please refer to our Web site at: www.psemi.com

Data Sheet Identification

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Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

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