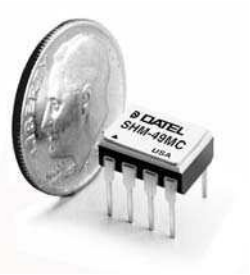
SHM-49

Miniature, High-Speed, Complete ±0.05% Sample Hold Amplifiers

New SMT Package

FEATURES

- Small 8-pin DIP or SMT package
- 200ns max. acquisition time to ±0.01%
- 100ns max. sample-to-hold settling time to ±0.01%
- 16MHz small signal bandwidth
- 74dB feedthrough attenuation
- ±25 picoseconds aperture uncertainty
- 415mW maximum power dissipation



GENERAL DESCRIPTION

DATEL's SHM-49 is a high-speed, highly accurate sample/hold designed for precision, high-speed analog signal processing applications. The SHM-49 features excellent dynamic specifications including a maximum acquisition time of only 200 nanoseconds for a 10V step to ±0.01%.

Sample-to-hold settling time, to ±0.01% accuracy, is 100 nanoseconds maximum with an aperture uncertainty of ±2 picoseconds.

The SHM-49 is a complete sample/hold circuit, containing a precision MOS hold capacitor and a MOSFET switching configuration which results in faster switching and better feedthrough attenuation. Additionally, a FET input amplifier design allows faster acquisition and settling times while maintaining a considerably lower droop rate.

INPUT/OUTPUT CONNECTIONS

Pin	Function
1	+5v Digital Supply
2	S/H Control
3	Analog Input
4	Analog Return
5	–15v Supply
6	Analog Output
7	+15v Analog Supply
8	Power Ground

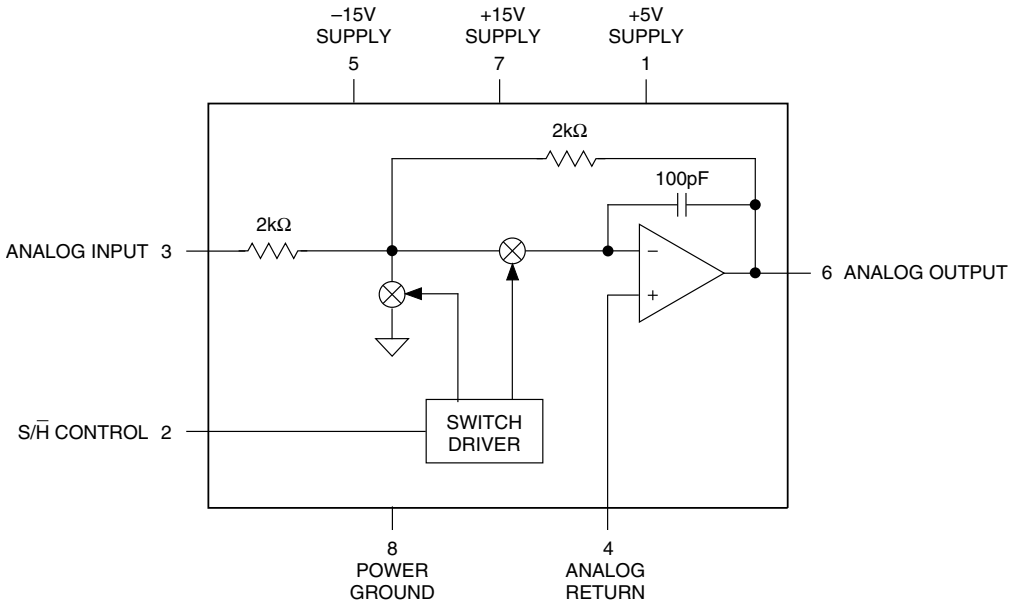


Figure 1. Functional Block Diagram

Absolute Maximum Ratings

±15V Supply Voltages	±18V
+5V Supply Voltages	–0.5V to +7V
Analog Input	±18V
Digital Input	–0.5V to +5.5V
Output Current	±65 mA

Functional Specifications

(Apply over the operating temperature range with ±15V and +5V supplies unless otherwise specified.)

ANALOG INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range				
±15V Nominal Supply	±10	±11.5	—	Volts
±12V Nominal Supply	±7	±8.5	—	Volts
Input Impedance	—	1000	—	Ω
Output Current	—	—	±65	mA
Output Impedance	—	0.1	—	Ω
Capacitive Load	100	250	—	pF
DIGITAL INPUT				
Input Logic Levels				
Logic 1	+2.0	—	+5.0	Volts
Logic 0	0	—	+0.8	Volts
Loading				
Logic 1	—	—	+5	µA
Logic 0	—	—	–5	µA
TRANSFER CHARACTERISTICS				
Gain	—	–1	—	V/V
Gain Error, +25°C	—	±0.05	±0.5	%
Linearity Error ①	—	±0.005	±0.01	%FS
Sample Mode Offset , +25°C	—	±2	7	mV
Sample-to-Hold Offset (Pedestal), +25°C ②	—	±2.5	±25	mV
Gain Drift	—	±0.5	±15	ppm/°C
Sample Mode Offset Drift ①	—	±3	±15	ppm of FSR/°C
Sample-to-Hold Off. (Pedestal) Drift	—	±5	±20	ppm of FSR/°C
DYNAMIC CHARACTERISTICS				
Acquisition Time				
10V to ±0.01%FS (±1 mV)				
+25°C	—	160	200	ns
–55 to +125°C	—	—	265	ns
10V to ±0.1%FS (±10 mV)				
+25°C	—	100	150	ns
–55 to +125°C	—	—	215	ns
10V to ±0.01%FS (±100 mV)	—	90	—	ns
1V to ±1%FS (±10 mV)	—	75	—	ns
Sample-to-Hold Settling Time				
10V to ±1%FS (±100 mV)	—	60	100	ns
1V to ±0.01%FS (±10 mV)	—	40	80	ns
Sample-to-Hold Transient	—	100	—	mVp-p
Aperture Delay Time	—	10	15	ns
Aperture Uncertainty (Jitter)	—	±25	±50	ps
Output Slew Rate	±200	±300	—	V/µs
Small Signal BW (–3dB)	10	16	—	MHz
Output Droop				
+25°C	—	±0.5	±15	µV/µs
0 to +70°C	—	±15	±30	µV/µs
–55 to +125°C	—	±1.2	±2.4	mV/µs
Feedthrough Rejection	69	74	—	dB

POWER REQUIREMENTS	MIN.	TYP.	MAX.	UNITS
Voltage Range				
+15V Supply	+11.5	+15.0	+15.5	Volts
–15V Supply	–11.5	–15.0	–15.5	Volts
+5V Supply	+4.75	+5.0	+5.25	Volts
Power Supply Rejection Ratio	—	±0.5	±1	mV/V
Quiescent Current Drain				
+15V Analog Supply	—	+12	+13.5	mA
–15V Supply	—	–12	–13.5	mA
+5V Supply	—	+1	–1.5	Volts
Power Consumption	—	365	415	mW
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range, Case				
SHM-49MC/GC	0 to +70°C			
SHM-49MM/GM	–55 to +125°C			
Storage Temperature Range	–65 to +150°C			
Thermal Impedance				
θjc	15°C/W			
θca	35°C/W			
Package Type	8-pin ceramic DIP (MC/MM) or SMT (GC/GM)			

Footnotes:

① Full Scale (FS) = 10V. Full Scale Range (FSR) = 20V.

② Sample-to-hold offset error (pedestal) is constant regardless of input/output level.

Ordering Information

MODEL	OPERATING TEMP. RANGE
SHM-49MC	0 to +70°C
SHM-49MM	–55 to +125°C
SHM-49GC	0 to 70°C
SHM-49GM	–55 to 125°C

For availability of high-reliability versions of the SHM-49, contact DATEL.

TECHNICAL NOTES

1. All ground pins should be tied together and connected to system analog ground as close to the package as possible. It is recommended to use a ground plane under the device and solder ground pins directly to it. Take care to ensure that no ground potentials can exist between ground pins.
2. External 0.1µF to 4.7µF tantalum bypass capacitors are required in critical applications.
3. A logic 1 on S/H puts the unit in the sample mode. A logic 0 puts the unit in hold mode.
4. The maximum capacitive load to avoid oscillation is typically 250pF. Recommended resistive load is 500Ω, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω and capacitive loads up to 50pF. Greater load capacitances will affect both acquisition and settling time.
5. Gain and offset adjusting can be accomplished using the external circuitry shown in Figure 2. Adjust offset with a 0V input. Adjust gain with a ±FS input. Adjust so that the output in the hold mode matches the input.

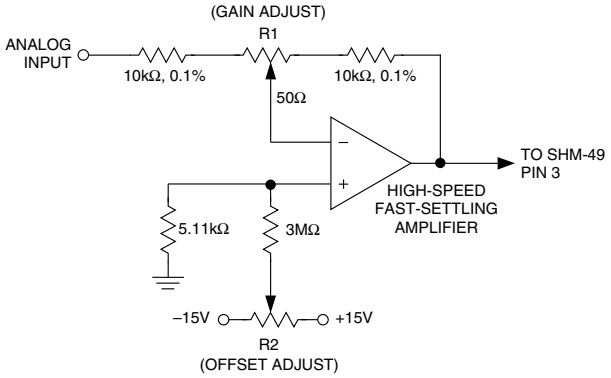
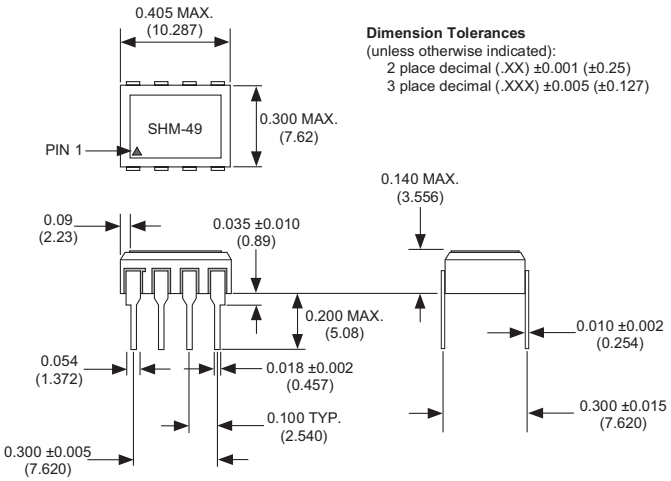


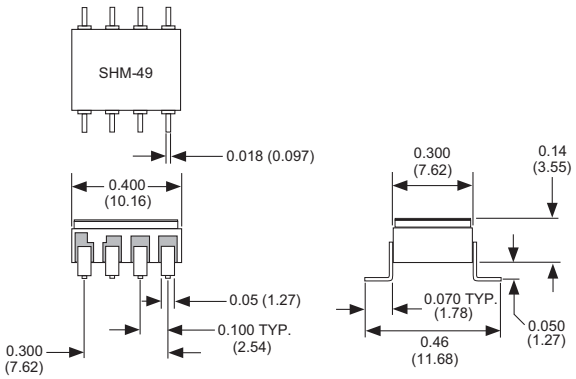
Figure 2. Offset and Gain Adjustments

MECHANICAL DIMENSIONS Inches (mm)

DIP Package



SMT Package



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