

# ADS-325 A 10-Bit, 20MHz Sampling A/D Converter

#### **FEATURES**

- 10-bit, 20MHz sampling
- ±1LSB max. differential nonlinearity
- · Internal calibration circuit
- · Internal S/H amplifier
- · 70MHz input bandwidth
- TTL/CMOS compatible in-out logic
- · Latched three-state output data
- Single +5V supply
- · Low 150mW power dissipation
- Small 48 pin LQFP package
- Low cost

## **GENERAL DESCRIPTION**

DATEL's ADS-325A is a low power, 10-bit, 20MHz, CMOS sampling A/D converter. Its small 48 pin plastic LQFP package contains a S/H amplifier, a 3-state output register, linearity calibration circuitry, and all necessary control logic. Only two external reference voltages, an A/D clock and a few digital inputs are required. The A/D clock may be applied with 50% duty cycle.

The excellent dynamic performance includes a spurious free dynamic range of 65dB and a signal-to-noise ratio with distortion of 54dB with a 3MHz input. ADS-325A is capable of operating from a single +5V power supply and typically consumes only 150mW. It can also operate from a +5V analog Vs with +3.3V digital Vs enabling an interface with 3.3V logic circuitry. The ADS-325A is ideally suited for high quality video/CCD imaging applications.



## INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 10 (LSB)	48	DIGITAL GROUND (DGND)
2	BIT 9	47	NO CONNECTION
3	BIT 8	46	NO CONNECTION
4	BIT 7	45	+DV <sub>S</sub> (Digital)
5	BIT 6	44	ANALOG GROUND (AGND)
6	DIGITAL GROUND (DGND)	43	ANALOG GROUND (AGND)
7	+DV <sub>S</sub> (Digital)	42	TEST SIGNAL IN
8	BIT 5	41	CALIBRATION (CAL)
9	BIT 4	40	NO CONNECTION
10	BIT 3	39	ANALOG INPUT (VIN)
11	BIT 2	38	TEST SIGNAL OUT
12	BIT 1 (MSB)	37	TEST SIGNAL IN
13	TEST PIN	36	ANALOG GROUND (AGND)
14	TEST SIGNAL IN	35	REFERENCE BOTTOM (VRB)
15	RESET	34	REFERENCE BOTTOM (VRB)
16	DIGITAL GROUND (DGND)	33	NO CONNECTION
17	SELECT (SEL)	32	NO CONNECTION
18	+AVS (Analog)	31	NO CONNECTION
19	TEST MODE	30	REFERENCE TOP (VRT)
20	LINV	29	REFERENCE TOP (VRT)
21	MINV	28	ANALOG GROUND (AGND)
22	A/D CLOCK	27	ANALOG GROUND (AGND)
23	OUTPUT ENABLE (OE)	26	+AVs (Analog)
24	CHIP ENABLE (CE)	25	+AVS (Analog)

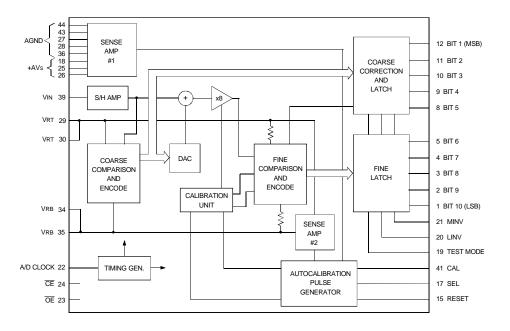


Figure 1. ADS-325A Functional Block Diagram



## **ABSOLUTE MAXIMUM RATINGS** (TA = +25°C)

PARAMETERS	LIMITS	UNITS	
Supply Voltages (+AV <sub>S</sub> and +DV <sub>S</sub> )	0 to +7	Volts	
Reference Voltage (VRT and VRB)	$-0.5$ to $+AV_S + 0.5$	Volts	
Input Voltage, Analog (VIN)	$-0.5$ to $+AV_S + 0.5$	Volts	
Input Voltage, Digital (VIH and VIL)	$-0.5$ to $+AV_S + 0.5$	Volts	
Output Voltage, Digital (V <sub>OH</sub> and V <sub>OL</sub> )	$-0.5$ to $+DV_S +0.5$	Volts	

## **FUNCTIONAL SPECIFICATIONS**

(Typical at  $f_S$  = 20MHz, +AV<sub>S</sub> = +5V, +DV<sub>S</sub> = +3.3V, V<sub>RB</sub> = +2.0V, V<sub>RT</sub> = +4.0V, and T<sub>A</sub> = +25°C unless otherwise specified.)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range, VIN		+2 to +4		Volts
Input Current VIN = +4V	_	40	50	μA
VIN = +2V Capacitance, CIN	-50 	-40 9	_	μA pF
Bandwidth (-1dB)	_	70	_	MHz
REFERENCE	•	•	•	
Reference Input Voltage			4.0	M. II.
VRT VRB	+1.8	+4 +2	+4.6 —	Volts Volts
Input Current	_	_		
IRT IRB	5 –11	7 -7	11 -5	mA mA
Offset Voltage		-		
VRT VRB	+40 -120	+90 -70	+140 -20	mV mV
Resistance (VRT – VRB)	180	280	380	Ω
DIGITAL INPUTS				
Input Voltage	2.2			V 11
VIH, Logic "1" VIL, Logic "0"	+2.3	_	+0.8	Volts Volts
Input Current				
IIH, Logic Loading "1" ① IIL, Logic Loading "0" ②	_	_	5 5	μA μA
A/D Clock Pulse Width				·
TPW1 TPW0	25 25	_	_	ns ns
DIGITAL OUTPUTS				
Output Logic Current				
Iон, Logic "1" ③ IoL, Logic "0" ④	-3.5 3.5	_	_	mA mA
Leak Current at OE = "1" (5)	_	_	1	μA
3-State Enable Time, TPZE 6 3-State Disable Time, TPEZ 7	10 20	15 25	20 30	ns ns
Data Delay, TDL (CL = 20pF)	8	13	18	ns
PERFORMANCE	•	•		
Resolution	10	_	_	Bits
Max. Throughput Rate ® Min. Throughput Rate ®	20 —	_	— 0.5	MHz MHz
Integral Linearity Error	_	±1.3	±2	LSB
Differential Linearity Error Differential Gain Error	_	±0.5 1.0	±1 —	LSB %
Differential Phase Error ®	_	0.3	_	Degrees
Aperture Delay, Tsd SNR & Distortion	2	4	6	ns
fin = 100kHz	_	53	_	dB
fin = 500kHz fin = 1MHz	_	52 53	_	dB dB
fin = 3MHz	_	54	_	dB
fin = 7MHz fin = 10MHz	_	47 45	_ _	dB dB
= 1011112		.0		45

PERFORMANCE (CONT.)	MIN.	TYP.	MAX.	UNITS
Spurious Free Dynamic Range fin = 100kHz fin = 500kHz fin = 1MHz fin = 3MHz fin = 7MHz fin = 10MHz	_ _ _ _ _	60 59 60 65 50 49	  -  -  -	dB dB dB dB dB
POWER REQUIREMENTS				
Power Supply Voltage +AVs +DVs 1DGND - AGND   Supply Current Analog, +Als Digital, +Dls Standby Current (CE = "1") Analog, +Als Digital, +Dls Power Dissipation	+4.75 +3.0 — 20 — — —	+5.0 — 27 3 — — 150	+5.25 +5.25 100 34 5 1	Volts Volts mV mA mA mA µA mW
PHYSICAL/ENVIRONMENTAL	•			
Operating Temperature Range Storage Temperature Range Weight Package	-20 -55	— 0.2 gr 48-pin plas		ပို

#### Footnotes:

- ①  $+DV_S = Max., V_{IH} = +DV_S$
- ② +DVs = Max., V<sub>IL</sub> = 0V
- $\overline{OE}$  = AGND, +DVs = Min., VOH = +DVs-0.5V
- OE = AGND, +DVs = Min., Vol = 0.4V
- ⑤  $\overline{OE}$  = +AVs, +DVs = Max., VoH = +DVs, and VoL = 0V
- $\ensuremath{\texttt{\textcircled{6}}}$  Hi-Z to Active, asynchronous with clock.
- ② Active to Hi-Z, asynchronous with clock.
- 8 Fin = 1kHz
- NTSC 401RE mod. ramp, fc = 14.3MHz

## **TECHNICAL NOTES**

- 1. **Caution to ESD:** Since the ADS-325A is a CMOS device, precautions against static electricity should be taken.
- 2. +AVs and +DVs: While the unit has separate pins for both the analog supply (+AVs) and the digital supply (+DVs), a time skew between supplying (or removing) both +AVs and +DVs may cause a latch-up problem. DATEL recommends using a common power supply for both +AVs and +DVs to avoid latch-up conditions. It is possible to use +3.3V for +DVs along with +5V for +AVs. Compared to the singe +5V supply application, there will be no significant difference in performance. However, special care should be taken to minimize the time skew between +AVs and +DVs when turning on/off.
- 3. PC board layout: To obtain fully specified performance careful attention to PC board layout is required. Place large ground planes on the board and connect both analog and digital grounds at one point right beneath the converter. In the case where the grounds are tied at a location distant from the converter, the voltage difference between the grounds must be within 100mV. Tie all ground pins directly to the appropriate ground plane beneath the converter. Bypass +AVs and +DVs pins to ground using 10μF tantalum capacitors in parallel with 0.1μF ceramic capacitors at locations as close to the unit as possible.
- Reference Input: Two external voltage references are required for the two reference inputs VRT (pin 29, 30) and VRB (pin 34, 35). Typically, these are +4V for VRT and +2V



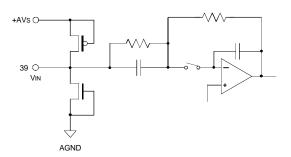
for VRB, which give an analog input range of +2V to +4V. The reference voltages must be within the following limitations:

$$+AVS - 0.4V > = VRT > VRB >= +1.8V$$
, and  $VRT - VRB > = 1.8V$ 

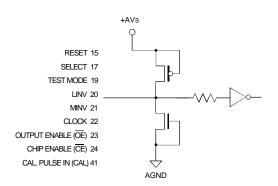
Stability of the reference will directly affect the accuracy of the A/D conversion. In this sense, the reference sources must be capable of driving more than 10mA. Also, the VRT and VRB pins should be bypassed to analog ground with 0.1µF ceramic capacitors placed as close to the pins as possible.

- Analog Input: ADS-325A has a broad input bandwidth of 70MHz (@-1dB) with only 9pF of input capacitance at its analog input. The analog input should be driven by a high speed buffer amplifier with sufficient current drive.
- Digital Inputs: All digital input pins including A/D clock input are CMOS compatible. Each of these pins has an internal overvoltage protection circuit with diodes as shown in Figure 2 (Equivalent circuit diagrams).
- Control Logic Inputs: ADS-325A has several control logic input pins. Functions of these pins are described in the following:

TEST MODE (pin 19), MINV (pin 21), LINV (pin 20) These three pins select the output data format. With a combination of these input states the output data takes any form of binary, complementary binary, 2's compliment, or certain test pattern. Refer to Table 1 (Output coding) and Table 2 (Truth table).



**Analog Signal Input** 



SEL, CLK, CAL, RESET, OE, CE, Test Mode, LINV and MINV Inputs

#### CE (Chip Enable, pin 24)

For normal operation the input to this pin should be logic low. Input high applied to the pin puts the unit into standby mode. In standby mode the unit dissipates only a few milliwatts or less.

## OE (Output Enable, pin 23)

Input logic low applied to this pin enables the three-state output bits (Bit 1 to Bit 10). Input high disables the outputs.

#### RESET (pin 15)

This pin can be used to re-initiate start-up calibration. Normally connect this pin to logic high. See Calibration Function for more details.

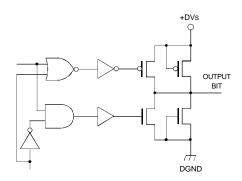
## CAL (Calibration Input, pin 41)

This pin is the input for an external calibration pulse. See Calibration Function for more details.

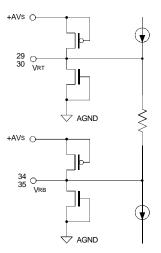
#### SEL (Select, pin 17)

Applying logic high to this pin allows use of the internal auto calibration function and blocks out the external pulse from the CAL input. Inputting logic low to the pin disables the internal cal function and allows usage of the external cal pulses.

- 8. **Test IN/OUT pins:** Test signal input/output pins are used in the production process. The test signal output pins (pin 13, 38) should normally be left open. Tie the test signal input pin 42 to +AVs and the pins 14 and 37 to +AVs or AGND.
- Three-state output buffer: A/D output buffer (BIT 1 to BIT 10) is a three-state register controlled by the OE pin. The output logic high level is dependent on +DVs.



**Digital Data Outputs** 



Reference Input



#### **CALIBRATION FUNCTION**

To achieve its superior linearity ADS-325A has an internal calibration circuit with a built-in calibration pulse generation circuit and an input pin for an external calibration pulse. The calibration circuit consists of three D/A converters, a pattern generator and an averaging circuit. With either internal or external calibration pulses applied to the calibration circuit, the circuit senses an offset of the x8 gain amplifier and two reference biases supplied from the VRT and the VRB to a fine comparator/encoder block, and compensates them using the three DACs.

With a single negative going calibration pulse a unit cycle of calibration is completed. It is initiated with the negative going edge of the calibration pulse and takes seven A/D clock periods to be completed. Due to the fact that this calibration cycle occupies the lower comparator for four A/D clock periods the lower five bits of the output data remain constant through 4 clock cycles after the completion of the cycle. Figure 3 shows the timing for the calibration cycle.

A sequence of seven unit calibration cycles initiated by seven calibration pulses, completes a single calibration process. The number of calibration processes required depends on the condition of the device and on the stability of the references and the power. Even in worst case, 80 calibration processes done by 560 calibration pulses are enough to finish the whole calibration.

There are three modes of the calibration function. These are:

- a. Start-up calibration function
- b. Internal auto-calibration function
- c. External calibration function

Table 1. Digital Output Coding

TEST MODE = 1, LINV = 0, MINV = 0

Analog Input Voltage	Step	Digit MSB	al Outpu	t Code LSB
3.998V	1023	11	1111	1111
3.996V	1022	11	1111	1110
:	:		:	
3.000V	512	10	0000	0000
2.998V	511	01	1111	1111
:	:		:	
2.002V	1	00	0000	0001
2.000V	0	00	0000	0000

For operation in modes a. and b. the ADS-325A has a built-in calibration pulse generation circuit. Figure 4a. illustrates a simplified block diagram of this circuit.

## **Start-up Calibration Function**

At power-up of the unit the initial calibration process requires over 600 calibration pulses. The internal start-up calibration function automatically generates these pulses when power is first applied to the ADS-325A. To initiate the start-up calibration, the following five conditions must be met. See Figure 4b.

- 1. The supply voltage +AVs must be at least 2.5 Volts higher than AGND.
- 2. The voltage difference between  $V_{\text{RT}}$  and  $V_{\text{RB}}$  must be at least 1 Volt.
- 3. The RESET pin (pin 15) must be set high.
- 4. The CE pin (pin 24) must be set low.
- 5. Condition 1 must be met before condition 2.

Once all of the above conditions have been met, the calibration pulses are generated by counting 16 A/D clock cycles on a 14-bit counter until closing the gate when the carry-out occurs. The time required for the start-up calibration is determined by the following formula:

Start-up Calibration Time = 1/fclk x 16 x 16,384

where fclk is the frequency of the A/D clock input. For example, a clock frequency of 14.3MHz requires a calibration time of 18.3ms.

#### **Table 2. Digital Output Truth Table**

P = Positive True; N = Negative True (inverted)

· · · · · · · · · · · · · · · · · · ·					
TEST MODE	LINV	MINV	MSB	igital Out	put LSB
1	0	0	PP	PPPP	PPPP
1	1	0	PN	NNNN	NNNN
1	0	1	NP	PPPP	PPPP
1	1	1	NN	NNNN	NNNN
0	1	1	10	1010	1010
0	0	1	11	0101	0101
0	1	0	00	1010	1010
0	0	0	01	0101	0101

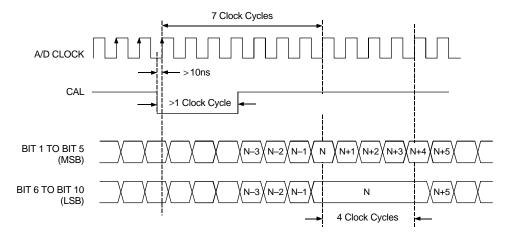


Figure 3. Calibration Timing Diagram



#### Re-initiating the Start-up Calibration

The start-up calibration function can be re-initiated at any time desired after the power and the references are supplied. Apply a positive pulse to  $\overline{\text{CE}}$  pin (pin 24) or a negative pulse to RESET pin (pin 15). The pulse width of these pulses must be equal to or wider than one A/D clock cycle. Also due to this feature, you can make sure of a proper start-up calibration at power-up by making a C-R delay connection with the RESET pin as shown in Figure 4c.

#### **Using Start-up Calibration Function Only**

Internal and external calibration functions need not be employed after start-up calibration. To use only the start-up calibration function, connect the SEL pin (pin 17) to AGND and the CAL pin (pin 14) to +AVs or AGND.

#### **Auto Calibration Function**

After the start up calibration is completed, the internal calibration function can periodically and automatically generate calibration pulses when the auto calibration mode is enabled. To enable this function connect the SEL pin (pin 17) and the CAL pin (pin 41) to +AVs. In this mode a 24-bit counter is counted with every 16 A/D clock cycles and the carry-out is used as the calibration pulse. The period of the calibration pulse generated is as follows:

Period of Auto-calibration pulse = 1/fclk x 16 x 16,777,216

For the case when the A/D clock frequency is 14.3MHz, the calibration pulse generation cycle is 18.8 seconds. Since a single calibration process is performed once every seven pulses, the total calibration cycle is approximately 132 seconds.

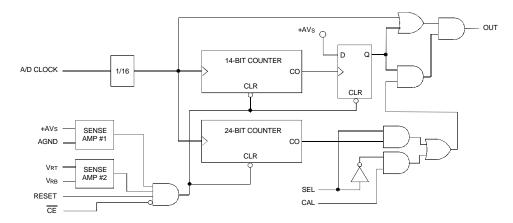


Figure 4a Internal Calibration Pulse Generation Circuit

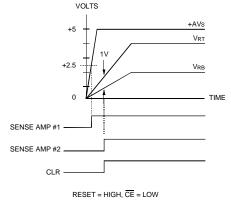


Figure 4b. Conditions for Start-Up Calibration

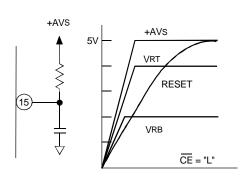


Figure 4c. Start-up Calibration using RESET

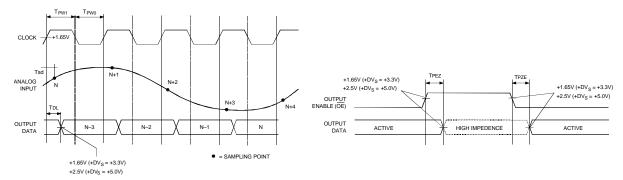


Figure 5. ADS-325A Timing Diagrams



As stated before, the five lower bits of the output data will remain constant for 4 clock cycles with every generation of the calibration pulse. Since the auto calibration pulses are generated asynchronously, this may create problems in certain applications.

#### **External Calibration Function**

To avoid the asynchronous data fixation due to the calibration

process, you can disable the internal auto calibration function and use an external calibration pulse which is synchronized with the analog input. Input the external calibration pulse to the CAL pin (pin 14) and tie the SEL pin (pin 17) to AGND. When digitizing a video signal, for example, you can synchronize the external calibration pulses with the V-sync or H-sync cycles of the video signal to avoid losing any data during the video signal cycles. See figure 6a. and 6b.

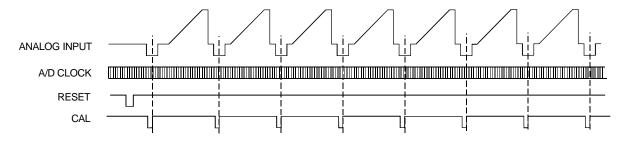


Figure 6a. Applying CAL Pulse Every H Sync.

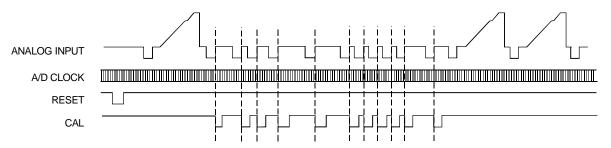


Figure 6b. Applying CAL Pulse Every V Sync.

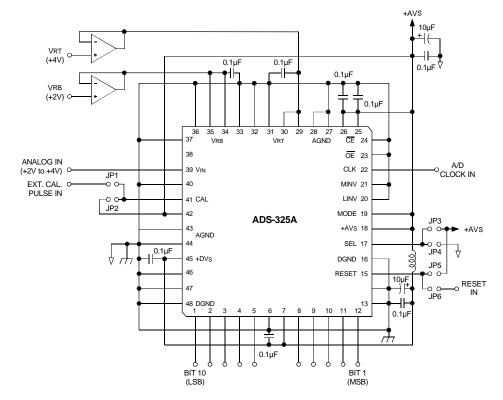


Figure 7. Typical ADS-325A Connection Diagram

#### NOTES:

- For using Start-up calibration and External CAL Pulse Mode, close JP1 and JP4, and open JP2 and JP3.
- For using Start-up calibration and Internal Auto-calibration Mode, close JP2 and JP3, and open JP1 and IP3
- For using Start-up calibration Mode only, close JP2 and JP4, and open JP1 and JP3.
- RESET pin (Pin 15) should normally be connected to +AVs (close JP5).
   To re-initiate the start-up calibration after power-up, close JP6 to apply external RESET pulse.



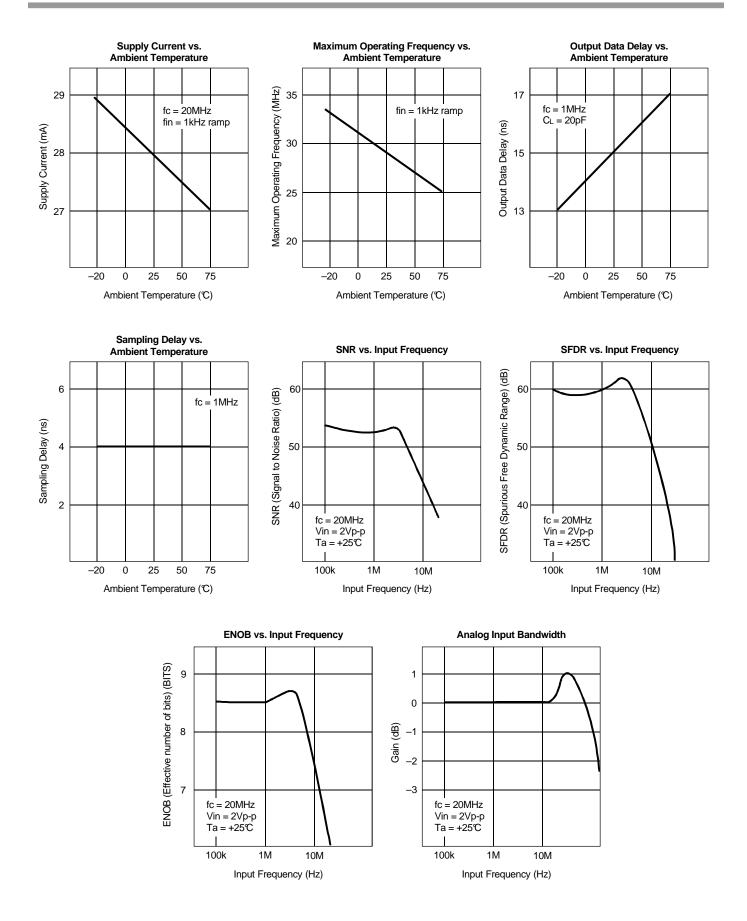
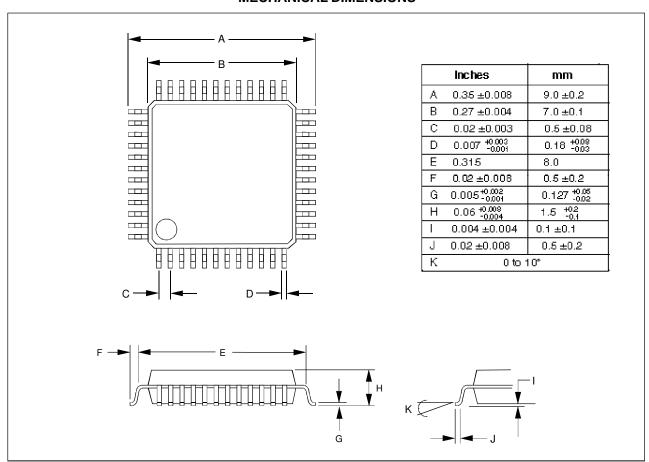


Figure 8. Typical Performance Curves



## **MECHANICAL DIMENSIONS**



## **ORDERING INFORMATION**

Model Number	Bits/Throughput Rate	Package
ADS-325A	10 Bits/20MHz	48-pin, plastic LQFP





DS-0297A 03/98