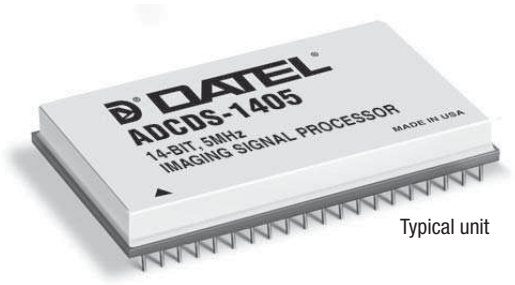
ADCDS-1405

14-Bit, 5 Megapixels/Second, CCD Signal Processor



Typical unit

FEATURES

- 14-bit resolution
- 5MPPS throughput rate (14-bits)
- Extended temperature range -55°C to +100°C
- 1 LSB RMS Noise
- Excellent Signal-to-Noise ratio
- Edge triggered
- Small, 40-pin, TDIP package
- Low power, 700mW typical
- Low cost, functionally complete
- Programmable Analog Bandwidth

PRODUCT OVERVIEW

The ADCDS-1405 is an application-specific video signal processor designed for electronic-imaging applications that employ CCD's (charge coupled devices) as their photodetector. The ADCDS-1405 incorporates a "user configurable" input amplifier, a CDS (correlated double sampler) and a sampling A/D converter in a single package, providing the user with a complete, high performance, low-cost, low-power, integrated solution.

The key to the ADCDS-1405's performance is a unique, high-speed, high-accuracy CDS circuit, which eliminates the effects of residual charge, charge injection and "kT/C" noise on the CCD's output floating capacitor, producing a "valid video" output signal. The ADCDS-1405 digitizes this resultant "valid video" signal using a high-speed, low-noise sampling A/D converter.

The ADCDS-1405 requires only the rising edge of start convert pulse to initiate its conversion process. Additional features of the ADCDS-1405 include gain adjust, offset adjust, precision +2.4V reference, and a programmable analog bandwidth function.

INPUT/OUTPUT CONNECTIONS			
Pin	Function	Pin	Function
1	Fine Gain Adjust	40	No Connect
2	Offset Adjust	39	+12v
3	Direct Input	38	–5va
4	Inverting Input	37	Analog Ground
5	Non-Inverting Input	36	+5va
6	+2.4v Ref. Output	35	Analog Ground
7	Analog Ground	34	+5vd
8	No Connect	33	Digital Ground
9	No Connect	32	Digital Ground
10	Bit 14 (Lsb)	31	A1
11	Bit 13	30	A0
12	Bit 12	29	No Connect
13	Bit 11	28	No Connect
14	Bit 10	27	$\overline{\text{Data Valid}}$
15	Bit 9	26	Reference Hold
16	Bit 8	25	Start Convert
17	Bit 7	24	Out-Of-Range
18	Bit 6	23	Bit 1 (Msb)
19	Bit 5	22	Bit 2
20	Bit 4	21	Bit 3

SIMPLIFIED SCHEMATIC

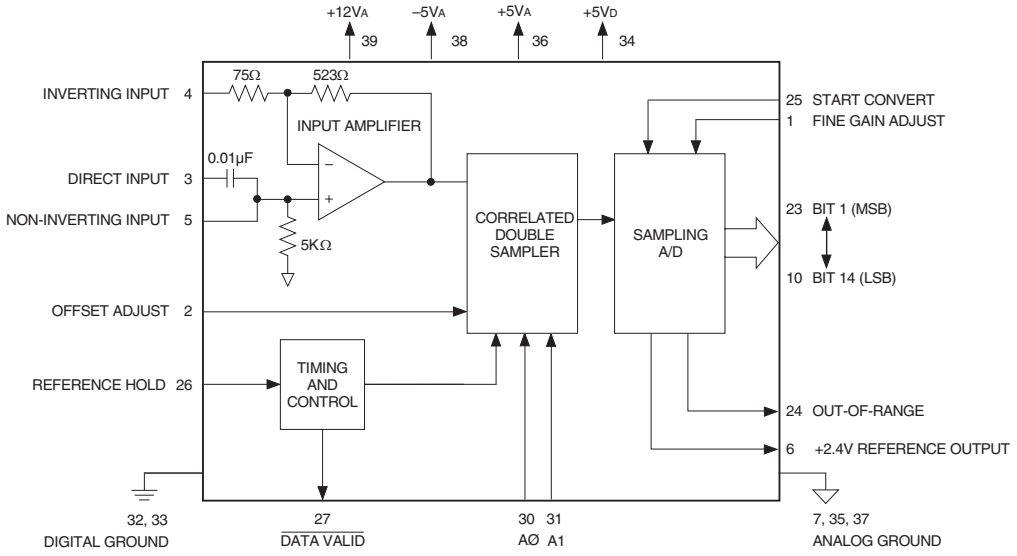


Figure 1. ADCDS-1405 Functional Block Diagram

Absolute Maximum Ratings				
PARAMETERS	MIN.	TYP.	MAX.	UNITS
+12V Supply (Pin 32)	0	—	+14	Volts
–5V Supply (Pin 31)	–0.3	—	+6.5	Volts
+5V Supply (Pin 28, 29)	0	—	–6.5	Volts
Digital Input (Pin 23, 24)	–0.3	—	Vdd+0.3V	Volts
Analog Input (Pin 3,4,5)	–5	—	+5	Volts
Lead Temperature (10 seconds)	—	—	300	°C

Functional Specifications

The following specifications apply over the operating temperature range, under the following conditions: Vcc=+12V, +Vdd=+5V, Vee=–5V, fin=98KHz, sample rate=5MSPS

ANALOG INPUT	MIN.	TYP.	MAX.	UNITS
Input Voltage Range (externally configurable)	0.350	2.8	—	Volts p-p
Input Resistance	—	5000	—	Ohm
Input Capacitance	—	10	—	pF
DIGITAL INPUTS				
Logic Levels				
Logic 1	+3.5	—	—	Volts
Logic 0	—	—	+.80	Volts
Logic Loading				
Logic 1	—	—	+10	uA
Logic 0	—	—	–10	uA
DIGITAL OUTPUTS				
Logic Levels				
Logic 1 (IOH = .5ma)	+2.4	—	—	Volts
Logic 1 (IOH = 50µa)	+4.5	—	—	Volts
Logic 0 (IOL = 1.6ma)	—	—	+0.4	Volts
Logic 0 (IOL = 50ua)	—	—	+0.1	Volts
Internal Reference Voltage (Fine gain adjust pin (1) grounded)				
+25°C	2.35	2.4	2.45	Volts
0 to 70°C	2.35	2.4	2.45	Volts
–55 to +100°C	2.35	2.4	2.45	Volts
External Current	—	1.0	—	mA
STATIC PERFORMANCE				
Differential Nonlinearity				
(Histogram, 98kHz) +25°C	–.99	±0.5	+1.5	LSB
0 to 70°C	–.99	±0.5	+1.5	LSB
–55 to +100°C	–.99	±0.6	+1.5	LSB
Integral Nonlinearity				
+25°C	—	±2.5	—	LSB
0 to 70°C	—	±2.5	—	LSB
–55 to +100°C	—	±2.5	—	LSB
Guaranteed No Missing Codes				
0 to 70°C	14	—	—	LSB
–55 to +100°C	14	—	—	LSB

STATIC PERFORMANCE, continued	MIN.	TYP.	MAX.	UNITS
DC Noise				
+25°C	—	0.65	0.85	LSB
0 to 70°C	—	0.65	0.85	LSB
–55 to +100°C	—	0.65	0.85	LSB
Offset Error				
+25°C	—	±0.6	±3.0	%FSR
0 to 70°C	—	±0.6	±3.0	%FSR
–55 to +100°C	—	±0.6	±6.0	%FSR
Gain Error				
+25°C	—	±1.00	±3.0	%FSR
0 to 70°C	—	±1.35	±3.0	%FSR
–55 to +100°C	—	±1.35	±6.0	%FSR
DYNAMIC PERFORMANCE				
Reference Hold				
Aquisition Time	70	—	—	ns
Droop				
@ 25°C	—	25	—	mV/us
@ –55 to +100°C	—	100	—	mV/us
Signal-to-Noise Ratio Without Distortion (CDD-IN, input on pin (3) Input @ 98kHz)				
@ +25 °C	73	75	—	dB
@ 0 to +70°C	73	75	—	dB
@ –55 to +100°C	70	73	—	dB
(Input on pin (5)				
Input @ 98kHz)				
@ +25 °C	73	75	—	dB
@ 0 to +70°C	73	75	—	dB
@ –55 to +100°C	70	73	—	dB
SIGNAL TIMING				
Conversion Rate				
–55 to +100°C	5	—	—	MSPS
Conversion Time	—	200	—	nsec
Start Convert Pulse Width	20	150	—	nsec
POWER REQUIREMENTS				
Power Supply Range				
+12V Supply	+11.4	+12.0	+12.6	Volts
+5V Supply	+4.75	+5.0	+5.25	Volts
–5V Supply	–4.75	–5.0	–5.25	Volts

POWER REQUIREMENTS	MIN.	TYP.	MAX.	UNITS
Power Supply Current				
+12V Supply	—	+20	+26	mA
Power Supply Current				
-5V Supply	—	-40	-45	mA
+5V Supply	—	+50	+56	mA
Power Dissipation	—	0.7	0.9	Watts
Power Supply Rejection				
(5%) @ +25°C	—	±0.04	±0.06	%FSR/%V
ENVIRONMENTAL				
Operating Temperature Range				
ADCDS-1405	0	—	+70	°C
ADCDS-1405EX	–55	—	+100	°C
Storage Temperature	–65	—	+150	°C
Package Type	40-pin, TDIP			
Weight	16.10 grams			

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADCDS-1405 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital grounds are connected to each other internally. Depending on the level of digital switching noise in the overall CCD system, the performance of the ADCDS-1405 may be improved by connecting all ground pins (7,32,33,35, 37) to a large analog ground plane beneath the package. The use of a single +5V analog supply for both the +5VA (pin 36) and +5VD (pin 34) may also be beneficial.
2. Bypass all power supplies to ground with a 4.7µf tantalum capacitor in parallel with a 0.1µf ceramic capacitor. Locate the capacitors as close to the package as possible.
3. If using the suggested offset and gain adjust circuits (Figure 3 & 5), place them as close to the ADCDS-1405's package as possible.
4. A0 and A1 (pins 30, 31) should be bypassed with 0.1µf capacitors to ground to reduce susceptibility to noise.

ADCDS-1405 Modes of Operation

The input amplifier stage of the ADCDS-1405 provides the designer with a tremendous amount of flexibility. The architecture of the ADCDS-1405 allows its input-amplifier to be configured in any of the following configurations:

- Direct Mode (AC coupled)
- Non-Inverting Mode
- Inverting Mode

When applying inputs which are less than 2.8Vp-p, a coarse gain adjustment (applying an external resistor to pin 4) must be performed to ensure that the full scale video input signal (saturated signal) produces a 2.8Vp-p signal at the input-amplifier's output (Vout).

In all three modes of operation, the video portion of the signal at the CDS input (i.e. input-amplifier's Vout) must be more negative than its associated reference level and Vout should
not exceed ±2.8V DC.

The ADCDS-1405 achieves it specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the FINE GAIN ADJUST (pin1) and OFFSET ADJUST (pin 2) features.

Direct Mode (AC Coupled)

This is the most common input configuration as it allows the ADCDS-1405 to interface directly to the output of the CCD with a minimum amount of analog "front-end" circuitry. This mode of operation is used with full-scale video input signals from 0.350Vp-p to 2.8Vp-p.

Figure 2a. describes the typical configuration for applications using a video input signal with a maximum amplitude of 0.350Vp-p. The coarse gain of the input amplifier is determined from the following equation: VOUT = 2.8Vp-p = VIN*(1+(523/75)), with all internal resistors having a 1% tolerance. Additional fine gain adjustment can be accomplished using the Fine Gain Adjust (pin 1 see Figure 5).

Figure 2b. describes the typical configuration for applications using a video input signal with an amplitude greater than 0.350Vp-p and less than 2.8Vp-p. Using a single external series resistor (see Figure 4.), the coarse gain of the ADCDS-1405 can be set, with additional fine gain adjustments being made using the Fine Gain Adjust function (pin 1 see Figure 5). The coarse gain of the input amplifier can be determined from the following equation:
VOUT = 2.8Vp-p = VIN*(1+(523/(75+Rext))), with all internal resistors having a 1% tolerance.

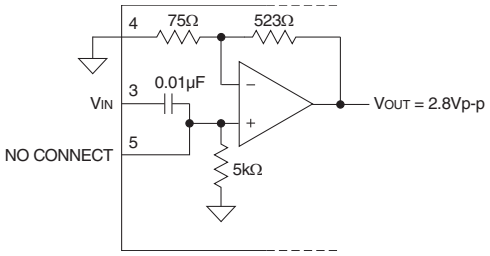


Figure 2a.

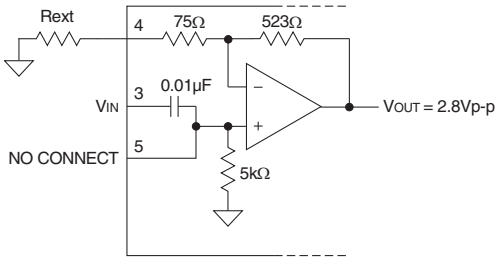


Figure 2b.

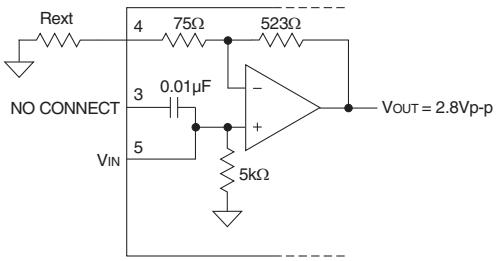


Figure 2c.

Non-Inverting Mode

The non-inverting mode of the ADCDS-1405 allows the designer to either attenuate or add non-inverting gain to the video input signal. This configuration also allows bypassing the ADCDS-1405's internal coupling capacitor, allowing the user to provide an external capacitor of appropriate value.

Figure 2c. describes the typical configuration for applications using video input signals with amplitudes greater than 0.350Vp-p and less than 2.8Vp-p (with common mode limit of ±2.5V DC). Using a single external series resistor (see Figure 4.), the coarse gain of the ADCDS-1405 can be set with additional fine gain adjustments being made using the Fine Gain Adjust function (pin 1 see Figure 5). The coarse gain of the circuit can be determined from the following equation:
VOUT = 2.8Vp-p = VIN*(1+(523/(75+Rext))), with all internal resistors having a 1% tolerance.

Figure 2d. describes the typical configuration for applications using a video input signal whose amplitude is greater than 2.8Vp-p. Using a single external series resistor (Rext 1) in conjunction with the internal 5K (1%) resistor to ground, an attenuation of the input signal can be achieved. Additional fine gain adjustments being made using the Fine Gain Adjust function (pin 1). The coarse gain of this circuit can be determined from the following equation:
VOUT = 2.8Vp-p = [VIN*(5000/(Rext1+5000))]* [1+(523/(75+Rext2))], with all internal resistors having a 1% tolerance.

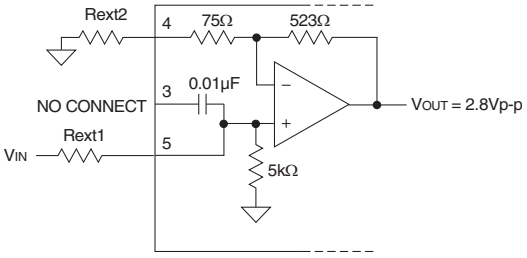


Figure 2d.

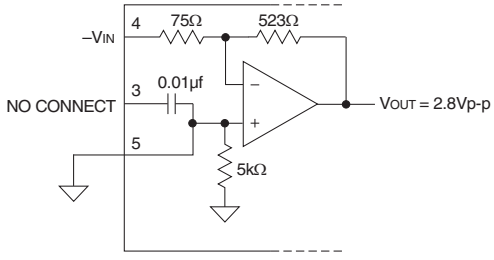


Figure 2e.

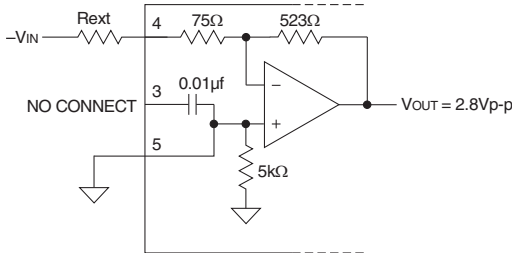


Figure 2f.

Inverting Mode

The inverting mode of operation can be used in applications where the analog input to the ADCDS-1405 has a video input signal whose amplitude is more positive than its associated reference level. The ADCDS-1405s correlated double sampler (i.e. input amplifier's VOUT) requires that the video signal's amplitude be more negative than its reference level at all times (see timing diagram for details). Using the ADCDS-1405 in the inverting mode allows the designer to perform an additional signal inversion to correct for any analog "front end" pre-processing that may have occurred prior to the ADCDS-1405.

Figure 2e. describes the typical configuration for applications using a video input signal with a maximum amplitude of 0.350Vp-p. Additional fine gain adjustments can be made using the Fine Gain Adjust function (pin 1). The coarse gain of this circuit can be determined from the following equation:
VOUT = 2.8Vp-p = –VIN*(523/75), with all internal resistors having a 1% tolerance.

Figure 2f. describes the typical configuration used in applications needing to invert video input signals whose amplitude is greater than 0.350Vp-p. Using a single external series resistor (see Figure 4.), the initial gain of the ADCDS-1405 can be set, with additional fine gain adjustments being made using the Fine Gain Adjust function (pin 1). The coarse gain of this circuit can be determined from the following equation:
VOUT = 2.8Vp-p = –VIN*(523/75+Rext), with all internal resistors having a 1% tolerance.

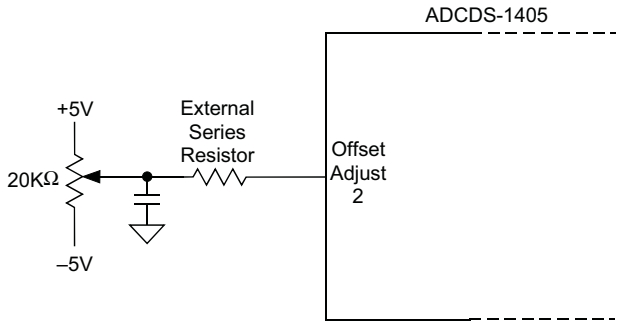


Figure 3. Offset Adjustment Circuit

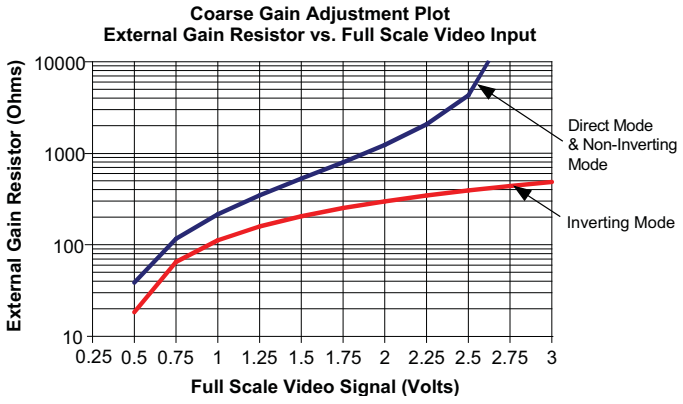


Figure 4. Coarse Gain Adjustment Plot

Offset Adjustment

Manual offset adjustment for the ADCDS-1405 can be accomplished using the adjustment circuit shown in Figure 3. A software controlled D/A converter can be substituted for the 20KΩ potentiometer. The offset adjustment feature allows the user to adjust the Offset/Dark Current level of the ADCDS-1405 until the output bits are 00 0000 0000 0000 and the LSB flickers between 0 and 1. Offset adjust should be performed before gain adjust to avoid interaction. The ADCDS-1405's offset adjustment is dependent on the value of the external series resistor used in the offset adjust circuit (Figure 3). The Offset Adjustment graph (Figure 6) illustrates the typical relationship between the external series resistor value and its offset adjustment capability utilizing ±5V supplies.

Offset Adjustment Sensitivity

It should be noted that with increasing amounts of offset adjustment (smaller values of external series resistors), the ADCDS-1405 becomes more susceptible to power supply noise or voltage variations seen at the wiper of the offset potentiometer.

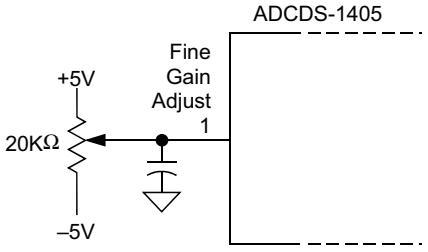


Figure 5. Fine Gain Adjustment Circuit

For Example:

External 50KΩ resistor:

1. 10mV of noise or voltage variation at the potentiometer will produce 0.25LSB's of output variation.
2. 100mV of noise or voltage variation at the potentiometer will produce 2.5LSB's of output variation.

The Offset Adjustment Sensitivity graph (Figure 7) illustrates the offset adjustment sensitivity over a wide range of external resistor and noise values. If a large offset voltage is required, it is recommended that a very low noise external reference be used in the offset adjust circuit in place of power supplies. The ADCDS-1405's +2.4V reference output could be configured to provide the reference voltage for this type of application.

Fine Gain Adjustment

Fine gain adjustment (pin 1) is provided to compensate for the tolerance of the external coarse gain resistor (Rext) and/or the unavailability of exact coarse gain resistor (Rext) values. Note, the fine gain adjustment will not change the expected input amplifier's full scale VOUT (2.8Vp-p.) Instead, the gain of the ADCDS-1405's internal A/D is adjusted allowing the actual input amplifier's full scale VOUT to produce an output code of all ones (11 1111 1111 1111).

Fine gain adjustment for the ADCDS-1405 is accomplished using the adjustment circuit shown below (Figure 5). A software controlled D/A converter can be substituted for the 20KΩ potentiometer. The fine gain adjust circuit ensures that the video input signal (saturated signal) will be properly scaled to obtain the desired Full Scale digital output of 11 1111 1111 1111, with the LSB flickering between 0 and 1. Fine gain adjust should be performed following the offset adjust to avoid interaction. The fine gain adjust provides ±256 codes of adjust when ±5V supplies are used for the Fine Gain Adjust Circuit.

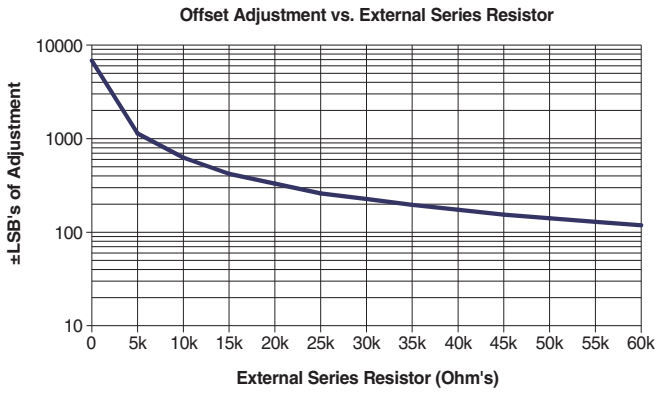


Figure 6. Offset Adjustment vs. External Series Resistor

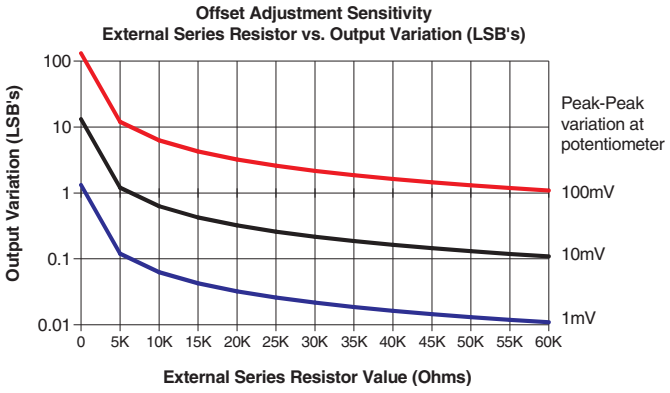


Figure 7. Offset Adjustment Sensitivity

Out-of-Range Indicator

The ADCDS-1405 provides a digital Out-of-Range output signal (pin 24) for situations when the video input signal (saturated signal) is beyond the input range of the internal A/D converter. The digital output bits and the Out-of-Range signal correspond to a particular sampled video input voltage, with both of these signals having a common pipeline delay.

Using the circuit described in Figure 8., both overrange and underrange conditions can be detected (see Table 1). When combined with a D/A converter, digital detection and orrection can be performed for both the gain and offset errors.

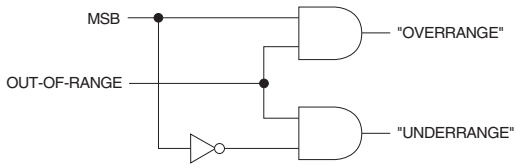


Figure 8. Overrange/ Underrange Circuit

Table 1. Out-of-Range Conditions

OUT OF RANGE	MSB	OVER RANGE	UNDER RANGE	INPUT SIGNAL
0	0	0	0	In Range
0	1	0	0	In Range
1	0	0	1	Underrrange
1	1	1	0	Overrange

Output Coding

The ADCDS-1405's output coding is Straight Binary as indicated in Table 2. The table shows the relationship between the output data coding and the difference between the reference signal voltage and its corresponding video signal voltage. (These voltages are referred to the output of the ADCDS-1405's input amplifier's VOUT).

Programmable Analog Bandwidth Function

When interfacing to CCD arrays with very high-speed "read-out" rates, the ADCDS-1405's input stage must have sufficient analog bandwidth to accurately reproduce the output signals of the CCD array. The amount of analog bandwidth determines how quickly and accurately the "Reference Hold" and the "CDS output" signals will settle. If only a single analog bandwidth was offered, the ADCDS-1405's bandwidth would be set to acquire and digitize CCD output signals to 14-bit accuracy, at maximum conversion rate of 5MHz (200ns see Figure 11. for details). Applications not requiring the maximum conversion rate would be forced to use the full analog bandwidth at the possible expense of noise performance.

The ADCDS-1405 avoids this situation by offering a fully programmable analog bandwidth function. The ADCDS-1405 allows the user to "bandwidth limit" the input stage in order to realize the highest level of noise performance (DC noise of 0.3 LSBs rms possible) for the application being considered. Table 3. describes how to select the appropriate reference hold "aquisition time" and CDS output "settling time" needed for a particular application. Each of the selections listed in Table 3. have been optimized to provide only enough analog bandwidth to acquire a full scale input step, to 14-bit accuracy, in a single conversion. Increasing the analog bandwidth (using a faster settling and acquisition time) would only serve to potentially increase the amount of noise at the ADCDS-1405's output. The ADCDS-1405 uses a two bit digital word to select four different analog bandwidths for the ADCDS-1405's input stage (See Table 3. for details).

Table 2. Output Coding

INPUT AMPLIFIER VOUT, ① (VOLTS P-P)		SCALE	DIGITAL OUTPUT	OUT-OF-RANGE
Video Signal-Reference Signal	> –2.80000	>Full Scale –1LSB	11 1111 1111 1111	1
	–2.80000	Full Scale –1LSB	11 1111 1111 1111	0
	–2.10000	3/4FS	11 0000 0000 0000	0
	–1.40000	1/2FS	10 0000 0000 0000	0
	–0.70000	1/4FS	01 0000 0000 0000	0
	–0.35000	1/8FS	00 1000 0000 0000	0
	–0.000171	1 LSB	00 0000 0000 0001	0
	0	0	00 0000 0000 0000	0
Video Signal-Reference Signal	<0 ②	<0	00 0000 0000 0000	1

Notes: ① Input Amplifier VOUT = (Video Signal - Reference Level)
② The video portion of the differential signal (input-amplifier's VOUT) must be more negative than its associated reference level and VOUT should not exceed ±2.8V DC.

Table 3. Programmable Analog Bandwidth

REFERENCE HOLD "AQUISITION TIME"	CDS OUTPUT "SETTLING TIME"	A0 (Pin 30)	A1 (Pin 31)	ADCDS-1405 MAX. CONVERSION RATE	-3dB BW
70ns	90ns	0	0	5MHz	10.5MHz
100ns	120ns	1	0	3MHz	6.6MHz
200ns	250ns	0	1	2MHz	3.7MHz
450ns	500ns	1	1	1MHz	2.5MHz

Note: See Figure 11. for timing details

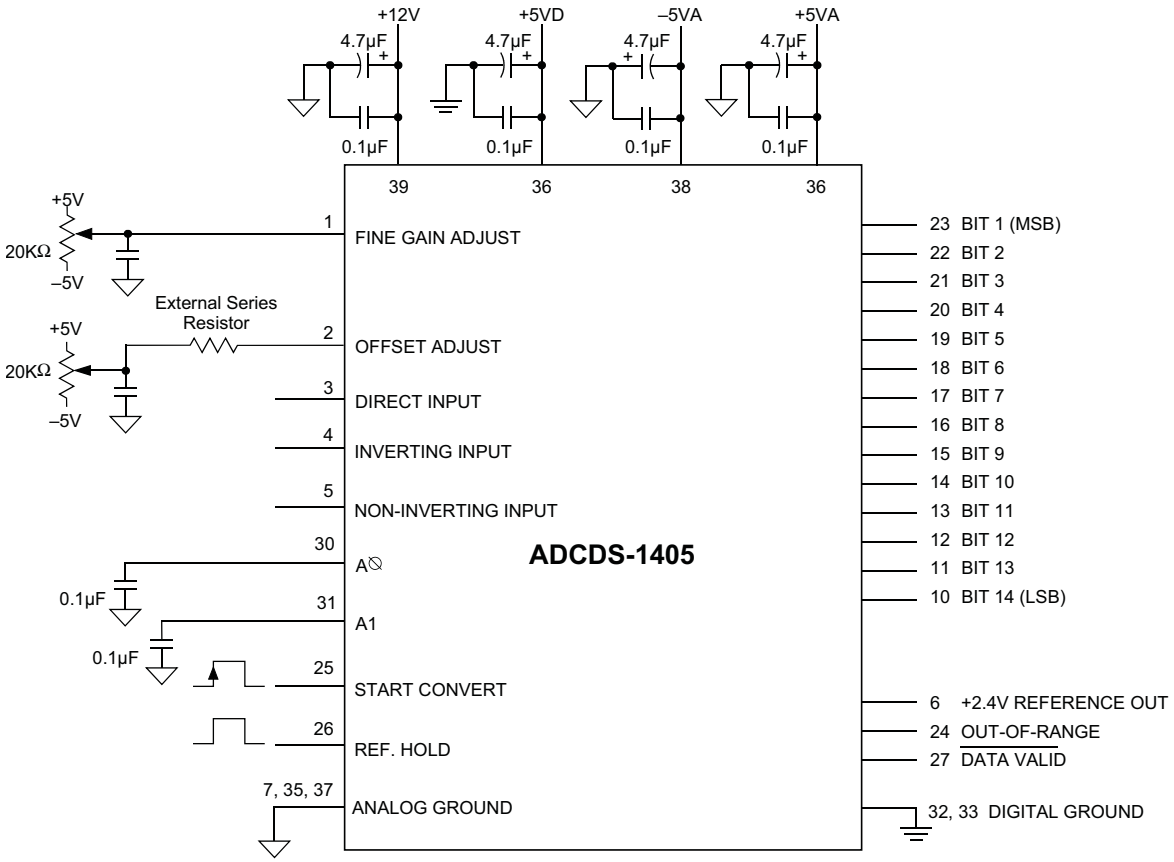


Figure 9. ADCDS-1405 Connection Diagram

Timing

The ADCDS-1405 requires two independently operated signals to accurately digitize the analog output signal from the CCD array.

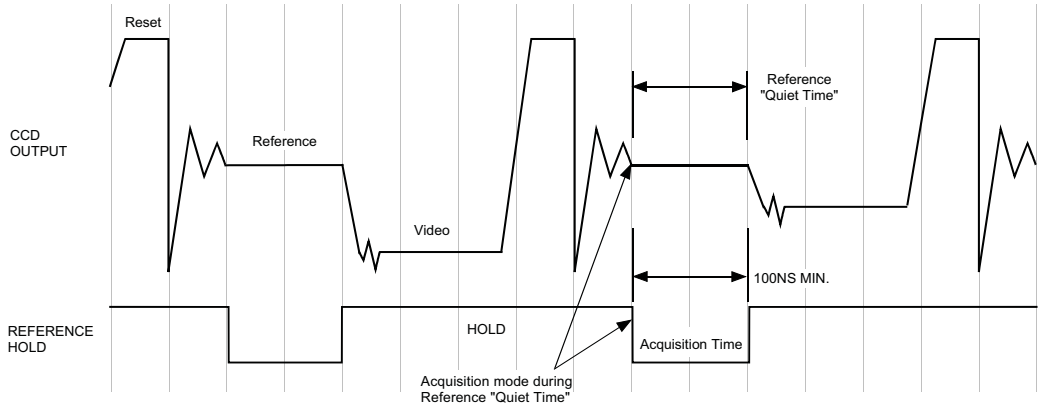
- Reference Hold (pin 26)
- Start Convert (pin 25)

The "Reference Hold" signal controls the operation of an internal sample-hold circuit. A logic "1" places the sample-hold into the hold mode, capturing the value of the CCD's reference signal. The Reference Hold Signal allows the user to control the exact moment when the sample-hold is placed into the "hold" mode. For optimal performance the sample-hold should be placed into the "hold" mode once the reference signal has fully settled from all switching transients to the desired accuracy (user defined).

Once the reference signal has been "held" and the video portion of the CCD's analog output signal appears at the ADCDS-1405's input, the ADCDS-1405's correlated double sampler produces a "CDS Output" signal (see Figure 11.)

which is the difference between the "held" reference level and its associated video level. When the "CDS Output" signal has settled to the desired accuracy (user defined), the A/D conversion process can be initiated with the rising edge of a single start convert (Pin 25) signal.

Once the A/D conversion has been initiated, Reference Hold (Pin 26) can be placed back into the "Acquisition" mode in order to begin aquiring the next reference level. For optimal performance the ADCDS-1405's internal sample-hold should be placed back into the "Aquisition" mode (Reference Hold to logic "0") during the CCD's "Reference Quiet Time" ("Reference Quiet Time" is defined as the period when the CCD's reference signal has settled from all switching transients to the desired accuracy (see Figure 10). Placing the sample-hold back into the "aquisition" mode during the "Reference Quiet Time" prevents the ADCDS-1405's internal amplifiers from unnecessarily tracking (reproducing) the large switching transients that occur during the CCD's reset to reference transition.



Note: For optimal performance (Fastest Acquisition Time), the ADCDS-1405 should be placed into the Acquisition mode (Reference Hold to logic "0") during the CCD output's Reference "Quiet Time". Reference "Quiet Time" is defined as the period when the reference signal's switching transients have settled to an acceptable (user defined) accuracy.

Figure 10. Reference Hold Timing

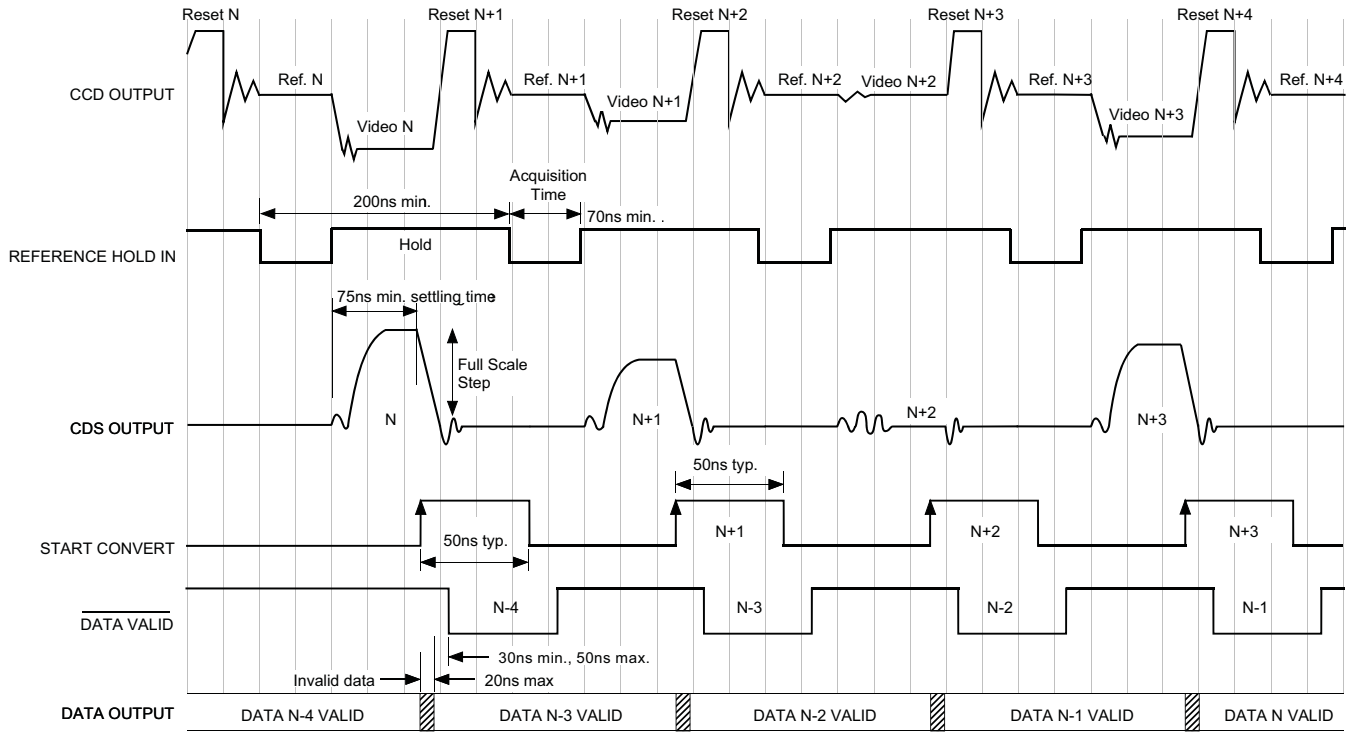
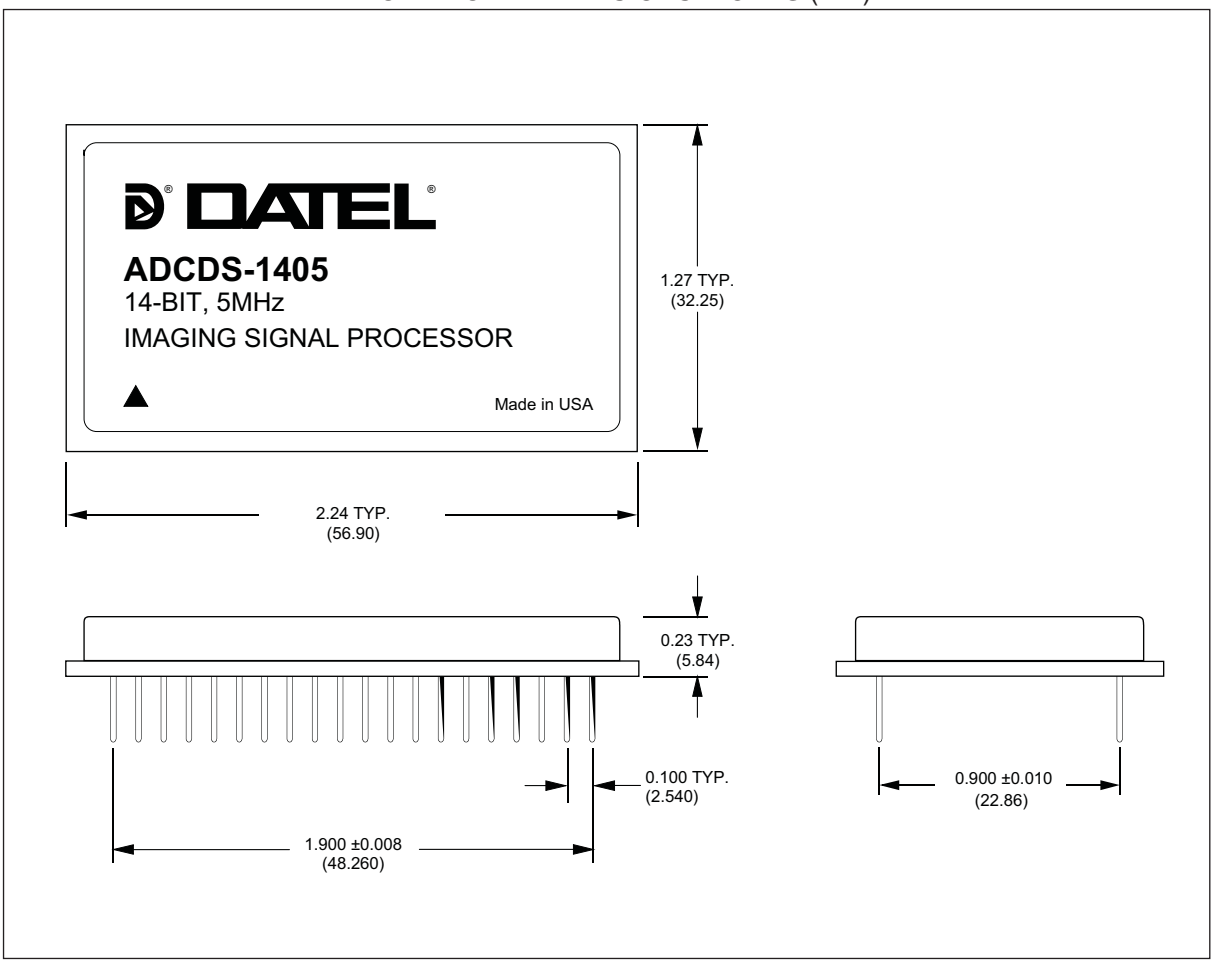


Figure 11. ADCDS-1405 Timing Diagram

MECHANICAL DIMENSIONS INCHES (mm)



ORDERING INFORMATION

MODEL	OPERATING TEMPERATURE RANGE	40-PIN PACKAGE
ADCDS-1405	0 to 70°C	TDIP
ADCDS-1405EX	–55 to 100°C	TDIP