

Processor Power Management Subsystem

DESCRIPTION

The WM8325-00C is an integrated power-management subsystem which provides a cost-effective, flexible, single-chip solution for power management. It is specifically targeted at the requirements of the Freescale i.MX53 multimedia applications processor.

The start-up behaviour and configuration is optimised for compatibility with the Freescale i.MX53 processor, and is stored in an integrated OTP non-volatile memory.

The WM8325-00C is a pre-programmed variant of the WM8325, pre-configured for the Freescale i.MX53 processor. Note that the WM8325 supports user-programming of the integrated OTP memory, providing full flexibility in configuring the device for a wide range of application and mobile processors for low-power consumer multimedia applications.

The WM8325-00C power management subsystem comprises four programmable DC-DC converters and eleven LDO regulators (four of which are low-noise for supplying sensitive analogue subsystems). The integrated OTP bootstrap circuitry controls the start-up sequencing and voltages of the converters and regulators as well as the sequencing of system clocks.

The DC-DC converters deliver high performance and high efficiency across a wide range of operating conditions. They are optimised to support the high load current transients seen in modern processor core domains. DC-DC3 / DC-DC4 are configured in 'dual' mode to support an increased current load of up to 1.6A.

An on-chip regulator provides power for always-on PMIC functions such as register map and the RTC. The device provides autonomous backup battery switchover. A low-power LDO is included to support 'Alive' processor power domains external to the WM8325-00C.

A 12-bit Auxiliary ADC supports a wide range of applications for internal as well as external analogue sampling, such as voltage detection and temperature measurement.

WM8325-00C includes a crystal oscillator and an internal RC oscillator to generate all clock signals for autonomous system start-up and processor clocking. A Secure Real-time Clock (S-RTC) and alarm function is included, capable of waking up the system from low-power modes. A watchdog function is provided to ensure system integrity.

To maximise battery life, highly-granular power management enables each function in the WM8325-00C subsystem to be independently powered down through a control interface or alternatively through register-configurable GPIOs. The device offers a standby power consumption of <7uA, making it particularly suitable for portable applications.

The WM8325-00C is supplied in an 8x8mm 81-lead QFN package, ideal for use in portable systems. The WM8325-00C forms part of the Wolfson series of audio and power management solutions, and is widely register compatible with the WM831X devices.

FEATURES

Power Management

- 1 x DC-DC synchronous buck converter (0.6V - 1.8V, 2.5A, DVS)
- 1 x DC-DC synchronous buck converter (0.6V - 1.8V, 1.25A, DVS)
- 1 x DC-DC synchronous buck converter (0.85V - 3.4V, 1.6A) - 2 converters in 'dual' mode
- 1 x LDO regulator (0.9V - 3.3V, 300mA, 1 Ω)
- 2 x LDO regulators (0.9V - 3.3V, 200mA, 1 Ω)
- 3 x LDO regulators (0.9V - 3.3V, 100mA, 2 Ω)
- 2 x Low-noise LDO regulators (1.0V - 3.5V, 200mA, 1 Ω)
- 2 x Low-noise LDO regulators (1.0V - 3.5V, 150mA, 2 Ω)
- 1 x 'Alive' regulator (0.8V - 1.55V, up to 25mA)

System Control

- OTP memory bootstrap configuration function, optimised for compatibility with the Freescale i.MX53 processor
- I²C or SPI compatible primary control interface
- Comprehensive interrupt scheme
- Watchdog timer and system reset control
- Autonomous power sequencing and fault detection

Additional Features

- Auxiliary ADC for multi-function analogue measurement
- 128-bit pseudo-random unique ID
- Secure Real-Time Clock with wake-up alarm
- 12 x configurable multi-function (GPIO) pins
- Comprehensive clocking scheme: low-power 32kHz RTC crystal oscillator, GPIO clock output and 4MHz RC clock for power management
- System LED outputs indicating device power state, and fault status

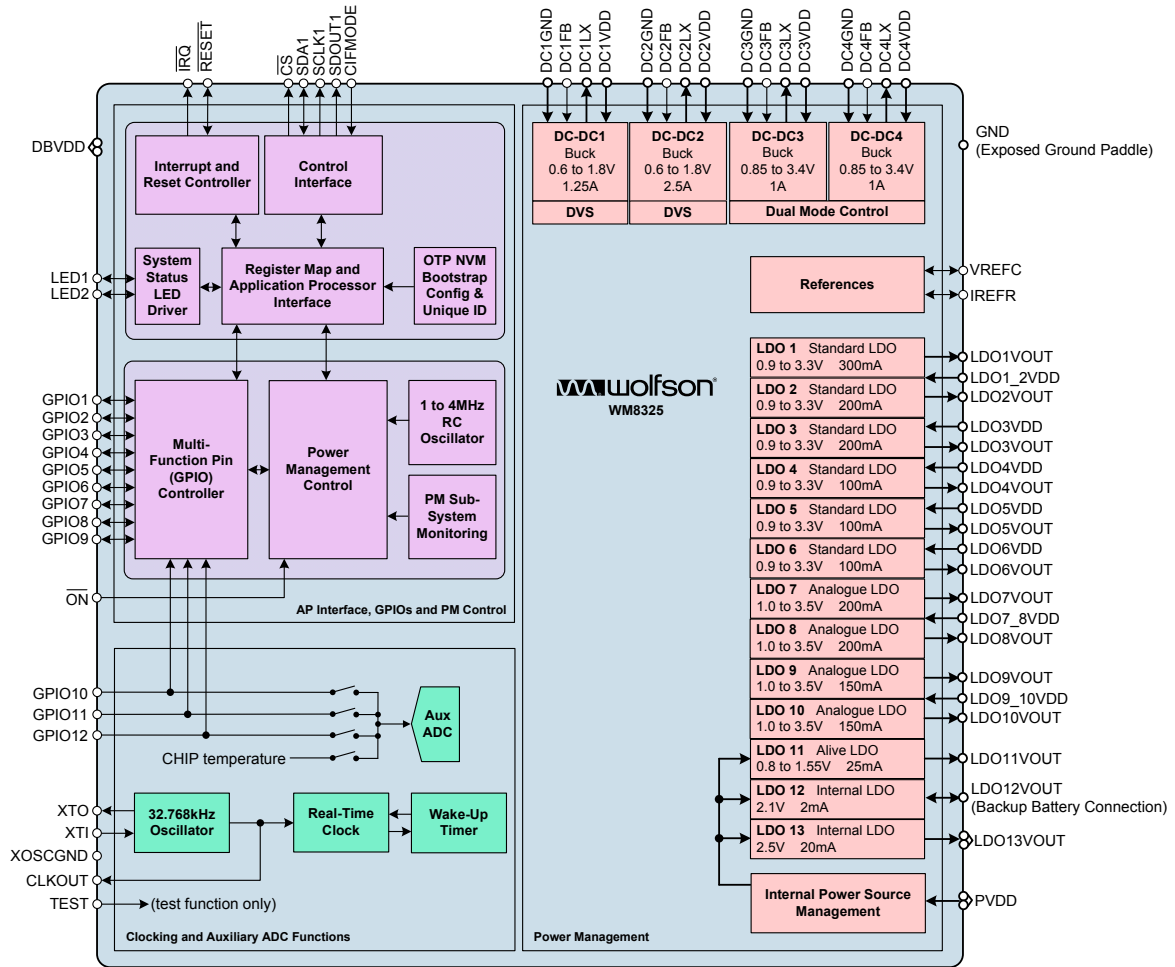
Package Options

- 8 x 8 x 0.85mm, 81-lead QFN package

APPLICATIONS

- Cellular Handsets / Smartphones
- Electronic Books
- Tablets
- Portable Media Players
- Mobile Internet Devices
- Electronic Gaming Devices
- Netbooks / Smartbooks
- Set Top Box
- Digital Picture Frames

BLOCK DIAGRAM



TYPICAL APPLICATIONS

The WM8325-00C is designed as a system PMIC device that generates configurable DC supplies to power the Freescale i.MX53 processor and associated peripherals within a system. The WM8325-00C provides four DC-DC synchronous buck (step-down) converters. Two of these are configured to operate in dual mode, providing an increased current capability. Eleven LDO regulators provide a high degree of flexibility to provide power to multiple devices, with the capability to power-up and power-down different circuits independently.

Two of the DC-DC buck converters incorporate Wolfson's BuckWise™ technology specifically designed to handle rapid changes in load current; programmable slew rate DVS is also provided, as required by modern application processors. Selectable operating modes on all of the DC-DC converters allow each converter to be optimally configured for light, heavy or transient load conditions. Flexible operating configurations allow the converters to be tailored for minimum PCB area, maximum performance, or for maximum efficiency. The analogue LDOs provide low-noise outputs suitable for powering sensitive circuits such as RF / Wi-Fi / cellular handset applications.

The WM8325-00C powers up the converters and LDOs according to a programmable sequence. A configurable 'SLEEP' state is also available, providing support for an alternate configuration, typically for low-power / standby operation. The power control sequences and many other parameters are optimised for compatibility with the Freescale i.MX53 processor, and are stored in an integrated OTP non-volatile memory.

A backup battery supply can be connected to the WM8325-00C in order to maintain the Real Time Clock (RTC) in the absence of the primary supply.

Programmable GPIO pins may be configured as hardware inputs for general use or for selecting different power management configurations. As outputs, the GPIOs can provide indications of the device status, or may be used as control signals for other power management circuits. The WM8325-00C also provides two LED drivers, which can be controlled manually or configured as external indicators of the device operating power state.

The WM8325-00C has been fully verified for compatibility with the Freescale i.MX53 application processor family. Recommended connections to the i.MX53 processor are illustrated in Section 30.

The Freescale i.MX53 application processor family comprises the following devices:

- MCIMX535DVV1C (19x19 BGA package, 1GHz CPU speed, Consumer Grade)
- MCIMX538DZK1C (12x12 PoP package, 1GHz CPU speed, Consumer Grade)
- MCIMX534AVV8C (19x19 BGA package, 800MHz CPU speed, Automotive Grade)
- MCIMX536AVV8C (19x19 BGA package, 800MHz CPU speed, Automotive Grade)
- MCIMX537CVV8C (19x19 BGA package, 800MHz CPU speed, Industrial Grade)

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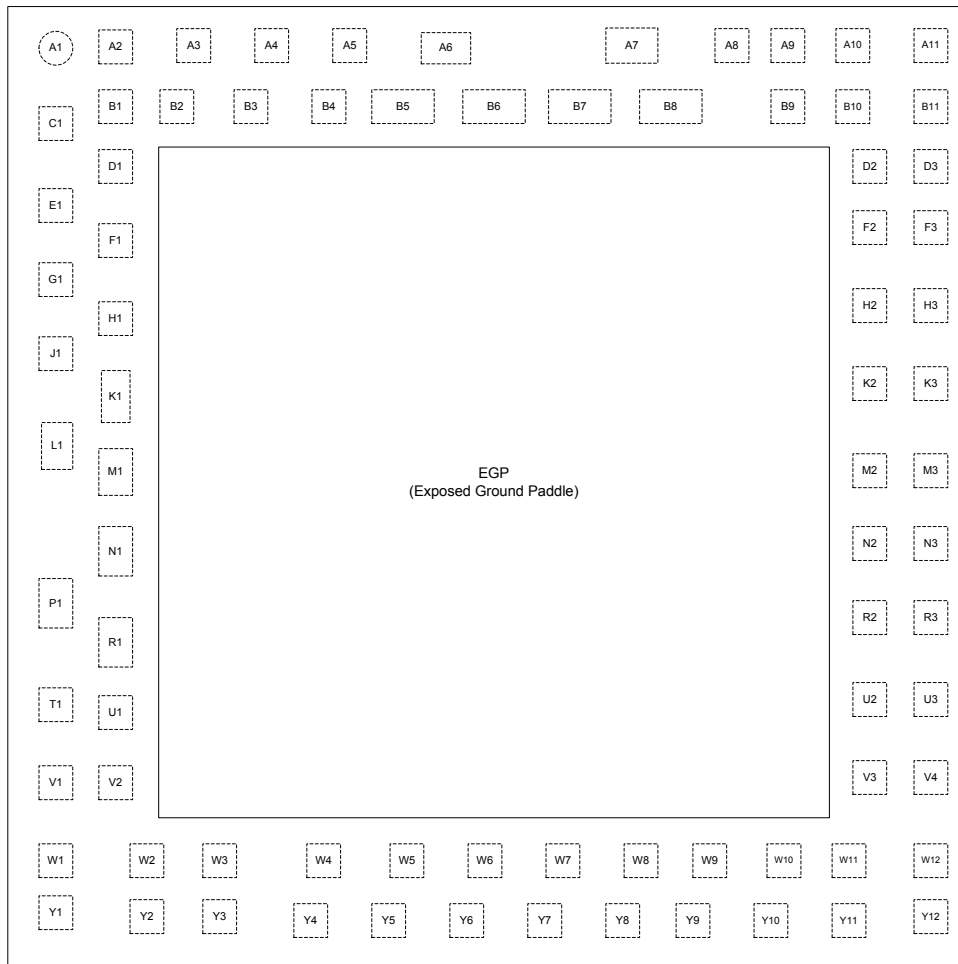
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1 PIN CONFIGURATION



Top View – WM8325-00C

2 ORDERING INFORMATION

ORDER CODE	OTP	TEMPERATURE RANGE (T _A)	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8325GEFL00C/RV	Custom	-40°C to +85°C	81-lead QFN (8 x 8mm) (Pb-free, tape and reel)	MSL3	260°C

Note:

Reel quantity = 2200

3 PIN DESCRIPTION

Notes:

1. Pins are sorted by functional groups.
2. The power domain associated with each pin is noted; VPMIC is the domain powered by LDO12 for the 'always-on' functions internal to the WM8325-00C.
3. Note that an external level-shifter may be required when interfacing between different power domains.

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
Clocking and Real Time Clock				
Y12	XTO	Analogue Output	VPMIC	Crystal Drive Output
Y11	XTI	Analogue Input		Crystal Drive Input or 32.768kHz CMOS Clock Input
W11	XOSCGND	Supply		Crystal Oscillator Ground
H1	CLKOUT	Digital Output	DBVDD	CMOS Clock Output Configurable Open Drain / CMOS mode. (External 4.7kΩ pull-up recommended in Open Drain mode.)
General Purpose Input / Output and Auxiliary ADC				
D3	GPIO1	Digital I/O	DBVDDor VPMIC	GPIO Pin 1 Selectable pull-up/pull-down.
F2	GPIO2	Digital I/O		GPIO Pin 2 Selectable pull-up/pull-down.
F3	GPIO3	Digital I/O		GPIO Pin 3 Selectable pull-up/pull-down.
W4	GPIO4	Digital I/O	DBVDDor PVDD	GPIO Pin 4 Selectable pull-up/pull-down.
Y4	GPIO5	Digital I/O		GPIO Pin 5 Selectable pull-up/pull-down.
W5	GPIO6	Digital I/O		GPIO Pin 6 Selectable pull-up/pull-down.
H2	GPIO7	Digital I/O	DBVDDor VPMIC	GPIO Pin 7 Selectable pull-up/pull-down.
H3	GPIO8	Digital I/O		GPIO Pin 8 Selectable pull-up/pull-down.
K3	GPIO9	Digital I/O		GPIO Pin 9 Selectable pull-up/pull-down.
Y5	GPIO10	Digital I/O	DBVDDor PVDD	GPIO Pin 10 / Auxiliary ADC input Selectable GPIO pull-up/pull-down.
Y6	GPIO11	Digital I/O		GPIO Pin 11 / Auxiliary ADC input Selectable GPIO pull-up/pull-down.
W6	GPIO12	Digital I/O		GPIO Pin 12 / Auxiliary ADC input Selectable GPIO pull-up/pull-down.

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION	
Processor Interface and IC Control					
W9	$\overline{\text{ON}}$	Digital Input	VPMIC	ON Request Pin (Internal pull-up)	
B10	$\overline{\text{RESET}}$	Digital I/O	DBVDD	System Reset Input and Open Drain Output. (Internal pull-up)	
A11	$\overline{\text{IRQ}}$	Digital Output	DBVDD	PMIC Interrupt Flag Output. Configurable Open Drain / CMOS mode. (Internal pull-up in Open Drain mode.)	
E1	CIFMODE	Digital Input	DBVDD	Primary Control Interface Mode Select: 0 = I ² C Compatible Control Interface Mode 1 = SPI Compatible Control Interface Mode	
				<i>SPI Compatible Control Interface Mode</i>	<i>I²C Compatible Control Interface Mode</i>
D2	SDOUT1	Digital Output	DBVDD	Control Interface Serial Data Out. Open Drain output; external 4.7k Ω pull-up recommended.	No Function
B9	SCLK1	Digital Input		Control Interface Serial Clock	Control Interface Serial Clock
A9	SDA1	Digital I/O		Control Interface Serial Data In	Control Interface Serial Data Input and Open Drain Output. External 4.7k Ω pull-up recommended. (Output can extend above DBVDD domain.)
A10	$\overline{\text{CS}}$	Digital Input		Control Interface Chip Select	I ² C Address Select: 0 = 68h 1 = 6Ch
B11	DBVDD1	Supply		Digital Buffer Supply	
F1	DBVDD2	Supply		Digital Buffer Supply	

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
DC-DC Converters and LDO Regulators				
B7	DC1GND	Supply		DC-DC1 Power Ground
A8	DC1FB	Analogue Input	DC1VDD	DC-DC1 Feedback Pin
A7	DC1LX	Analogue I/O		DC-DC1 Inductor Connection
B8	DC1VDD	Supply		DC-DC1 Power Input (connect to PVDD system supply)
B6	DC2GND	Supply		DC-DC2 Power Ground
A5	DC2FB	Analogue Input	DC2VDD	DC-DC2 Feedback Pin
A6	DC2LX	Analogue I/O		DC-DC2 Inductor Connection
B5	DC2VDD	Supply		DC-DC2 Power Input (connect to PVDD system supply)
M1	DC3GND	Supply		DC-DC3 Power Ground
J1	DC3FB	Analogue Input	DC3VDD	DC-DC3 Feedback Pin
L1	DC3LX	Analogue I/O		DC-DC3 Inductor Connection
K1	DC3VDD	Supply		DC-DC3 Power Input (connect to PVDD system supply)
N1	DC4GND	Supply		DC-DC4 Power Ground
T1	DC4FB	Analogue Input	DC4VDD	DC-DC4 Feedback Pin
P1	DC4LX	Analogue I/O		DC-DC4 Inductor Connection
R1	DC4VDD	Supply		DC-DC4 Power Input (connect to PVDD system supply)
A3	LDO1_2VDD	Supply		LDO1 & LDO2 Power Input
B2	LDO1VOUT	Analogue Output	LDO1VDD	LDO1 Power Output
B3	LDO2VOUT	Analogue Output	LDO2VDD	LDO2 Power Output
B4	LDO3VDD	Supply		LDO3 Power Input
A4	LDO3VOUT	Analogue Output	LDO3VDD	LDO3 Power Output
W3	LDO4VDD	Supply		LDO4 Power Input
Y2	LDO4VOUT	Analogue Output	LDO4VDD	LDO4 Power Output
Y1	LDO5VDD	Supply		LDO5 Power Input
W2	LDO5VOUT	Analogue Output	LDO5VDD	LDO5 Power Output
W1	LDO6VDD	Supply		LDO6 Power Input
V1	LDO6VOUT	Analogue Output	LDO6VDD	LDO6 Power Output
R3	LDO7_8VDD	Supply		LDO7 & LDO8 Power Input
N2	LDO7VOUT	Analogue Output	LDO7VDD	LDO7 Power Output
R2	LDO8VOUT	Analogue Output	LDO8VDD	LDO8 Power Output
M2	LDO9_10VDD	Supply		LDO9 Power Input
M3	LDO9VOUT	Analogue Output	LDO9VDD	LDO9 Power Output
N3	LDO10VOUT	Analogue Output	LDO10VDD	LDO10 Power Output
V3	LDO11VOUT	Analogue Output	PVDD	LDO11 (Alive) Power Output
Y8	LDO12VOUT	Analogue I/O	PVDD	LDO12 (Internal VPMIC) Output; Backup battery supply input / output
W7	LDO13VOUT1	Analogue I/O	PVDD	LDO13 (Internal INTVDD) Output; not for general use
K2	LDO13VOUT2	Analogue I/O	PVDD	LDO13 - Connect to LDO13VOUT1 (W7)
Voltage and Current References				
W8	VREFC	Analogue I/O	VPMIC	Voltage Reference capacitor connection point
Y9	IREFR	Analogue I/O		Current Reference resistor connection point
System LED Drivers				
U3	LED1	Digital Output	PVDD	Status LED Driver 1. Open Drain Output
U2	LED2	Digital Output		Status LED Driver 2. Open Drain Output

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
System Power				
U1	PVDD1	Supply		System VDD Supply
Y7	PVDD2	Supply		System VDD Supply
V4	PVDD3	Supply		System VDD Supply
EGP	Exposed Ground Paddle	Analogue Ground		Ground
Miscellaneous				
A1, A2, B1, C1, D1, V2, Y3, Y10, W10	DNC			Do Not Connect
G1, W12	TEST			Test function (connect to GND)

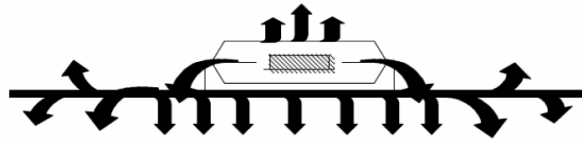
4 THERMAL CHARACTERISTICS

Thermal analysis must be performed in the intended application to prevent the WM8325-00C from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the GND balls through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air:

- Package top to air (convection and radiation).
- Package bottom to PCB (convection and radiation).
- Package leads to PCB (conduction).

(Note that radiation is not normally significant at the moderate temperatures experienced in typical applications.)



The temperature rise T_R is given by $T_R = P_D * \Theta_{JA}$

- P_D is the power dissipated by the device.
- Θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air.
- For WM8325-00C, $\Theta_{JA} = 24^\circ\text{C/W}$
- The quoted Θ_{JA} is based on testing to the EIA/JEDEC-51-2 test environment (ie. 1ft³ box, still air, with specific PCB stack-up and tracking rules). Note that this is not guaranteed to reflect all typical end applications.

The junction temperature T_J is given by $T_J = T_A + T_R$

- T_A , is the ambient temperature.

The worst case conditions are when the WM8325-00C is operating in a high ambient temperature, and under conditions which cause high power dissipation, such as the DC-DC converters operating at low supply voltage, high duty cycle and high output current. Under such conditions, it is possible that the heat dissipated could cause the maximum junction temperature of the device to be exceeded. Care must be taken to avoid this situation. An example calculation of the junction temperature is given below.

- $P_D = 500\text{mW}$ (example figure)
- $\Theta_{JA} = 24^\circ\text{C/W}$
- $T_R = P_D * \Theta_{JA} = 12^\circ\text{C}$
- $T_A = 85^\circ\text{C}$ (example figure)
- $T_J = T_A + T_R = 97^\circ\text{C}$

The minimum and maximum operating junction temperatures for the WM8325-00C are quoted in Section 5. The maximum junction temperature is 125°C . Therefore, the junction temperature in the above example is within the operating limits of the WM8325-00C.

5 ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The WM8325-00C has been classified as MSL3.

CONDITION	MIN	MAX
System supply (PVDD1, PVDD2, PVDD3)	-0.3V	7.0V
Input voltage for LDO regulators	-0.3V	7.0V
Input voltage for DC-DC converters	-0.3V	7.0V
Digital buffer supply (DBVDD1, DBVDD2)	-0.3V	4.5V
Voltage range for digital inputs	-0.3V	DBVDD + 0.3V
Operating Temperature Range, T _A	-40°C	+85°C
Junction Temperature, T _J	-40°C	+125°C
Thermal Impedance Junction to Ambient, θ _{JA}		24°C/W
Storage temperature prior to soldering	30°C max / 60% RH max	
Storage temperature after soldering	-65°C	+150°C
Soldering temperature (10 seconds)		+260°C
Note: These ratings assume that all ground pins are at 0V.		

6 RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
System power source	PVDD1, PVDD2, PVDD3	2.7		5.5	V
Digital buffer supply	DBVDD1, DBVDD2	1.71		3.6	V
Ground	Exposed Ground Paddle (EGP), DC1GND, DC2GND, DC3GND, DC4GND, XOSCGND		0		V

7 ELECTRICAL CHARACTERISTICS

7.1 DC-DC SYNCHRONOUS BUCK CONVERTERS

DC-DC1

Unless otherwise noted: $V_{IN} = 3.8V$, $V_{OUT} = 1.2V$, MODE = FCCM⁽¹⁾, $T_J = -40^{\circ}C$ to $+125^{\circ}C$; typical values are at $T_J = 25^{\circ}C$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		2.7		5.5	V
Programmable Output Voltage	V_{OUT}		0.6		1.8	V
V_{OUT} Step Size	V_{OUT_STEP}			12.5		mV
V_{OUT} Accuracy	V_{OUT_ACC}	$V_{IN} = 2.7V$ to $5.5V$, $I_{OUT} = 0mA$ to $1250mA$	-2.5		+2.5	%
Undervoltage margin	V_{UV}	$0.6V \leq V_{OUT} < 0.9V$		50		mV
		$0.9V \leq V_{OUT} < 1.3V$		80		
		$1.3V \leq V_{OUT} \leq 1.8V$		100		
Overvoltage margin	V_{OV}	$0.6V \leq V_{OUT} \leq 1.8V$		100		mV
Output Current	I_{OUT}	FCCM ⁽¹⁾ and Auto (CCM/DCM with PS ⁽²⁾) Modes	0		1250	mA
		Hysteretic Mode	0		150	
		LDO Mode	0		10	
P-channel Current Limit	I_{P_LIM}			1850		mA
Quiescent Current	I_Q	$I_{OUT} = 0mA$, FCCM ⁽¹⁾ and Auto (CCM/DCM with PS ⁽²⁾) Modes (excluding switching losses)		585		μA
		$I_{OUT} = 0mA$, Hysteretic Mode		100		
		$I_{OUT} = 0mA$, LDO Mode		25		
Shutdown Current	I_{SD}	DC1_ENA = 0		0.01		μA
P-channel On Resistance	R_{DSP}	$V_{IN} = V_{GS} = 3.8V$, $I_{DCmLX} = 100mA$		150		$m\Omega$
N-channel On Resistance	R_{DSN}	$V_{IN} = V_{GS} = 3.8V$, $I_{DCmLX} = -100mA$		140		$m\Omega$
Switching Frequency	F_{SW}			2		MHz

Notes:

1. Forced Continuous Conduction Mode
2. Continuous / Discontinuous Conduction with Pulse-Skipping Mode

DC-DC2

Unless otherwise noted: $V_{IN} = 3.8V$, $V_{OUT} = 1.2V$, $MODE = FCCM^{(1)}$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$; typical values are at $T_J = 25^{\circ}C$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		2.7		5.5	V
Programmable Output Voltage	V_{OUT}		0.6		1.8	V
V_{OUT} Step Size	V_{OUT_STEP}			12.5		mV
V_{OUT} Accuracy	V_{OUT_ACC}	$V_{IN} = 2.7V$ to $5.5V$, $I_{OUT} = 0mA$ to $2500mA$	-2.5		+2.5	%
Undervoltage margin	V_{UV}	$0.6V \leq V_{OUT} < 0.9V$		50		mV
		$0.9V \leq V_{OUT} < 1.3V$		80		
		$1.3V \leq V_{OUT} \leq 1.8V$		100		
Overvoltage margin	V_{OV}	$0.6V \leq V_{OUT} \leq 1.8V$		100		mV
Output Current	I_{OUT}	FCCM ⁽¹⁾ and Auto (CCM/DCM with PS ⁽²⁾) Modes	0		2500	mA
		Hysteretic Mode	0		150	
		LDO Mode	0		10	
P-channel Current Limit	I_{P_LIM}			3650		mA
Quiescent Current	I_Q	$I_{OUT} = 0mA$, FCCM ⁽¹⁾ and Auto (CCM/DCM with PS ⁽²⁾) Modes (excluding switching losses)		585		μA
		$I_{OUT} = 0mA$, Hysteretic Mode		100		
		$I_{OUT} = 0mA$, LDO Mode		25		
Shutdown Current	I_{SD}	DC2_ENA = 0		0.01		μA
P-channel On Resistance	R_{DSP}	$V_{IN} = V_{GS} = 3.8V$, $I_{DCmLX} = 100mA$		115		$m\Omega$
N-channel On Resistance	R_{DSN}	$V_{IN} = V_{GS} = 3.8V$, $I_{DCmLX} = -100mA$		105		$m\Omega$
Switching Frequency	F_{SW}			2		MHz

Notes:

1. Forced Continuous Conduction Mode
2. Continuous / Discontinuous Conduction with Pulse-Skipping Mode

DC-DC3 and DC-DC4 (Operating in conjunction, in 'Dual' mode)Unless otherwise noted: $V_{IN} = 3.8V$, $V_{OUT} = 1.2V$, MODE = FCCM⁽¹⁾, $T_J = -40^{\circ}C$ to $+125^{\circ}C$; typical values are at $T_J = 25^{\circ}C$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		2.7		5.5	V
Programmable Output Voltage	V_{OUT}		0.85 ⁽²⁾		3.4	V
V_{OUT} Step Size	V_{OUT_STEP}			25		mV
V_{OUT} Accuracy	V_{OUT_ACC}	$V_{IN} = 2.7V$ to $5.5V$, $I_{OUT} = 0mA$ to $1600mA$	-4		4	%
Undervoltage margin	V_{UV}	$0.85V \leq V_{OUT} \leq 3.4V$		50		mV
Output Current	I_{OUT}	FCCM ⁽¹⁾ Mode	0		1600	mA
		Hysteretic Mode, DC3_STNBY_LIM=01	0		100 ⁽³⁾	
		LDO Mode	0		10	
P-channel Current Limit	I_{P_LIM}			1600		mA
Quiescent Current	I_Q	$I_{OUT} = 0mA$, FCCM ⁽¹⁾ Mode (excluding switching losses)		330		μA
		$I_{OUT} = 0mA$, Hysteretic Mode		110		
		$I_{OUT} = 0mA$, LDO Mode		20		
Shutdown Current	I_{SD}	DC3_ENA = 0		0.01		μA
P-channel On Resistance	R_{DSP}	$V_{IN} = V_{GS} = 3.8V$, $I_{DC3LX} = 100mA$		165		$m\Omega$
N-channel On Resistance	R_{DSN}	$V_{IN} = V_{GS} = 3.8V$, $I_{DC3LX} = -100mA$		155		$m\Omega$
Switching Frequency	F_{SW}			2		MHz

Notes:

1. Forced Continuous Conduction Mode
2. In FCCM mode, the minimum V_{OUT} is 1.2V
3. The maximum output current in Hysteretic mode can be adjusted using the DC3_STNBY_LIM registers

7.2 LDO REGULATORS

LDO1

Unless otherwise noted: $V_{IN} = 3.8V$, $V_{OUT} = 1.8V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$; Typical values are at $T_J = +25^{\circ}C$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		1.5		5.5	V
Programmable Output Voltage	V_{OUT}		0.9		3.3	V
V_{OUT} Step Size	V_{OUT_STEP}	$V_{OUT} = 0.9V$ to $1.6V$		50		mV
		$V_{OUT} = 1.7V$ to $3.3V$		100		
Output Current	I_{OUT}	Normal mode	0		300	mA
		Low power mode, $LDO\eta_LP_MODE=0$	0		50	
		Low power mode, $LDO\eta_LP_MODE=1$	0		20	
V_{OUT} Accuracy	V_{OUT_ACC}	$I_{LOAD} = 1mA$	-3		3	%
Line Regulation	V_{OUT_LINE}	$V_{IN} = (V_{OUT} + 0.5)$ to $5.5V$, $I_{LOAD} = 150mA$ Note that V_{IN} must be $\geq 1.5V$		0.1		%/V
Load Regulation	V_{OUT_LOAD}	$I_{LOAD} = 1mA$ to $300mA$		0.011		%/mA
Dropout Voltage	$V_{IN} - V_{OUT}$	$I_{LOAD} = 150mA$, $V_{OUT} > 2.7V$		250		mV
		$I_{LOAD} = 150mA$, $V_{OUT} 1.8V$ to $2.7V$		300		
		$I_{LOAD} = 150mA$, $V_{OUT} < 1.8V$		500		
Undervoltage level	V_{OUT}	V_{OUT} Falling		88		%
Quiescent Current	I_Q	Normal mode, no load		30		μA
		Low power mode, $LDO\eta_LP_MODE=0$, no load		10		
		Low power mode, $LDO\eta_LP_MODE=1$, no load		5		
		$I_{LOAD} = 1mA$ to $300mA$		I_Q (no load) + 1% of load		
Power Supply Rejection Ratio	PSRR	$I_{LOAD} = 150mA$, $\leq 1kHz$		53		dB
		$I_{LOAD} = 150mA$, $10kHz$		53		
		$I_{LOAD} = 150mA$, $100kHz$		32		
On Resistance (Switch mode)	$R_{DS(on)}$	$V_{IN} = 1.5V$, $I_{LOAD} = 100mA$		1.5		Ω
		$V_{IN} = 1.8V$, $I_{LOAD} = 100mA$		1.2		
		$V_{IN} = 2.5V$, $I_{LOAD} = 100mA$		0.85		
		$V_{IN} = 3.3V$, $I_{LOAD} = 100mA$		0.7		
Current Limit (Switch mode)	I_{CL}	$V_{OUT} = 0V$		600		mA
Start-up time	t_{start_up}	No load, Output cap $2.2 \mu F$, 90% of V_{OUT}		10		μs
Shutdown time	t_{shut_down}	No load, Output cap $2.2 \mu F$, 10% of V_{OUT}			10	ms

LDO2, LDO3

Unless otherwise noted: $V_{IN} = 3.8V$, $V_{OUT} = 1.8V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$; Typical values are at $T_J = +25^{\circ}C$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		1.5		5.5	V
Programmable Output Voltage	V_{OUT}		0.9		3.3	V
V_{OUT} Step Size	V_{OUT_STEP}	$V_{OUT} = 0.9V$ to $1.6V$		50		mV
		$V_{OUT} = 1.7V$ to $3.3V$		100		
Output Current	I_{OUT}	Normal mode	0		200	mA
		Low power mode, $LDO\eta_LP_MODE=0$	0		50	
		Low power mode, $LDO\eta_LP_MODE=1$	0		20	
V_{OUT} Accuracy	V_{OUT_ACC}	$I_{LOAD} = 1mA$	-3		3	%
Line Regulation	V_{OUT_LINE}	$V_{IN} = (V_{OUT} + 0.5)$ to $5.5V$, $I_{LOAD} = 100mA$ Note that V_{IN} must be $\geq 1.5V$		0.1		%/V
Load Regulation	V_{OUT_LOAD}	$I_{LOAD} = 1mA$ to $200mA$		0.011		%/mA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dropout Voltage	$V_{IN} - V_{OUT}$	$I_{LOAD} = 100\text{mA}$, $V_{OUT} > 2.7\text{V}$		200		mV
		$I_{LOAD} = 100\text{mA}$, $V_{OUT} 1.8\text{V to } 2.7\text{V}$		250		
		$I_{LOAD} = 100\text{mA}$, $V_{OUT} < 1.8\text{V}$		400		
Undervoltage level	V_{OUT}	V_{OUT} Falling		88		%
Quiescent Current	I_Q	Normal mode, no load		30		μA
		Low power mode, $LDO_{n_LP_MODE}=0$, no load		10		
		Low power mode, $LDO_{n_LP_MODE}=1$, no load		5		
		$I_{LOAD} = 1\text{mA to } 200\text{mA}$		I_Q (no load) + 1% of load		
Power Supply Rejection Ratio	PSRR	$I_{LOAD} = 100\text{mA}$, $\leq 1\text{kHz}$		55		dB
		$I_{LOAD} = 100\text{mA}$, 10kHz		55		
		$I_{LOAD} = 100\text{mA}$, 100kHz		32		
On Resistance (Switch mode)	R_{DSON}	$V_{IN} = 1.5\text{V}$, $I_{LOAD} = 100\text{mA}$		1.5		Ω
		$V_{IN} = 1.8\text{V}$, $I_{LOAD} = 100\text{mA}$		1.2		
		$V_{IN} = 2.5\text{V}$, $I_{LOAD} = 100\text{mA}$		0.85		
		$V_{IN} = 3.3\text{V}$, $I_{LOAD} = 100\text{mA}$		0.7		
Current Limit (Switch mode)	I_{CL}	$V_{OUT} = 0\text{V}$		400		mA
Start-up time	t_{start_up}	No load, Output cap 2.2 μF , 90% of V_{OUT}		10		μs
Shutdown time	t_{shut_down}	No load, Output cap 2.2 μF , 10% of V_{OUT}			10	ms

LDO4, LDO5, LDO6

Unless otherwise noted: $V_{IN} = 3.8\text{V}$, $V_{OUT} = 1.8\text{V}$, $T_J = -40^\circ\text{C to } +125^\circ\text{C}$; Typical values are at $T_J = +25^\circ\text{C}$.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		1.5		5.5	V
Programmable Output Voltage	V_{OUT}		0.9		3.3	V
V_{OUT} Step Size	V_{OUT_STEP}	$V_{OUT} = 0.9\text{V to } 1.6\text{V}$		50		mV
		$V_{OUT} = 1.7\text{V to } 3.3\text{V}$		100		
Output Current	I_{OUT}	Normal mode	0		100	mA
		Low power mode, $LDO_{n_LP_MODE}=0$	0		50	
		Low power mode, $LDO_{n_LP_MODE}=1$	0		20	
V_{OUT} Accuracy	V_{OUT_ACC}	$I_{LOAD} = 1\text{mA}$	-3		3	%
Line Regulation	V_{OUT_LINE}	$V_{IN} = (V_{OUT} + 0.5)$ to 5.5V, $I_{LOAD} = 50\text{mA}$ Note that V_{IN} must be $\geq 1.5\text{V}$		0.1		%/V
Load Regulation	V_{OUT_LOAD}	$I_{LOAD} = 1\text{mA to } 100\text{mA}$		0.022		%/mA
Dropout Voltage	$V_{IN} - V_{OUT}$	$I_{LOAD} = 100\text{mA}$, $V_{OUT} > 2.7\text{V}$		200		mV
		$I_{LOAD} = 100\text{mA}$, $V_{OUT} 1.8\text{V to } 2.7\text{V}$		250		
		$I_{LOAD} = 100\text{mA}$, $V_{OUT} < 1.8\text{V}$		400		
Undervoltage level	V_{OUT}	V_{OUT} Falling		88		%
Quiescent Current	I_Q	Normal mode, no load		30		μA
		Low power mode, $LDO_{n_LP_MODE}=0$, no load		10		
		Low power mode, $LDO_{n_LP_MODE}=1$, no load		5		
		$I_{LOAD} = 1\text{mA to } 100\text{mA}$		I_Q (no load) + 1% of load		
Power Supply Rejection Ratio	PSRR	$I_{LOAD} = 50\text{mA}$, $\leq 1\text{kHz}$		55		dB
		$I_{LOAD} = 50\text{mA}$, 10kHz		55		
		$I_{LOAD} = 50\text{mA}$, 100kHz		32		
On Resistance (Switch mode)	R_{DSON}	$V_{IN} = 1.5\text{V}$, $I_{LOAD} = 100\text{mA}$		3.2		Ω
		$V_{IN} = 1.8\text{V}$, $I_{LOAD} = 100\text{mA}$		2.1		
		$V_{IN} = 2.5\text{V}$, $I_{LOAD} = 100\text{mA}$		1.35		
		$V_{IN} = 3.3\text{V}$, $I_{LOAD} = 100\text{mA}$		1.1		

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Limit (Switch mode)	I_{CL}	$V_{OUT} = 0V$		230		mA
Start-up time	t_{start_up}	No load, Output cap 2.2 μF , 90% of V_{OUT}		10		μs
Shutdown time	t_{shut_down}	No load, Output cap 2.2 μF , 10% of V_{OUT}			10	ms

LDO7, LDO8

Unless otherwise noted: $V_{IN} = 3.8V$, $V_{OUT} = 1.8V$, $T_J = -40^\circ C$ to $+125^\circ C$; Typical values are at $T_J = +25^\circ C$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		1.71		5.5	V
Programmable Output Voltage	V_{OUT}		1.0		3.5	V
V_{OUT} Step Size	V_{OUT_STEP}	$V_{OUT} = 1.0V$ to $1.6V$		50		mV
		$V_{OUT} = 1.7V$ to $3.5V$		100		
Output Current	I_{OUT}	Normal mode	0		200	mA
		Low Power mode	0		50	
V_{OUT} Accuracy	V_{OUT_ACC}	$I_{LOAD} = 1mA$	-2.5		+2.5	%
Line Regulation	V_{OUT_LINE}	$V_{IN} = (V_{OUT} + 0.5)$ to $5.5V$, $I_{LOAD} = 100mA$ Note that V_{IN} must be $\geq 1.71V$		0.025		%/V
Load Regulation	V_{OUT_LOAD}	$I_{LOAD} = 1mA$ to $200mA$		0.003		%/mA
Dropout Voltage	$V_{IN} - V_{OUT}$	$I_{LOAD} = 100mA$, $V_{OUT} = 1.8V$		95		mV
		$I_{LOAD} = 100mA$, $V_{OUT} = 2.5V$		65		
		$I_{LOAD} = 100mA$, $V_{OUT} = 3.3V$		60		
Undervoltage level	V_{OUT}	V_{OUT} Falling		93		%
Quiescent Current	I_Q	Normal mode, no load		110		μA
		Low Power mode, no load		70		
		$I_{LOAD} = 1mA$ to $200mA$		I_Q (no load) + 0.1% of load		
Power Supply Rejection Ratio	PSRR	$I_{LOAD} = 100mA$, $\leq 1kHz$		70		dB
		$I_{LOAD} = 100mA$, $10kHz$		67		
		$I_{LOAD} = 100mA$, $100kHz$		48		
Output noise voltage	V_{OUT}	$f = 10Hz$ to $100kHz$; $V_{OUT} = 2.8V$, $I_{LOAD} = 1mA$		30		μV_{RMS}
		$f = 10Hz$ to $100kHz$; $V_{OUT} = 2.8V$, $I_{LOAD} = 10mA$		32		
		$f = 10Hz$ to $100kHz$; $V_{OUT} = 2.8V$, $I_{LOAD} = 100mA$		32		
On Resistance (Switch mode)	$R_{DS(on)}$	$V_{IN} = 1.71V$, $I_{LOAD} = 100mA$		550		m Ω
		$V_{IN} = 1.8V$, $I_{LOAD} = 100mA$		500		
		$V_{IN} = 2.5V$, $I_{LOAD} = 100mA$		330		
		$V_{IN} = 3.5V$, $I_{LOAD} = 100mA$		250		
Current Limit (Switch mode)	I_{CL}	$V_{OUT} = 0V$		320		mA
Start-up time	t_{start_up}	No load, Output cap 4.7 μF , 90% of V_{OUT}		50		μs
Shutdown time	t_{shut_down}	No load, Output cap 4.7 μF , 10% of V_{OUT}			10	ms

LDO9, LDO10

Unless otherwise noted: $V_{IN} = 3.8V$, $V_{OUT} = 1.8V$, $T_J = -40^\circ C$ to $+125^\circ C$; Typical values are at $T_J = +25^\circ C$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		1.71		5.5	V
Programmable Output Voltage	V_{OUT}		1.0		3.5	V
V_{OUT} Step Size	V_{OUT_STEP}	$V_{OUT} = 1.0V$ to $1.6V$		50		mV
		$V_{OUT} = 1.7V$ to $3.5V$		100		
Output Current	I_{OUT}	Normal mode	0		150	mA
		Low Power mode	0		50	

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OUT} Accuracy	V _{OUT_ACC}	I _{LOAD} = 1mA	-2.5		+2.5	%
Line Regulation	V _{OUT_LINE}	V _{IN} = (V _{OUT} + 0.5) to 5.5V, I _{LOAD} = 75mA Note that V _{IN} must be >= 1.71V		0.025		%/V
Load Regulation	V _{OUT_LOAD}	I _{LOAD} = 1mA to 150mA		0.004		%/mA
Dropout Voltage	V _{IN} - V _{OUT}	I _{LOAD} = 100mA, V _{OUT} = 1.8V		135		mV
		I _{LOAD} = 100mA, V _{OUT} = 2.5V		100		
		I _{LOAD} = 100mA, V _{OUT} = 3.3V		90		
Undervoltage level	V _{OUT}	V _{OUT} Falling		93		%
Quiescent Current	I _Q	Normal mode, no load		110		μA
		Low Power mode, no load		70		
		I _{LOAD} = 1mA to 150mA	I _Q (no load) + 0.1% of load			
Power Supply Rejection Ratio	PSRR	I _{LOAD} = 75mA, <= 1kHz		73		dB
		I _{LOAD} = 75mA, 10kHz		69		
		I _{LOAD} = 75mA, 100kHz		49		
Output noise voltage	V _{OUT}	f=10Hz to 100kHz; V _{OUT} =2.8V, I _{LOAD} = 1mA		30		μV _{RMS}
		f=10Hz to 100kHz; V _{OUT} =2.8V, I _{LOAD} = 10mA		32		
		f=10Hz to 100kHz; V _{OUT} =2.8V, I _{LOAD} = 100mA		32		
On Resistance (Switch mode)	R _{DSON}	V _{IN} = 1.71V, I _{LOAD} = 100mA		1000		mΩ
		V _{IN} = 1.8V, I _{LOAD} = 100mA		930		
		V _{IN} = 2.5V, I _{LOAD} = 100mA		610		
		V _{IN} = 3.5V, I _{LOAD} = 100mA		430		
Current Limit (Switch mode)	I _{CL}	V _{OUT} = 0V		250		mA
Start-up time	t _{start_up}	No load, Output cap 4.7 μF, 90% of V _{OUT}		70		μs
Shutdown time	t _{shut_down}	No load, Output cap 4.7 μF, 10% of V _{OUT}			10	ms

LDO11

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.2V, T_J = -40°C to +125°C; Typical values are at T_J = +25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Programmable Output Voltage	V _{OUT}		0.8		1.55	V
V _{OUT} Step Size	V _{OUT_STEP}			50		mV
Output Current	I _{OUT}	PVDD < 3.1V	0		10	mA
		PVDD ≥ 3.1V	0		25	
V _{OUT} Accuracy	V _{OUT}	V _{IN} = 2.7 to 5.5V; I _{LOAD} = 100μA	-4		+4	%
Line Regulation	V _{OUT_LINE}	V _{IN} = 2.7 to 5.5V; I _{LOAD} = 1mA		0.4		%/V
Load Regulation	V _{OUT_LOAD}	I _{LOAD} = 100μA to 10mA		0.2		%/mA
Quiescent Current	I _Q	No load		2.5		μA
Start-up time	t _{start_up}	No load, Output cap 0.1 μF, 90% of V _{OUT}		0.3	1	ms
Shutdown time	t _{shut_down}	No load, Output cap 0.1 μF, 10% of V _{OUT}		0.3	1	ms

7.3 RESET THRESHOLDS

Unless otherwise noted: $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$; Typical values are at $T_J = +25^{\circ}\text{C}$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power On Reset						
Power on Reset threshold VPMIC (LDO12VOUT) voltage at which device transitions between NO POWER and BACKUP states	$V_{\text{POR, DE-ASSERT}}$	VPMIC rising		1.18		V
	$V_{\text{POR, ASSERT}}$	VPMIC falling		1.08		V
Power on Reset hysteresis	$V_{\text{POR, HYST}}$			100		mV
Device Reset Control						
Device Reset threshold VPMIC (LDO12VOUT) voltage at which device transitions between BACKUP and OFF states	$V_{\text{RES, DE-ASSERT}}$	VPMIC rising		1.89		V
	$V_{\text{RES, ASSERT}}$	VPMIC falling		1.80		V
Device Reset hysteresis	$V_{\text{RES, HYST}}$			90		mV
Device Shutdown						
Shutdown threshold PVDD voltage at which the device forces an OFF transition	V_{SHUTDOWN}	PVDD falling		2.7		V
SYSLO threshold accuracy PVDD voltage at which SYSLO is asserted	V_{SYSLO}	PVDD falling, V_{SYSLO} set by SYSLO_THR (2.8V to 3.5V)	-3		+3	%
SYSOK threshold accuracy PVDD voltage at which SYSOK is asserted.	V_{SYSOK}	PVDD rising, V_{SYSOK} set by SYSOK_THR (2.8V to 3.5V) Note the SYSOK hysteresis margin ($V_{\text{SYSOK, HYST}}$) is added to SYSOK_THR.	-3		+3	%
SYSOK hysteresis	$V_{\text{SYSOK, HYST}}$			40		mV

7.4 REFERENCES

Unless otherwise noted: $T_J = +25^{\circ}\text{C}$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage Reference	V_{VREFC}			0.8		V
Current Reference	V_{IREFR}	100k Ω to GND		0.5		V

7.5 GENERAL PURPOSE INPUTS / OUTPUTS (GPIO)

Unless otherwise noted: $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$; Typical values are at $T_J = +25^{\circ}\text{C}$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO1, GPIO2, GPIO3, GPIO7, GPIO8, GPIO9						
Input HIGH Level	V_{IH}		0.75 x VDD			V
Input LOW Level	V_{IL}				0.25 x VDD	V
Output HIGH Level	V_{OH}	$I_{OH} = 1\text{mA}$	0.8 x VDD			V
Output LOW Level	V_{OL}	$I_{OL} = -1\text{mA}$			0.2 x VDD	V
Pull-up resistance to VDD	R_{PU}	GPn_PWR_DOM=0 and DBVDD=1.8V or GPn_PWR_DOM=1		180		k Ω
Pull-down resistance	R_{PD}			180		k Ω
GPIO4, GPIO5, GPIO6, GPIO10, GPIO11, GPIO12						
Input HIGH Level	V_{IH}		0.85 x VDD			V
Input LOW Level	V_{IL}				0.2 x VDD	V
Output HIGH Level	V_{OH}	$I_{OH} = 1\text{mA}$	0.75 x VDD			V
Output LOW Level	V_{OL}	$I_{OL} = -1\text{mA}$			0.2 x VDD	V
Pull-up resistance to VDD	R_{PU}	GPn_PWR_DOM=0 and DBVDD=1.8V or GPn_PWR_DOM=1 and PVDD=3.8V		180		k Ω
Pull-down resistance	R_{PD}			180		k Ω

Notes:

1. 'VDD' is the voltage of the applicable power domain for each pin (selected by the corresponding GPn_PWR_DOM register).
2. Pull-up / pull-down resistance only applies when enabled using the GPn_PULL registers.
3. Pull-up / pull-down resistors are disabled when the GPIO pin is tri-stated.
4. Pull-up / pull-down resistance may change with the applicable power domain (as selected by GPn_PWR_DOM).

7.6 DIGITAL INTERFACES

Unless otherwise noted: $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$; Typical values are at $T_J = +25^{\circ}\text{C}$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ON, RESET, IRQ, CIFMODE, SDOOUT1, SCLK1, SDA1, CS						
Input HIGH Level	V_{IH}		0.75 x VDD			V
Input LOW Level	V_{IL}				0.2 x VDD	V
Output HIGH Level	V_{OH}	$I_{OH} = 1\text{mA}$	0.8 x VDD			V
Output LOW Level	V_{OL}	$I_{OL} = -1\text{mA}$			0.2 x VDD	V
'VDD' is the voltage of the applicable power domain for each pin, as defined in Section 3.						
ON pin pull-up resistance	R_{PU}			140		k Ω
RESET pin pull-up resistance	R_{PU}	DBVDD=1.8V		180		k Ω
		DBVDD=3.6V		85		
IRQ pin pull-up resistance	R_{PU}	DBVDD=1.8V		180		k Ω
		DBVDD=3.6V		85		

7.7 AUXILIARY ADC

Unless otherwise noted: $T_J = +25^{\circ}\text{C}$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input resistance	$R_{GPIO10, 11, 12}$	During measurement		400		k Ω
Input voltage range	$V_{GPIO10, 11, 12}$	GPn_PWR_DOM = 0	0		V_{DBVDD}	V
		GPn_PWR_DOM = 1	0		V_{PVDD}	
Input capacitance	$C_{GPIO10, 11, 12}$			2		pF
AUXADC Resolution				12		bits
AUXADC Conversion Time				39		μs
AUXADC accuracy		Input voltage = 3V	-2.5		+2.5	%

7.8 SYSTEM STATUS LED DRIVERS

Unless otherwise noted: $T_J = +25^{\circ}\text{C}$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LED1 and LED2						
Sink current		$V_{LED1/2} = 1\text{V}$		10		mA

8 TYPICAL POWER CONSUMPTION

Data to follow

9 TYPICAL PERFORMANCE DATA

9.1 DC-DC CONVERTERS

Data to follow

9.2 LDO REGULATORS

Data to follow

10 SIGNAL TIMING REQUIREMENTS

10.1 CONTROL INTERFACE

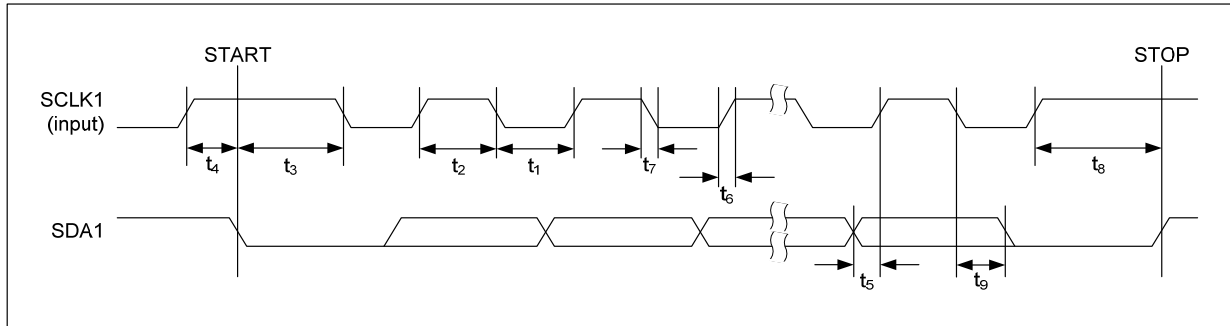


Figure 1 Control Interface Timing - 2-wire (I2C) Control Mode

Test Conditions

$T_j = -40^\circ\text{C}$ to $+125^\circ\text{C}$ unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK1 Frequency		0		400	kHz
SCLK1 Low Pulse-Width	t_1	1300			ns
SCLK1 High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDA1, SCLK1 Rise Time	t_6			300	ns
SDA1, SCLK1 Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

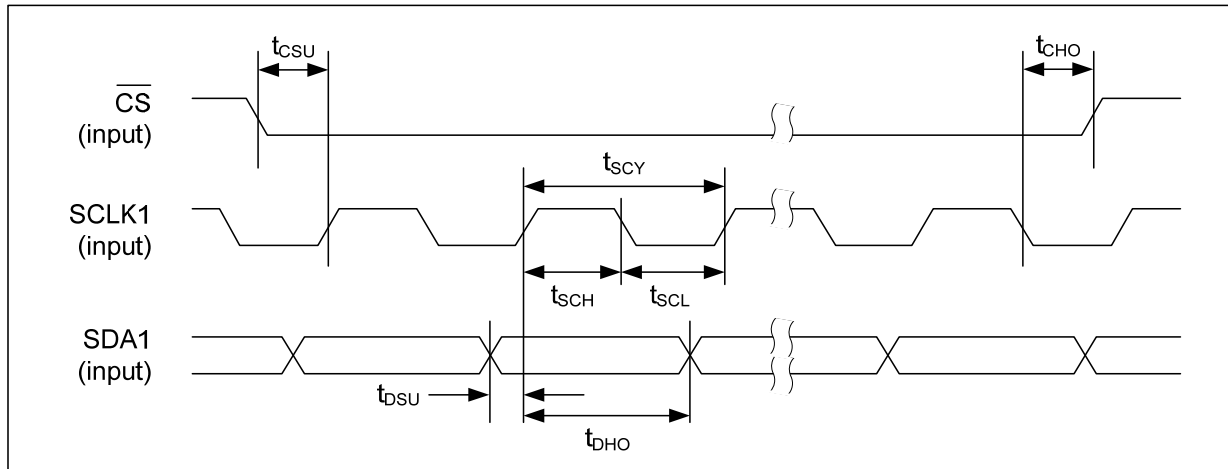


Figure 2 Control Interface Timing - 4-wire (SPI) Control Mode (Write Cycle)

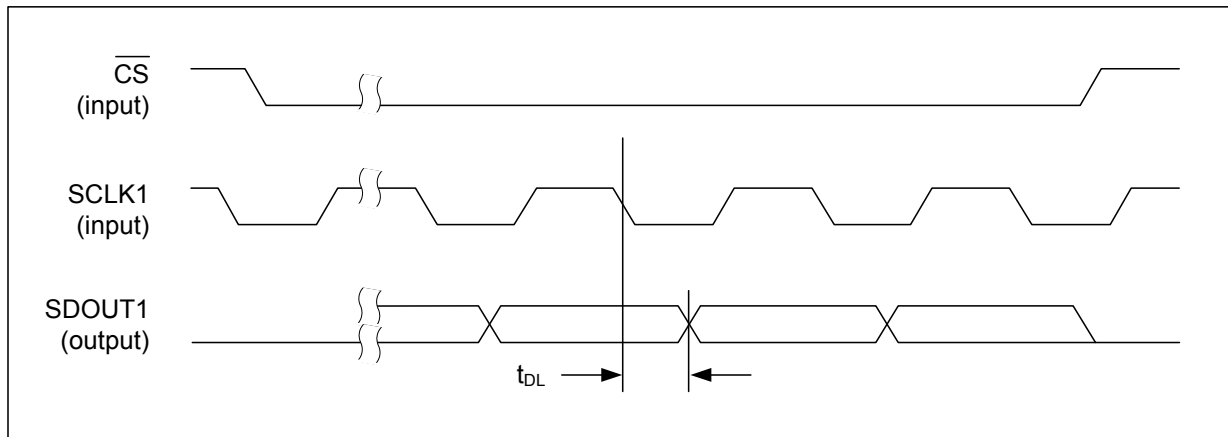


Figure 3 Control Interface Timing - 4-wire (SPI) Control Mode (Read Cycle)

Test Conditions

$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
$\overline{\text{CS}}$ falling edge to SCLK1 rising edge	t_{CSU}	40			ns
SCLK1 falling edge to $\overline{\text{CS}}$ rising edge	t_{CHO}	10			ns
SCLK1 pulse cycle time	t_{SCY}	200			ns
SCLK1 pulse width low	t_{SCL}	80			ns
SCLK1 pulse width high	t_{SCH}	80			ns
SDA1 to SCLK1 set-up time	t_{DSU}	40			ns
SDA1 to SCLK1 hold time	t_{DHO}	10			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns
SCLK1 falling edge to SDOUT1 transition	t_{DL}			40	ns

The $\overline{\text{CS}}$ pin must be held high for at least $1\mu\text{s}$ after every register write operation in SPI mode.

11 DEVICE DESCRIPTION

11.1 GENERAL DESCRIPTION

The WM8325-00C is a multi-purpose Power Management device with a comprehensive range of features. The WM8325-00C provides 4 DC-DC synchronous buck converters and 11 LDO regulators which are all programmable to application-specific requirements. The on-board oscillator and two additional LDOs support the clocking and control functions for the DC-DC converters and other core functions.

The WM8325-00C provides a 32.768kHz crystal oscillator and secure Real Time Clock (SRTC). An auxiliary ADC is included, for measurement of external voltages. Other features include flexible GPIO capability, and LED outputs for system status indications.

Under typical operating conditions, the device is powered up and shut down under the control of the \overline{ON} pin. The device executes a controlled sequence of enabling or disabling the DC-DC converters, LDOs and other functions when commanded to power up or shut down respectively. An alternate device state (SLEEP power state) is provided, in which selected functions may be separately configured for a low-power or other operating condition. The configuration of the normal operating state is stored on the integrated OTP non-volatile memory - this is optimised for compatibility with the Freescale i.MX53 processor.

In the absence of a main power supply, the WM8325-00C automatically reverts to a backup state, under which a minimal functionality is maintained to enable a smooth return to normal operation when the supply is restored. With a backup battery present, the RTC is updated in the backup state, allowing the main battery to be depleted or changed without loss of RTC function. Without a backup battery, a small capacitor is sufficient to maintain the RTC (unlocked) for up to 5 minutes.

11.2 POWER STATES

The WM8325-00C has 5 main power states, which are described below. Different levels of functionality are associated with each of the power states. Some of the state transitions are made autonomously by the WM8325-00C (eg. transitions to/from BACKUP are scheduled according to the available power supply conditions). Other transitions are initiated as a result of instructions issued over the Control Interface or as a result of software functions (eg. Watchdog timer) or hardware functions such as the \overline{ON} pin. The valid transitions and the associated conditions are detailed below.

NO POWER - This is the device state when no power is available. All functions are disabled and all register data is lost.

OFF - This is the device state when power is available but the device is switched off. The RTC is enabled and the register map contents are maintained. The RESET pin is pulled low in this state. LDO11 may optionally be enabled in this state; all other DC-DCs and LDOs are disabled (apart from LDO12, which supports internal functions).

ON - This is the normal operating state when the device is switched on. All device functions are available in this state.

SLEEP - This is a user-configurable operating state which is intended for a low-power operating condition. Selected functions may be enabled, disabled or re-configured according to the user's requirements. A programmable configuration sequence for the DC-DCs and LDOs is executed on transition to/from SLEEP mode.

BACKUP - This is the operating state when the PVDD power supply is below the reset threshold of the device. Typically, this means that the PVDD supply has been removed. All DC-DC converters and LDO regulators are disabled in this state. The RTC and oscillator and a 'software scratch' memory area can be maintained from the backup supply (if available) in this state. All other functions and registers are reset in BACKUP. (Note that, for power saving, an 'unlocked' mode, in which the RTC is held constant, may be selected if required.)

The valid power state transitions are illustrated in Figure 4.

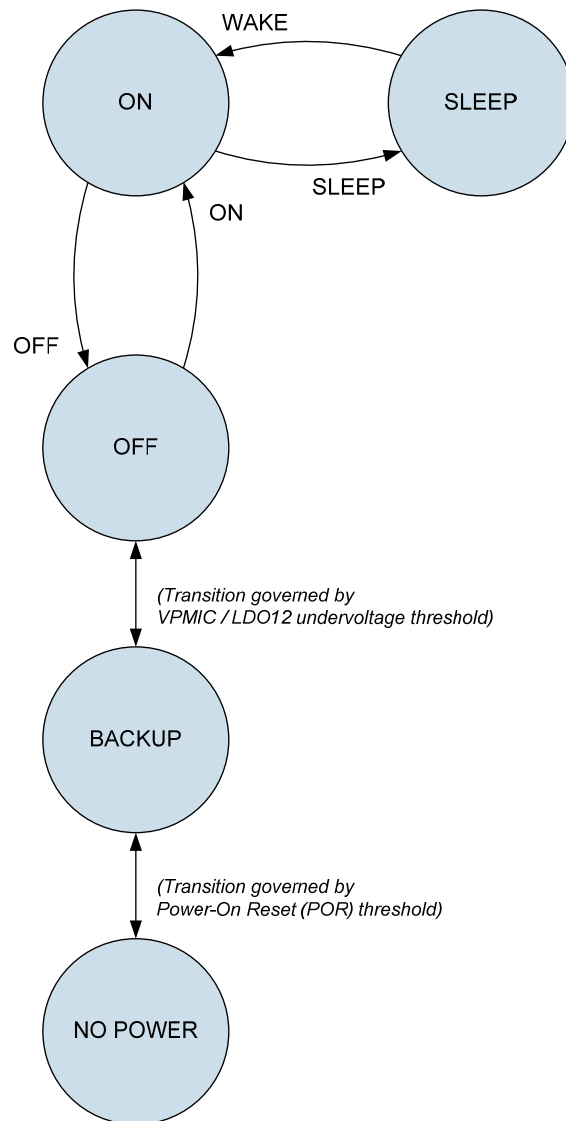


Figure 4 Power States and Transitions

State transitions to/from the NO POWER state are controlled automatically by the internal supply (VPMIC) voltage generated by LDO12. The device is in the NO POWER state when this voltage is below the Power-On Reset (POR) threshold. See Section 24 for more details on Power-On Reset.

State transitions to/from the BACKUP state are controlled automatically by the internal supply (VPMIC) voltage generated by LDO12. The device is in the BACKUP state when this voltage is below the Device Reset threshold. See Section 24 for more details on Resets.

The remaining transitions between the OFF, ON and SLEEP states may be initiated by a number of different mechanisms - some of them automatic, some of them user-controlled. Transitions between these states are time-controlled sequences of events. These are the OFF, ON, SLEEP and WAKE sequences shown in Figure 4. These transitions are programmable, using data stored in the integrated OTP memory. See Section 14 for details.

Note that a transition from the SLEEP state to the OFF state is not a controlled transition. If an 'OFF' event occurs whilst in the SLEEP state, then the WM8325-00C will select the OFF state, but all the enabled converters and regulators will be disabled immediately; the time-controlled sequence is not implemented in this case. See Section 11.3 for details of the WM8325-00C 'OFF' events.

The current power state of the WM8325-00C can be read from the MAIN_STATE register field. A restricted definition of this field is shown in Table 1. Note that other values of MAIN_STATE are

defined for transition states, but it is recommended that only the values quoted below should be used to confirm power state transitions.

A power state transition to the BACKUP, SLEEP, ON or OFF state is indicated by the Interrupt bits described in Section 11.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16397 (400Dh) System Status	4:0	MAIN_STATE [4:0]	0_0000	Main State Machine condition 0_0000 = OFF 1_1100 = SLEEP 1_1111 = ACTIVE (ON)

Table 1 Power State Readback

11.3 POWER STATE CONTROL

The OFF, ON, SLEEP and WAKE sequences are initiated by many different conditions. When such a condition occurs, the WM8325-00C schedules a series of 5 timeslots, enabling a sequence of enable/disable events to be controlled. The nominal duration of the timeslots is fixed at 2ms, though this may be extended if any selected circuit has not started up within this time, as described later in this section. The OFF, SLEEP and WAKE sequences commence after a programmable delay set by PWRSTATE_DLY. This allows a host processor to request a WM8325-00C state transition and then complete other tasks before the transition actually occurs.

The ON sequence is the transition from OFF to ON power states. Each LDO and each DC-DC Converter is associated with one of the available timeslots in the ON sequence. This determines the time, within the sequence, at which that DC-DC Converter or LDO will be enabled following an 'ON' event. See Section 30.2 for details of the ON sequence that is implemented on the WM8325-00C.

The clock output (CLKOUT) and GPIO pins configured as External Power Enable (EPE) outputs can also be associated with any one of the available timeslots in the ON sequence. The EPE function is a logic output that may be used to control external circuits, including external DC-DC converters.

An example 'ON' state transition sequence is illustrated in Figure 5. Each of the DC-DC Converters and LDO regulators is individually assigned to one of the five timeslots (shown as T1, T2, T3, T4, T5), providing total flexibility in the power sequence. See Section 30.2 for details of the ON sequence that is implemented on the WM8325-00C.

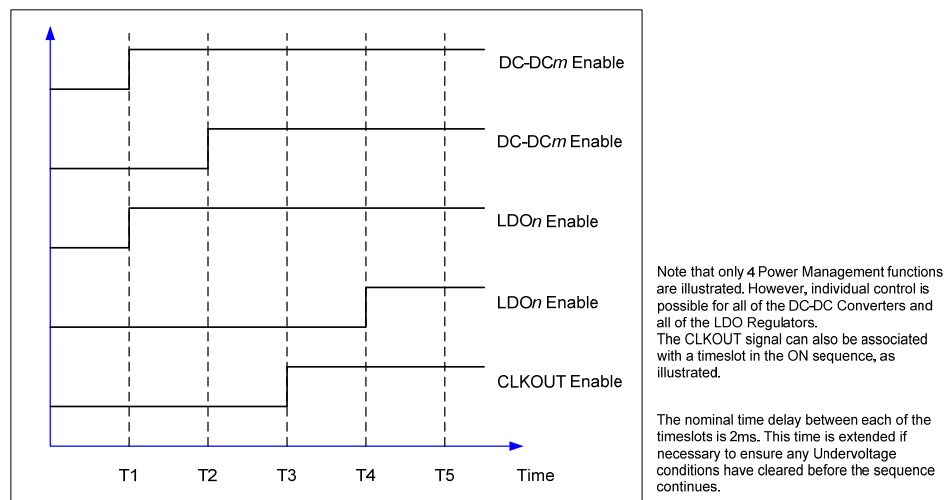


Figure 5 Example Control Sequence for 'ON' State Transition

The possible 'ON' events that may trigger the ON sequence are listed in Table 3. The ON sequence is only permitted when the supply voltage PVDD exceeds a programmable threshold SYSOK. See Section 24 for details of PVDD voltage monitoring.

The OFF sequence is the reverse of the ON sequence. Each DC-DC Converter, LDO Regulator or GPIO output that is associated with a timeslot in the ON sequence is switched off in the reverse sequence following an 'OFF' event. If CLKOUT is assigned to a timeslot in the ON sequence, then this is disabled in the reverse (OFF) sequence also.

The possible 'OFF' events are listed in Table 3. Note that it is possible to modify the OFF sequence by writing to the associated registers in the ON power state if required; this allows the OFF sequence to be independent of the ON sequence.

The SLEEP sequence is the transition from ON to SLEEP power states. Each LDO and each DC-DC Converter may be associated with any one of the available timeslots in the SLEEP sequence. This determines the time, within the sequence, at which that DC Converter or LDO will be disabled following a 'SLEEP' event.

Note that the SLEEP sequence is not pre-configured on the WM8325-00C; this must be programmed as required using the register settings described in Section 15.3.

The clock output (CLKOUT) and GPIO pins configured as External Power Enable (EPE) outputs can also be associated with any one of the available timeslots in the SLEEP sequence. The possible 'SLEEP' events are listed in Table 3.

The WAKE sequence is the reverse of the SLEEP sequence. Each DC-DC Converter, LDO Regulator or GPIO output that is associated with a timeslot in the SLEEP sequence is switched on in the reverse sequence following a 'WAKE' event. If CLKOUT is assigned to a timeslot in the SLEEP sequence, then this is disabled in the reverse (WAKE) sequence also.

The possible 'WAKE' events are listed in Table 3. Note that it is possible to modify the WAKE sequence by writing to the associated registers in the SLEEP power state if required; this allows the WAKE sequence to be independent of the SLEEP sequence.

Any DC-DC Converter or LDO that is not associated with one of the 5 timeslots in the ON sequence may, instead, be configured to be hardware controlled via a GPIO pin configured as one of the Hardware Enable inputs. See Section 21 for details of the GPIO functions. Any DC-DC Converter or LDO that is not under Hardware control may be enabled or disabled under Software control in the ON state, regardless of whether it is associated with any timeslot in the ON sequence.

When a valid OFF event occurs, any DC-DC Converter or LDO which is not allocated a timeslot in the ON sequence is disabled immediately. This includes any DC-DC Converter or LDO which is under GPIO (Hardware Enable) control. The only exception is LDO11 which may, optionally, be configured to be enabled in the OFF state.

The WM8325-00C monitors the DC-DC Converters and LDOs during the ON sequence to ensure that the required circuits have powered up successfully before proceeding to the next timeslot. The nominal timeslot durations are extended if necessary in order to wait for the selected DC-DC Converters or LDOs to power up. If the ON sequence has not completed within 2 seconds of starting the transition, then a Power Sequence Failure has occurred, resulting in the OFF state being forced.

The most recent ON or WAKE event can be determined by reading the bits in the "ON Source" register, R400Eh. The most recent OFF event can be determined by reading the bits in the "OFF Source" register, R400Fh.

The "ON Source" register is updated when a new ON event occurs. The "OFF Source" register is updated when a new OFF event occurs. Note that some Reset conditions (see Section 24) result in an OFF transition followed by an ON transition; these events are recorded as Reset events in the "ON Source" register.

The ON Source and OFF Source register fields are defined in Table 2.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16387 (4003h) Power State	15	CHIP_ON	0	Indicates whether the system is ON or OFF. 0 = OFF 1 = ON (or SLEEP) OFF can be commanded by writing CHIP_ON = 0. Note that writing CHIP_ON = 1 is not a valid 'ON' event, and will not trigger an ON transition.
	14	CHIP_SLP	0	Indicates whether the system is in the SLEEP state. 0 = Not in SLEEP 1 = SLEEP WAKE can be commanded by writing CHIP_SLP = 0. SLEEP can be commanded by writing CHIP_SLP = 1.
	11:10	PWRSTATE_DLY	10	Power State transition delay 00 = No delay 01 = No delay 10 = 1ms 11 = 10ms
R16398 (400Eh) ON Source	15	ON_TRANS	0	Most recent ON/WAKE event type 0 = WAKE transition 1 = ON transition
	11	ON_GPIO	0	Most recent ON/WAKE event type 0 = Not caused by GPIO input 1 = Caused by GPIO input
	10	ON_SYSLO	0	Most recent WAKE event type 0 = Not caused by PVDD 1 = Caused by SYSLO threshold. Note that the SYSLO threshold cannot trigger an ON event.
	7	ON_WDOG_TO	0	Most recent WAKE event type 0 = Not caused by Watchdog timer 1 = Caused by Watchdog timer
	6	ON_SW_REQ	0	Most recent WAKE event type 0 = Not caused by software WAKE 1 = Caused by software WAKE command (CHIP_SLP = 0)
	5	ON_RTC_ALM	0	Most recent ON/WAKE event type 0 = Not caused by RTC Alarm 1 = Caused by RTC Alarm
	4	ON_ON_PIN	0	Most recent ON/WAKE event type 0 = Not caused by the ON pin 1 = Caused by the ON pin
	3	RESET_CNV_UV	0	Most recent ON event type 0 = Not caused by undervoltage 1 = Caused by a Device Reset due to a Converter (LDO or DC-DC) undervoltage condition
	2	RESET_SW	0	Most recent ON event type 0 = Not caused by Software Reset 1 = Caused by Software Reset

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	RESET_HW	0	Most recent ON event type 0 = Not caused by Hardware Reset 1 = Caused by Hardware Reset
	0	RESET_WDOG	0	Most recent ON event type 0 = Not caused by the Watchdog 1 = Caused by a Device Reset triggered by the Watchdog timer
R16399 (400Fh) OFF Source	13	OFF_INTLDO_ERR	0	Most recent OFF event type 0 = Not caused by LDO13 Error condition 1 = Caused by LDO13 Error condition
	12	OFF_PWR_SEQ	0	Most recent OFF event type 0 = Not caused by Power Sequence Failure 1 = Caused by a Power Sequence Failure
	11	OFF_GPIO	0	Most recent OFF event type 0 = Not caused by GPIO input 1 = Caused by GPIO input
	10	OFF_PVDD	0	Most recent OFF event type 0 = Not caused by PVDD 1 = Caused by the SYSLO or SHUTDOWN threshold
	9	OFF_THERR	0	Most recent OFF event type 0 = Not caused by temperature 1 = Caused by over-temperature
	6	OFF_SW_REQ	0	Most recent OFF event type 0 = Not caused by software OFF 1 = Caused by software OFF command (CHIP_ON = 0)
	4	OFF_ON_PIN	0	Most recent OFF event type 0 = Not caused by the ON pin 1 = Caused by the ON pin

Table 2 Power State Control Registers

Table 3 lists all of the events which can trigger an ON, WAKE, OFF or SLEEP transition sequence. It also lists the associated status bits of the 'ON Source' and 'OFF Source' register bits which are asserted under each condition.

TRANSITION SEQUENCE	EVENT	NOTES	ON SOURCE / OFF SOURCE
ON (see note 1)	RTC alarm	An ON request occurs if the RTC Alarm occurs in the OFF power state. See Section 20.	ON_TRANS, ON_RTC_ALM
	GPIO ON request	Requires a GPIO to be configured as "Power On request" or "Power On/Off request". See Section 21.	ON_TRANS, ON_GPIO
	$\overline{\text{ON}}$ pin request	Requires the $\overline{\text{ON}}$ pin to be configured to generate ON request. See Section 11.6.	ON_TRANS, ON_ON_PIN
WAKE	Software WAKE	Writing CHIP_SLP = 0. See Table 2.	ON_SW_REQ
	Watchdog timeout	Requires the Watchdog to be configured to generate WAKE request. See Section 25.	ON_WDOG_TO
	RTC alarm	A WAKE request occurs if the RTC Alarm occurs in the SLEEP power state. See Section 20.	ON_RTC_ALM
	GPIO WAKE request	Requires a GPIO to be configured as "Sleep/Wake request". See Section 21.	ON_GPIO
	PVDD undervoltage	Requires the PVDD monitor circuit to be configured to generate WAKE request. See Section 24.4.	ON_SYSLO
	$\overline{\text{ON}}$ pin request	Requires the $\overline{\text{ON}}$ pin to be configured to generate WAKE request. See Section 11.6.	ON_ON_PIN
OFF	Watchdog timeout	Requires the Watchdog to be configured to generate Device Reset. See Section 25.	RESET_WDOG (See note 2)
	Hardware Reset	See Section 24.	RESET_HW (See note 2)
	Software Reset	See Section 24.	RESET_SW (See note 2)
	Power Management Undervoltage Reset	Configurable option for each LDO/DC-DC converter. See Section 15.	RESET_CNV_UV (See note 2)
	Software OFF request	Writing CHIP_ON = 0. See Table 2.	OFF_SW_REQ
	ON pin request	Requires the $\overline{\text{ON}}$ pin to be configured to generate OFF request. See Section 11.6.	OFF_ON_PIN
	Thermal shutdown	See Section 26.	OFF_THERR
	PVDD undervoltage	Requires the PVDD monitor circuit to be configured to generate OFF request. See Section 24.4.	OFF_PVDD
	PVDD shutdown	PVDD has fallen below the SHUTDOWN threshold. See Section 24.4.	OFF_PVDD
	GPIO OFF request	Requires a GPIO to be configured as "Power On/Off request". See Section 21.	OFF_GPIO
	Power Sequence failure	DC-DC converters, LDOs or CLKOUT circuits have failed to start up within the permitted time.	OFF_PWR_SEQ
	Internal LDO error	Error condition detected in LDO13	OFF_INTLDO_ERR
SLEEP	Software SLEEP request	Writing CHIP_SLP = 1. See Table 2.	See note 3
	GPIO SLEEP request	Requires a GPIO to be configured as "Sleep request" or "Sleep/Wake request". See Section 21.	See note 3

Table 3 Power State Transition Events

Notes:

1. An ON sequence is only permitted when the supply voltage PVDD exceeds a programmable threshold V_{SYSOK} . See Section 24.4 for details of PVDD voltage monitoring.
2. These Reset conditions result in an OFF transition followed by an ON transition. These events are recorded as Reset events in the 'ON Source' register.
3. SLEEP events are not recorded in the 'OFF Source' register.

11.4 POWER STATE INTERRUPTS

Power State transitions are associated with a number of Interrupt event flags. Transitions to BACKUP, SLEEP, ON or OFF states are indicated by the Interrupt bits described in Table 4. Each of these secondary interrupts triggers a primary Power State Interrupt, PS_INT (see Section 23). This can be masked by setting the mask bit(s) as described in Table 4.

ADDRESS	BIT	LABEL	DESCRIPTION
R16402 (4012h) Interrupt Status 2	2	PS_POR_EINT	Power On Reset interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
	1	PS_SLEEP_OFF_EINT	SLEEP or OFF interrupt (Power state transition to SLEEP or OFF states) (Rising Edge triggered) Note: Cleared when a '1' is written.
	0	PS_ON_WAKE_EINT	ON or WAKE interrupt (Power state transition to ON state) (Rising Edge triggered) Note: Cleared when a '1' is written.
R16410 (401Ah) Interrupt Status 2 Mask	2	IM_PS_POR_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	1	IM_PS_SLEEP_OFF_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	0	IM_PS_ON_WAKE_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 4 Power State Interrupts

11.5 POWER STATE GPIO INDICATION

The WM8325-00C can be configured to generate logic signals via GPIO pins to indicate the current Power State. See Section 21 for details of configuring GPIO pins.

A GPIO pin configured as "ON state" output will be asserted when the WM8325-00C is in the ON state.

A GPIO pin configured as "SLEEP state" output will be asserted when the WM8325-00C is in the SLEEP state.

11.6 ON PIN FUNCTION

The $\overline{\text{ON}}$ pin is intended for connection to the master power switch on the user's application. It can be used to start-up the WM8325-00C from the SLEEP or OFF states and also to power down the system. This pin operates on the LDO12 (VPMIC) power domain and has an internal pull-up resistor. This pin is asserted by shorting it to GND. A de-bounce circuit is provided on this input pin.

The behaviour of the $\overline{\text{ON}}$ pin is programmable. The primary action taken on asserting this pin is determined by the ON_PIN_PRIMACT register field. Note that the ON_PIN_INT interrupt event is always raised when the $\overline{\text{ON}}$ pin is asserted.

If the pin is held asserted for longer than the timeout period set by ON_PIN_TO, then a secondary action is executed. The secondary action is determined by the ON_PIN_SECACT register field.

If the pin is held asserted for a further timeout period, then a tertiary action is executed. The tertiary action is not programmable, and is to generate an OFF request.

The status of the $\overline{\text{ON}}$ pin can be read at any time via the ON_PIN_STS register.

Note that the $\overline{\text{ON}}$ pin control registers are locked by the WM8325-00C User Key. These registers can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16389 (4005h) ON Pin Control	9:8	ON_PIN_SECACT	01	Secondary action of $\overline{\text{ON}}$ pin (taken after 1 timeout period) 00 = Interrupt 01 = ON request 10 = OFF request 11 = Reserved <i>Protected by user key</i>
	5:4	ON_PIN_PRIMACT	00	Primary action of $\overline{\text{ON}}$ pin 00 = Ignore 01 = ON request 10 = OFF request 11 = Reserved Note that an Interrupt is always raised. <i>Protected by user key</i>
	3	ON_PIN_STS	0	Current status of $\overline{\text{ON}}$ pin 0 = Asserted (logic 0) 1 = Not asserted (logic 1)
	1:0	ON_PIN_TO	00	$\overline{\text{ON}}$ pin timeout period 00 = 1s 01 = 2s 10 = 4s 11 = 8s <i>Protected by user key</i>

Table 5 ON Pin Control Registers

The $\overline{\text{ON}}$ pin interrupt event is always raised as part of the primary action when the $\overline{\text{ON}}$ pin is asserted or de-asserted. (Note that the $\overline{\text{ON}}$ pin interrupt is raised on the rising and falling edges of this $\overline{\text{ON}}$ pin input signal.) The $\overline{\text{ON}}$ pin interrupt is a selectable option as the secondary action.

The $\overline{\text{ON}}$ pin interrupt event is indicated by the ON_PIN_CINT register field. This secondary interrupt triggers a primary ON Pin Interrupt, ON_PIN_INT (see Section 23). This can be masked by setting the mask bit as described in Table 6.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	12	ON_PIN_CINT	ON pin interrupt. (Rising and Falling Edge triggered) Note: Cleared when a '1' is written.
R16409 (4019h) Interrupt Status 1 Mask	12	IM_ON_PIN_CINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 6 ON Pin Interrupt

11.7 RESET PIN FUNCTION

The $\overline{\text{RESET}}$ pin is an active low input/output which is used to command Hardware Resets in the WM8325-00C and in other connected devices. The pin is an open-drain type, with integrated pull-up; it can be driven low by external sources or by the WM8325-00C itself.

The WM8325-00C drives the $\overline{\text{RESET}}$ pin low in the OFF state. The output status of the $\overline{\text{RESET}}$ pin in SLEEP is configurable; this is determined by the RST_SLPENA register bit as defined in Table 7.

The WM8325-00C clears the $\overline{\text{RESET}}$ pin following the transition to ON. On completion of the state transition, the $\overline{\text{RESET}}$ pin is held low for a further delay time period, extending the $\overline{\text{RESET}}$ low duration. The $\overline{\text{RESET}}$ delay period is set by the RST_DUR register bit. See Figure 6 for further details.

The WM8325-00C detects a Hardware Reset request whenever the $\overline{\text{RESET}}$ pin is driven low by an external source. In this event, the WM8325-00C resets the internal control registers (excluding the RTC) and initiates a start-up sequence. See Section 24.

It is possible to mask the $\overline{\text{RESET}}$ pin input in the SLEEP state by setting the RST_SLP_MSK register bit. In SLEEP mode, if RST_SLP_MSK is set, the WM8325-00C will take no action if the $\overline{\text{RESET}}$ pin is pulled low.

Note that the $\overline{\text{RESET}}$ pin control registers are locked by the WM8325-00C User Key. These registers can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16390 (4006h) Reset Control	5	RST_SLP_MSK	1	Masks the $\overline{\text{RESET}}$ pin input in SLEEP mode 0 = External $\overline{\text{RESET}}$ active in SLEEP 1 = External $\overline{\text{RESET}}$ masked in SLEEP <i>Protected by user key</i>
	4	RST_SLPENA	1	Sets the output status of $\overline{\text{RESET}}$ pin in SLEEP 0 = $\overline{\text{RESET}}$ high (not asserted) 1 = $\overline{\text{RESET}}$ low (asserted) <i>Protected by user key</i>
	1:0	RST_DUR	11	Delay period for releasing $\overline{\text{RESET}}$ after ON or WAKE sequence 00 = 3ms 01 = 11ms 10 = 51ms 11 = 101ms <i>Protected by user key</i>

Table 7 RESET Pin Control Registers

The WM8325-00C can generate an Auxiliary Reset output via a GPIO pin configured as “Auxiliary Reset” output (see Section 21). This signal is asserted in the OFF state. The status of the Auxiliary Reset in the SLEEP state is configurable, using the AUXRST_SLPENA register bit as defined in Table 8.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16390 (4006h) Reset Control	6	AUXRST_SLPE NA	1	Sets the output status of Auxiliary Reset (GPIO) function in SLEEP 0 = Auxiliary Reset not asserted 1 = Auxiliary Reset asserted <i>Protected by user key</i>

Table 8 Auxiliary Reset (GPIO) Control

The timing details of the $\overline{\text{RESET}}$ pin relative to an ON state transition are illustrated in Figure 6.

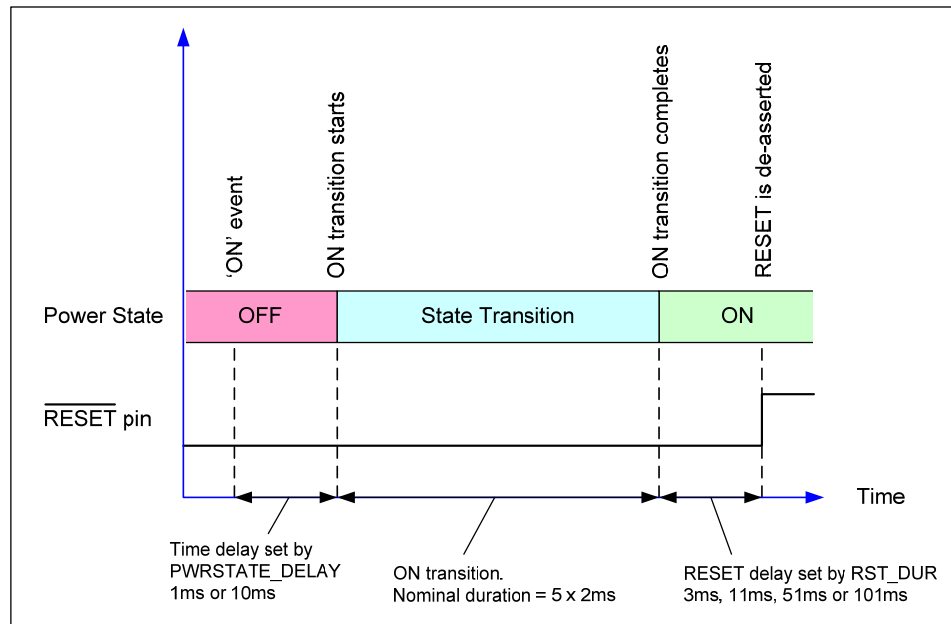


Figure 6 RESET Pin Output

12 CONTROL INTERFACE

12.1 GENERAL DESCRIPTION

The WM8325-00C is controlled by writing to its control registers. Readback is available for all registers, including Chip ID, power management status and GPIO status. The control interface can operate as a 2-wire (I2C) or 4-wire (SPI) control interface. Readback is provided on the bi-directional pin SDA1 in 2-wire (I2C) mode. The WM8325-00C Control Interface is powered by the DBVDD power domain.

The control interface mode is determined by the logic level on the CIFMODE pin as shown in Table 9.

CIFMODE	INTERFACE FORMAT
Low	2-wire (I2C) mode
High	4-wire (SPI) mode

Table 9 Control Interface Mode Selection

12.2 2-WIRE (I2C) CONTROL MODE

In 2-wire (I2C) mode, the WM8325-00C is a slave device on the control interface; SCLK1 is a clock input, while SDA1 is a bi-directional data pin. To allow arbitration of multiple slaves (and/or multiple masters) on the same interface, the WM8325-00C transmits logic 1 by tri-stating the SDA1 pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA1 line high so that the logic 1 can be recognised by the master.

In order to allow many devices to share a single 2-wire control bus, every device on the bus has a unique 8-bit device ID (this is not the same as the 16-bit address of each register in the WM8325-00C). The device ID is determined by the logic level on the \overline{CS} pin as shown in Table 10. The LSB of the device ID is the Read/Write bit; this bit is set to logic 1 for "Read" and logic 0 for "Write".

\overline{CS}	DEVICE ID
Low	0110 100x = 68h(write) / 69h(read)
High	0110 110x = 6Ch(write) / 6Dh(read)

Table 10 Control Interface Device ID Selection

The WM8325-00C operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDA1 while SCLK1 remains high. This indicates that a device ID, register address and data will follow. The WM8325-00C responds to the start condition and shifts in the next eight bits on SDA1 (8-bit device ID including Read/Write bit, MSB first). If the device ID received matches the device ID of the WM8325-00C, then the WM8325-00C responds by pulling SDA1 low on the next clock pulse (ACK). If the device ID is not recognised or the R/W bit is '1' when operating in write only mode, the WM8325-00C returns to the idle condition and waits for a new start condition and valid address.

If the device ID matches the device ID of the WM8325-00C, the data transfer continues as described below. The controller indicates the end of data transfer with a low to high transition on SDA1 while SCLK1 remains high. After receiving a complete address and data sequence the WM8325-00C returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDA1 changes while SCLK1 is high), the device returns to the idle condition.

The WM8325-00C supports the following read and write operations:

- Single write
- Single read
- Multiple write using auto-increment
- Multiple read using auto-increment

The sequence of signals associated with a single register write operation is illustrated in Figure 7.

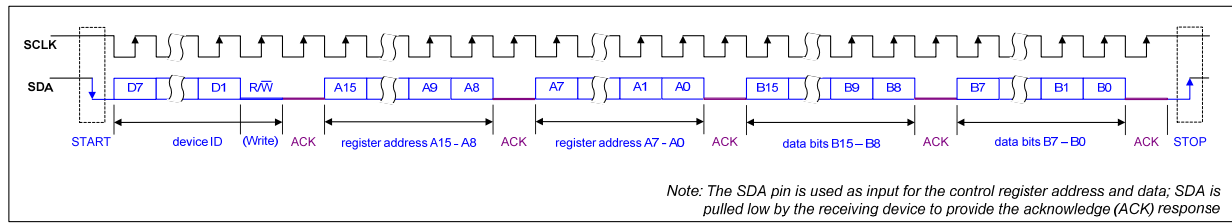


Figure 7 Control Interface 2-wire (I2C) Register Write

The sequence of signals associated with a single register read operation is illustrated in Figure 8.

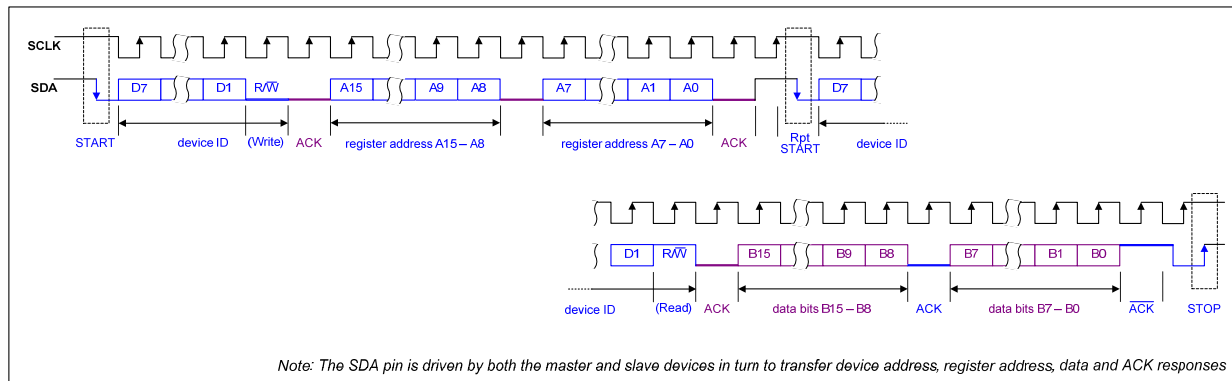


Figure 8 Control Interface 2-wire (I2C) Register Read

The Control Interface also supports other register operations, as listed above. The interface protocol for these operations is summarised below. The terminology used in the following figures is detailed in Table 11.

Note that, for multiple write and multiple read operations, the auto-increment option must be enabled. This feature is enabled by default; it is described in Table 12 below.

TERMINOLOGY	DESCRIPTION	
S	Start Condition	
Sr	Repeated start	
A	Acknowledge (SDA Low)	
\bar{A}	Not Acknowledge (SDA High)	
P	Stop Condition	
R/ \bar{W}	ReadNotWrite	0 = Write 1 = Read
[White field]	Data flow from bus master to WM8325-00C	
[Grey field]	Data flow from WM8325-00C to bus master	

Table 11 Control Interface Terminology

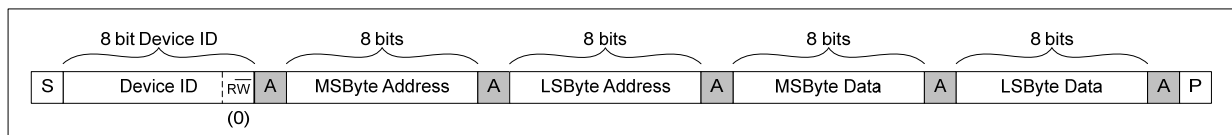


Figure 9 Single Register Write to Specified Address

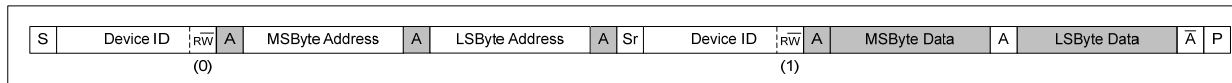


Figure 10 Single Register Read from Specified Address

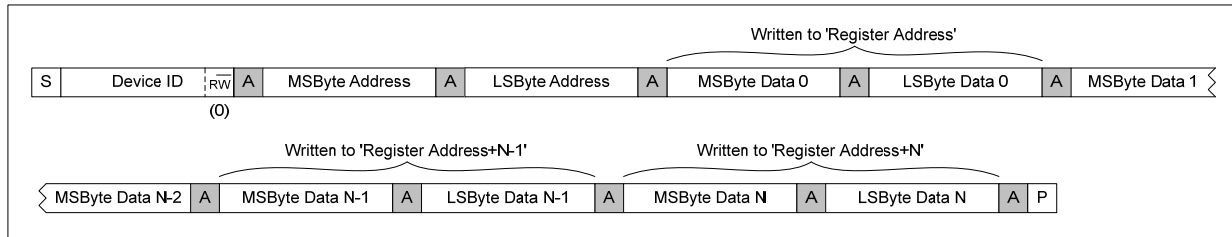


Figure 11 Multiple Register Write to Specified Address using Auto-increment

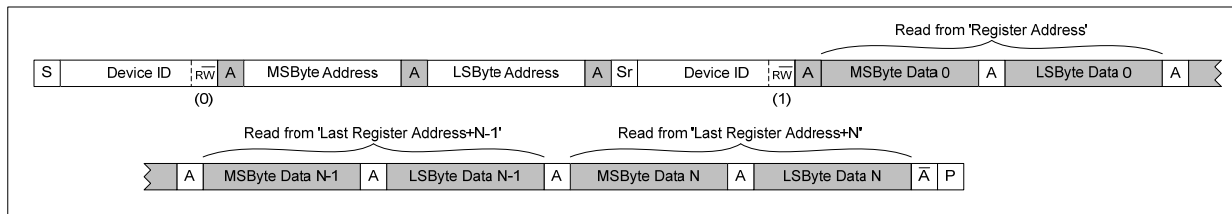


Figure 12 Multiple Register Read from Specified Address using Auto-increment

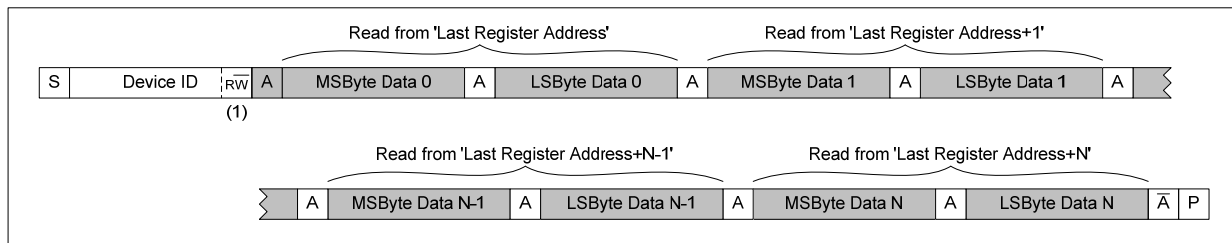


Figure 13 Multiple Register Read from Last Address using Auto-increment

Multiple Write and Multiple Read operations enable the host processor to access sequential blocks of the data in the WM8325-00C register map faster than is possible with single register operations. The auto-increment option is enabled when the AUTOINC register bit is set. This bit is defined in Table 12. Auto-increment is enabled by default.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16391 (4007h) Control Interface	2	AUTOINC	1	Enable Auto-Increment function 0 = Disabled 1 = Enabled

Table 12 Auto-Increment Control

12.3 4-WIRE (SPI) CONTROL MODE

In this mode, the WM8325-00C registers are accessed using a 4-wire serial control interface. The \overline{CS} and SCLK1 pins provide the 'Chip Select' and 'Serial Data Clock' functions respectively. Serial data input is supported on the SDA1 pin; serial data output is supported on the SDOUT1 pin.

A control word consists of 32 bits. The first bit is the read/write bit (R/W), which is followed by 15 address bits (A14 to A0) that determine which control register is accessed. The remaining 16 bits (B15 to B0) are data bits, corresponding to the 16 bits in each control register.

In Write operations (R/W=0), all SDA1 bits are driven by the controlling device. Each rising edge of SCLK1 clocks in one data bit from the SDA1 pin. A rising edge on \overline{CS} latches in a complete control word consisting of the last 32 bits.

In Read operations, the SDA1 pin is ignored following receipt of the valid register address. The data bits are output by the WM8325-00C on the SDOUT1 pin. SDOUT1 is undriven (high impedance) when not outputting register data bits.

The SDOUT1 pin is an Open Drain output; an external pull-up resistor to DBVDD is required on SDOUT1 in 4-wire (SPI) mode.

The sequence of signals associated with a register write operation is illustrated in Figure 14.

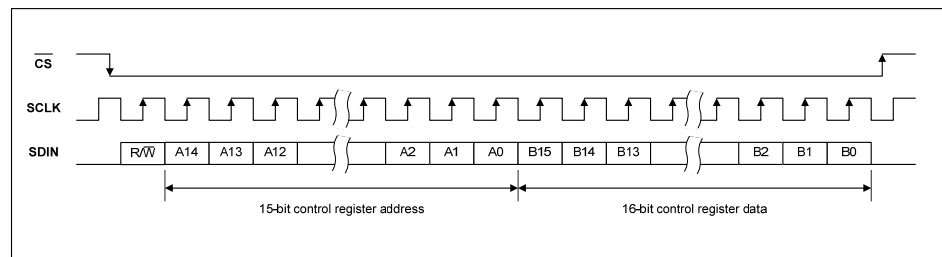


Figure 14 Control Interface 4-wire (SPI) Register Write

The sequence of signals associated with a register read operation is illustrated in Figure 15.

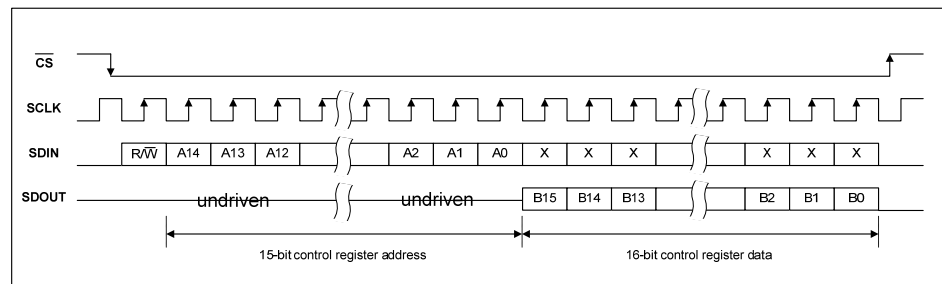


Figure 15 Control Interface 4-wire (SPI) Register Read

12.4 REGISTER LOCKING

Selected registers are protected by a security key. These registers can only be written to when the appropriate 'unlock' code has been written to the Security Key register.

The protected registers include those associated with Reset Control, OTP Programming and RTC Trim. Other selected functions also include protected registers; the affected registers are identified in the Register Map definitions throughout the document, and also in Section 29.

To unlock the protected registers, a value of 9716h must be written to the Security register (R16392), as defined in Table 13.

It is recommended to re-lock the protected registers immediately after writing to them. This helps protect the system against accidental overwriting of register values. To lock the protected registers, a value of 0000h should be written to the Security register.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16392 (4008h) Security Key	15:0	SECURITY [15:0]	0000h	Security Key A value of 9716h must be written to this register to access the user-keyed registers.

Table 13 Security Key Registers

12.5 SOFTWARE RESET AND CHIP ID

A Software Reset can be commanded by writing to Register 0000h. This is a read-only register field and the contents of this register will not be affected by a write operation. For more details of the different reset types, see Section 24.

Note that a maximum of 6 Software Resets is permitted. If more than 6 Software Resets are scheduled, the WM8325-00C will remain in the OFF state until the next valid ON state transition event occurs.

The Chip ID can be read back from Register 0000h. Other ID fields can be read from the registers defined in Table 14.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (0000h) Reset/ID	15:0	CHIP_ID [15:0]	0000h	Writing to this register causes a Software Reset. The register map contents may be reset, depending on SW_RESET_CFG. Reading from this register will indicate Chip ID.
R1 (0001h) Revision	15:8	PARENT_REV [7:0]	00h	The revision number of the parent die
	7:0	CHILD_REV [7:0]	00h	The revision number of the child die (when present)
R16384 (4000h) Parent ID	15:0	PARENT_ID [15:0]	6246h	The ID of the parent die

Table 14 Reading Device Information

12.6 SOFTWARE SCRATCH REGISTER

The WM8325-00C provides one 16-bit register as a "Software Scratch" register. This is available for use by the host processor to store data for any purpose required by the application.

The contents of the Software Scratch register are retained in the BACKUP power state.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16393 (4009h) Software Scratch	15:0	SW_SCRATCH [15:0]	0000h	Software Scratch Register for use by the host processor. Note that this register's contents are retained in the BACKUP power state.

Table 15 Software Scratch Register

13 CLOCKING AND OSCILLATOR CONTROL

13.1 GENERAL DESCRIPTION

The WM8325-00C incorporates a 32.768kHz crystal oscillator in order to maintain the Real Time Clock (RTC). An external crystal is normally required. Alternatively, a 32.768kHz signal may be input directly on the XTI pin. The crystal oscillator and RTC are enabled at all times, including the OFF and BACKUP power states. It is possible to disable the crystal oscillator in BACKUP for power-saving RTC 'unlocked' mode if desired. The WM8325-00C clock functions are illustrated in Figure 16.

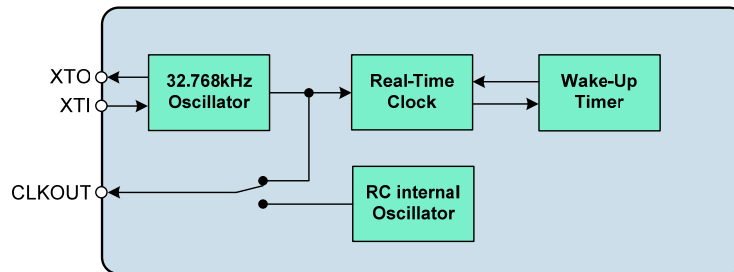


Figure 16 Clocking Configuration

The crystal oscillator is enabled at all times in the OFF, ON and SLEEP power states. The status of the crystal oscillator in BACKUP is selected using the XTAL_BKUPENA register.

The crystal oscillator can be disabled in the BACKUP state by setting the XTAL_BKUPENA register bit to 0. This feature may be used to minimise the device power consumption in the BACKUP state, as described in Section 20.5. The crystal oscillator is maintained in the BACKUP state if both XTAL_BKUPENA is set to 1.

The CLKOUT signal, derived from the 32.768kHz oscillator, can be enabled or disabled directly by writing to the CLKOUT_ENA register in the ON or SLEEP power states. The CLKOUT can also be controlled as part of the power state transitions using the CLKOUT_SLOT and CLKOUT_SLP_SLOT register fields. See Section 11.3 for a description of the state transition timeslots.

The CLKOUT pin may be configured as a CMOS output or as an Open-Drain output. The CLKOUT signal is referenced to the DBVDD power domain.

The status of the crystal oscillator is indicated by the XTAL_OK register bit. If the crystal oscillator fails to start, or if it stops for any reason, then the XTAL_OK register will be set to 0.

An internal RC oscillator is available in order to provide CLKOUT functionality during start-up of the crystal oscillator. This function is selectable using the XTAL_INH register bit, as described below.

If XTAL_INH = 0, then the internal RC oscillator provides the CLKOUT signal in the event that the crystal oscillator has not fully started up prior to an 'ON' state transition event. A glitch-free transition between the clock sources is implemented after the crystal oscillator is ready.

If XTAL_INH = 1, then an 'ON' state transition is delayed until the crystal oscillator has fully started up. This may be desirable if the CLKOUT signal is used as a clock for another circuit, to ensure that CLKOUT signal has been verified before the 'ON' state transition occurs. Note that the CLKOUT output is always disabled in the OFF power state; it is typically enabled as part of the 'ON' state transition sequence. Setting XTAL_INH = 1 ensures that the CLKOUT output cannot be enabled until the crystal frequency has been verified.

If XTAL_INH = 1, and the crystal oscillator fails to start, then a System Reset will be scheduled after a timeout period of approximately 32 seconds. See Section 24 for details of System Resets.

The WM8325-00C provides two interrupt flags associated with the crystal oscillator, as described in Section 13.2. These interrupts will provide indication of a crystal oscillator start-up failure, or detection of an interruption to the crystal oscillator (eg, due to tampering).

The CLKOUT control fields are described in Table 16.

Note that the XTAL_INH and CLKOUT_SLOT fields are also programmed on the integrated OTP memory (see Section 14). The default values noted below are valid when the WM8325-00C powers up to the OFF state, or if the Register Map is reset following a Device Reset or Software Reset event. The XTAL_INH and CLKOUT_SLOT registers are overwritten with the respective OTP memory contents when an ON transition is scheduled. See Section 30.3 for details of the OTP program that is implemented on the WM8325-00C.

The 32.768kHz oscillator may also be output on a GPIO pin, as described in Section 21. Note that a GPIO pin configured as 32.768kHz output will continue to output the oscillator clock in the OFF power state; this may be used to provide clocking to the processor in the OFF state, provided that the selected power domain for that GPIO pin remains enabled in the OFF state. The CLKOUT output is always disabled in the OFF power state.

The internal RC oscillator generates the required clocks for the integrated DC-DC Converters on the WM8325-00C. Note that a 2MHz 'External Power Clock', derived from this oscillator, may be output on a GPIO pin to provide synchronised clocking of external DC-DC Converters if required (see Section 21). The 2MHz External Power Clock is only enabled when either of the External Power Enable signals EPE1 or EPE2 is asserted. The External Power Enable (EPE) signals are controlled as described in Section 15.3.

Note that the CLKOUT_ENA control register is locked by the WM8325-00C User Key. This register can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16397 (400Dh) System Status	7	XTAL_OK	0	Crystal Oscillator Status 0 = Disabled or in start-up phase 1 = Enabled and verified
R16528 (4090h) Clock Control 1	15	CLKOUT_EN A	0	CLKOUT output enable 0 = Disabled 1 = Enabled <i>Protected by user key</i>
	13	CLKOUT_OD	0	CLKOUT pin configuration 0 = CMOS 1 = Open Drain
	10:8	CLKOUT_SLO T	000	CLKOUT output enable ON slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Do not enable 111 = Do not enable
	6:4	CLKOUT_SLP SLOT	000	CLKOUT output SLEEP slot select 000 = Controlled by CLKOUT_ENA 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = Controlled by CLKOUT_ENA 111 = Controlled by CLKOUT_ENA

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16529 (4091h) Clock Control 2	15	XTAL_INH	0	Crystal Start-Up Inhibit 0 = Disabled 1 = Enabled When XTAL_INH=0, the internal RC oscillator will provide CLKOUT until the crystal oscillator is valid. When XTAL_INH=1, the 'ON' transition is inhibited until the crystal oscillator is valid.
	12	XTAL_BKUPE NA	1	Selects the RTC and 32.768kHz oscillator in BACKUP state 0 = RTC unlocked in BACKUP 1 = RTC maintained in BACKUP

Table 16 Clocking Control

13.2 CRYSTAL OSCILLATOR INTERRUPTS

The Crystal Oscillator (XTAL) is associated with two Interrupt event flags.

The XTAL_START_EINT interrupt is set if the crystal oscillator fails to start-up within a timeout period of approximately 24 seconds.

The XTAL_TAMPER_EINT interrupt is set if the crystal oscillator is stopped unexpectedly (eg. due to tampering). Note that this interrupt is only supported if the crystal oscillator has previously started up successfully. The XTAL_TAMPER_EINT is also set if the crystal oscillator is re-started following an unexpected interruption.

Each of these secondary interrupts triggers a primary Real Time Clock and Crystal Oscillator Interrupt, RTC_INT (see Section 23). In the case of XTAL_START_EINT, this can be masked by setting the mask bit(s) as described in Table 17.

ADDRESS	BIT	LABEL	DESCRIPTION
R16404 (4014h) Interrupt Status 4	7	XTAL_START_EINT	Crystal Oscillator Start Failure interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
	6	XTAL_TAMPER_EINT	Crystal Oscillator Tamper interrupt (Rising and Falling Edge triggered) Note: Cleared when a '1' is written.
R16412 (401Ch) Interrupt Status 4 Mask	7	IM_XTAL_START_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 17 Crystal Oscillator (XTAL) Interrupts

13.3 CRYSTAL OSCILLATOR CONNECTIONS

The crystal oscillator generates a 32.768kHz reference clock, which is used to provide reference clock for the Real Time Clock (RTC) in the WM8325-00C. The oscillator requires an external crystal on the XT1 and XTO pins, as well as two capacitors, connected as shown in Figure 17.

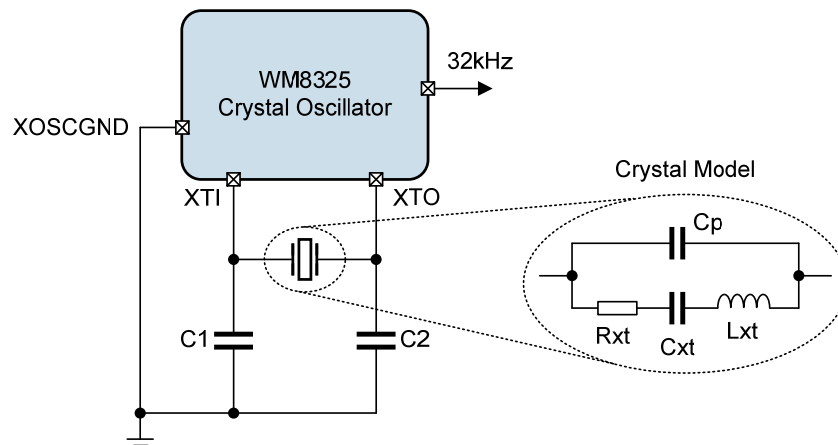


Figure 17 Crystal Oscillator

A suitable crystal oscillator should be selected in accordance with the following requirements:

PARAMETER	MIN	MAX	UNITS
Nominal frequency	32.768		kHz
Series resistance	50	70	kΩ
Maximum driving level	0.5		μW

Table 18 Selection of Crystal Oscillator Component

The load capacitors C1 and C2 should be selected according to the recommended load capacitance, C_L of the crystal, which is given by the following equation:

$$\text{Load Capacitance } C_L = \frac{C1 \times C2}{C1 + C2} + C_{\text{STRAY}}$$

Assuming $C1 = C2$ and $C_{\text{STRAY}} = 2.75\text{pF}$ (typical pad i/o capacitance), then:

$$C1 = C2 = 2 \times (C_L - 2.75\text{pF}).$$

For example, if the crystal has a load capacitance $C_L = 9\text{pF}$, then $C1 = C2 = 12.5\text{pF}$.

If a suitable 32.768kHz clock is already present elsewhere in the system, it is possible for the WM8325-00C to use that external clock instead. The external clock should be applied to pin XT1, and the XTO pin left floating in this case.

14 OTP MEMORY CONTROL

14.1 GENERAL DESCRIPTION

The WM8325-00C is specifically designed for compatibility with the Freescale i.MX53 processor. The sequencing and voltage control of the integrated DC-DC Converters and LDOs in power-up and shut-down is crucial to the robust operation of an application.

The essential device configuration data, tailored specifically to the requirements of the Freescale i.MX53 processor, is stored within an integrated One-Time Programmable (OTP) memory. This allows the WM8325-00C to start up and shut down the system with no dependency on any other devices for processor-specific configuration parameters.

A description of the OTP memory, and associated control registers, is provided in the following pages. See Section 30.3 for details of the OTP program that is implemented on the WM8325-00C.

Note that the OTP memory on the WM8325-00C device is pre-programmed and cannot be edited. The WM8325-00C is an equivalent device to the WM8325, but the OTP memory on the WM8325 is not pre-programmed, and supports user-configuration and programming.

14.2 OTP MEMORY DEFINITION

An illustration of the WM8325-00C memory locations is shown in Figure 18.

The main Register Map of the WM8325-00C contains a block of data in a 'Window' area which is mirrored in the OTP memory. The Window is called the Device Configuration Register Window (DCRW).

The device start-up configuration data is loaded from the OTP Memory into the Window area when an 'ON' transition is scheduled. The data in this Window is mirrored in other locations within the WM8325-00C Register Map.

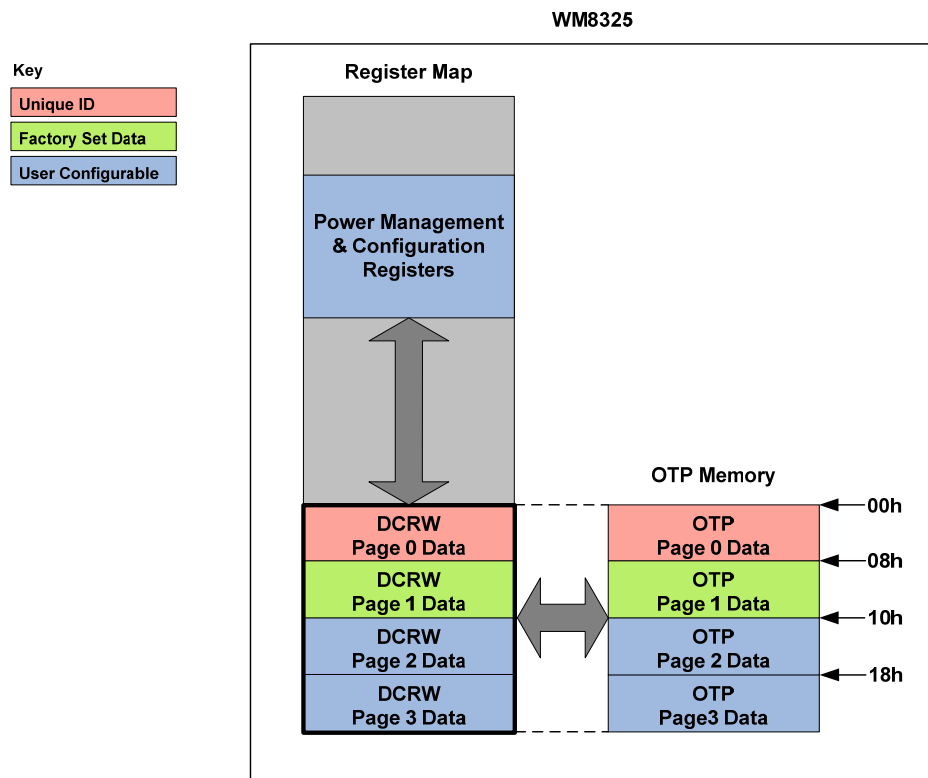


Figure 18 OTP Memory Layout

The DCRW contains 4 pages of data, as illustrated in Figure 18.

Page 0 of the DCRW contains a 128-bit pseudo-random unique ID. The unique ID is written to the OTP at the time of manufacture.

Page 1 of the DCRW contains factory-set calibration and configuration data. This data is written to the OTP at the time of manufacture.

Page 2 and Page 3 of the DCRW contain bootstrap configuration data. This defines the sequence and voltage requirements for powering up the WM8325-00C, and for configuring functions such as the clocks, GPIO1-6 and LED status indicators. The bootstrap data is tailored specifically to the requirements of the Freescale i.MX53 processor.

The OTP contains 4 pages of data, as illustrated in Figure 18. The contents of the OTP pages correspond to Pages 0, 1, 2 and 3 of the DCRW register map addresses. The OTP memory data is copied to the DCRW when the WM8325-00C schedules an 'ON' transition. The OTP memory data cannot be changed.

The DCRW can be accessed directly using the Control Interface in the OFF, ON and SLEEP power states. Note that Read/Write access to the OTP memory is not possible directly; this can only be accessed by copying to/from the DCRW.

14.3 BOOTSTRAP (START-UP) FUNCTION

The WM8325-00C configuration data is loaded when the WM8325-00C schedules an 'ON' transition.

The factory-set calibration data is loaded into Page 0 and Page 1 of the DCRW from the integrated OTP.

The bootstrap configuration data, tailored specifically to the requirements of the Freescale i.MX53 processor, is loaded into Page 2 and Page 3 of the DCRW from the integrated OTP. See Section 30.3 for details of the OTP program that is implemented on the WM8325-00C.

14.4 DCRW MEMORY CONTENTS

The DCRW is the OTP Register Window, as described in Section 14.2. This memory area is initialised with data from the integrated OTP memory whenever an 'ON' state transition is scheduled. The DCRW memory addresses range from R30720 (7800h) to R30751 (781Fh). The complete register map definition is described in Section 28.

The register fields in the DCRW allow the start-up configuration of the DC-DC Converters, the LDO Regulators, GPIO pins 1-6 and Status LED outputs to be programmed. The DCRW also provides control of selected Clocking functions and the Start-Up (SYSOK) voltage threshold.

Most of the DCRW contents are duplicates of control registers that exist in the main register area below the DCRW addresses. In these cases, reading or writing to either address will have the same effect.

Some register fields are defined only in the DCRW area; a detailed description of these fields is provided in the following sub-sections.

14.4.1 DCRW PAGE 0

Page 0 of the DCRW occupies register addresses R30720 (7800h) to R30727 (7807h). This contains factory-preset data which is loaded from OTP when an 'ON' state transition is scheduled.

Page 0 of the DCRW contains a 128-bit unique ID. Note that these fields are Read-Only in the OTP and cannot be changed.

14.4.2 DCRW PAGE 1

Page 1 of the DCRW occupies register addresses R30728 (7808h) to R30735 (780Fh). This contains factory-preset data which is loaded from OTP when an 'ON' state transition is scheduled.

Page 1 of the DCRW contains trim parameters that ensure the accuracy of the voltage references and the power management RC oscillator. Note that these fields are Read-Only in the OTP and cannot be changed.

14.4.3 DCRW PAGE 2

Page 2 of the DCRW occupies register addresses R30736 (7810h) to R30743 (7817h). This contains configuration data that is tailored specifically to the requirements of the Freescale i.MX53 processor.

This page of data is loaded from OTP when 'ON' state transition is scheduled.

The OTP_CUST_ID field is used to hold a Customer Identifier for the OTP data contents. Whenever an 'ON' state transition is requested, then the OTP_CUST_ID field is checked to confirm valid OTP data. If the OTP_CUST_ID field is set to zero, then the WM8325-00C remains in the OFF power state. A non-zero OTP_CUST_ID field is used to confirm valid OTP contents.

The OTP_CUST_FINAL bit is used to control whether the user-programmable OTP data (Page 2 and Page 3) is finalised. If OTP_CUST_FINAL is set in the OTP and also set in the DCRW, then the WM8325-00C prevents any further Writes to the OTP.

The above registers are defined in Table 19.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30736 (7810h) Customer OTP ID	14:1	OTP_CUST_ID [13:0]	0000h	This field is checked when an 'ON' transition is requested. A non-zero value is used to confirm valid data.
	0	OTP_CUST_FINAL	0	If OTP_CUST_FINAL is set in the OTP and also set in the DCRW, then no further Writes are possible to the OTP.

Table 19 OTP Registers - DCRW Page 2

The remaining contents of DCRW Page 2 include the registers listed in Table 20, which are defined in other sections of this datasheet.

REGISTER	FUNCTION	REFERENCE
DC1_ON_SLOT [2:0]	DC-DC Converter 1	See Section 15.11.2
DC1_PHASE		See Section 15.11.2
DC1_ON_VSEL [6:2]		See Section 15.11.2
DC2_ON_SLOT [2:0]	DC-DC Converter 2	See Section 15.11.2
DC2_PHASE		See Section 15.11.2
DC2_ON_VSEL [6:2]		See Section 15.11.2
DC3_ON_SLOT [2:0]	DC-DC Converter 3 and DC-DC Converter 4	See Section 15.11.2
DC3_PHASE [1:0]		See Section 15.11.2
DC3_ON_VSEL [6:2]		See Section 15.11.2
LDO1_ON_SLOT [2:0]	LDO Regulator 1	See Section 15.11.3
LDO1_ON_VSEL [4:0]		See Section 15.11.3
LDO2_ON_SLOT [2:0]	LDO Regulator 2	See Section 15.11.3
LDO2_ON_VSEL [4:0]		See Section 15.11.3
LDO3_ON_SLOT [2:0]	LDO Regulator 3	See Section 15.11.3
LDO3_ON_VSEL [4:0]		See Section 15.11.3
LDO4_ON_SLOT [2:0]	LDO Regulator 4	See Section 15.11.3
LDO4_ON_VSEL [4:0]		See Section 15.11.3
LDO5_ON_SLOT [2:0]	LDO Regulator 5	See Section 15.11.3
LDO5_ON_VSEL [4:0]		See Section 15.11.3
LDO6_ON_SLOT [2:0]	LDO Regulator 6	See Section 15.11.3
LDO6_ON_VSEL [4:0]		See Section 15.11.3
LDO7_ON_SLOT [2:0]	LDO Regulator 7	See Section 15.11.3

REGISTER	FUNCTION	REFERENCE
LDO7_ON_VSEL [4:0]		See Section 15.11.3
LDO8_ON_SLOT [2:0]	LDO Regulator 8	See Section 15.11.3
LDO8_ON_VSEL [4:0]		See Section 15.11.3

Table 20 DCRW Page 2

14.4.4 DCRW PAGE 3

Page 3 of the DCRW occupies register addresses R30744 (7818h) to R30751 (781Fh). This contains configuration data that is tailored specifically to the requirements of the Freescale i.MX53 processor.

This page of data is loaded from OTP when 'ON' state transition is scheduled.

The contents of DCRW Page 3 include the registers listed in Table 21.

REGISTER	FUNCTION	REFERENCE	
LDO9_ON_SLOT [2:0]	LDO Regulator 9	See Section 15.11.3	
LDO9_ON_VSEL [4:0]		See Section 15.11.3	
LDO10_ON_SLOT [2:0]	LDO Regulator 10	See Section 15.11.3	
LDO10_ON_VSEL [4:0]		See Section 15.11.3	
LDO11_ON_SLOT [2:0]	LDO Regulator 11	See Section 15.11.3	
LDO11_ON_VSEL [3:0]		See Section 15.11.3	
EPE1_ON_SLOT [2:0]	External Power Converter Enable	See Section 15.11.4	
EPE2_ON_SLOT [2:0]		See Section 15.11.4	
GP1_DIR	GPIO1	See Section 21.3	
GP1_PULL [1:0]		See Section 21.3	
GP1_INT_MODE		See Section 21.3	
GP1_PWR_DOM		See Section 21.3	
GP1_POL		See Section 21.3	
GP1_OD		See Section 21.3	
GP1_ENA		See Section 21.3	
GP1_FN [3:0]		See Section 21.3	
GP2_DIR		GPIO2	See Section 21.3
GP2_PULL [1:0]			See Section 21.3
GP2_INT_MODE	See Section 21.3		
GP2_PWR_DOM	See Section 21.3		
GP2_POL	See Section 21.3		
GP2_OD	See Section 21.3		
GP2_ENA	See Section 21.3		
GP2_FN [3:0]	See Section 21.3		
GP3_DIR	GPIO3	See Section 21.3	
GP3_PULL [1:0]		See Section 21.3	
GP3_INT_MODE		See Section 21.3	
GP3_PWR_DOM		See Section 21.3	
GP3_POL		See Section 21.3	
GP3_OD		See Section 21.3	
GP3_ENA		See Section 21.3	
GP3_FN [3:0]		See Section 21.3	
GP4_DIR	GPIO4	See Section 21.3	
GP4_PULL [1:0]		See Section 21.3	
GP4_INT_MODE		See Section 21.3	
GP4_PWR_DOM		See Section 21.3	
GP4_POL		See Section 21.3	
GP4_OD		See Section 21.3	
GP4_ENA		See Section 21.3	

REGISTER	FUNCTION	REFERENCE	
GP4_FN [3:0]		See Section 21.3	
GP5_DIR	GPIO5	See Section 21.3	
GP5_PULL [1:0]		See Section 21.3	
GP5_INT_MODE		See Section 21.3	
GP5_PWR_DOM		See Section 21.3	
GP5_POL		See Section 21.3	
GP5_OD		See Section 21.3	
GP5_ENA		See Section 21.3	
GP5_FN [3:0]		See Section 21.3	
GP6_DIR		GPIO6	See Section 21.3
GP6_PULL [1:0]			See Section 21.3
GP6_INT_MODE	See Section 21.3		
GP6_PWR_DOM	See Section 21.3		
GP6_POL	See Section 21.3		
GP6_OD	See Section 21.3		
GP6_ENA	See Section 21.3		
GP6_FN [3:0]	See Section 21.3		
CLKOUT_SLOT [2:0]	Clocking	See Section 13.1	
XTAL_INH		See Section 13.1	
WDOG_ENA	Watchdog Timer	See Section 25	
LED1_SRC [1:0]	System Status LED Drivers	See Section 22.2	
LED2_SRC [1:0]		See Section 22.2	
SYSOK_THR [2:0]	Supply Voltage Monitoring	See Section 24.4	

Table 21 DCRW Page 3

15 POWER MANAGEMENT

15.1 GENERAL DESCRIPTION

The WM8325-00C provides 4 DC-DC synchronous buck converters and 11 LDO regulators. The regulators comprise general purpose LDOs (LDO1 - LDO6) and low-noise analogue LDOs (LDO7 - LDO10). The analogue LDOs offer superior PSRR, noise and load-transient performance. LDO11 is a low power LDO intended for powering “always on” circuits connected to the WM8325-00C; this LDO can be configured to remain enabled in the OFF state.

These power management components are designed to support application processors and associated peripherals. DC-DC1 and DC-DC2 are intended to provide power to the processor voltage domains; DC-DC3 and DC-DC4 are ideally suited for powering memory circuits. The output voltage of each of the buck converters and regulators is programmable in software through control registers.

DC-DC Converters 3 and 4 are configured to operate in 'Dual' mode, where the two converters are ganged together to support an increased current capability. The two converters employ a common voltage feedback circuit in order to ensure the two outputs are accurately aligned. Both converters are controlled using the DC-DC 3 control registers, and the two circuits operate as a single converter.

The WM8325-00C can execute programmable sequences of enabling and disabling the DC-DC Converters and LDO Regulators as part of the transitions between the ON, OFF and SLEEP power states. The WM8325-00C power management circuits can also interface with configurable hardware control functions supported via GPIO pins. These include GPIO inputs for selecting alternate voltages or operating modes, and GPIO outputs for controlling external power management circuits.

The configuration of the power management circuits, together with some of the GPIO pins and other functions, are stored in the integrated OTP memory. The configuration is optimised for compatibility with the Freescale i.MX53 processor, and avoids any dependence on a host processor to configure the WM8325-00C at start-up.

15.2 DC-DC CONVERTER AND LDO REGULATOR ENABLE

The integrated DC-DC Converters and LDO Regulators can each be enabled in the ON or SLEEP power states by setting the DCm_ENA or LDO_n_ENA bits as defined in Section 15.11.1. Note that setting the DCm_ENA or LDO_n_ENA bits in the OFF state will not enable the DC-DC Converters or LDO Regulators. These bits should not be written to when the WM8325-00C is in the OFF state; writing to these bits in the OFF state may cause a malfunction.

Note that DC-DC Converters 3 and 4 are configured in 'Dual mode' on the WM8325-00C. As such, both converters are controlled using the DC-DC 3 control registers, and the two circuits operate as a single converter.

In many applications, there will be no need to write to the DCm_ENA or LDO_n_ENA bits, as these bits are controlled by the WM8325-00C when a power state transition is scheduled. Dynamic, run-time control of the DC-DC Converters or LDO Regulators is also possible by writing to these registers.

The DC-DC Converters and LDO Regulators can be assigned to a Hardware Enable (GPIO) input for external enable/disable control. In this case, the converter or regulator is not affected by the associated DCm_ENA or LDO_n_ENA bits. See Section 15.3 for further details.

The WM8325-00C can also control other circuits, including external DC-DC Converters or LDO Regulators using the External Power Enable (EPE) outputs. The External Power Enable outputs are alternate functions supported via GPIO - see Section 21. The External Power Enable outputs can be controlled in the same way as the internal DC-DC Converters and LDO Regulators. The associated control bits are $EPE1_ENA$ and $EPE2_ENA$, as defined in Section 15.11.1.

LDO Regulator 11 is a Low Power LDO Regulator, which is configured differently to the other LDOs. It is a low-power LDO intended for “Always-On” functions external to the WM8325-00C and can be enabled when the WM8325-00C is in the OFF power state.

When $LDO11_FRCENA$ is set, then LDO11 is enabled at all times in the OFF, ON and SLEEP states. Note that LDO11 is always disabled in the BACKUP and NO POWER states. See Section 15.11.3 for the definition of $LDO11_FRCENA$.

The current commanded state of each of the DC-DC Converters, LDO Regulators and EPE outputs is indicated in the DCm_STS , LDO_n_STS and EPE_n_STS register bits.

If a fault condition causes any converter or regulator to be disabled, then the associated $_ENA$ and $_STS$ fields are reset to 0.

15.3 TIMESLOT CONTROL AND HARDWARE ENABLE (GPIO) CONTROL

The DC-DC Converters (1-4) and LDO Regulators (1-11) are programmed to switch on in a selected timeslot within the ON sequence using the DCm_ON_SLOT or $LDO_n_ON_SLOT$ fields. These register fields are defined in Section 15.11.2 and Section 15.11.3. Alternatively, these fields can be used to assign a converter / regulator to one of the Hardware Enable Inputs. (The Hardware Enable Inputs are alternate functions supported via GPIO - see Section 21.)

The ON sequence timeslot configuration is stored on the integrated OTP non-volatile memory - this is optimised for compatibility with the Freescale i.MX53 processor. See Section 30.2 for details of the ON sequence that is implemented on the WM8325-00C.

Note that DC-DC Converters 3 and 4 are configured in 'Dual mode' on the WM8325-00C. As such, both converters are controlled using the DC-DC 3 control registers, and the two circuits operate as a single converter.

Converters / regulators which are assigned to one of the Hardware Enable Inputs are enabled or disabled according to the logic level of the respective GPIO input in the ON or SLEEP power states. The Hardware Enable Inputs are effective from the end of the ON sequence until the start of the OFF sequence. Note that the GPIO Hardware Enable function is not the same as the GPIO Hardware Control function.

Any converters / regulators which are assigned to timeslots within the ON sequence will be disabled in the reverse sequence when an OFF sequence is scheduled. Any converters / regulators which are not assigned to timeslots, or are assigned to Hardware Enable Inputs, will be disabled immediately at the start of the OFF sequence.

Each of the converters / regulators may also be programmed to be disabled in a selected timeslot within the SLEEP sequence using the DCm_SLP_SLOT or $LDO_n_SLP_SLOT$ fields. In the case of converters / regulators which are not disabled by the SLEEP sequence, these fields determine in which timeslot each converter or regulator enters its SLEEP configuration.

Note that the SLEEP sequence is not pre-configured on the WM8325-00C; this must be programmed as required using the register fields defined in Section 15.11.2 and Section 15.11.3.

Any converters / regulators which are disabled as part of the SLEEP sequence will be enabled in the reverse sequence when a WAKE transition is scheduled.

By default, the OFF sequence is the reverse of the ON sequence. Similarly, the WAKE sequence is the reverse of the SLEEP sequence. If a different behaviour is required, this can be achieved by writing to the $_ON_SLOT$ or $_SLP_SLOT$ registers between transitions in order to re-define the sequences.

Any converters / regulators which are assigned to Hardware Enable Inputs will remain under control of the Hardware Enable Inputs in the SLEEP power state. In this case, the DCm_SLP_SLOT or $LDO_n_SLP_SLOT$ fields determine in which timeslot the converter / regulator enters its SLEEP configuration.

The WM8325-00C will control the DCm_ENA or LDO_n_ENA bit (see Section 15.2) for any converter / regulator that is enabled or disabled during the power state transitions. In the case of a converter / regulator assigned to a Hardware Enable (GPIO) input, the DCm_ENA or LDO_n_ENA bit is not controlled and the converter / regulator is not affected by this bit.

The DC-DC converters include a soft-start feature that limits in-rush current at start-up. However, in order to further reduce supply in-rush current, it is recommended that the individual converters are programmed to start up in different time slots within the start-up sequence, as described in Section 11.3.

Similarly, it is recommended that the individual LDO regulators are programmed to start up in different time slots within the start-up sequence, as described in Section 11.3.

The External Power Enable (EPE) outputs, EPE1 and EPE2, may also be assigned to timeslots in the ON / SLEEP sequences or assigned to Hardware Enable inputs using the $EPE_n_ON_SLOT$ and $EPE_n_SLP_SLOT$ fields described in 15.11.4.

Note that a transition from the SLEEP state to the OFF state is not a controlled transition. If an 'OFF' event occurs whilst in the SLEEP state, then the WM8325-00C will select the OFF state, but all the enabled converters and regulators will be disabled immediately; the time-controlled sequence is not implemented in this case. See Section 11.3 for details of the WM8325-00C 'OFF' events.

15.4 OPERATING MODE CONTROL

15.4.1 DC-DC SYNCHRONOUS BUCK CONVERTERS

The DC-DC Converters can be configured to operate in four different operating modes. The operating modes are summarised in Table 22. For more detailed information on the DC-DC (Buck) Converter operating modes, see Section 15.14.2.

Note that Auto Mode is not supported on DC-DC3 / DC-DC4 when configured in 'Dual mode'. These converters are configured in 'Dual mode' on the WM8325-00C.

DC-DC CONVERTER OPERATING MODE	DESCRIPTION
Forced Continuous Conduction Mode (FCCM)	High performance mode for all static and transient load conditions.
Auto Mode: Continuous / Discontinuous Conduction with Pulse-Skipping Mode (CCM/DCM with PS)	High efficiency mode for all static and transient load conditions. Performance may be less than FCCM mode for heavy load transients. (Note - not supported on DC-DC3 / DC-DC4 when configured in 'Dual mode'.)
Hysteretic Mode	High efficiency mode for light static and light transient loads only. Maximum load current is restricted; output voltage ripple is increased.
LDO Mode	Power saving mode for light loads only. High efficiency for ultra light loads. Low current soft-start control.

Table 22 DC-DC Synchronous Buck Converter Operating Modes

The operating mode of the DC-DC Converters in the ON power state is selected using the DCm_ON_MODE register fields. The operating mode of the DC-DC Converters in the SLEEP power state is selected using the DCm_SLP_MODE register fields.

Note that DC-DC Converters 3 and 4 are configured in 'Dual mode' on the WM8325-00C. As such, both converters are controlled using the DC-DC 3 control registers, and the two circuits operate as a single converter.

When changing the operating mode of the DC-DC Converters in preparation for an increased load, a set-up time of 100 μ s should be allowed for the operating mode to be established before applying the new load.

Note that the operating mode of the DC-DC Converters may also be controlled by the Hardware Control inputs. The Hardware Control inputs are alternate functions supported via GPIO. See Section 15.8 for details of Hardware Control.

15.4.2 LDO REGULATORS

The LDO Regulators LDO1 - LDO10 can be configured to operate in Normal operating mode or in Low Power mode.

The operating mode of the LDO Regulators in the ON power state is selected using the $LDO_n_ON_MODE$ register fields. The operating mode of the LDO Regulators in the SLEEP power state is selected using the $LDO_n_SLP_MODE$ register fields.

For the standard LDOs, LDO1 - LDO6, two different Low Power modes are provided, offering limited load current capability and reduced quiescent current. When Low Power mode is selected in the ON

or SLEEP power states, then the LDO n _LP_MODE register bits determine which Low Power mode is selected.

Note that the operating mode and output voltage of the LDO Regulators may also be controlled by the Hardware Control inputs. The Hardware Control inputs are alternate functions supported via GPIO. See Section 15.8 for details of Hardware Control.

15.5 OUTPUT VOLTAGE CONTROL

15.5.1 DC-DC SYNCHRONOUS BUCK CONVERTERS

The output voltage of the DC-DC Converters 1-4 in the ON power state is selected using the DC m _ON_VSEL register fields. The output voltage of these converters in the SLEEP power state is selected using the DC m _SLP_VSEL register fields.

The default output voltage of the DC-DC Converters 1-4 in the ON power state is stored on the integrated OTP non-volatile memory - this is optimised for compatibility with the Freescale i.MX53 processor. See Section 30.3 for details of the OTP program that is implemented on the WM8325-00C.

Note that DC-DC Converters 3 and 4 are configured in 'Dual mode' on the WM8325-00C. As such, both converters are controlled using the DC-DC 3 control registers, and the two circuits operate as a single converter.

The DC-DC Converters are dynamically programmable - the output voltage may be adjusted in software at any time. These converters are step-down converters; their output voltage can therefore be lower than the input voltage, but cannot be higher.

Note that the output voltage of DC-DC Converters 1 and 2 may also be controlled using the Dynamic Voltage Scaling features described in Section 15.6. Software control (using register writes) and hardware control (using the Hardware DVS Control inputs supported via GPIO) is supported.

Note that the output voltage of the DC-DC Converters may also be controlled by the Hardware Control inputs. The Hardware Control inputs are alternate functions supported via GPIO. See Section 15.8 for details of Hardware Control.

When changing the output voltage of DC-DC Converters 1 and 2, the GPIO output "DC-DC m DVS Done" can be used to confirm the DVS Control has completed; see Section 15.6 for details.

15.5.2 LDO REGULATORS 1-10

The output voltage of the LDO Regulators 1-10 in the ON power state is selected using the LDO n _ON_VSEL register fields. The output voltage of the LDO Regulators in the SLEEP power state is selected using the LDO n _SLP_VSEL register fields.

The default output voltage of the LDO Regulators 1-10 in the ON power state is stored on the integrated OTP non-volatile memory - this is optimised for compatibility with the Freescale i.MX53 processor. See Section 30.3 for details of the OTP program that is implemented on the WM8325-00C.

The LDO Regulators are dynamically programmable - the output voltage may be adjusted in software at any time.

Note that the output voltage of the LDO Regulators may also be controlled by the Hardware Control inputs. The Hardware Control inputs are alternate functions supported via GPIO. See Section 15.8 for details of Hardware Control.

15.5.3 LDO REGULATOR 11

The output voltage of LDO11 can be set in two ways - it can be commanded directly, or it can be commanded to follow the DC-DC Converter 1 output voltage.

When LDO11_VSEL_SRC = 0, then the output voltage of LDO11 is set by LDO11_ON_VSEL (in the ON state) or by LDO11_SLP_VSEL (in the SLEEP state) in the same way as the other LDOs.

When LDO11_VSEL_SRC = 1, the output voltage of LDO11 follows the output voltage of DC-DC Converter 1. This enables both domains to be changed at the same time, eg. the processor core and

processor 'alive' domains. In this case, the LDO11 output voltage follows DC1_ON_VSEL or DC1_SLP_VSEL in the ON state or SLEEP state respectively.

Note that, when LDO11_VSEL_SRC = 1, the LDO11 regulator adopts the nearest achievable output voltage, which may not be identical to the DC-DC1 voltage, due to the more limited range and resolution of LDO11 - the output voltage of LDO11 is in the range 0.8V to 1.55V in 50mV steps; the output voltage of DC-DC1 is in the range 0.6V to 1.8V in 12.5mV steps. If DC-DC1 is disabled, then the LDO11 voltage tracking feature is not supported, and the LDO11 output voltage will be 0.8V.

15.6 DC-DC SYNCHRONOUS BUCK CONVERTER CONTROL

15.6.1 DC-DC1 AND DC-DC2

Soft-Start control is provided for each of the DC-DC synchronous buck converters, using the DCm_SOFT_START register fields. When a DC-DC Converter is switched on, the soft-start circuit will apply current limiting in order to control the in-rush current. For DC-DC1 and DC-DC2, the current limit is increased through up to 8 stages to the full load condition. The DCm_SOFT_START registers select the duration of these stages.

When a DC-DC Converter is disabled, the output pin can be configured to be floating or to be actively discharged. This is selected using DCm_FLT.

The switching phase of each DC-DC converter can be set using the DCm_PHASE bits. The supply current ripple can be minimised by selecting a different switching phase for different converters.

The Dynamic Voltage Scaling (DVS) feature on DC-DC1 and DC-DC2 enables hardware or software selection of an alternate output voltage, DCm_DVS_VSEL. This may be useful if a short-term variation in output voltage is required.

The DVS voltage (set by DCm_DVS_VSEL) may be selected by setting DCm_DVS_SRC = 01. Alternatively, the DVS voltage may be selected under control of one of the Hardware DVS Control inputs supported via the GPIO pins. See Section 21 for details of configuring the GPIO pins as Hardware DVS Control inputs.

Whenever the DVS voltage is selected by any method, the DVS selection takes precedence over the ON, SLEEP or Hardware Control (HWC) configuration. See Section 15.8 for details of Hardware Control options.

The output voltage ramp rate is selectable for DC-DC Converters 1 and 2. The DCm_RATE field selects the rate of change of output voltage, whether this is in response to an operating mode transition, or any hardware or software command. Note that the DCm_RATE field is accurate in Forced Continuous Conduction Mode (FCCM); in other modes, the actual slew rate may be longer in the case of a decreasing output voltage selection, especially under light load conditions.

The WM8325-00C can indicate the status of the Dynamic Voltage Scaling via a GPIO pin configured as a "DC-DC1 DVS Done" or "DC-DC2 DVS Done" output (see Section 21). When a GPIO pin is configured to indicate the DVS status, this signal is temporarily de-asserted during a DVS transition on the associated DC-DC Converter, and is subsequently asserted to indicate the transition has completed.

Note that the GPIO DVS outputs indicate the progress of all output voltage slews; they are not limited to transitions associated with DCm_DVS_SRC; the GPIO DVS output also indicates the status of a slew caused by a write to the DCm_ON_VSEL register, or a slew to the DCm_SLP_VSEL voltage. Note also that the GPIO DVS outputs are indicators of the DVS control mechanism only; they do not confirm the output voltage accuracy. The output voltage can be checked using the voltage status bits if required (see Section 15.2).

15.6.2 DC-DC3 AND DC-DC4 - DUAL MODE CONVERTERS

DC-DC Converters 3 and 4 are configured in 'Dual mode' on the WM8325-00C. As such, both converters are controlled using the DC-DC 3 control registers, and the two circuits operate as a single converter.

Soft-Start control is provided for each of the DC-DC synchronous buck converters, using the DC3_SOFT_START register fields. When a DC-DC Converter is switched on, the soft-start circuit will

apply current limiting in order to control the in-rush current. For DC-DC3 and DC-DC4, the current limit is increased through up to 3 stages to the full load condition. The DC3_SOFT_START registers select the duration of these stages. (Note that, under light loads, the full start-up may be achieved in fewer than 3 stages.)

When DC-DC3 and DC-DC4 are operating in Hysteretic Mode, the maximum DC output current can be set using the DC3_STNBY_LIM register. See Section 15.4.1 for details of the DC-DC3 and DC-DC4 operating modes.

When a DC-DC Converter is disabled, the output pin can be configured to be floating or to be actively discharged. This is selected using DC3_FLT.

The switching phase of each DC-DC converter can be set using the DC3_PHASE bits. The supply current ripple can be minimised by selecting a different switching phase for different converters.

15.7 LDO REGULATOR CONTROL

The LDO Regulators 1-10 can be configured to act as Current Limited Switches by setting the LDO_n_SWI field. When this bit is selected, there is no voltage regulation and the operating mode and output voltage controls of the corresponding LDO are ignored. In Switch mode, the switch is enabled (closed) and disabled (opened) by enabling or disabling the LDO.

Note that Switch mode, when required, must be configured after the WM8325-00C has entered the ON state.

When the LDO Regulator is disabled (and Switch mode is not selected), the output pin can be configured to be floating or to be actively discharged. This is selected using LDO_n_FLT.

15.8 HARDWARE CONTROL (GPIO)

The DC-DC Converters, LDO Regulators and EPE outputs may be controlled by the Hardware Control inputs supported via the GPIO pins. The DC_m_HWC_SRC, LDO_n_HWC_SRC or EPE_n_HWC_SRC fields determine which of these Hardware Control inputs is effective.

See Section 21 for details of configuring the GPIO pins as Hardware Control inputs. Note that the GPIO Hardware Control function is not the same as the GPIO Hardware Enable function.

Hardware Control is only possible when the applicable DC_m_ENA, LDO_n_ENA or EPE_n_ENA control bit is set (see Section 15.2), or if a Hardware Enable has been assigned to the relevant function and is asserted.

The action taken in response to the selected Hardware Control inputs is configurable for each DC-DC Converter, LDO Regulator or EPE output. The available options are described below.

When a Hardware Control input is assigned to a DC-DC Buck Converter, and is asserted, the operating mode and output voltage of the relevant DC-DC Converter is determined by the DC_m_HWC_VSEL and DC_m_HWC_MODE fields; this takes precedence over the normal ON or SLEEP settings.

Note that the Hardware Control input can be used to disable a DC-DC Buck Converter if required, by setting DC_m_HWC_MODE = 01.

When a Hardware Control input is assigned to LDO Regulators 1-10, and is asserted, the operating mode and output voltage of the relevant LDO Regulators is determined by the LDO_n_HWC_VSEL and LDO_n_HWC_MODE fields; this takes precedence over the normal ON or SLEEP settings.

Note that, for the standard LDOs (LDO1 - LDO6), when Low Power Mode is selected (LDO_n_HWC_MODE = 00 or 10), then the Low Power mode type is determined by the LDO_n_LP_MODE register bits.

When a Hardware Control input is assigned to the External Power Enable (EPE) outputs, and is asserted, the relevant EPE outputs are controlled as determined by the EPE_n_HWC_ENA field; this takes precedence over the normal ON or SLEEP settings. The available options are to de-assert the EPE, or for the EPE to remain under control of EPE_n_ENA.

15.9 FAULT PROTECTION

Each of the DC-DC Buck Converters (1 to 4) is monitored for voltage accuracy and fault conditions. An undervoltage condition is set if the output voltage falls below the required level by more than the applicable undervoltage margin, as specified in Section 7.1.

Each LDO Regulator (1 to 10) is monitored for voltage accuracy and fault conditions. An undervoltage condition is set if the output voltage falls below the required level by more than the undervoltage margin, as specified in Section 7.2.

The `DCm_ERR_ACT` and `LDOn_ERR_ACT` fields configure the fault response to an Undervoltage condition. An Interrupt is always triggered under this condition (see Section 15.12); additional action can also be selected independently for each converter / regulator. The options are to ignore the fault, shut down the converter, or to shut down the system. To prevent false alarms during short current surges, faults are only signalled if the fault condition persists.

If a fault condition is detected, and the selected response is to shut down the converter or regulator, then the associated `_ENA` and `_STS` fields are reset to 0, as described in Section 15.2.

If a fault condition is detected, and the selected response is to shut down the system, then a Device Reset is triggered, as described in Section 24.1, forcing a transition to the OFF state. The WM8325-00C will automatically return to the ON state after performing the Device Reset.

Note that, if the fault condition persists, then a maximum of 6 Device Resets will be attempted to initiate the start-up sequence. If the sequence fails more than 6 times, the WM8325-00C will remain in the OFF state until the next valid ON state transition event occurs.

Note that DC-DC1 and DC-DC2 overvoltage and high current conditions can be detected and reported as described in Section 15.10. The `DCm_ERR_ACT` fields have no relation to these conditions.

The DC-DC3 and DC-DC4 Converters have a selectable overvoltage protection feature, controlled by `DC3_OVP` or `DC4_OVP`. This affects the converter response when the applicable converter is enabled or when its output voltage is increased. When the overvoltage protection is enabled, there is less overshoot in the output voltage, but some oscillation may occur as the voltage settles. This function should only be enabled if steep load transients are present on the output of the DC-DC Converter and if voltage overshoot is critical.

15.10 MONITORING AND FAULT REPORTING

Each of the DC-DC Converters (1 to 4) and LDOs (1 to 10) is monitored for voltage accuracy and fault conditions. An undervoltage condition is detected if the voltage falls below the required level by more than a pre-determined tolerance. If an undervoltage condition occurs, then this is indicated using the corresponding status bit(s) defined in Section 15.11.5. An undervoltage condition also triggers an Undervoltage Interrupt (see Section 15.12). Additional actions to shut down the converter or perform a Device Reset may also be selected.

The Internal LDO (LDO13) is also monitored for voltage accuracy and fault conditions. An undervoltage condition in LDO13 is indicated using the `INTLDO_UV_STS` bit. This undervoltage condition also causes an OFF transition to be scheduled, as described in Section 11.3.

DC-DC Converters 1 and 2 are monitored for overvoltage conditions. An overvoltage condition is set if the voltage is more than 100mV above the required level. If an overvoltage condition occurs, then this is indicated using the corresponding status bit(s). Note that there is no Interrupt or other selectable response to an overvoltage condition.

The current draw on DC-DC Converters 1 and 2 can be monitored against user-programmable thresholds in order to detect a high current condition. This feature is enabled using `DCm_HC_IND_ENA` and the current threshold is set using `DCm_HC_THR`. Note that the high current threshold is not the same as the maximum current capability of the DC-DC Converters, but is set according to the application requirements. If a high current condition occurs, then this is indicated using the corresponding status bit(s). A high current condition also triggers a High Current Interrupt (see Section 15.12).

15.11 POWER MANAGEMENT REGISTER DEFINITIONS

15.11.1 DC-DC CONVERTER AND LDO REGULATOR ENABLE

The Enable and Status register bits for the DC-DC Converters and LDO Regulators are defined in Table 23.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16464 (4050h) DCDC Enable	3:0	DCm_ENA	0	DC-DCm Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in DCm_STS)
R16465 (4051h) LDO Enable	10:0	LDO _n _ENA	0	LDO _n Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO _n _STS)
R16466 (4052h) DCDC Status	3:0	DCm_STS	0	DC-DCm Status 0 = Disabled 1 = Enabled
R16467 (4053h) LDO Status	10:0	LDO _n _STS	0	LDO _n Status 0 = Disabled 1 = Enabled
Notes:				
1. <i>n</i> is a number between 1 and 11 that identifies the individual LDO Regulator.				
2. <i>m</i> is a number between 1 and 4 that identifies the individual DC-DC Converter.				
3. DC-DC Converters 3 and 4 are configured in 'Dual mode'. Both converters are controlled using the DC-DC 3 control registers.				

Table 23 DC-DC Converter and LDO Regulator Control

The Enable and Status register bits for the External Power Enable (EPE) Controls are defined in Table 24.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16464 (4050h) DCDC Enable	7	EPE2_ENA	0	EPE2 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in EPE2_STS)
	6	EPE1_ENA	0	EPE1 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in EPE1_STS)
R16466 (4052h) DCDC Status	7	EPE2_STS	0	EPE2 Status 0 = Disabled 1 = Enabled
	6	EPE1_STS	0	EPE1 Status 0 = Disabled 1 = Enabled

Table 24 External Power Enable (EPE) Control

15.11.2 DC-DC SYNCHRONOUS BUCK CONVERTER CONTROL

The register controls for configuring the DC-DC synchronous buck converters 1-4 are defined in Table 25.

Note that the DCm_ON_SLOT and DCm_PHASE fields and the 5 MSBs of DCm_ON_VSEL are also programmed on the integrated OTP memory (see Section 14). The default values noted below are valid when the WM8325-00C powers up to the OFF state, or if the Register Map is reset following a Device Reset or Software Reset event. The DCm_ON_SLOT , DCm_PHASE and DCm_ON_VSEL registers are overwritten with the respective OTP memory contents when an ON transition is scheduled. See Section 30.3 for details of the OTP program that is implemented on the WM8325-00C.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16470 (4056h) DC1 Control 1	15:14	DC1_RATE [1:0]	10	DC-DC1 Voltage Ramp rate 00 = 1 step every 32us 01 = 1 step every 16us 10 = 1 step every 8us 11 = Immediate voltage change
	12	DC1_PHASE	0	DC-DC1 Clock Phase Control 0 = Normal 1 = Inverted
	7	DC1_FLT	0	DC-DC1 Output float 0 = DC-DC1 output discharged when disabled 1 = DC-DC1 output floating when disabled
	5:4	DC1_SOFT_START [1:0]	00	DC-DC1 Soft-Start Control (Duration in each of the 8 startup current limiting steps.) 00 = 32us steps 01 = 64us steps 10 = 128us steps 11 = 256us steps
R16471 (4057h) DC1 Control 2	15:14	DC1_ERR_ACT [1:0]	00	DC-DC1 Error Action (Undervoltage) 00 = Ignore 01 = Shut down converter 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.
	12:11	DC1_HWC_SRC [1:0]	00	DC-DC1 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2
	10	DC1_HWC_VSEL	0	DC-DC1 Hardware Control Voltage select 0 = Set by DC1_ON_VSEL 1 = Set by DC1_SLP_VSEL
	9:8	DC1_HWC_MODE [1:0]	11	DC-DC1 Hardware Control Operating Mode 00 = Forced Continuous Conduction Mode 01 = Disabled 10 = LDO Mode 11 = Hysteretic Mode

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6:4	DC1_HC_THR [2:0]	000	DC-DC1 High Current threshold 000 = 125mA 001 = 250mA 010 = 375mA 011 = 500mA 100 = 625mA 101 = 750mA 110 = 875mA 111 = 1000mA
	0	DC1_HC_IN D_ENA	0	DC-DC1 High Current detect enable 0 = Disabled 1 = Enabled
R16472 (4058h) DC1 ON Config	15:13	DC1_ON_SLOT [2:0]	000	DC-DC1 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2
	9:8	DC1_ON_MODE [1:0]	00	DC-DC1 ON Operating Mode 00 = Forced Continuous Conduction Mode 01 = Auto Mode (Continuous / Discontinuous Conduction with Pulse-Skipping) 10 = LDO Mode 11 = Hysteretic Mode
	6:2	DC1_ON_VSEL [6:2]	00000	DC-DC1 ON Voltage select DC1_ON_VSEL[6:0] selects the DC-DC1 output voltage from 0.6V to 1.8V in 12.5mV steps. DC1_ON_VSEL[6:2] also exist in OTP memory, controlling the voltage in 50mV steps.
	1:0	DC1_ON_VSEL [1:0]	00	DC1_ON_VSEL[6:0] is coded as follows: 00h to 08h = 0.6V 09h = 0.6125V ... 67h = 1.7875V 68h to 7Fh = 1.8V

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16473 (4059h) DC1 SLEEP Control	15:13	DC1_SLP_S LOT [2:0]	000	DC-DC1 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If DC-DC1 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the converter enters its SLEEP condition.
	9:8	DC1_SLP_M ODE [1:0]	00	DC-DC1 SLEEP Operating Mode 00 = Forced Continuous Conduction Mode 01 = Auto Mode (Continuous / Discontinuous Conduction with Pulse- Skipping) 10 = LDO Mode 11 = Hysteretic Mode
	6:0	DC1_SLP_V SEL [6:0]	000_0000	DC-DC1 SLEEP Voltage select 0.6V to 1.8V in 12.5mV steps 00h to 08h = 0.6V 09h = 0.6125V ... 67h = 1.7875V 68h to 7Fh = 1.8V
R16474 (405Ah) DC1 DVS Control	12:11	DC1_DVS_S RC [1:0]	00	DC-DC1 DVS Control Source 00 = Disabled 01 = Enabled 10 = Controlled by Hardware DVS1 11 = Controlled by Hardware DVS2
	6:0	DC1_DVS_V SEL [6:0]	000_0000	DC-DC1 DVS Voltage select 0.6V to 1.8V in 12.5mV steps 00h to 08h = 0.6V 09h = 0.6125V ... 67h = 1.7875V 68h to 7Fh = 1.8V
R16475 (405Bh) DC2 Control 1	15:14	DC2_RATE [1:0]	10	<i>Same as DC-DC1</i>
	12	DC2_PHASE	0	<i>Same as DC-DC1</i>
	7	DC2_FLT	0	<i>Same as DC-DC1</i>
	5:4	DC2_SOFT_ START [1:0]	00	<i>Same as DC-DC1</i>
R16476 (405Ch) DC2 Control 2	15:14	DC2_ERR_A CT [1:0]	00	<i>Same as DC-DC1</i>
	12:11	DC2_HWC_ SRC [1:0]	00	<i>Same as DC-DC1</i>
	10	DC2_HWC_ VSEL	0	<i>Same as DC-DC1</i>

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	9:8	DC2_HWC_MODE [1:0]	11	<i>Same as DC-DC1</i>
	6:4	DC2_HC_THR [2:0]	000	DC-DC2 High Current threshold 000 = 250mA 001 = 500mA 010 = 750mA 011 = 1000mA 100 = 1250mA 101 = 1500mA 110 = 1750mA 111 = 2000mA
	0	DC2_HC_IN D_ENA	0	<i>Same as DC-DC1</i>
R16477 (405Dh) DC2 ON Config	15:13	DC2_ON_SLOTT [2:0]	000	<i>Same as DC-DC1</i>
	9:8	DC2_ON_MODE [1:0]	00	<i>Same as DC-DC1</i>
	6:2	DC2_ON_VSEL [6:2]	00000	<i>Same as DC-DC1</i>
	1:0	DC2_ON_VSEL [1:0]	00	
R16478 (405Eh) DC2 SLEEP Control	15:13	DC2_SLP_SLOTT [2:0]	000	<i>Same as DC-DC1</i>
	9:8	DC2_SLP_MODE [1:0]	00	<i>Same as DC-DC1</i>
	6:0	DC2_SLP_VSEL [6:0]	000_0000	<i>Same as DC-DC1</i>
R16479 (405Fh) DC2 DVS Control	12:11	DC2_DVS_SRC [1:0]	00	<i>Same as DC-DC1</i>
	6:0	DC2_DVS_VSEL [6:0]	000_0000	<i>Same as DC-DC1</i>
R16480 (4060h) DC3 Control 1	12	DC3_PHASE	0	<i>Same as DC-DC1</i>
	7	DC3_FLT	0	<i>Same as DC-DC1</i>
	5:4	DC3_SOFT_START [1:0]	01	DC-DC3 Soft-Start Control (Duration in each of the 3 intermediate startup current limiting steps.) 00 = Immediate start-up 01 = 512us steps 10 = 4.096ms steps 11 = 32.768ms steps
	3:2	DC3_STNBY_LIM [1:0]	01	DC-DC3 Current Limit Sets the maximum DC output current in Hysteretic Mode. Typical values shown below. 00 = 50mA 01 = 100mA 10 = 200mA 11 = 400mA <i>Protected by user key</i>
R16481 (4061h) DC3 Control 2	15:14	DC3_ERR_ACT [1:0]	00	<i>Same as DC-DC1</i>
	12:11	DC3_HWC_SRC [1:0]	00	<i>Same as DC-DC1</i>
	10	DC3_HWC_VSEL	0	<i>Same as DC-DC1</i>

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	9:8	DC3_HWC_MODE [1:0]	11	<i>Same as DC-DC1</i>
	7	DC3_OVP	0	DC-DC3 Overvoltage Protection 0 = Disabled 1 = Enabled
R16482 (4062h) DC3 ON Config	15:13	DC3_ON_SL OT [2:0]	000	<i>Same as DC-DC1</i>
	9:8	DC3_ON_MODE [1:0]	00	DC-DC3 ON Operating Mode 00 = Forced Continuous Conduction Mode 01 = Forced Continuous Conduction Mode 10 = LDO Mode 11 = Hysteretic Mode
	6:2	DC3_ON_VSEL [6:2]	00000	DC-DC3 ON Voltage select DC3_ON_VSEL[6:0] selects the DC-DC3 output voltage from 0.85V to 3.4V in 25mV steps. DC3_ON_VSEL[6:2] also exist in OTP memory, controlling the voltage in 100mV steps.
	1:0	DC3_ON_VSEL [1:0]	00	DC3_ON_VSEL[6:0] is coded as follows: 00h = 0.85V 01h = 0.875V ... 65h = 3.375V 66h to 7Fh = 3.4V
R16483 (4063h) DC3 SLEEP Control	15:13	DC3_SLP_SLOT [2:0]	000	<i>Same as DC-DC1</i>
	9:8	DC3_SLP_MODE [1:0]	00	DC-DC3 SLEEP Operating Mode 00 = Forced Continuous Conduction Mode 01 = Forced Continuous Conduction Mode 10 = LDO Mode 11 = Hysteretic Mode
	6:0	DC3_SLP_VSEL [6:0]	000_0000	DC-DC3 SLEEP Voltage select 0.85V to 3.4V in 25mV steps 00h = 0.85V 01h = 0.875V ... 65h = 3.375V 66h to 7Fh = 3.4V

Table 25 DC-DC Converter Control

Note that DC-DC Converters 3 and 4 are configured in 'Dual mode'. Both converters are controlled using the DC-DC 3 control registers.

15.11.3 LDO REGULATOR CONTROL

The register controls for configuring the LDO Regulators 1-6 are defined in Table 26.

Note that the LDO_n_ON_SLOT and LDO_n_ON_VSEL fields are also programmed on the integrated OTP memory (see Section 14). The default values noted below are valid when the WM8325-00C

powers up to the OFF state, or if the Register Map is reset following a Device Reset or Software Reset event. The LDO_n_ON_SLOT and LDO_n_ON_VSEL registers are overwritten with the respective OTP memory contents when an ON transition is scheduled. See Section 30.3 for details of the OTP program that is implemented on the WM8325-00C.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16488 (4068h) LDO1 Control	15:14	LDO1_ERR_ACT [1:0]	00	LDO1 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.
	12:11	LDO1_HWC_SRC [1:0]	00	LDO1 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2
	10	LDO1_HWC_VSEL	0	LDO1 Hardware Control Voltage select 0 = Set by LDO1_ON_VSEL 1 = Set by LDO1_SLP_VSEL
	9:8	LDO1_HWC_MODE	10	LDO1 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO1_ON_MODE
	7	LDO1_FLT	0	LDO1 Output float 0 = LDO1 output discharged when disabled 1 = LDO1 output floating when disabled
	6	LDO1_SWI	0	LDO1 Switch Mode 0 = LDO mode 1 = Switch mode
	0	LDO1_LP_MODE	0	LDO1 Low Power Mode Select 0 = 50mA (reduced quiescent current) 1 = 20mA (minimum quiescent current) Selects which Low Power mode is used in ON, SLEEP, or under HWC modes.
R16489 (4069h) LDO1 ON Control	15:13	LDO1_ON_SLOT [2:0]	000	LDO1 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	8	LDO1_ON_MODE	0	LDO1 ON Operating Mode 0 = Normal mode 1 = Low Power mode
	4:0	LDO1_ON_VSEL [4:0]	00000	LDO1 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V
R16490 (406Ah) LDO1 SLEEP Control	15:13	LDO1_SLP_SLOT [2:0]	000	LDO1 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO1 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.
	8	LDO1_SLP_MODE	0	LDO1 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode
	4:0	LDO1_SLP_VSEL [4:0]	00000	LDO1 SLEEP Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V
R16491 (406Bh) LDO2 Control	15:14	LDO2_ERR_ACT [1:0]	00	<i>Same as LDO1</i>
	12:11	LDO2_HWC_SRC [1:0]	00	<i>Same as LDO1</i>
	10	LDO2_HWC_VSEL	0	<i>Same as LDO1</i>
	9:8	LDO2_HWC_MODE	10	<i>Same as LDO1</i>
	7	LDO2_FLT	0	<i>Same as LDO1</i>
	6	LDO2_SWI	0	<i>Same as LDO1</i>
	0	LDO2_LP_MODE	0	<i>Same as LDO1</i>

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16492 (406Ch) LDO2 ON Control	15:13	LDO2_ON_S LOT [2:0]	000	Same as LDO1
	8	LDO2_ON_ MODE	0	Same as LDO1
	4:0	LDO2_ON_V SEL [4:0]	00000	Same as LDO1
R16493 (406Dh) LDO2 SLEEP Control	15:13	LDO2_SLP_ SLOT [2:0]	000	Same as LDO1
	8	LDO2_SLP_ MODE	0	Same as LDO1
	4:0	LDO2_SLP_ VSEL [4:0]	00000	Same as LDO1
R16494 (406Eh) LDO3 Control	15:14	LDO3_ERR_ ACT [1:0]	00	Same as LDO1
	12:11	LDO3_HWC _SRC [1:0]	00	Same as LDO1
	10	LDO3_HWC _VSEL	0	Same as LDO1
	9:8	LDO3_HWC _MODE	10	Same as LDO1
	7	LDO3_FLT	0	Same as LDO1
	6	LDO3_SWI	0	Same as LDO1
	0	LDO3_LP_M ODE	0	Same as LDO1
R16495 (406Fh) LDO3 ON Control	15:13	LDO3_ON_S LOT [2:0]	000	Same as LDO1
	8	LDO3_ON_ MODE	0	Same as LDO1
	4:0	LDO3_ON_V SEL [4:0]	00000	Same as LDO1
R16496 (4070h) LDO3 SLEEP Control	15:13	LDO3_SLP_ SLOT [2:0]	000	Same as LDO1
	8	LDO3_SLP_ MODE	0	Same as LDO1
	4:0	LDO3_SLP_ VSEL [4:0]	00000	Same as LDO1
R16497 (4071h) LDO4 Control	15:14	LDO4_ERR_ ACT [1:0]	00	Same as LDO1
	12:11	LDO4_HWC _SRC [1:0]	00	Same as LDO1
	10	LDO4_HWC _VSEL	0	Same as LDO1
	9:8	LDO4_HWC _MODE	10	Same as LDO1
	7	LDO4_FLT	0	Same as LDO1
	6	LDO4_SWI	0	Same as LDO1
	0	LDO4_LP_M ODE	0	Same as LDO1
R16498 (4072h) LDO4 ON Control	15:13	LDO4_ON_S LOT [2:0]	000	Same as LDO1
	8	LDO4_ON_ MODE	0	Same as LDO1
	4:0	LDO4_ON_V SEL [4:0]	00000	Same as LDO1
R16499 (4073h)	15:13	LDO4_SLP_ SLOT [2:0]	000	Same as LDO1

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
LDO4 SLEEP Control	8	LDO4_SLP_MODE	0	Same as LDO1
	4:0	LDO4_SLP_VSEL [4:0]	00000	Same as LDO1
R16500 (4074h) LDO5 Control	15:14	LDO5_ERR_ACT [1:0]	00	Same as LDO1
	12:11	LDO5_HWC_SRC [1:0]	00	Same as LDO1
	10	LDO5_HWC_VSEL	0	Same as LDO1
	9:8	LDO5_HWC_MODE	10	Same as LDO1
	7	LDO5_FLT	0	Same as LDO1
	6	LDO5_SWI	0	Same as LDO1
	0	LDO5_LP_MODE	0	Same as LDO1
R16501 (4075h) LDO5 ON Control	15:13	LDO5_ON_SLOT [2:0]	000	Same as LDO1
	8	LDO5_ON_MODE	0	Same as LDO1
	4:0	LDO5_ON_VSEL [4:0]	00000	Same as LDO1
R16502 (4076h) LDO5 SLEEP Control	15:13	LDO5_SLP_SLOT [2:0]	000	Same as LDO1
	8	LDO5_SLP_MODE	0	Same as LDO1
	4:0	LDO5_SLP_VSEL [4:0]	00000	Same as LDO1
R16503 (4077h) LDO6 Control	15:14	LDO6_ERR_ACT [1:0]	00	Same as LDO1
	12:11	LDO6_HWC_SRC [1:0]	00	Same as LDO1
	10	LDO6_HWC_VSEL	0	Same as LDO1
	9:8	LDO6_HWC_MODE	10	Same as LDO1
	7	LDO6_FLT	0	Same as LDO1
	6	LDO6_SWI	0	Same as LDO1
	0	LDO6_LP_MODE	0	Same as LDO1
R16504 (4078h) LDO6 ON Control	15:13	LDO6_ON_SLOT [2:0]	000	Same as LDO1
	8	LDO6_ON_MODE	0	Same as LDO1
	4:0	LDO6_ON_VSEL [4:0]	00000	Same as LDO1
R16505 (4079h) LDO6 SLEEP Control	15:13	LDO6_SLP_SLOT [2:0]	000	Same as LDO1
	8	LDO6_SLP_MODE	0	Same as LDO1
	4:0	LDO6_SLP_VSEL [4:0]	00000	Same as LDO1

Table 26 LDO Regulators 1-6 Control

The register controls for configuring the LDO Regulators 7-10 are defined in Table 27.

Note that the LDO_n_ON_SLOT and LDO_n_ON_VSEL fields are also programmed on the integrated OTP memory (see Section 14). The default values noted below are valid when the WM8325-00C powers up to the OFF state, or if the Register Map is reset following a Device Reset or Software Reset event. The LDO_n_ON_SLOT and LDO_n_ON_VSEL registers are overwritten with the respective OTP memory contents when an ON transition is scheduled. See Section 30.3 for details of the OTP program that is implemented on the WM8325-00C.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16506 (407Ah) LDO7 Control	15:14	LDO7_ERR_ACT [1:0]	00	LDO7 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.
	12:11	LDO7_HWC_SRC [1:0]	00	LDO7 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2
	10	LDO7_HWC_VSEL	0	LDO7 Hardware Control Voltage select 0 = Set by LDO7_ON_VSEL 1 = Set by LDO7_SLP_VSEL
	9:8	LDO7_HWC_MODE	00	LDO7 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO7_ON_MODE
	7	LDO7_FLT	0	LDO7 Output float 0 = LDO7 output discharged when disabled 1 = LDO7 output floating when disabled
	6	LDO7_SWI	0	LDO7 Switch Mode 0 = LDO mode 1 = Switch mode
R16507 (407Bh) LDO7 ON Control	15:13	LDO7_ON_SLOT [2:0]	000	LDO7 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2
	8	LDO7_ON_MODE	0	LDO7 ON Operating Mode 0 = Normal mode 1 = Low Power mode

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	4:0	LDO7_ON_VSEL [4:0]	00000	LDO7 ON Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V ... 0Ch = 1.60V 0Dh = 1.70V ... 1Eh = 3.40V 1Fh = 3.50V
R16508 (407Ch) LDO7 SLEEP Control	15:13	LDO7_SLP_SLOT [2:0]	000	LDO7 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO7 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.
	8	LDO7_SLP_MODE	0	LDO7 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode
	4:0	LDO7_SLP_VSEL [4:0]	00000	LDO7 SLEEP Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V ... 0Ch = 1.60V 0Dh = 1.70V ... 1Eh = 3.40V 1Fh = 3.50V
R16509 (407Dh) LDO8 Control	15:14	LDO8_ERR_ACT [1:0]	00	<i>Same as LDO7</i>
	12:11	LDO8_HWC_SRC [1:0]	00	<i>Same as LDO7</i>
	10	LDO8_HWC_VSEL	0	<i>Same as LDO7</i>
	9:8	LDO8_HWC_MODE	00	<i>Same as LDO7</i>
	7	LDO8_FLT	0	<i>Same as LDO7</i>
	6	LDO8_SWI	0	<i>Same as LDO7</i>
R16510 (407Eh)	15:13	LDO8_ON_SLOT [2:0]	000	<i>Same as LDO7</i>

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
LDO8 ON Control	8	LDO8_ON_MODE	0	Same as LDO7
	4:0	LDO8_ON_VSEL [4:0]	00000	Same as LDO7
R16511 (407Fh) LDO8 SLEEP Control	15:13	LDO8_SLP_SLOT [2:0]	000	Same as LDO7
	8	LDO8_SLP_MODE	0	Same as LDO7
	4:0	LDO8_SLP_VSEL [4:0]	00000	Same as LDO7
R16512 (4080h) LDO9 Control	15:14	LDO9_ERR_ACT [1:0]	00	Same as LDO7
	12:11	LDO9_HWC_SRC [1:0]	00	Same as LDO7
	10	LDO9_HWC_VSEL	0	Same as LDO7
	9:8	LDO9_HWC_MODE	00	Same as LDO7
	7	LDO9_FLT	0	Same as LDO7
	6	LDO9_SWI	0	Same as LDO7
R16513 (4081h) LDO9 ON Control	15:13	LDO9_ON_SLOT [2:0]	000	Same as LDO7
	8	LDO9_ON_MODE	0	Same as LDO7
	4:0	LDO9_ON_VSEL [4:0]	00000	Same as LDO7
R16514 (4082h) LDO9 SLEEP Control	15:13	LDO9_SLP_SLOT [2:0]	000	Same as LDO7
	8	LDO9_SLP_MODE	0	Same as LDO7
	4:0	LDO9_SLP_VSEL [4:0]	00000	Same as LDO7
R16515 (4083h) LDO10 Control	15:14	LDO10_ERR_ACT [1:0]	00	Same as LDO7
	12:11	LDO10_HWC_SRC [1:0]	00	Same as LDO7
	10	LDO10_HWC_VSEL	0	Same as LDO7
	9:8	LDO10_HWC_MODE	00	Same as LDO7
	7	LDO10_FLT	0	Same as LDO7
	6	LDO10_SWI	0	Same as LDO7
R16516 (4084h) LDO10 ON Control	15:13	LDO10_ON_SLOT [2:0]	000	Same as LDO7
	8	LDO10_ON_MODE	0	Same as LDO7
	4:0	LDO10_ON_VSEL [4:0]	00000	Same as LDO7
R16517 (4085h) LDO10 SLEEP Control	15:13	LDO10_SLP_SLOT [2:0]	000	Same as LDO7
	8	LDO10_SLP_MODE	0	Same as LDO7
	4:0	LDO10_SLP_VSEL [4:0]	00000	Same as LDO7

Table 27 LDO Regulators 7-10 Control

The register controls for configuring the LDO Regulator 11 are defined in Table 28.

Note that the LDO11_ON_SLOT and LDO11_ON_VSEL fields are also programmed on the integrated OTP memory (see Section 14). The default values noted below are valid when the WM8325-00C powers up to the OFF state, or if the Register Map is reset following a Device Reset or Software Reset event. The LDO11_ON_SLOT and LDO11_ON_VSEL registers are overwritten with the respective OTP memory contents when an ON transition is scheduled. See Section 30.3 for details of the OTP program that is implemented on the WM8325-00C.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16519 (4087h) LDO11 ON Control	15:13	LDO11_ON_SLOT [2:0]	000	LDO11 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2
	12	LDO11_FRC ENA	0	LDO11 Force Enable (forces LDO11 to be enabled at all times in the OFF, ON and SLEEP states) 0 = Disabled 1 = Enabled
	7	LDO11_VSEL_SRC	0	LDO11 Voltage Select source 0 = Normal (LDO11 settings) 1 = Same as DC-DC Converter 1
	3:0	LDO11_ON_VSEL [3:0]	0000	LDO11 ON Voltage select 0.80V to 1.55V in 50mV steps 0h = 0.80V 1h = 0.85V 2h = 0.90V ... Eh = 1.50V Fh = 1.55V
R16520 (4088h) LDO11 SLEEP Control	15:13	LDO11_SLP_SLOT [2:0]	000	LDO11 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO11 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:0	LDO11_SLP_VSEL [3:0]	0000	LDO11 SLEEP Voltage select 0.80V to 1.55V in 50mV steps 0h = 0.80V 1h = 0.85V 2h = 0.90V ... Eh = 1.50V Fh = 1.55V

Table 28 LDO Regulator 11 Control

15.11.4 EXTERNAL POWER ENABLE (EPE) CONTROL

The register controls for configuring the External Power Enable (EPE) outputs are defined in Table 29.

Note that the EPE1_ON_SLOT and EPE2_ON_SLOT fields are also programmed on the integrated OTP memory (see Section 14). The default values noted below are valid when the WM8325-00C powers up to the OFF state, or if the Register Map is reset following a Device Reset or Software Reset event. The EPE1_ON_SLOT and EPE2_ON_SLOT registers are overwritten with the respective OTP memory contents when an ON transition is scheduled. See Section 30.3 for details of the OTP program that is implemented on the WM8325-00C.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16521 (4089h) EPE1 Control	15:13	EPE1_ON_SLOT [2:0]	000	EPE1 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2
	12:11	EPE1_HWC_SRC [1:0]	00	EPE1 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2
	8	EPE1_HWC_ENA	0	EPE1 Hardware Control Enable 0 = EPE1 is controlled by EPE1_ENA (Hardware Control input(s) are ignored) 1 = EPE1 is controlled by HWC inputs (Hardware Control input(s) force EPE1 to be de-asserted)
	7:5	EPE1_SLP_SLOT [2:0]	000	EPE1 SLEEP Slot select 000 = No action 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = No action 111 = No action

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1652 (408Ah) EPE2 Control	15:13	EPE2_ON_S LOT [2:0]	000	Same as EPE1
	12:11	EPE2_HWC _SRC [1:0]	00	Same as EPE1
	8	EPE2_HWC ENA	0	Same as EPE1
	7:5	EPE2_SLP_ SLOT [2:0]	000	Same as EPE1

Table 29 External Power Enable (EPE) Control

15.11.5 MONITORING AND FAULT REPORTING

The overvoltage, undervoltage and high current status registers are defined in Table 30.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16468 (4054h) DCDC UV Status	13	DC2_OV_ST S	0	DC-DC2 Overvoltage Status 0 = Normal 1 = Overvoltage
	12	DC1_OV_ST S	0	DC-DC1 Overvoltage Status 0 = Normal 1 = Overvoltage
	9	DC2_HC_ST S	0	DC-DC2 High Current Status 0 = Normal 1 = High Current
	8	DC1_HC_ST S	0	DC-DC1 High Current Status 0 = Normal 1 = High Current
	3:0	DC m _UV_S TS	0	DC-DC m Undervoltage Status 0 = Normal 1 = Undervoltage
R16469 (4055h) LDO UV Status	15	INTLDO_UV _STS	0	LDO13 (Internal LDO) Undervoltage Status 0 = Normal 1 = Undervoltage
	9:0	LDO n _UV_S TS	0	LDO n Undervoltage Status 0 = Normal 1 = Undervoltage
Notes:				
1. n is a number between 1 and 10 that identifies the individual LDO Regulator (LDO1 - 10).				
2. m is a number between 1 and 4 that identifies the individual DC-DC Converter (DC-DC1 - 4).				

Table 30 DC Converter and LDO Regulator Status

15.12 POWER MANAGEMENT INTERRUPTS

Undervoltage monitoring is provided on all DC-DC Converters and LDO Regulators, as described in Section 15.10. The associated interrupt flags indicate an undervoltage condition in each individual DC-DC Converter or LDO Regulator. Each of these secondary interrupts triggers a primary Undervoltage Interrupt, UV_INT (see Section 23). This can be masked by setting the mask bit(s) as described in Table 31.

Current monitoring is provided on DC-DC1 and DC-DC2, as described in Section 15.10. The interrupt flags HC_DC1_EINT and HC_DC2_EINT indicate a high current condition in DC-DC1 and DC-DC2 respectively. Each of these secondary interrupts triggers a primary High Current Interrupt, HC_INT (see Section 23). This can be masked by setting the mask bit(s) as described in Table 31.

The high current thresholds are programmable; these are set by DC1_HC_THR and DC2_HC_THR for DC-DC1 and DC-DC2 respectively. See Section 15.11.2 for details of these register fields. Note

that these functions are for current monitoring; they do not equate to the DC-DC Converter maximum current limit.

ADDRESS	BIT	LABEL	DESCRIPTION
R16403 (4013h) Interrupt Status 3	9:0	UV_LDO _n _EINT	LDO _n Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
R16404 (4014h) Interrupt Status 4	9	HC_DC2_EINT	DC-DC2 High current interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
	8	HC_DC1_EINT	DC-DC1 High current interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
	3:0	UV_DC _m _EINT	DC-DC _m Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
R16411 (401Bh) Interrupt Status 3 Mask	9:0	IM_UV_LDO _n _EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
R16412 (401Ch) Interrupt Status 4 Mask	9	IM_HC_DC2_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	8	IM_HC_DC1_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	3:0	IM_UV_DC _m _EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
Notes:			
1. <i>n</i> is a number between 1 and 10 that identifies the individual LDO Regulator (LDO1 - 10).			
2. <i>m</i> is a number between 1 and 4 that identifies the individual DC-DC Converter (DC-DC1 - 4).			

Table 31 Power Management Interrupts

15.13 POWER GOOD INDICATION

The WM8325-00C can indicate the status of the DC-DC Converters and LDO Regulators via a GPIO pin configured as a "PWR_GOOD" output (see Section 21).

Each DC-DC Converter and LDO Regulator to be monitored in this way must be individually enabled as an input to the PWR_GOOD function using the register bits defined in Table 32.

When a GPIO pin is configured as a "PWR_GOOD" output, this signal is asserted when all selected DC-DC Converters and LDO Regulators are operating correctly. If any of the enabled DC-DC Converters or LDO Regulators is undervoltage, then the PWR_GOOD will be de-asserted. In this event, the host processor should read the Undervoltage Interrupt fields to determine which DC-DC Converter or LDO Regulator is affected.

Note that an Undervoltage condition may lead to a Converter being switched off automatically. In this case, the disabled Converter will not indicate the fault condition via PWR_GOOD. Accordingly, the PWR_GOOD signal may not be a reliable output in cases where the WM8325-00C is configured to shut down any Converters automatically under Undervoltage conditions. It is recommended that the host processor should read the Undervoltage Interrupts in response to PWR_GOOD being de-asserted. The host processor can then initiate the most appropriate response.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16526 (408Eh) Power Good Source 1	3	DC4_OK	0	DC-DC4 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	2	DC3_OK	1	DC-DC3 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	1	DC2_OK	1	DC-DC2 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	0	DC1_OK	1	DC-DC1 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
R16527 (408Fh) Power Good Source 2	9	LDO10_OK	1	LDO10 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	8	LDO9_OK	1	LDO9 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	7	LDO8_OK	1	LDO8 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	6	LDO7_OK	1	LDO7 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	5	LDO6_OK	1	LDO6 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	4	LDO5_OK	1	LDO5 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	3	LDO4_OK	1	LDO4 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	2	LDO3_OK	1	LDO3 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	1	LDO2_OK	1	LDO2 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	0	LDO1_OK	1	LDO1 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled

Table 32 PWR_GOOD (GPIO) Configuration

15.14 DC-DC SYNCHRONOUS BUCK CONVERTER OPERATION

15.14.1 OVERVIEW

The WM8325-00C provides four DC-DC switching converters. Each of these is a synchronous buck (step-down) converter. The principal characteristics of each DC-DC converter are shown below. Converters DC-DC3 and DC-DC4 are configured in 'Dual mode', effectively operating as a single converter with increased current capability.

	DC-DC1 / DC-DC2	DC-DC3 / DC-DC4
Converter Type	Buck (step-down)	Buck (step-down)
Input Voltage Range	2.7V to 5.5V	2.7V to 5.5V
Output Voltage Range	0.6V to 1.8V	0.85V to 3.4V
Load Current Rating	Up to 1250mA (DC-DC1) Up to 2500mA (DC-DC2)	Up to 1600mA (dual mode)
Switching Frequency	2MHz	2MHz

Table 33 DC-DC Converter Overview

15.14.2 DC-DC SYNCHRONOUS BUCK CONVERTERS

DC-DC Converters 1, 2, 3 and 4 are synchronous buck converters which deliver high performance and high efficiency across a wide variety of operating conditions.

The high switching frequency, together with the current mode architecture, delivers exceptional transient performance suitable for supplying processor power domains and similar applications requiring high stability through fast-changing load (or line) conditions.

The current mode architecture enables extended bandwidth of the control loop, allowing the DC-DC converter to adapt for changes in input or output conditions more rapidly than can be achieved using other feedback mechanisms. This improves the converter's performance under transient load conditions.

The flexible design of the DC-DC Converters allows a selection of different operating configurations, which can be chosen according to the performance, efficiency, space or external component cost requirements.

The DC-DC Converters are compatible with a range of external output capacitors. A larger capacitor (eg. 47 μ F) will deliver best transient performance, whilst a smaller capacitor (eg. 22 μ F) may be preferred for size or cost reasons.

Four different operating modes can be selected, allowing the user to configure the converter performance and efficiency according to different demands. This includes power-saving modes for light load conditions and a high performance mode for best transient load performance. A low power LDO regulator mode is also provided. The DC-DC Converters maintain output voltage regulation when switching between operating modes.

Forced Continuous Conduction Mode (FCCM)

This mode delivers the best load transient performance across the entire operating load range of the converter. It also provides the best EMI characteristics due to the fixed, regular switching pattern.

For normal DC-DC buck converter operation, there is an inductor charging phase followed by a discharging phase. Under light load conditions, the inductor current may be positive or negative during this cycle. (Note that the load current corresponds to the average inductor current.) The negative portion of the cycle corresponds to inefficient operation, as the output capacitor is discharged unnecessarily by the converter circuit. Accordingly, this mode is not optimally efficient for light load conditions.

This mode offers excellent performance under transient load conditions. It exceeds the performance of the other operating modes in the event of a decreasing current demand or a decreasing voltage selection. This is because FCCM mode can actively pull down the output voltage to the required level, whilst other modes rely on the load to pull the converter voltage down under these conditions.

Another important benefit of this mode is that the switching pattern is fixed, regardless of load conditions. This provides best compatibility with noise-sensitive circuits where the noise frequency spectrum must be well-defined.

Although this mode is not optimally efficient for light loads, it delivers the best possible transient load performance and fixed frequency switching. This mode should be selected when best performance is required, delivering minimum output voltage ripple across all static or transient load conditions.

Auto Mode: Continuous / Discontinuous Conduction with Pulse-Skipping (CCM/DCM with PS)

This is an automatic mode that selects different control modes according to the load conditions. The converter supports the full range of load conditions in this mode, and automatically selects power-saving mechanisms when the load conditions are suitable. Under light load conditions, the efficiency in this mode is superior to the FCCM mode. The transient load performance may be slightly worse than FCCM mode.

The converter operates in Continuous Conduction Mode (CCM) for heavy load conditions, and Discontinuous Conduction Mode (DCM) under lighter loads. Discontinuous conduction is when the inductor current falls to zero during the discharge phase, and the converter disables the synchronous rectifier transistor in order that the inductor current remains at zero until the next charge phase. Negative inductor current is blocked in this mode, eliminating the associated losses, and improving efficiency.

The transient response in this mode varies according to the operating conditions; it differs from FCCM in the case of a decreasing current demand or a decreasing voltage, as the converter uses the load to pull the output voltage down to the required level. A light load will result in a slow response time.

A minimum inductor charge time is applied in DCM mode; this leads to a minimum average inductor current when operating as described above. Under very light load conditions, pulse skipping is used to reduce the average inductor current to the level required by the load. In pulse-skipping mode, the charge phase of selected cycles is not scheduled, and the load is supported by the output capacitor over more than one cycle of the switching frequency. As well as supporting very light load current conditions, this mechanism offers power savings, as the switching losses associated with the skipped pulses are eliminated. A disadvantage of this is that the transient response is degraded even further with respect to DCM. When the pulse-skipping behaviour is invoked, an increased output voltage ripple may be observed under some load conditions.

This mode is suitable for a wide range of operating conditions. It supports the full range of load currents, and offers efficiency savings under light load conditions.

Note that Auto Mode is not supported on DC-DC3 / DC-DC4 when configured in 'Dual mode'. These converters are configured in 'Dual mode' on the WM8325-00C.

Hysteretic Mode

Hysteretic mode is a power-saving mode. It does not support the full load capability of the DC-DC converter, but offers efficiency improvements over the FCCM and Auto (CCM/DCM with PS) modes.

The control circuit in Hysteretic mode operates very differently to the Pulse-Skipping mode that is available in Auto mode. In Pulse-Skipping mode, selected switching cycles are dropped in order to reduce the output current to match a light load condition, whilst maintaining good output voltage ripple as far as possible. In Hysteretic mode, the converter uses switched operation on an adaptive intermittent basis to deliver the required average current to the load.

In the switched operation portion of the Hysteretic mode, the converter drives the output voltage up; this is followed by a power-saving period in which the control circuit is largely disabled whilst the load pulls the output voltage down again over a period of many switching cycles. The duration of the fixed frequency bursts and the time between bursts is adapted automatically by the output voltage monitoring circuit.

In this mode, the power dissipation is reduced to a very low level by disabling parts of the control circuitry for the duration of selected switching cycles. This improves the overall efficiency, but also leads to output voltage ripple and limited performance. This mode produces a larger output voltage ripple than the Pulse-Skipping mode. In order to limit the degradation of the DC-DC converter performance in Hysteretic mode, the control circuit is designed for a restricted range of load conditions only. Note that the irregular switching pattern also results in degraded EMI behaviour.

Hysteretic mode and Pulse Skipping mode are both Pulse Frequency Modulation (PFM)-type modes, where the switching pulse frequency is adjusted dynamically according to the load requirements. A consequence of this frequency modulation is that the circuit's EMI characteristics are less predictable. In Hysteretic mode in particular, the EMI effects arising from the DC-DC switching are present across a wider frequency band than is the case in CCM and DCM. It is more difficult to effectively suppress the wide band interference, and this factor may result in Hysteretic mode being unsuitable for some operating conditions.

Hysteretic mode is suitable for light load conditions only, and only suitable for operating modes that are not sensitive to wide band RF/EMI effects. The output voltage ripple (and frequency) is load dependent, and is generally worse than Pulse-Skipping operation in the Auto mode. Provided that the EMI and voltage ripple can be tolerated, the Hysteretic mode offers an efficiency advantage over the Auto (CCM/DCM with PS) mode.

LDO Mode

In this mode, there is no FET switching at all, and the converter operates as a Low Drop-Out (LDO) regulator. In this mode, the FET switching losses are eliminated, as is the power consumption of the DC-DC control circuit. Under suitable operating conditions, this provides the most efficient option for light loads, without any of the EMI or voltage ripple limitations of Hysteretic mode.

As with any LDO, the output voltage is constant, and there is no internal source of voltage ripple. Unlike the switching modes, the power efficiency of the LDO mode is highly dependent on the input and output voltages; the LDO is most efficient when the voltage drop between input and output is small. The power dissipated as heat loss by an LDO increases rapidly as the input - output voltage difference increases.

LDO mode is suitable for light loads, and provides a ripple-free output. The LDO mode features a very low start-up current; this mode can be used to avoid the higher in-rush current that occurs in the switching converter modes. The efficiency is dependent on the input - output voltage configuration; the LDO mode can be highly efficient, but may also be unacceptably inefficient. If an improvement in power efficiency is required, then Hysteretic mode may be the preferred choice or, for better EMI and voltage ripple, the Auto (CCM/DCM with PS) mode may be the optimum selection.

Operating Mode Summary

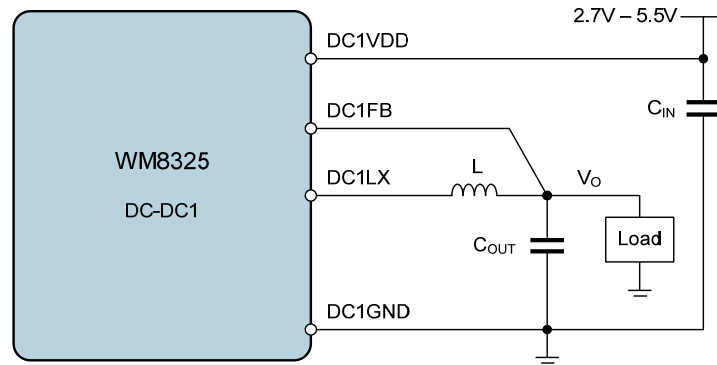
MODE	DESCRIPTION	APPLICATION
Forced Continuous Conduction Mode (FCCM)	Buck converter operation where inductor current is continuous at all times.	High performance for all static and transient load conditions. Fixed frequency switching offers best compatibility with sensitive circuits.
Auto Mode: Continuous / Discontinuous Conduction with Pulse-Skipping Mode (CCM/DCM with PS)	Buck converter operation where inductor current may be discontinuous under reduced loads; pulse-skipping also enabled under lighter loads.	High efficiency for all static and transient load conditions. Performance may be less than FCCM mode for heavy load transients.
Hysteretic Mode	The converter uses a hysteretic control scheme with pulsed switching operation. The control circuitry is disabled intermittently for power saving.	High efficiency for light static and light transient loads only. Maximum load current is restricted; output voltage ripple is increased.
LDO Mode	No FET switching at all; linear regulator operation.	Power saving mode for light loads only. High efficiency for ultra light loads. Low current soft-start control.

Table 34 DC-DCSynchronous Buck Converter Operating Modes Summary

Typical Connections - DC-DC1 and DC-DC2

The typical connections to DC-DC Converters 1 and 2 are illustrated in Figure 19.

The input voltage connection to DC-DC Converters 1 and 2 is provided on DC1VDD and DC2VDD respectively; these pins must be connected to the PVDD power supply voltage node.



Note: Equivalent circuit applies for DC-DC2

Figure 19 DC-DC1 and DC-DC2 Synchronous Buck Converter Connections

See Section 30.5 for details of specific recommended external inductor and capacitor components.

Typical Connections - DC-DC3 and DC-DC4

DC-DC Converters 3 and 4 are configured to operate in 'Dual' mode, where the two converters are ganged together to support an increased current capability. The external component configuration is similar to DC-DC1 and DC-DC2; output load connection points (V_o) are connected together.

The typical connections to DC-DC Converters 1 and 2 are illustrated in Figure 20.

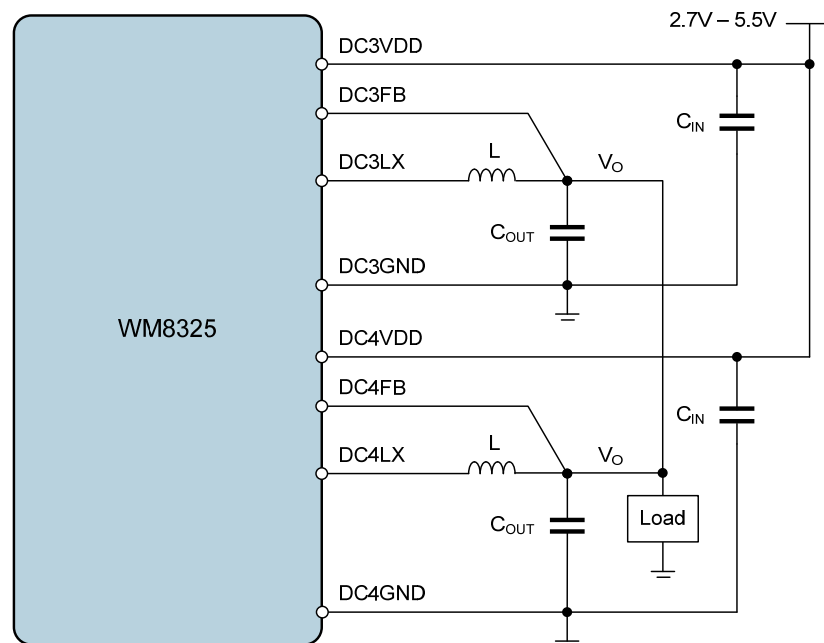


Figure 20 DC-DC3 and DC-DC4 Dual Mode Converter Connections

See Section 30.5 for details of specific recommended external inductor and capacitor components.

15.15 LDO REGULATOR OPERATION

15.15.1 OVERVIEW

The WM8325-00C provides 11 LDO Regulators. Four of these are low-noise analogue LDOs. One of the LDO Regulators (LDO11) can be configured to be enabled even when the WM8325-00C is in the OFF state. The principal characteristics of the LDO Regulators are shown below.

	LDO1	LDO2, 3	LDO4, 5, 6	LDO7, 8	LDO9, 10	LDO11
Converter Type	General Purpose	General Purpose	General Purpose	Analogue	Analogue	General Purpose
Input Voltage Range	1.5V to 5.5V	1.5V to 5.5V	1.5V to 5.5V	1.71V to 5.5V	1.71V to 5.5V	1.8V to 5.5V
Output Voltage Range	0.9V to 3.3V	0.9V to 3.3V	0.9V to 3.3V	1.0V to 3.5V	1.0V to 3.5V	0.8V to 1.55V
Load Current Rating	Up to 300mA	Up to 200mA	Up to 100mA	Up to 200mA	Up to 150mA	Up to 25mA
Pass device impedance @ 2.5V	1Ω	1Ω	2Ω	1Ω	2Ω	n/a

Table 35 LDO Regulator Overview

15.15.2 LDO REGULATORS

The LDO Regulators are configurable circuits which generate accurate, low-noise supply voltages for various system components. The LDO Regulators are dynamically programmable and can be re-configured at any time. Two low power modes are provided for the general purpose LDOs 1-6; a single low power mode is provided for the analogue LDOs 7-10; this enables the overall device power consumption to be minimised at all times.

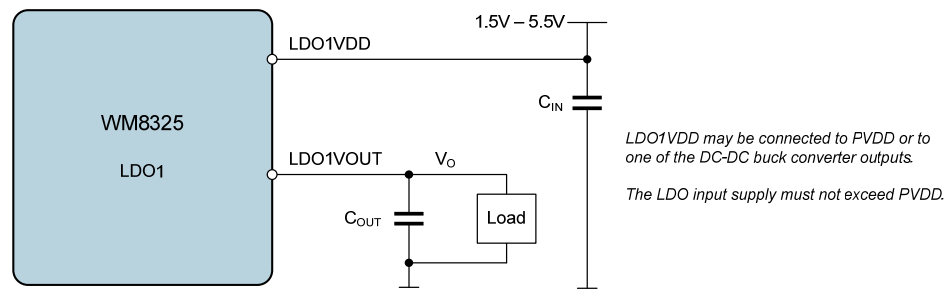
The LDOs 1-10 can also operate as current-limited switches, with no voltage regulation; this is useful for 'Hot Swap' outputs, i.e. supply rails for external devices that are plugged in when the system is already powered up - the current-limiting function prevents the in-rush current into the external device from disturbing other system power supplies.

The input voltage to these LDOs is provided on pins LDO3VDD, LDO4VDD, LDO5VDD, LDO6VDD for LDO3 through to LDO6 respectively. The other LDO inputs are shared on pins LDO1_2VDD, LDO7_8VDD and LDO9_10VDD for each corresponding pair of LDOs.

The LDO input supply pins may be connected to the PVDD power supply voltage node, or else can be connected to the output pin of one of the DC-DC buck converters. Note that the LDO input supply pins must not be connected to a voltage higher than PVDD.

LDO11 is a configurable LDO intended for 'always-on' functions external to the WM8325-00C. The WM8325-00C contains a further two non-configurable LDOs which support internal functions only.

The connections to LDO Regulator 1 are illustrated in Figure 21. The equivalent circuit applies to LDO2 through to LDO10.



Note: Equivalent circuit applies for LDO2 through to LDO10.

Figure 21 LDO Regulator Connections

An input and output capacitor are recommended for each LDO Regulator, as illustrated above.

See Section 30.6 for details of specific recommended external components.

16 RESERVED

17 POWER SUPPLY CONTROL

17.1 GENERAL DESCRIPTION

The primary power supply to the WM8325-00C is provided via the PVDD pin. This supply is required for normal device functionality. The PVDD voltage is monitored internally to detect a low voltage condition where the device can no longer operate. A Power Path Management Interrupt is raised when PVDD falls below an undervoltage threshold, as described in Section 17.2.

A backup power source may be provided for the WM8325-00C. This enables the Real Time Clock (RTC) and other selected registers to be maintained when PVDD is not available. This is described in Section 17.3.

17.2 POWER PATH MANAGEMENT INTERRUPTS

The Power Path Management circuit is associated with an Interrupt event flag.

The PPM_SYSLO_EINT interrupt bit is set when the internal signal $\overline{\text{SYSLO}}$ is asserted. This indicates a PVDD undervoltage condition, described in Section 24.4. This secondary interrupt triggers a primary Power Path Management Interrupt, PPM_INT (see Section 23). This can be masked by setting the mask bit as described in Table 36.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	15	PPM_SYSLO_EINT	Power Path SYSLO interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
R16409 (4019h) Interrupt Status 1 Mask	15	IM_PPM_SYSLO_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 36 Power Path Management Interrupt

17.3 BACKUP POWER

As an option, a backup power source can be provided for the WM8325-00C. This is provided using a coin cell, super/gold capacitor, or else a standard capacitor, connected to the LDO12VOUT pin.

Note that a 22k Ω series resistor should also be connected to the backup power source.

The LDO12VOUT pin provides a constant voltage output for charging the backup power source whenever the PVDD power domain is available.

The purpose of the backup is to power the always-on functions such as the crystal oscillator, RTC and ALARM control registers. The backup power also maintains a 'software scratch' memory area in the register map - see Section 12.6. Maintaining these functions at all times provides system continuity even when the main battery is removed and no other power supply is available.

The backup duration will vary depending upon the backup power source characteristics. A typical coin cell can provide power to the WM8325-00C in BACKUP mode for a month or more whilst also maintaining the RTC and the 'software scratch' register.

If a standard capacitor is used as the backup power source, then it is particularly important to minimise the device power consumption in the BACKUP state. A 22 μ F capacitor will maintain the device settings for up to 5 minutes in 'unlocked' mode, where power consumption is minimised by stopping the RTC in the BACKUP state. The RTC is unlocked in the BACKUP state if the XTAL_BKUPENA register field is set to 0, as described in Section 20.5.

18 AUXILIARY ADC

18.1 GENERAL DESCRIPTION

The WM8325-00C incorporates a 12-bit Auxiliary ADC (AUXADC). This can be used to perform a number of system measurements (including supply voltages and battery temperature) and can also be used to measure analogue voltages from external sources and sensors.

External inputs to the AUXADC should be connected to the pins GPIO10, GPIO11 and GPIO12. The maximum voltage that can be measured is determined by the power domain associated with each; this is selectable on a pin by pin basis as described in Section 21.3.

Note that, when GPIO10, GPIO11 or GPIO12 is used as an input to the AUXADC, then the normal GPIO functionality cannot be supported on the affected pin(s). In this case, it is recommended that the respective GPIO(s) are tri-stated, as described in Section 21.3.

18.2 AUXADC CONTROL

The AUXADC is enabled by setting the AUX_ENA register bit. By default, the AUXADC is not enabled in the SLEEP state, but this can be selected using the AUX_SLPENA field.

The AUXADC measurements can be initiated manually or automatically. For automatic operation, the AUX_RATE register is set according to the required conversion rate, and conversions are enabled by setting the AUX_CVT_ENA bit. For manual operation, the AUX_RATE register is set to 00h, and each manual conversion is initiated by setting the AUX_CVT_ENA bit. In manual mode, the AUX_CVT_ENA bit is reset by the WM8325-00C after each conversion. (Note that the conversion result is not available for readback until the AUXADC interrupt is asserted, as described in Section 18.5.)

The AUXADC has 5 available input sources. Each of these inputs is enabled by setting the respective bit in the AuxADC Source Register (R16431).

For each AUXADC measurement event (in Manual or Automatic modes), the WM8325-00C selects the next enabled input source. Any number of inputs may be selected simultaneously; the AUXADC will measure each one in turn. Note that only a single AUXADC measurement is made on any Manual or Automatic trigger.

For example, if the GPIO10, GPIO12 and PVDD voltages are enabled for AUXADC measurement, then GPIO10 would be measured in the first instance, and GPIO12 then PVDD would be measured on the next manual or automatic AUXADC triggers. In this case, a total of three manual or automatic AUXADC triggers would be required to measure all of the selected inputs.

The control fields associated with initiating AUXADC measurements are defined in Table 37.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16430 (402Eh) AuxADC Control	15	AUX_ENA	0	AUXADC Enable 0 = Disabled 1 = Enabled Note - this bit is reset to 0 when the OFF power state is entered.
	14	AUX_CVT_ENA	0	AUXADC Conversion Enable 0 = Disabled 1 = Enabled In automatic mode, conversions are enabled by setting this bit. In manual mode (AUX_RATE = 0), setting this bit will initiate a conversion; the bit is reset automatically after each conversion.
	12	AUX_SLPENA	0	AUXADC SLEEP Enable 0 = Disabled 1 = Controlled by AUX_ENA

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	5:0	AUX_RATE [5:0]	00_0000	AUXADC Conversion Rate 0 = Manual 1 = 2 samples/s 2 = 4 samples/s 3 = 6 samples/s ... 31 = 62 samples/s 32 = Reserved 33 = 16 samples/s 34 = 32 samples/s 35 = 48 samples/s ... 63 = 496 samples/s
R16431 (402Fh) AuxADC Source	6	AUX_PVDD_SEL	0	AUXADC PVDD input select 0 = Disable PVDD measurement 1 = Enable PVDD measurement
	4	AUX_CHIP_TEMP_SEL	0	AUXADC Chip Temp input select 0 = Disable Chip Temp measurement 1 = Enable Chip Temp measurement
	2	AUX_GPIO12_SEL	0	AUXADC GPIO12 input select 0 = Disable GPIO12 measurement 1 = Enable GPIO12 measurement
	1	AUX_GPIO11_SEL	0	AUXADC GPIO11 input select 0 = Disable GPIO11 measurement 1 = Enable GPIO11 measurement
	0	AUX_GPIO10_SEL	0	AUXADC GPIO10 input select 0 = Disable GPIO10 measurement 1 = Enable GPIO10 measurement

Table 37 AUXADC Control

18.3 AUXADC READBACK

Measured data from the AUXADC is read via the AuxADC Data Register (R16429), which contains two fields. The AUXADC Data Source is indicated in the AUX_DATA_SRC field; the associated measurement data is contained in the AUX_DATA field.

Reading from the AuxADC Data Register returns a 12-bit code which represents the most recent AUXADC measurement on the associated channel. It should be noted that every time an AUXADC measurement is written to the AuxADC Data Register, the previous data is overwritten - the host processor should ensure that data is read from this register before it is overwritten. The AUXADC interrupts can be used to indicate when new data is available - see Section 18.5.

The 12-bit AUX_DATA field can be equated to the actual voltage (or temperature) according to the following equations, where AUX_DATA is regarded as an unsigned integer:

$$\text{Voltage (mV)} = \text{AUX_DATA} \times 1.465$$

$$\text{Chip Temp (}^{\circ}\text{C)} = \frac{498 - \text{AUX_DATA}}{1.09}$$

The maximum voltage that can be measured on the input pins GPIO10, GPIO11 and GPIO12 is determined by the power domain associated with each; this is selectable on a pin by pin basis using the GPN_PWR_DOM register bits described in Section 21.3. The input voltage at the GPIO pin must not exceed the voltage of the respective power domain (ie. DBVDD or PVDD).

In a typical application, it is anticipated that the AUXADC Interrupts would be used to control the AUXADC readback - the host processor should read the AUXADC Data Register in response to the AUXADC Interrupt event. See Section 18.5 for details of AUXADC Interrupts. In Automatic AUXADC mode, the processor should complete this action before the next measurement occurs, in order to avoid losing any AUXADC samples. In Manual conversion mode, the interrupt signal provides confirmation that the commanded measurement has been completed.

The control fields associated with initiating AUXADC readback are defined in Table 38.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16429 (402Dh) AuxADC Data	15:12	AUX_DATA_SRC [3:0]	000	AUXADC Data Source 1 = GPIO10 2 = GPIO11 3 = GPIO12 5 = Chip Temperature 7 = PVDD voltage All other values are Reserved
	11:0	AUX_DATA [11:0]	000h	AUXADC Measurement Data Voltage (mV) = AUX_DATA x 1.465 ChipTemp (°C) = (498 - AUX_DATA) / 1.09

Table 38 AUXADC Readback

18.4 DIGITAL COMPARATORS

The WM8325-00C has four digital comparators which may be used to compare AUXADC measurement data against programmable threshold values. Each comparator has a status bit, and also an associated interrupt flag (described in Section 18.5), which indicates that the associated data is beyond the threshold value.

The digital comparators are enabled using the DCMP n _ENA register bits as described in Table 37.

After an AUXADC conversion, the measured value is compared with the threshold level of any associated comparator(s). Note that this comparison is only performed following a conversion.

The source data for each comparator is selected using the DCMP n _SRC register bits; this selects one of the AUXADC channels for each comparator. If required, the same AUXADC channel may be selected for more than one comparator; this would allow more than one threshold to be monitored on the same AUXADC channel. Note that the Backup Battery voltage input can only be monitored using DCMP4.

The DCMP n _GT register bits select whether the status bit and associated interrupt flag will be asserted when the measured value is above the threshold or when the measured value is below the threshold. The output of the most recent threshold comparison is indicated in the DCOMP n _STS fields.

The threshold DCMP n _THR is a 12-bit code for each comparator. This field follows the same voltage or temperature coding as the associated AUXADC channel source (see Section 18.3).

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16432 (4030h) Comparator Control	11	DCOMP4_STS	0	Digital Comparator 4 status 0 = Comparator 4 threshold not detected 1 = Comparator 4 threshold detected (Trigger is controlled by DCMP4_GT)
	10	DCOMP3_STS	0	Digital Comparator 3 status 0 = Comparator 3 threshold not detected 1 = Comparator 3 threshold detected (Trigger is controlled by DCMP3_GT)
	9	DCOMP2_STS	0	Digital Comparator 2 status 0 = Comparator 2 threshold not detected 1 = Comparator 2 threshold detected (Trigger is controlled by DCMP2_GT)
	8	DCOMP1_STS	0	Digital Comparator 1 status 0 = Comparator 1 threshold not detected 1 = Comparator 1 threshold detected (Trigger is controlled by DCMP1_GT)
	3	DCMP4_ENA	0	Digital Comparator 4 Enable 0 = Disabled 1 = Enabled
	2	DCMP3_ENA	0	Digital Comparator 3 Enable 0 = Disabled 1 = Enabled
	1	DCMP2_ENA	0	Digital Comparator 2 Enable 0 = Disabled 1 = Enabled
	0	DCMP1_ENA	0	Digital Comparator 1 Enable 0 = Disabled 1 = Enabled

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16433 (4031h) Comparator 1	15:13	DCMP1_SRC [2:0]	000	Digital Comparator 1 source select 0 = Reserved 1 = GPIO10 2 = GPIO11 3 = GPIO12 4 = Reserved 5 = Chip Temperature 6 = Reserved 7 = PVDD voltage
	12	DCMP1_GT	0	Digital Comparator 1 interrupt control 0 = interrupt when less than threshold 1 = interrupt when greater than or equal to threshold
	11:0	DCMP1_THR	000h	Digital Comparator 1 threshold (12-bit unsigned binary number; coding is the same as AUX_DATA)
R16434 (4032h) Comparator 2	15:13	DCMP2_SRC [2:0]	000	Digital Comparator 2 source select 0 = Reserved 1 = GPIO10 2 = GPIO11 3 = GPIO12 4 = Reserved 5 = Chip Temperature 6 = Reserved 7 = PVDD voltage
	12	DCMP2_GT	0	Digital Comparator 2 interrupt control 0 = interrupt when less than threshold 1 = interrupt when greater than or equal to threshold
	11:0	DCMP2_THR	000h	Digital Comparator 2 threshold (12-bit unsigned binary number; coding is the same as AUX_DATA)
R16435 (4033h) Comparator 3	15:13	DCMP3_SRC [2:0]	000	Digital Comparator 3 source select 0 = Reserved 1 = GPIO10 2 = GPIO11 3 = GPIO12 4 = Reserved 5 = Chip Temperature 6 = Reserved 7 = PVDD voltage
	12	DCMP3_GT	0	Digital Comparator 3 interrupt control 0 = interrupt when less than threshold 1 = interrupt when greater than or equal to threshold
	11:0	DCMP3_THR	000h	Digital Comparator 3 threshold (12-bit unsigned binary number; coding is the same as AUX_DATA)

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16436 (4034h) Comparator 4	15:13	DCMP4_SRC [2:0]	000	Digital Comparator 4 source select 0 = Backup Battery voltage 1 = GPIO10 2 = GPIO11 3 = GPIO12 4 = Reserved 5 = Chip Temperature 6 = Reserved 7 = PVDD voltage
	12	DCMP4_GT	0	Digital Comparator 4 interrupt control 0 = interrupt when less than threshold 1 = interrupt when greater than or equal to threshold
	11:0	DCMP4_THR	000h	Digital Comparator 4 threshold (12-bit unsigned binary number; coding is the same as AUX_DATA)

Table 39 AUXADC Digital Comparator Control

18.5 AUXADC INTERRUPTS

The AUXADC is associated with a number of Interrupt event flags to indicate when new AUXADC data is ready, or to indicate that one or more of the digital comparator thresholds has been crossed. Each of these secondary interrupts triggers a primary AUXADC Interrupt, AUXADC_INT (see Section 23). This can be masked by setting the mask bit(s) as described in Table 40.

Note that AUXADC_DATA_EINT is not cleared by reading the measured AUXADC data, it can only be cleared by writing '1' to the AUXADC_DATA_EINT register.

The AUXADC interrupts can be programmed using bits in Table 40.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	8	AUXADC_DATA_EINT	AUXADC Data Ready interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
	7:4	AUXADC_DCOMP _n _EINT	AUXADC Digital Comparator <i>n</i> interrupt (Trigger is controlled by DCMP _n _GT) Note: Cleared when a '1' is written.
R16409 (4019h) Interrupt Status 1 Mask	8	IM_AUXADC_DATA_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	7:4	IM_AUXADC_DCOMP _n _EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
Note: <i>n</i> is a number between 1 and 4 that identifies the individual Comparator.			

Table 40 AUXADC Interrupts

19 RESERVED

20 REAL-TIME CLOCK (RTC)

20.1 GENERAL DESCRIPTION

The WM8325-00C provides a Real Time Clock (RTC) in the form of a 32-bit counter. The RTC uses the 32.768kHz crystal oscillator as its clock source and increments the register value once per second. (Note that a direct CMOS input may be used in place of the crystal oscillator; both options are described in Section 13.) To compensate for errors in the clock frequency, the RTC includes a frequency trim capability.

The RTC is enabled at all times, including when the WM8325-00C is in the BACKUP state. When required, the RTC can be maintained via a backup battery in the absence of any other power supply. In the absence of a backup battery, the RTC contents can be held (unlocked) for a limited period of up to 5 minutes via a 22 μ F capacitor.

The RTC incorporates an Alarm function. The Alarm time is held in a 32-bit register. When the RTC counter matches the Alarm time, a selectable response will be actioned.

For digital rights management purposes, the RTC includes security features designed to detect unauthorised modifications to the RTC counter.

20.2 RTC CONTROL

The 32-bit RTC counter value, RTC_TIME is held in two 16-bit registers, R16417 (4021h) and R16418 (4022h). The value of RTC_TIME is incremented by the WM8325-00C once per second. On initial power-up (from the NO POWER state), these registers will be initialised to default values. Once either of these registers has been written to, the RTC_VALID bit is set to indicate that the RTC_TIME registers contain valid data.

When RTC registers are updated, the RTC_SYNC_BUSY bit indicates that the RTC is busy. The RTC registers should not be written to when RTC_SYNC_BUSY = 1.

The RTC_WR_CNT field is provided as a security feature for the RTC. After initialisation, this field is updated on every write to R16417 (4021h) or to R16418 (4022h). This enables the host processor to detect unauthorised modifications to the RTC counter value. See Section 20.4 for more details.

For additional security, the WM8325-00C does not allow the RTC to be updated more than 8 times in a one-hour period. Additional write attempts will be ignored.

The RTC Alarm time is held in registers R16419 (4023h) and R16420 (4024h). The Alarm function is enabled when RTC_ALM_ENA is set. When the Alarm is enabled, and the RTC counter matches the Alarm time, the RTC Alarm Interrupt is triggered, as described in Section 20.3.

If the RTC Alarm occurs in the SLEEP power state, then a WAKE transition request is generated. If the RTC Alarm occurs in the OFF power state, then an ON transition request is generated. See Section 11.3 for details.

When updating the RTC Alarm time, it is recommended to disable the Alarm first, by setting RTC_ALM_ENA = 0. The RTC Alarm registers should not be written to when RTC_SYNC_BUSY = 1.

The RTC has a frequency trim feature to allow compensation for known and constant errors in the crystal oscillator frequency up to ± 8 Hz. The RTC_TRIM field is a 10-bit fixed point 2's complement number. MSB scaling = -8Hz. To compensate for errors in the clock frequency, this register should be set to the error (in Hz) with respect to the ideal (32768Hz) of the input crystal frequency.

For example, if the actual crystal frequency = 32769.00Hz, then the frequency error = +1Hz. The value of RTC_TRIM in this case is 0001_000000.

For example, if the actual crystal frequency = 32763.78Hz, then the frequency error = -4.218750Hz. The value of RTC_TRIM in this case is 1011_110010.

Note that the RTC_TRIM control register is locked by the WM8325-00C User Key. This register can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16416 (4020h) RTC Write Counter	15:0	RTC_WR_CNT	0000h	RTC Write Counter. This random number is updated on every write to the RTC_TIME registers.
R16417 (4021h) RTC Time 1	15:0	RTC_TIME [31:16]	0000h	RTC Seconds counter (MSW) RTC_TIME increments by 1 every second. This is the 16 MSBs.
R16418 (4022h) RTC Time 2	15:0	RTC_TIME [15:0]	0000h	RTC Seconds counter (LSW) RTC_TIME increments by 1 every second. This is the 16 LSBs.
R16419 (4023h) RTC Alarm 1	15:0	RTC_ALM [31:16]	0000h	RTC Alarm time (MSW) 16 MSBs of RTC_ALM
R16420 (4024h) RTC Alarm 2	15:0	RTC_ALM [15:0]	0000h	RTC Alarm time (LSW) 16 LSBs of RTC_ALM
R16421 (4025h) RTC Control	15	RTC_VALID	0	RTC Valid status 0 = RTC_TIME has not been set since Power On Reset 1 = RTC_TIME has been written to since Power On Reset
	14	RTC_SYNC_BUSY	0	RTC Busy status 0 = Normal 1 = Busy The RTC registers should not be written to when RTC_SYNC_BUSY = 1.
	10	RTC_ALM_ENA	0	RTC Alarm Enable 0 = Disabled 1 = Enabled
R16422 (4026h) RTC Trim	9:0	RTC_TRIM	000h	RTC frequency trim. Value is a 10bit fixed point <4,6> 2's complement number. MSB Scaling = -8Hz. The register indicates the error (in Hz) with respect to the ideal 32768Hz) of the input crystal frequency. <i>Protected by user key</i>

Table 41 Real Time Clock (RTC) Control

20.3 RTC INTERRUPTS

The Real Time Clock (RTC) is associated with two Interrupt event flags.

The RTC_PER_EINT interrupt is set each time a periodic timeout occurs. The periodic timeout is configured using the RTC_PINT_FREQ field described in Table 43.

The RTC_ALM_EINT interrupt is set when the RTC Alarm is triggered. The RTC Alarm time is configured as described in Section 20.2.

Each of these secondary interrupts triggers a primary Real Time Clock Interrupt, RTC_INT (see Section 23). This can be masked by setting the mask bit(s) as described in Table 42.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	3	RTC_PER_EINT	RTC Periodic interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
	2	RTC_ALM_EINT	RTC Alarm interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
R16409 (4019h) Interrupt Status 1 Mask	3	IM_RTC_PER_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	2	IM_RTC_ALM_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 42 Real Time Clock (RTC) Interrupts

The frequency of the RTC periodic interrupts is set by the RTC_PINT_FREQ field, as described in Table 43.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16421 (4025h) RTC Control	6:4	RTC_PINT_FREQ [2:0]	000	RTC Periodic Interrupt timeout period 000 = Disabled 001 = 2s 010 = 4s 011 = 8s 100 = 16s 101 = 32s 110 = 64s 111 = 128s

Table 43 Real Time Clock (RTC) Periodic Interrupt Control

20.4 DIGITAL RIGHTS MANAGEMENT

The Real Time Clock (RTC) maintains a continuous record of the time; this is maintained at all times, including when the WM8325-00C is powered down and the RTC function is maintained by the backup battery.

It is highly desirable to be able to write to the RTC counter in order to configure it for logical translation into hours/minutes and to support calendar functions. However, for digital rights management purposes, it is important that malicious modification of the RTC is either prevented or detected.

The security measure implemented on the WM8325-00C is the RTC Write Counter. This register is initialised to 0000h during Power On Reset, and is updated automatically whenever a Write operation is scheduled on either of the RTC_TIME registers. Note that, when the RTC Write Counter is updated, the new value is generated at random; it is not a sequential counter.

It is assumed that legitimate updates to the RTC_TIME are only those initiated by the Application Processor (AP). When the AP makes an update to the RTC_TIME, the AP can also read the new value of the RTC Write Counter, and should store the value in non-volatile memory. If the AP detects a change in value of the RTC Write Counter, and this was not caused by the AP itself writing to the RTC_TIME, this means that an unauthorised write to the RTC_TIME registers has occurred.

In order to make it difficult for an unauthorised RTC_TIME update to be masked by simply writing to the RTC Write Counter, the RTC_WR_CNT field is generated at random by the WM8325-00C whenever the RTC_TIME field is updated.

For additional security, the WM8325-00C does not allow the RTC to be updated more than 8 times in a one-hour period. Additional write attempts will be ignored.

The RTC Control registers are described in Table 41.

20.5 BACKUP MODE CLOCKING OPTIONS

The BACKUP state is entered when the PVDD power supply is below the reset threshold of the device. Typically, this means that the PVDD supply has been removed. Most of the device functions and registers are reset in this state.

The RTC and oscillator and a 'software scratch' memory area can be maintained from a backup power source in the BACKUP state. This is provided using a coin cell, super/gold capacitor, or else a standard capacitor, connected to the LDO12VOUT pin via a 22k Ω resistor. See Section 17.3 for further details.

The RTC and oscillator can be disabled in the BACKUP state by setting the XTAL_BKUPENA register bit to 0. This feature may be used to minimise the device power consumption in the BACKUP state. A 22 μ F capacitor connected to LDO12VOUT can maintain the RTC value, unlocked, for up to 5 minutes in BACKUP if the oscillator is disabled.

The XTAL_BKUPENA register bit is defined in Section 13.1. For more details on backup power, see Section 17.3.

21 GENERAL PURPOSE INPUTS / OUTPUTS (GPIO)

21.1 GENERAL DESCRIPTION

The WM8325-00C has 12 general-purpose input/output (GPIO) pins, GPIO1 - GPIO12. These can be configured as inputs or outputs, active high or active low, with optional on-chip pull-up or pull-down resistors. GPIO outputs can either be CMOS driven or Open Drain configuration. Each GPIO pin can be tri-stated and can also be used to trigger Interrupts.

The function of each GPIO pin is selected individually. Different voltage power domains are selectable on a pin by pin basis for GPIOs 1-12. Input de-bounce is automatically implemented on selected GPIO functions.

Note that, when GPIO10, GPIO11 or GPIO12 is used as an input to the AUXADC (see Section 18), then the normal GPIO functionality cannot be supported on the affected pin(s). It is recommended that the respective GPIO(s) are tri-stated, as described in Section 21.3.

21.2 GPIO FUNCTIONS

The list of GPIO functions supported by the WM8325-00C is contained in Table 44 (for input functions) and Table 45 (for output functions). The input functions are selected when the respective GPn_DIR register bit is 1. The output functions are selected when the respective GPn_DIR register bit is 0.

The selected function for each GPIO pin is selected by writing to the respective GPn_FN register bits. All functions are available on all GPIO pins. The polarity of each input or output GPIO function can be selected using the applicable GPn_POL register bit.

The available power domains for each pin are specific to different GPIOs.

The de-bounce time for the GPIO input functions is determined by the GPn_FN field. Some of the input functions allow a choice of de-bounce times, as detailed in Table 44.

The register controls for configuring the GPIO pins are defined in Section 21.3.

GPn_FN	GPIO INPUT FUNCTION	DESCRIPTION	DE-BOUNCE TIME
0h	GPIO	GPIO input. Logic level is read from the GPn_LVL register bits. See Section 21.3.	32 μ s to 64 μ s
1h			4ms to 8ms
2h	ON/OFF Request	Control input for requesting an ON/OFF state transition. See Section 11.3. Under default polarity ($GPn_POL=1$), a rising edge requests the ON state and a falling edge requests the OFF state.	32ms 64ms
3h	SLEEP/WAKE Request	Control input for requesting a SLEEP/WAKE state transition. See Section 11.3. Under default polarity ($GPn_POL=1$), a rising edge requests the SLEEP state and a falling edge requests the WAKE transition to the ON state.	32 μ s to 64 μ s
4h			32ms to 64ms
5h	SLEEP Request	Control input for requesting a SLEEP state transition. See Section 11.3. Under default polarity ($GPn_POL=1$), a rising edge requests the SLEEP state and a falling edge has no effect.	32 μ s to 64 μ s
6h	ON Request	Control input for requesting an ON state transition. See Section 11.3. Under default polarity ($GPn_POL=1$), a rising edge requests the ON state and a falling edge has no effect.	32 μ s to 64 μ s
7h	Watchdog Reset	Control input for resetting the Watchdog Timer. See Section 25.	32 μ s to 64 μ s

GPn_FN	GPIO INPUT FUNCTION	DESCRIPTION	DE-BOUNCE TIME
8h	Hardware DVS control 1	Control input for selecting the DVS output voltage in one or more DC-DC Converters. See Section 15.6.	None
9h	Hardware DVS control 2	Control input for selecting the DVS output voltage in one or more DC-DC Converters. See Section 15.6.	None
Ah	Hardware Enable 1	Control input for enabling one or more DC-DC Converters and LDO Regulators. See Section 15.	32 μ s to 64 μ s
Bh	Hardware Enable 2	Control input for enabling one or more DC-DC Converters and LDO Regulators. See Section 15.	32 μ s to 64 μ s
Ch	Hardware Control input 1	Control input for selecting the operating mode and/or output voltage of one or more DC-DC Converters and LDO Regulators. See Section 15.	32 μ s to 64 μ s
Dh	Hardware Control input 2	Control input for selecting the operating mode and/or output voltage of one or more DC-DC Converters and LDO Regulators. See Section 15.	32 μ s to 64 μ s
Eh	Hardware Control input 1	Control input for selecting the operating mode and/or output voltage of one or more DC-DC Converters and LDO Regulators. See Section 15.	32ms to 64ms
Fh	Hardware Control input 2	Control input for selecting the operating mode and/or output voltage of one or more DC-DC Converters and LDO Regulators. See Section 15.	32ms to 64ms

Table 44 List of GPIO Input Functions

Further details of the GPIO input de-bounce time are noted in Section 21.3.

GPn_FN	GPIO OUTPUT FUNCTION	DESCRIPTION
0h	GPIO	GPIO output. Logic level is set by writing to the GPn_LVL register bits. See Section 21.3.
1h	Oscillator clock	32.768kHz clock output. See Section 13.
2h	ON state	Logic output indicating that the WM8325-00C is in the ON state. See Section 11.5.
3h	SLEEP state	Logic output indicating that the WM8325-00C is in the SLEEP state. See Section 11.5.
4h	Power State Change	Logic output asserted whenever a Power On Reset, or an ON, OFF, SLEEP or WAKE transition has completed. Under default polarity (GPn_POL=1), the logic level is the same as the PS_INT interrupt status flag. Note that, if any of the associated Secondary interrupts is masked, then the respective event will not affect the Power State Change GPIO output. See Section 11.2 and Section 11.4.
8h	DC-DC1 DVS Done	Logic output indicating that DC-DC1 buck converter DVS slew has been completed. This signal is temporarily de-asserted during voltage transitions (including non-DVS transitions). See Section 15.6.
9h	DC-DC2 DVS Done	Logic output indicating that DC-DC2 buck converter DVS slew has been completed. This signal is temporarily de-asserted during voltage transitions (including non-DVS transitions). See Section 15.6.

GPn_FN	GPIO OUTPUT FUNCTION	DESCRIPTION
Ah	External Power Enable 1	Logic output assigned to one of the timeslots in the ON/OFF and SLEEP/WAKE sequences. This can be used for sequenced control of external circuits. See Section 15.3.
Bh	External Power Enable 2	Logic output assigned to one of the timeslots in the ON/OFF and SLEEP/WAKE sequences. This can be used for sequenced control of external circuits. See Section 15.3.
Ch	System Supply Good (PVDD Good)	Logic output from PVDD monitoring circuit. This function represents the internal SYSOK signal. See Section 24.4.
Dh	Converter Power Good (PWR_GOOD)	Status output indicating that all selected DC-DC converters and LDO regulators are operating correctly. Only asserted in ON and SLEEP modes. See Section 15.13.
Eh	External Power Clock	2MHz clock output suitable for clocking external DC-DC converters. This clock signal is synchronized with the WM8325-00C DC Converters clocking signal. See Section 13. This clock output is only enabled when either of the External Power Enable signals (EPE1 or EPE2) is asserted. These signals can be assigned to one of the timeslots in the ON/OFF and SLEEP/WAKE sequences. See Section 15.3.
Fh	Auxiliary Reset	Logic output indicating a Reset condition. This signal is asserted in the OFF state. The status in SLEEP mode is configurable. See Section 11.7. Note that the default polarity for this function (GPn_POL=1) is "Active High". Setting GPn_POL=0 will select "Active Low" function.

Table 45 List of GPIO Output Functions

21.3 CONFIGURING GPIO PINS

The GPIO pins are configured using the Register fields defined in Table 46.

The function of each GPIO is selected using the GPn_FN register field. The pin direction field GPn_DIR selects between input functions and output functions. See Section 21.2 for a summary of the available GPIO functions.

The polarity of each GPIO can be configured using the GPn_POL bits. This inversion is effective both on GPIO inputs and outputs. When GPn_POL = 1, the non-inverted 'Active High' polarity applies. The opposite logic can be selected by setting GPn_POL = 0.

The voltage power domain of each GPIO is determined by the GPn_PWR_DOM register. Note that the available options vary between different GPIO pins, as described in Table 48.

A GPIO output may be either CMOS driven or Open Drain. This is selected using the GPn_OD bits.

Internal pull-up or pull-down resistors can be enabled on each pin using the GPn_PULL field. Both resistors are available for use when the associated GPIO is an input. When the GPIO pin is configured as an Open Drain output, the internal pull-up resistor may be required if no external pull-up resistors are present.

A GPIO pin may be tri-stated using the GPn_ENA register field. When GPn_ENA = 0, the respective pin is tri-stated. A tri-stated pin exhibits high impedance to any external circuit and is disconnected from the internal GPIO circuits. The pull-up and pull-down resistors are disabled when a GPIO pin is tri-stated.

GPIO pins can generate an interrupt (see Section 21.4). The GPn_INT_MODE field selects whether the interrupt occurs on a single active edge only, or else on both rising and falling edges. When single edge is selected, the active edge is the rising edge (when GPn_POL = 1) or the falling edge (when GPn_POL = 0).

When GPIO10, GPIO11 or GPIO12 is used as an input to the AUXADC (see Section 18), it is recommended that the respective GPIO(s) are tri-stated (ie. GPn_ENA = 0). The normal GPIO functionality cannot be supported on a GPIO pin that is enabled as an input to the AUXADC.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16440 (4038h)	15	GPn_DIR	1	GPIO n pin direction 0 = Output 1 = Input
to				
R16451 (4043h)	14:13	GPn_PULL [1:0]	01	GPIO n Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved
	12	GPn_INT_M ODE	0	GPIO n Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GPn_POL=1) or falling edge triggered (if GPn_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges
	11	GPn_PWR_D OM	0	GPIO n Power Domain See Table 48.
	10	GPn_POL	1	GPIO n Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)
	9	GPn_OD	0	GPIO n Output pin configuration 0 = CMOS 1 = Open Drain
	7	GPn_ENA	0	GPIO n Enable control 0 = GPIO pin is tri-stated 1 = Normal operation
	3:0	GPn_FN [3:0]	0000	GPIO n Pin Function See Table 49.
<p>Note: n is a number between 1 and 12 that identifies the individual GPIO.</p> <p>Note: The default values noted are valid when the WM8325-00C powers up to the OFF state, or if the Register Map is reset following a Device Reset or Software Reset event. In the case of GPIO pins 1 to 6, these registers are overwritten with the respective OTP memory contents when an ON transition is scheduled. See Section 30.3 for details of the OTP program that is implemented on the WM8325-00C.</p>				

Table 46 GPIO Pin Configuration

When the GPIO output function is selected (GPn_FN = 0h, GPn_DIR = 0), the state of a GPIO output is controlled by writing to the corresponding GPn_LVL register bit, as defined in Table 47.

The logic level of a GPIO input is determined by reading the corresponding GPn_LVL register bit. If GPn_POL is set, then the read value of the GPn_LVL field for a GPIO input is the inverse of the external signal. Note that, when the GPIO input level changes, the logic level of GPn_LVL will only be updated after the maximum de-bounce period, as listed in Table 44. An input pulse that is shorter than the minimum de-bounce period will be filtered by the de-bounce function and will be ignored.

If a GPIO is configured as a CMOS output (ie. GPn_OD = 0), then the read value of the GPn_LVL field will indicate the logic level of that output. If GPn_POL is set, then the read value of the GPn_LVL field for a GPIO output is the inverse of the level on the external pad.

If a GPIO is configured as an Open Drain output, then the read value of GPn_LVL is only valid when the internal pull-up resistor is enabled on the pin (ie. when GPn_PULL = 10). The read value is also affected by the GPn_POL bit, as described above for the CMOS case.

If a GPIO is tri-stated (GPn_ENA = 0), then the read value of the corresponding GPn_LVL field is invalid.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16396 (400Ch) GPIO Level	11	GP12_LVL	0	GPIO _n level. When GP _n _FN = 0h and GP _n _DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP _n _POL is 0, the register contains the opposite logic level to the external pin.
	10	GP11_LVL	0	
	9	GP10_LVL	0	
	8	GP9_LVL	0	
	7	GP8_LVL	0	
	6	GP7_LVL	0	
	5	GP6_LVL	0	
	4	GP5_LVL	0	
	3	GP4_LVL	0	
	2	GP3_LVL	0	
	1	GP2_LVL	0	
	0	GP1_LVL	0	

Table 47 GPIO Level Register

The power domain for each GPIO is controlled using the GP_n_PWR_DOM registers as described in Table 48.

The selected power domain for each GPIO affects the maximum input voltage that can be supported on the respective pin(s). Note that this is also applicable when GPIO10, GPIO11 or GPIO12 are used as inputs to the AUXADC (see Section 18). The input voltage at the GPIO pin must not exceed the voltage of the respective power domain.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16440 (4038h) GPIO1 Control	11	GP1_PWR_DOM	0	GPIO1 Power Domain select 0 = DBVDD 1 = VPMIC (LDO12)
R16441 (4039h) GPIO2 Control	11	GP2_PWR_DOM	0	GPIO2 Power Domain select 0 = DBVDD 1 = VPMIC (LDO12)
R16442 (403Ah) GPIO3 Control	11	GP3_PWR_DOM	0	GPIO3 Power Domain select 0 = DBVDD 1 = VPMIC (LDO12)
R16443 (403Bh) GPIO4 Control	11	GP4_PWR_DOM	0	GPIO4 Power Domain select 0 = DBVDD 1 = PVDD
R16444 (403Ch) GPIO5 Control	11	GP5_PWR_DOM	0	GPIO5 Power Domain select 0 = DBVDD 1 = PVDD
R16445 (403Dh) GPIO6 Control	11	GP6_PWR_DOM	0	GPIO6 Power Domain select 0 = DBVDD 1 = PVDD
R16446 (403Eh) GPIO7 Control	11	GP7_PWR_DOM	0	GPIO7 Power Domain select 0 = DBVDD 1 = VPMIC (LDO12)
R16447 (403Fh) GPIO8 Control	11	GP8_PWR_DOM	0	GPIO8 Power Domain select 0 = DBVDD 1 = VPMIC (LDO12)
R16448 (4040h) GPIO9 Control	11	GP9_PWR_DOM	0	GPIO9 Power Domain select 0 = DBVDD 1 = VPMIC (LDO12)
R16449 (4041h) GPIO10 Control	11	GP10_PWR_DOM	0	GPIO10 Power Domain select 0 = DBVDD 1 = PVDD

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16450 (4042h) GPIO11 Control	11	GP11_PWR_D OM	0	GPIO11 Power Domain select 0 = DBVDD 1 = PVDD
R16451 (4043h) GPIO12 Control	11	GP12_PWR_D OM	0	GPIO12 Power Domain select 0 = DBVDD 1 = PVDD

Table 48 GPIO Power Domain Registers

The function of each GPIO is controlled using the GPn_FN registers defined in Table 49. Note that the selected function also depends on the associated GPn_DIR field described in Table 46.

See also Section 21.2 for additional details of each GPIO function, including the applicable de-bounce times for GPIO input functions.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16440 (4038h) GPIO1 Control	3:0	GP1_FN [3:0]	0000	Input functions: 0h = GPIO input (long de-bounce) 1h = GPIO input 2h = Power On/Off request 3h = Sleep/Wake request 4h = Sleep/Wake request (long de-bounce) 5h = Sleep request 6h = Power On request 7h = Watchdog Reset input 8h = DVS1 input 9h = DVS2 input Ah = HW Enable1 input Bh = HW Enable2 input Ch = HW Control1 input Dh = HW Control2 input Eh = HW Control1 input (long de-bounce) Fh = HW Control2 input (long de-bounce) Output functions: 0h = GPIO output 1h = 32.768kHz oscillator output 2h = ON state 3h = SLEEP state 4h = Power State Change 5h = Reserved 6h = Reserved 7h = Reserved 8h = DC1 DVS Done 9h = DC2 DVS Done Ah = External Power Enable1 Bh = External Power Enable2 Ch = System Supply Good (SYSOK) Dh = Converter Power Good (PWR_GOOD) Eh = External Power Clock (2MHz) Fh = Auxiliary Reset
R16441 (4039h) GPIO2 Control	3:0	GP2_FN [3:0]	0000	
R16442 (403Ah) GPIO3 Control	3:0	GP3_FN [3:0]	0000	
R16443 (403Bh) GPIO4 Control	3:0	GP4_FN [3:0]	0000	
R16444 (403Ch) GPIO5 Control	3:0	GP5_FN [3:0]	0000	
R16445 (403Dh) GPIO6 Control	3:0	GP6_FN [3:0]	0000	
R16446 (403Eh) GPIO7 Control	3:0	GP7_FN [3:0]	0000	
R16447 (403Fh) GPIO8 Control	3:0	GP8_FN [3:0]	0000	
R16448 (4040h) GPIO9 Control	3:0	GP9_FN [3:0]	0000	
R16449 (4041h) GPIO10 Control	3:0	GP10_FN [3:0]	0000	
R16450 (4042h) GPIO11 Control	3:0	GP11_FN [3:0]	0000	
R16451 (4043h) GPIO12 Control	3:0	GP12_FN [3:0]	0000	

Table 49 GPIO Function Select Registers

Note that GPIO input functions 2h, 3h, 4h, 5h and 6h are edge-triggered only. The associated state transition(s) are scheduled only when a rising or falling edge is detected on the respective GPIO pin. At other times, it is possible that other state transition events may cause a state transition regardless of the state of the GPIO input. See Section 11.3 for details of all the state transition events.

21.4 GPIO INTERRUPTS

Each GPIO pin has an associated interrupt flag, GPn_EINT , in Register R16405 (4015h). Each of these secondary interrupts triggers a primary GPIO Interrupt, GP_INT (see Section 23). This can be masked by setting the mask bit(s) as described in Table 50.

See Section 28 and Section 29 for a definition of the register bit positions applicable to each GPIO.

ADDRESS	BIT	LABEL	DESCRIPTION
R16405 (4015h) Interrupt Status 5	15:0	GPn_EINT	GPIO interrupt. (Trigger is controlled by GPn_INT_MODE) Note: Cleared when a '1' is written.
R16413 (401Dh) Interrupt Status 5 Mask	15:0	IM_GPn_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
Note: n is a number between 1 and 12 that identifies the individual GPIO.			

Table 50 GPIO Interrupts

22 SYSTEM STATUS LED DRIVERS

22.1 GENERAL DESCRIPTION

The WM8325-00C provides two System Status LED Drivers. These are digital outputs intended for driving LEDs directly. The LED outputs can be assigned to indicate Power State status. They can also be commanded directly via register control, in order to provide any other required functionality.

22.2 LED DRIVER CONTROL

LED Drivers are configurable in the ON and SLEEP power states only. The functionality of the LED Drivers is controlled by the LEDn_SRC register bits, as described in Table 51.

Note that the LEDn_SRC fields are also programmed on the integrated OTP memory (see Section 14). The default values noted below are valid when the WM8325-00C powers up to the OFF state, or if the Register Map is reset following a Device Reset or Software Reset event. The LEDn_SRC registers are overwritten with the respective OTP memory contents when an ON transition is scheduled. See Section 30.3 for details of the OTP program that is implemented on the WM8325-00C.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16460 (404Ch) Status LED1	15:14	LED1_SRC [1:0]	11	LED1 Source (Selects the LED1 function.) 00 = Off 01 = Power State Status 10 = Reserved 11 = Manual Mode
R16461 (404Dh) Status LED2	15:14	LED2_SRC [1:0]	11	LED2 Source (Selects the LED2 function.) 00 = Off 01 = Power State Status 10 = Reserved 11 = Manual Mode

Table 51 System Status LED Control

22.2.1 POWER STATE STATUS

Setting LEDn_SRC = 01 configures the associated LED to indicate Power State status. Under this selection, four different conditions may be indicated, as defined in Table 52.

LED DRIVER	DESCRIPTION	DRIVE MODE	LED 'ON' TIME	ON:OFF DUTY CYCLE
LED1 or LED2	Power Sequence Failure	Pulsed sequence (4 pulses)	1s	1:1
	PVDD Low	Continuous pulsed	250ms	1:3
	ON state	Constant	n/a	n/a
	SLEEP state	Continuous pulsed	250ms	1:7

Table 52 System Status LED Outputs - Power State Status

If more than one of the conditions listed occurs simultaneously, then the LED output pattern is controlled by the condition in the highest position within the list above.

For example, if the PVDD Low condition occurs while in the ON or SLEEP states, then the LED output follows the pattern defined for the PVDD Low condition.

The PVDD Low indication is asserted if PVDD is less than the user-selectable threshold SYSLO_THR, as described in Section 24.4.

Note that, in the case of Power Sequence Failure, the transition to OFF occurs after the 4 LED pulses have been emitted.

22.2.2 MANUAL MODE

Setting LEDn_SRC = 11 configures the associated LED to operate in Manual Mode, which is configured using additional register fields.

In Manual Mode, the LED output can be commanded as Off, On (Constant), Continuous Pulsed or Pulsed Sequence. The selected operation is determined by the LEDn_MODE registers as described in Table 53.

In Continuous Pulsed mode and Pulsed Sequence mode, the 'On' time and the Duty Cycle can be configured using the LEDn_DUR and LEDn_DUTY_CYC registers respectively.

In Pulsed Sequence mode, the number of pulses in the sequence can be selected using the LEDn_SEQ_LEN register. On completion of the commanded number of pulses, the LED remains off until LEDn_MODE or LEDn_SRC is changed to another value.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16460 (404Ch) Status LED1	9:8	LED1_MODE [1:0]	00	LED1 Mode (Controls LED1 in Manual Mode only.) 00 = Off 01 = Constant 10 = Continuous Pulsed 11 = Pulsed Sequence
	5:4	LED1_SEQ_LEN [1:0]	10	LED1 Pulse Sequence Length (when LED1_MODE = Pulsed Sequence) 00 = 1 pulse 01 = 2 pulses 10 = 4 pulses 11 = 7 pulses
	3:2	LED1_DUR [1:0]	01	LED1 On time (when LED1_MODE = Continuous Pulsed or Pulsed Sequence) 00 = 1 second 01 = 250ms 10 = 125ms 11 = 62.5ms
	1:0	LED1_DUTY_CYC [1:0]	10	LED1 Duty Cycle (On:Off ratio) (when LED1_MODE = Continuous Pulsed or Pulsed Sequence) 00 = 1:1 (50% on) 01 = 1:2 (33.3% on) 10 = 1:3 (25% on) 11 = 1:7 (12.5% on)
R16461 (404Dh) Status LED2	9:8	LED2_MODE [1:0]	00	LED2 Mode (Controls LED2 in Manual Mode only.) 00 = Off 01 = Constant 10 = Continuous Pulsed 11 = Pulsed Sequence
	5:4	LED2_SEQ_LEN	10	LED2 Pulse Sequence Length

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
		N [1:0]		(when LED2_MODE = Pulsed Sequence) 00 = 1 pulse 01 = 2 pulses 10 = 4 pulses 11 = 7 pulses
	3:2	LED2_DUR [1:0]	01	LED2 On time (when LED2_MODE = Continuous Pulsed or Pulsed Sequence) 00 = 1 second 01 = 250ms 10 = 125ms 11 = 62.5ms
	1:0	LED2_DUTY_CYC [1:0]	10	LED2 Duty Cycle (On:Off ratio) (when LED2_MODE = Continuous Pulsed or Pulsed Sequence) 00 = 1:1 (50% on) 01 = 1:2 (33.3% on) 10 = 1:3 (25% on) 11 = 1:7 (12.5% on)

Table 53 System Status LED Outputs - Manual Mode Control

22.3 LED DRIVER CONNECTIONS

The recommended connection for System Status LEDs is illustrated in Figure 22. The LED outputs are referenced to the PVDD power domain. A series resistor may be required, depending on the LED characteristics and the PVDD voltage.

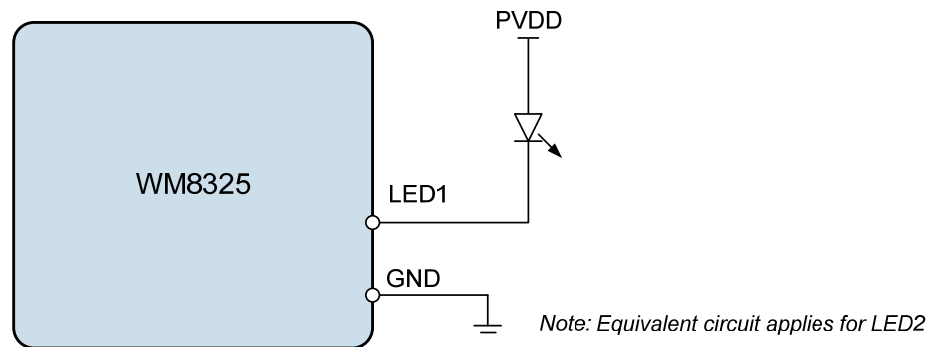


Figure 22 System Status LED Connections

23 INTERRUPT CONTROLLER

The WM8325-00C has a comprehensive Interrupt logic capability. The dedicated $\overline{\text{IRQ}}$ pin can be used to alert a host processor to selected events or fault conditions. Each of the interrupt conditions can be individually enabled or masked. Following an interrupt event, the host processor should read the interrupt registers in order to determine what caused the interrupt, and take appropriate action if required.

The WM8325-00C interrupt controller has two levels:

Secondary interrupts indicate a single event in one of the circuit blocks. The event is indicated by setting a register bit. This bit is a latching bit - once it is set, it remains at logic 1 even if the trigger condition is cleared. The secondary interrupts are cleared by writing a logic 1 to the relevant register bit. Note that reading the register does not clear the secondary interrupt.

Primary interrupts are the logical OR of the associated secondary interrupts (usually all the interrupts associated with one particular circuit block). Each of the secondary interrupts can be individually masked or enabled as an input to the corresponding primary interrupt. The primary interrupt register R16400 (4010h) is read-only.

The status of the $\overline{\text{IRQ}}$ pin reflects the logical NOR of the primary interrupts. A logic 0 indicates that one or more of the primary interrupts is asserted. Each of the primary interrupts can be individually masked or enabled as an input to the $\overline{\text{IRQ}}$ pin output.

The $\overline{\text{IRQ}}$ pin output can either be CMOS driven or Open Drain (integrated pull-up) configuration, as determined by the IRQ_OD register bit. When the $\overline{\text{IRQ}}$ pin is Open Drain, it is actively driven low when asserted; the pull-up causes a logic high output when not asserted. The Open Drain configuration enables multiple devices to share a common Interrupt line with the host processor.

The $\overline{\text{IRQ}}$ pin output can be masked by setting the IM_IRQ register bit. When the $\overline{\text{IRQ}}$ pin is masked, it is held in the logic 1 (or Open Drain) state regardless of any internal interrupt event.

Note that the secondary interrupt bits are always valid - they are set as normal, regardless of whether the bit is enabled or masked as an input to the corresponding primary interrupt. The primary interrupt bits are set and cleared as normal in response to any unmasked secondary interrupt, regardless of whether the primary interrupt bit is enabled or masked as an input to the $\overline{\text{IRQ}}$ pin output.

Note also that if any internal condition is configured to trigger an event other than an Interrupt (eg. the Watchdog timer triggers Reset), these events are always actioned, regardless of the state of any interrupt mask bits.

The $\overline{\text{IRQ}}$ pin output is configured using the register bits described in Table 54.

ADDRESS	BIT	LABEL	DESCRIPTION
R16407 (4017h) IRQ Config	1	IRQ_OD	IRQ pin configuration 0 = CMOS 1 = Open Drain (integrated pull-up)
	0	IM_IRQ	IRQ pin output mask 0 = Normal 1 = IRQ output is masked

Table 54 IRQ Pin Configuration

The interrupt logic is illustrated in Figure 23.

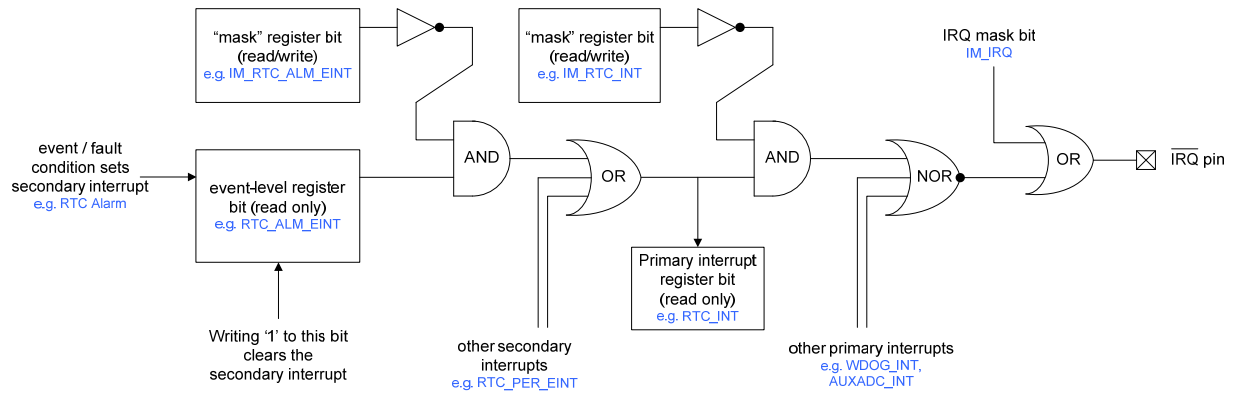


Figure 23 Interrupt Logic

Following the assertion of the \overline{IRQ} pin to indicate an Interrupt event, the host processor can determine which primary interrupt caused the event by reading the primary interrupt register R16400 (4010h). This register is defined in Section 23.1.

After reading the primary interrupt register, the host processor must read the corresponding secondary interrupt register(s) in order to determine which specific event caused the \overline{IRQ} pin to be asserted. The host processor clears the secondary interrupt bit by writing a logic 1 to that bit.

23.1 PRIMARY INTERRUPTS

The primary interrupts are defined in Table 55. These bits are Read Only. They are set when any of the associated unmasked secondary interrupts is set. They can only be reset when all of the associated secondary resets are cleared or masked.

Each primary interrupt can be masked. When a mask bit is set, the corresponding primary interrupt is masked and does not cause the \overline{IRQ} pin to be asserted. The primary interrupt bits in R16408 (4018h) are valid regardless of whether the mask bit is set. The primary interrupts are all masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16400 (4010h) System Interrupts	15	PS_INT	Power State primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	14	TEMP_INT	Thermal primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	13	GP_INT	GPIO primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	12	ON_PIN_INT	ON Pin primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	11	WDOG_INT	Watchdog primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	8	AUXADC_INT	AUXADC primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	7	PPM_INT	Power Path Management primary interrupt

ADDRESS	BIT	LABEL	DESCRIPTION
			0 = No interrupt 1 = Interrupt is asserted
	5	RTC_INT	Real Time Clock and Crystal Oscillator primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	1	HC_INT	High Current primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	0	UV_INT	Undervoltage primary interrupt 0 = No interrupt 1 = Interrupt is asserted
R16408 (4018h) System Interrupts Mask	15	IM_PS_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	14	IM_TEMP_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	13	IM_GP_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	12	IM_ON_PIN_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	11	IM_WDOG_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	8	IM_AUXADC_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	7	IM_PPM_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	5	IM_RTC_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	1	IM_HC_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	0	IM_UV_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 55 Primary Interrupt Status and Mask Bits

23.2 SECONDARY INTERRUPTS

The following sections define the secondary interrupt status and control bits associated with each of the primary interrupt bits defined in Table 55.

23.2.1 POWER STATE INTERRUPT

The primary PS_INT interrupt comprises three secondary interrupts as described in Section 11.4. The secondary interrupt bits are defined in Table 56.

Each of the secondary interrupts can be masked. When a mask bit is set, the corresponding interrupt event is masked and does not trigger a PS_INT interrupt. The secondary interrupt bits in R16402 (4012h) are valid regardless of whether the mask bit is set. The secondary interrupts are all masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16402 (4012h) Interrupt Status 2	2	PS_POR_EINT	Power On Reset interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
	1	PS_SLEEP_OFF_EINT	SLEEP or OFF interrupt (Power state transition to SLEEP or OFF states) (Rising Edge triggered) Note: Cleared when a '1' is written.
	0	PS_ON_WAKE_EINT	ON or WAKE interrupt (Power state transition to ON state) (Rising Edge triggered) Note: Cleared when a '1' is written.
R16410 (401Ah) Interrupt Status 2 Mask	2	IM_PS_POR_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	1	IM_PS_SLEEP_OFF_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	0	IM_PS_ON_WAKE_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 56 Power State Interrupts

23.2.2 THERMAL INTERRUPTS

The primary TEMP_INT interrupt comprises a single secondary interrupt as described in Section 26. The secondary interrupt bit is defined in Table 57.

The secondary interrupt can be masked. When the mask bit is set, the corresponding interrupt event is masked and does not trigger a TEMP_INT interrupt. The secondary interrupt bit in R16401 (4011h) is valid regardless of whether the mask bit is set. The secondary interrupt is masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	1	TEMP_THW_CINT	Thermal Warning interrupt (Rising and Falling Edge triggered) Note: Cleared when a '1' is written.
R16410 (4019h) Interrupt Status 1 Mask	1	IM_TEMP_THW_CINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 57 Thermal Interrupts

23.2.3 GPIO INTERRUPTS

The primary GP_INT interrupt comprises sixteen secondary interrupts as described in Section 21.4. The secondary interrupt bits are defined in Table 58.

Each of the secondary interrupts can be masked. When a mask bit is set, the corresponding interrupt event is masked and does not trigger a GP_INT interrupt. The secondary interrupt bits in R16405 (4015h) are valid regardless of whether the mask bit is set. The secondary interrupts are all masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16405 (4015h) Interrupt Status 5	15:0	GP _n _EINT	GPIO interrupt. (Trigger is controlled by GP _n _INT_MODE) Note: Cleared when a '1' is written.
R16413 (401Dh) Interrupt Status 5 Mask	15:0	IM_GP _n _EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Note: *n* is a number between 1 and 12 that identifies the individual GPIO.

Table 58 GPIO Interrupts

23.2.4 ON PIN INTERRUPTS

The primary ON_PIN_INT interrupt comprises a single secondary interrupt as described in Section 11.6. The secondary interrupt bit is defined in Table 59.

The secondary interrupt can be masked. When the mask bit is set, the corresponding interrupt event is masked and does not trigger an ON_PIN_INT interrupt. The secondary interrupt bit in R16401 (4011h) is valid regardless of whether the mask bit is set. The secondary interrupt is masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	12	ON_PIN_CINT	ON pin interrupt. (Rising and Falling Edge triggered) Note: Cleared when a '1' is written.
R16409 (4019h) Interrupt Status 1 Mask	12	IM_ON_PIN_CINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 59 ON Pin Interrupt

23.2.5 WATCHDOG INTERRUPTS

The primary WDOG_INT interrupt comprises a single secondary interrupt as described in Section 25. The secondary interrupt bit is defined in Table 60.

The secondary interrupt can be masked. When the mask bit is set, the corresponding interrupt event is masked and does not trigger a WDOG_INT interrupt. The secondary interrupt bit in R16401 (4011h) is valid regardless of whether the mask bit is set. The secondary interrupt is masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	11	WDOG_TO_EINT	Watchdog timeout interrupt. (Rising Edge triggered) Note: Cleared when a '1' is written.
R16409 (4019h) Interrupt Status 1 Mask	11	IM_WDOG_TO_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 60 Watchdog Timer Interrupts

23.2.6 AUXADC INTERRUPTS

The primary AUXADC_INT interrupt comprises five secondary interrupts as described in Section 18.5. The secondary interrupt bits are defined in Table 61.

Each of the secondary interrupts can be masked. When a mask bit is set, the corresponding interrupt event is masked and does not trigger a AUXADC_INT interrupt. The secondary interrupt bits in R16401 (4011h) are valid regardless of whether the mask bit is set. The secondary interrupts are all masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	8	AUXADC_DATA_EINT	AUXADC Data Ready interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
	7:4	AUXADC_DCOMP n _EINT	AUXADC Digital Comparator n interrupt (Trigger is controlled by DCMP n _GT) Note: Cleared when a '1' is written.
R16409 (4019h) Interrupt Status 1 Mask	8	IM_AUXADC_DATA_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	7:4	IM_AUXADC_DCOMP n _EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Note: n is a number between 1 and 4 that identifies the individual Comparator.

Table 61 AUXADC Interrupts

23.2.7 POWER PATH MANAGEMENT INTERRUPTS

The primary PPM_INT interrupt comprises a single secondary interrupt as described in Section 17.2. The secondary interrupt bit is defined in Table 62.

The secondary interrupt can be masked. When the mask bit is set, the corresponding interrupt event is masked and does not trigger a PPM_INT interrupt. The secondary interrupt bit in R16401 (4011h) are valid regardless of whether the mask bit is set. The secondary interrupt is masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	15	PPM_SYSLO_EINT	Power Path SYSLO interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
R16409 (4019h) Interrupt Status 1 Mask	15	IM_PPM_SYSLO_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 62 Power Path Management Interrupts

23.2.8 REAL TIME CLOCK AND CRYSTAL OSCILLATOR INTERRUPTS

The primary RTC_INT interrupt comprises four secondary interrupts as described in Section 20.3. The secondary interrupt bits are defined in Table 63.

Each of the secondary interrupts can be masked except for XTAL_TAMPER_EINT, which cannot be masked. When a mask bit is set, the corresponding interrupt event is masked and does not trigger a RTC_INT interrupt. The secondary interrupt bits in R16401 (4011h) and R16404 (4014h) are valid regardless of whether the mask bit is set.

The secondary interrupts are all masked by default, except for XTAL_TAMPER_EINT, which cannot be masked.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	3	RTC_PER_EINT	RTC Periodic interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
	2	RTC_ALM_EINT	RTC Alarm interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
R16404 (4014h) Interrupt Status 4	7	XTAL_START_EINT	Crystal Oscillator Start Failure interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
	6	XTAL_TAMPER_EINT	Crystal Oscillator Tamper interrupt (Rising and Falling Edge triggered) Note: Cleared when a '1' is written.
R16409 (4019h) Interrupt Status 1 Mask	3	IM_RTC_PER_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	2	IM_RTC_ALM_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
R16412 (401Ch) Interrupt Status 4 Mask	7	IM_XTAL_START_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 63 Real Time Clock (RTC) and Crystal Oscillator (XTAL) Interrupts

23.2.9 HIGH CURRENT INTERRUPTS

The primary HC_INT interrupt comprises two secondary interrupts as described in Section 15.12. The secondary interrupt bits are defined in Table 64.

Each of the secondary interrupts can be masked. When a mask bit is set, the corresponding interrupt event is masked and does not trigger a HC_INT interrupt. The secondary interrupt bits in R16404 (4014h) are valid regardless of whether the mask bit is set. The secondary interrupts are all masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16404 (4014h) Interrupt Status 4	9	HC_DC2_EINT	DC-DC2 High Current interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
	8	HC_DC1_EINT	DC-DC1 High Current interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
R16412 (401Ch) Interrupt Status 4 Mask	9	IM_HC_DC2_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	8	IM_HC_DC1_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 64 Overcurrent Interrupts

23.2.10 UNDERVOLTAGE INTERRUPTS

The primary UV_INT interrupt comprises fourteen secondary interrupts as described in Section 15.12). The secondary interrupt bits are defined in Table 65.

Each of the secondary interrupts can be masked. When a mask bit is set, the corresponding interrupt event is masked and does not trigger a UV_INT interrupt. The secondary interrupt bits in R16403 (4013h) and R16404 (4014h) are valid regardless of whether the mask bit is set. The secondary interrupts are all masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16403 (4013h) Interrupt Status 3	9:0	UV_LDO _n _EINT	LDO _n Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
R16404 (4014h) Interrupt Status 4	3:0	UV_DC _m _EINT	DC-DC _m Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
R16411 (401Bh) Interrupt Status 3 Mask	9:0	IM_UV_LDO _n _EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
R16412 (401Ch) Interrupt Status 4 Mask	3:0	IM_UV_DC _m _EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
Notes:			
1. <i>n</i> is a number between 1 and 10 that identifies the individual LDO Regulator (LDO1-LDO10).			
2. <i>m</i> is a number between 1 and 4 that identifies the individual DC-DC Converter (DC1-DC4).			

Table 65 Undervoltage Interrupts

24 RESETS AND SUPPLY VOLTAGE MONITORING

24.1 RESETS

The WM8325-00C provides hardware and software monitoring functions as inputs to a Reset management system. These functions enable the device to take appropriate action when power supplies are critically low or if a hardware or software fault condition is detected.

There are different levels of Resets, providing different response mechanisms according to the condition that caused the Reset event. Where applicable, the WM8325-00C will automatically return to the ON state and resume normal operation as quickly as possible following a Reset.

A System Reset occurs in the event of a Power Sequence Failure, Device overtemperature, PVDD undervoltage, Software 'OFF' request or VPMIC (LDO12) undervoltage condition. Under these conditions, the WM8325-00C asserts the $\overline{\text{RESET}}$ pin and transitions to the OFF state. In the case of VPMIC undervoltage, the WM8325-00C enters the BACKUP state. The contents of the Register map are not reset under System Reset conditions.

A Device Reset occurs in the event of a Watchdog Timeout, Hardware Reset request or Converter (LDO or DC-DC) Undervoltage condition. Under these conditions, the WM8325-00C asserts the $\overline{\text{RESET}}$ pin and transitions to the OFF state. The contents of the Register map are cleared to default values, except for the RTC and software scratch registers, which are maintained. The WM8325-00C will automatically return to the ON state after performing the Device Reset.

A Software Reset occurs when any value is written to Register 0000h, as described in Section 12.5. In this event, the WM8325-00C asserts the $\overline{\text{RESET}}$ pin and transitions to the OFF state. The Register map contents may or may not be affected, depending on the value of the SW_RESET_CFG field. See Section 24.3 for further details of Software Reset configuration. The WM8325-00C will automatically return to the ON state after performing the Software Reset.

A Power-On Reset occurs when the supply voltage is less than the Power-On Reset threshold, as described in Section 24.4. In this event, the WM8325-00C is forced into the NO POWER state, as described in Section 11.2. All the contents of the Register map are lost in the NO POWER state.

A summary of the WM8325-00C Resets is contained in Table 66 .

RESET TYPE	RESET CONDITION	DESCRIPTION	RESPONSE	AUTOMATIC RECOVERY
System Reset	Power Sequence Failure	DC Converters, LDOs or CLKOUT circuits have failed to start up within the permitted time. See Section 11.3.	Assert $\overline{\text{RESET}}$ pin. Select OFF state.	No
	Device overtemperature	An overtemperature condition has been detected. See Section 26.	If the Reset Condition is VPMIC (LDO12) undervoltage, then the WM8325-00C enters the BACKUP state.	No
	PVDD undervoltage (1)	PVDD is less than the user-selectable threshold SYSLO_THR and SYSLO_ERR_ACT is configured to select OFF in this condition. See Section 24.4.		No
	PVDD undervoltage (2)	PVDD is less than the SHUTDOWN voltage. See Section 24.4.		No
	Software OFF request	OFF has been commanded by writing CHIP_ON = 0. See Section 11.3		No
	VPMIC (LDO12) undervoltage	The WM8325-00C supply voltage is less than the System Reset threshold. See Section 24.4.		No
Device Reset	Watchdog timeout	Watchdog timer has expired and the selected response is to generate a Device Reset. See Section 25.	Assert $\overline{\text{RESET}}$ pin. Shutdown and restart the WM8325-00C. Reset Register map (Note the RTC and software scratch registers are not reset.)	Yes
	Hardware Reset	The $\overline{\text{RESET}}$ pin has been pulled low by an external source. See Section 24.2.		Yes
	Converter (LDO or DC-DC) Undervoltage	An undervoltage condition has been detected and the selected response is "Shut down system (Device Reset)" See Section 15.		Yes
Software Reset	Software Reset	Software Reset has been commanded by writing to Register 0000h. See Section 12.5.	Assert $\overline{\text{RESET}}$ pin. Shutdown and restart the WM8325-00C. See Section 24.3 for configurable options regarding the Register Map contents.	Yes
Power On Reset	Power On Reset	The WM8325-00C supply voltage is less than the Power-On Reset (POR) threshold. See Section 24.4.	The WM8325-00C is in the NO POWER state. All register contents are lost.	No

Table 66 Resets Summary

In the cases where Automatic Recovery is supported (as noted in Table 66), the WM8325-00C will re-start the WM8325-00C following the Reset, and return the device to the ON state. The particular Reset condition which caused the return to the ON state will be indicated in the "ON Source" register - see Section 11.3.

Note that, if a Watchdog timeout or Converter undervoltage fault persists, a maximum of 6 Device Resets will be attempted to initiate the start-up sequence. Similarly, a maximum of 6 Software Resets is permitted. If these limits are exceeded, the WM8325-00C will remain in the OFF state until the next valid ON state transition event occurs.

The WM8325-00C asserts the $\overline{\text{RESET}}$ low as soon as the device begins the shutdown sequence. $\overline{\text{RESET}}$ is held low for the duration of the shutdown sequence and is held low in the OFF state. In the cases where Automatic Recovery is supported, $\overline{\text{RESET}}$ is automatically cleared (high) after successful completion of the startup sequence. The duration of the $\overline{\text{RESET}}$ low period after the

startup sequence has completed is governed by the RST_DUR register field described in Section 11.7.

24.2 HARDWARE RESET

A Hardware Reset is triggered when an external source pulls the $\overline{\text{RESET}}$ pin low. Under this condition, the WM8325-00C transitions to the OFF state. The contents of the Register map are cleared to default values, except for the RTC and software scratch registers, which are maintained. The WM8325-00C will then automatically schedule an ON state transition to resume normal operation.

If the external source continues to pull the $\overline{\text{RESET}}$ pin low, then the WM8325-00C cannot fully complete the ON state transition following the Hardware Reset. In this case, the WM8325-00C will mask the external reset for up to 32 seconds. If the $\overline{\text{RESET}}$ pin is released (ie. it returns to logic '1') during this time, then the ON state transition is completed and the Hardware Reset input is valid again from this point. If the $\overline{\text{RESET}}$ pin is not released, then the WM8325-00C will force an OFF condition on expiry of the 32 seconds timeout. Recovery from this forced OFF condition cannot occur until the external reset condition is de-asserted, followed by a valid ON event. If an ON event occurs before the external reset is de-asserted, then start-up will be attempted, but the transition will be unsuccessful, causing a return to the OFF state.

It is possible to mask the $\overline{\text{RESET}}$ pin input in the SLEEP state by setting the RST_SLP_MSK register bit as described in Section 11.7.

24.3 SOFTWARE RESET

A Software Reset is triggered by writing to Register 0000h, as described in Section 12.5. In this event, the WM8325-00C asserts the $\overline{\text{RESET}}$ pin and transitions to the OFF state. If the Reset occurred in the ON state, then the WM8325-00C will automatically return to the ON state following the Reset.

The SWRST_DLY register field determines whether a time delay is applied between the Software Reset command and the resultant shutdown and start-up sequences. When the SWRST_DLY bit is set, the programmable time delay PWRSTATE_DLY is applied before commencing the shutdown sequence.

The timing of the Software Reset is illustrated in Figure 24. See Section 11.3 for a definition of the PWRSTATE_DLY register.

The SW_RESET_CFG register field determines if the Register Map is reset under a Software Reset condition.

Note that the SW_RESET_CFG control register is locked by the WM8325-00C User Key. This register can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16387 (4003h) Power State	9	SWRST_DLY	0	Software Reset Delay 0 = No delay 1 = Software Reset is delayed by PWRSTATE_DLY following the Software Reset command
R16390 (4006h) Reset Control	10	SW_RESET_CFG	1	Software Reset Configuration. Selects whether the register map is reset to default values when Software Reset occurs. 0 = All registers except RTC and Software Scratch registers are reset by Software Reset 1 = Register Map is not affected by Software Reset <i>Protected by user key</i>

Table 67 Software Reset Configuration

The timing details of the Software Reset are illustrated in Figure 24.

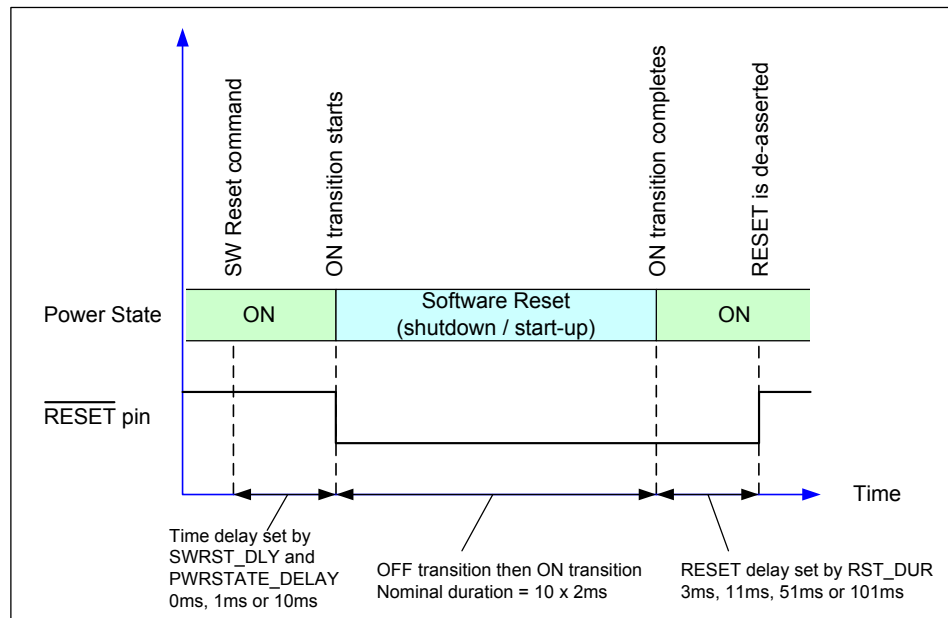


Figure 24 Software Reset Timing

24.4 SUPPLY VOLTAGE MONITORING

The WM8325-00C includes a number of mechanisms to prevent the system from starting up, or to force it to shut down, when the power sources are critically low.

The internal regulator LDO12 is powered from an internal domain equivalent to PVDD and generates an internal supply (VPMIC) to support various “always-on” functions. In the absence of the PVDD supply, LDO12 can be powered from a backup battery. (Note that PVDD is not maintained by the backup battery.) The VPMIC monitoring function controls the Power-On Reset circuit, which sets the threshold below which the WM8325-00C cannot operate.

The operation of the VPMIC monitoring circuit is illustrated in Figure 25. The internal signal $\overline{\text{PORRST}}$ is governed by the V_{POR} thresholds. These determine when the WM8325-00C is kept in the NO POWER state. The internal signal $\overline{\text{PMICRST}}$ is governed by the V_{RES} thresholds. These determine when the WM8325-00C is kept in the BACKUP state.

The VPMIC monitoring thresholds illustrated in Figure 25 are fixed. The voltage levels are defined in the Electrical Characteristics - see Section 7.3.

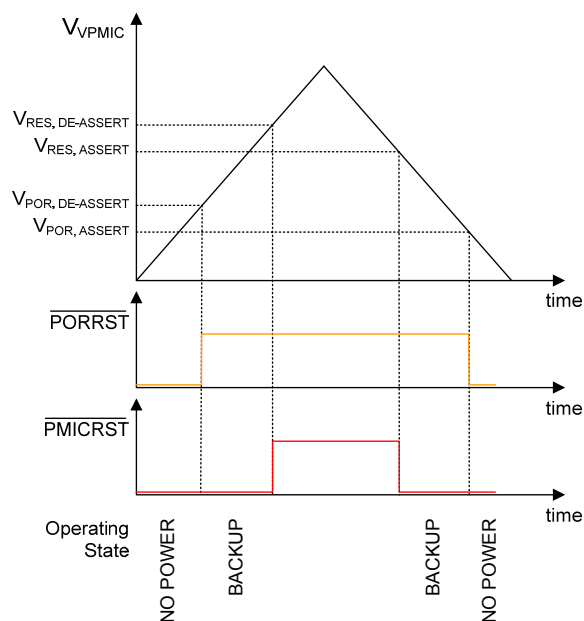


Figure 25 VPMIC Monitoring

The operation of the PVDD monitoring circuit is illustrated in Figure 26. The V_{SHUTDOWN} threshold is the voltage below which the WM8325-00C forces an OFF transition. This threshold voltage is fixed and is defined in the Electrical Characteristics - see Section 7.3.

The V_{SYSOK} threshold is the level at which the internal signal SYSOK is asserted. Any ON request will be inhibited if SYSOK is not set. The V_{SYSOK} threshold can be set using the SYSOK_THR register field in accordance with the minimum voltage requirements of the application. Note that a hysteresis margin is added to the SYSOK_THR setting; see Section 7.3 for details.

The V_{SYSLO} threshold is the level at which the internal signal SYSLO is asserted. This indicates a PVDD undervoltage condition, at which a selectable response can be initiated. The V_{SYSLO} threshold can be set using the SYSLO_THR register field. The action taken under this undervoltage condition is selected using the SYSLO_ERR_ACT register field, as defined in Table 68. An Interrupt event is associated with the SYSLO condition - see Section 17.2.

The SYSLO status can be read from the SYSLO_STS register bit. This bit is asserted when PVDD is below the SYSLO threshold.

The WM8325-00C can also indicate the status of the SYSOK signal via a GPIO pin configured as a "PVDD Good" output (see Section 21). A GPIO pin configured as "PVDD Good" output will be asserted when the PVDD is above the SYSOK threshold.

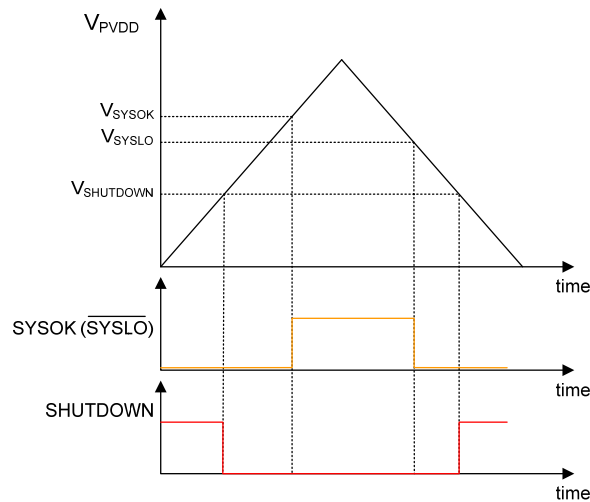


Figure 26 PVDD Monitoring

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16385 (4001h) PVDD Control	15:14	SYSLO_ERR_ACT	00	SYSLO Error Action Selects the action taken when SYSLO is asserted 00 = Interrupt 01 = WAKE transition 10 = Reserved 11 = OFF transition
	11	SYSLO_STS	0	SYSLO Status 0 = Normal 1 = PVDD is below SYSLO threshold
	6:4	SYSLO_THR [2:0]	010	SYSLO threshold (falling PVDD) This is the falling PVDD voltage at which SYSLO will be asserted 000 = 2.8V 001 = 2.9V ... 111 = 3.5V
	2:0	SYSOK_THR [2:0]	101	SYSOK threshold (rising PVDD) This is the rising PVDD voltage at which SYSOK will be asserted 000 = 2.8V 001 = 2.9V ... 111 = 3.5V Note that the SYSOK hysteresis margin is added to these threshold levels.

Table 68 PVDD Monitoring Control

Note that the SYSOK_THR field is also programmed on the integrated OTP memory (see Section 14). The default value noted is valid when the WM8325-00C powers up to the OFF state, or if the Register Map is reset following a Device Reset or Software Reset event. The SYSOK_THR register is overwritten with the respective OTP memory contents when an ON transition is scheduled. See Section 30.3 for details of the OTP program that is implemented on the WM8325-00C.

25 WATCHDOG TIMER

The WM8325-00C includes a Watchdog Timer designed to detect a possible software fault condition where the host processor has locked up. The Watchdog Timer is a free-running counter driven by the internal RC oscillator.

The Watchdog Timer is enabled by default; it can be enabled or disabled by writing to the WDOG_ENA register bit. The Watchdog behaviour in SLEEP is configurable; it can either be set to continue as normal or to be disabled. The Watchdog behaviour in SLEEP is determined by the WDOG_SLPENA bit.

The watchdog timer duration is set using WDOG_TO. The watchdog timer can be halted for debug purposes using the WDOG_DEBUG bit.

The Watchdog reset source is selectable between Software and Hardware triggers. (Note that the de-selected reset source has no effect.) If the Watchdog is not reset within a programmable timeout period, this is interpreted by the WM8325-00C as a fault condition. The Watchdog Timer then either triggers a Device Reset, or issues a WAKE request or raises an Interrupt. This primary action is determined by the WDOG_PRIMACT register field.

If the Watchdog is not reset within a further timeout period of the Watchdog counter, a secondary action is triggered. The secondary action taken at this point is determined by the WDOG_SECACT register field.

The Watchdog reset source is selected using the WDOG_RST_SRC register bit. When Software WDOG reset source is selected, the Watchdog is reset by writing a '1' to the WDOG_RESET field. When Hardware WDOG reset source is selected, the Watchdog is reset by toggling a GPIO pin that has been configured as a Watchdog Reset Input (see Section 21).

If a Device Reset is triggered by the watchdog timeout, the WM8325-00C asserts the $\overline{\text{RESET}}$ pin, resets the internal control registers (excluding the RTC) and initiates a start-up sequence. Note that, following a Device Reset, the action taken on subsequent timeout of the Watchdog Timer will be determined by the WDOG_PRIMACT register. If the watchdog timeout fault persists, then a maximum of 6 Device Reset attempts will be made. See Section 24. If the watchdog timeout occurs more than 6 times, the WM8325-00C will remain in the OFF state until the next valid ON state transition event occurs.

Note that the Watchdog control registers are locked by the WM8325-00C User Key. These registers can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

Note that the WDOG_ENA field is also programmed on the integrated OTP memory (see Section 14). The default setting noted below is valid when the WM8325-00C powers up to the OFF state, or if the Register Map is reset following a Device Reset or Software Reset event. The WDOG_ENA register is overwritten with the respective OTP memory contents when an ON transition is scheduled. See Section 30.3 for details of the OTP program that is implemented on the WM8325-00C.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16388 (4004h) Watchdog	15	WDOG_ENA	1	Watchdog Timer Enable 0 = Disabled 1 = Enabled (enables the watchdog; does not reset it) <i>Protected by user key</i>
	14	WDOG_DEBU G	0	Watchdog Pause 0 = Disabled 1 = Enabled (halts the Watchdog timer for system debugging) <i>Protected by user key</i>
	13	WDOG_RST_S RC	1	Watchdog Reset Source 0 = Hardware only 1 = Software only <i>Protected by user key</i>
	12	WDOG_SLPE NA	0	Watchdog SLEEP Enable 0 = Disabled

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				1 = Controlled by WDOG_ENA <i>Protected by user key</i>
	11	WDOG_RESE T	0	Watchdog Software Reset 0 = Normal 1 = Watchdog Reset (resets the watchdog, if WDOG_RST_SRC = 1) <i>Protected by user key</i>
	9:8	WDOG_SECA CT	10	Secondary action of Watchdog timeout (taken after 2 timeout periods) 00 = No action 01 = Interrupt 10 = Device Reset 11 = WAKE transition <i>Protected by user key</i>
	5:4	WDOG_PRIMA CT	01	Primary action of Watchdog timeout 00 = No action 01 = Interrupt 10 = Device Reset 11 = WAKE transition <i>Protected by user key</i>
	2:0	WDOG_TO [2:0]	111	Watchdog timeout period 000 = 0.256s 001 = 0.512s 010 = 1.024s 011 = 2.048s 100 = 4.096s 101 = 8.192s 110 = 16.384s 111 = 32.768s <i>Protected by user key</i>

Table 69 Controlling the Watchdog Timer

The Watchdog timeout interrupt event is indicated by the WDOG_TO_EINT register field. This secondary interrupt triggers a primary Watchdog Interrupt, WDOG_INT (see Section 23). This can be masked by setting the mask bit as described in Table 70.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	11	WDOG_TO_EINT	Watchdog timeout interrupt. (Rising Edge triggered) Note: Cleared when a '1' is written.
R16409 (4019h) Interrupt Status 1 Mask	11	IM_WDOG_TO_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 70 Watchdog Timer Interrupts

26 TEMPERATURE SENSING

The WM8325-00C provides temperature monitoring as status information and also for self-protection of the device. Temperature monitoring is always enabled in the ON and SLEEP states.

The thermal warning temperature can be set using the THW_TEMP register field. The thermal warning hysteresis ensures that the THW_TEMP is not reset until the device temperature has dropped below the threshold by a suitable margin. The extent of the hysteresis can be selected using the THW_HYST register field.

The Thermal Warning condition can be read using the THW_STS register bit. An overtemperature condition causes the thermal warning interrupt (TEMP_THW_CINT) to be set. The thermal warning interrupt is also set when the overtemperature condition clears, ie. when the device has returned to its normal operating limits.

The thermal shutdown temperature is set at a fixed level. If a thermal shutdown condition is detected whilst in the ON or SLEEP states, then a System Reset is triggered, as described in Section 24.1, forcing a transition to the OFF state.

The temperature sensing circuit is configured and monitored using the register fields described in Table 71.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16386 (4002h)	3	THW_HYST	1	Thermal Warning hysteresis 0 = 8 degrees C 1 = 16 degrees C
	1:0	THW_TEMP [1:0]	10	Thermal Warning temperature 00 = 90 degrees C 01 = 100 degrees C 10 = 110 degrees C 11 = 120 degrees C
R16397 (400Dh)	15	THW_STS	0	Thermal Warning status 0 = Normal 1 = Overtemperature Warning (warning temperature is set by THW_TEMP)

Table 71 Temperature Sensing Control

The thermal warning interrupt event is indicated by the TEMP_THW_CINT register field. This secondary interrupt triggers a primary Thermal Interrupt, TEMP_INT (see Section 23). This can be masked by setting the mask bit as described in Table 72.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	1	TEMP_THW_CINT	Thermal Warning interrupt (Rising and Falling Edge triggered) Note: Cleared when a '1' is written.
R16410 (4019h) Interrupt Status 1 Mask	1	IM_TEMP_THW_CINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 72 Thermal Interrupts

27 VOLTAGE AND CURRENT REFERENCES

27.1 VOLTAGE REFERENCE (VREF)

The main voltage reference generated by the WM8325-00C is bonded to the VREFC pin. The accuracy of this reference is optimised by factory-set trim registers.

The voltage reference (VREF) requires an external decoupling capacitor; a 100nF X5R capacitor is recommended, as noted in Section 30.4. Omitting this capacitor will result in increased noise on the voltage reference; this will particularly affect the analogue LDOs.

The voltage reference circuit includes a low-power mode, which enables power consumption to be minimised where appropriate. The low-power reference mode may lead to increased noise on the voltage reference; this mode should only be selected when minimum power consumption is more important than voltage stability. Note that the Low Power Reference mode is not supported when the Auxiliary ADC function is enabled.

The Low Power Reference mode is enabled when REF_LP register is set. The Low Power Reference mode should only be enabled when the Auxiliary ADC is disabled. Enabling the Low Power Reference mode will lead to a malfunction of the Auxiliary ADC function.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16387 (4003h)	12	REF_LP	0	Low Power Voltage Reference Control 0 = Normal 1 = Low Power Reference Mode select Note that Low Power Reference Mode is only supported when the Auxiliary ADC is disabled.

Table 73 Low Power Voltage Reference Control

27.2 CURRENT REFERENCE (IREF)

The Power Management circuits of the WM8325-00C use an integrated current reference.

This current reference (IREF) requires the connection of an external resistor to the IREFR pin; a 100k Ω (1%) resistor is recommended, as noted in Section 30.4. The WM8325-00C will malfunction if this resistor is omitted.

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bin Default				
0	0000	Reset ID	CHIP_ID[15:0]																0000_0000_0000_0000				
1	0001	Revision	PARENT_REV[7:0]								CHILD_REV[7:0]								0000_0000_0000_0000				
2	0002	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000				
3	0003	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000				
4	0004	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000				
5	0005	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000				
6	0006	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000				
7	0007	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000				
16384	4000	Parent ID	PARENT_ID[15:0]																0110_0010_0100_0110				
16385	4001	PVDD Control	SYSLO_ERR_ACT[1:0]				0	0	SYSLO_STS		0	0	0	0	SYSLO_THR[2:0]			0	SYSOK_THR[2:0]			0000_0000_0010_0101	
16386	4002	Thermal Monitoring	0	0	0	0	0	0	0	0	0	0	0	0	0	THW_HYST	0	THW_TEMP[1:0]			0000_0000_0000_1010		
16387	4003	Power State	CHIP_ON	CHIP_SLP	0	REF_LP	PWRSTATE_DLY[1:0]			SWRST_DLY	0	0	0	0	0	0	0	0	0	0	0	0	U000_1000_0000_0000
16388	4004	Watchdog	WDOG_ENA	WDOG_DEBUG	WDOG_RST_SRC	WDOG_SLP_ENA	WDOG_RES_ENA	0	WDOG_SECACT[1:0]			0	0	WDOG_FRMACT[1:0]			0	WDOG_TO[2:0]			1010_F010_0001_0111		
16389	4005	ON Pn Control	0	0	0	0	0	0	0	ON_PIN_SECACT[1:0]			0	0	ON_PIN_FRMACT[1:0]			ON_PIN_STS	0	ON_PIN_TO[1:0]		0000_0001_0000_0000	
16390	4006	Reset Control	1	0	0	0	0	0	SW_RESET_CFG	0	0	0	0	AUXRST_LPENA	RST_SLP_MSK	RST_SLPEN_A	0	0	RST_DUR[1:0]		1000_0100_0111_0011		
16391	4007	Control Interface	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AUTOINC	0	0	0000_0000_0000_0100			
16392	4008	Security Key	SECURITY[15:0]																0000_0000_0000_0000				
16393	4009	Software Scratch	SW_SCRATCH[15:0]																0000_0000_0000_0000				
16394	400A	OTP Control	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	U010_0000_0000_0000	
16395	400B	Security Key 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000	
16396	400C	GPIO Level	0	0	0	0	0	GP12_LVL	GP11_LVL	GP10_LVL	GP9_LVL	GP8_LVL	GP7_LVL	GP6_LVL	GP5_LVL	GP4_LVL	GP3_LVL	GP2_LVL	GP1_LVL	0000_0000_0000_0000			
16397	400D	System Status	THW_STS	0	0	0	0	0	0	0	0	0	XTAL_OK	0	0	MAIN_STATE[4:0]				0000_0000_0000_0000			
16398	400E	ON Source	ON_TRANS	0	0	0	0	ON_GPIO	ON_SYSLO	0	0	ON_WDOG_TO	ON_SW_REQ	ON_RTC_ALM	ON_ON_PIN	RESET_CNV_UV	RESET_SW	RESET_HW	RESET_WDOG	0000_0000_0000_0000			
16399	400F	OFF Source	0	0	OFF_INTLDO_ERR	OFF_PWR_SEQ	OFF_GPIO	OFF_PVDD	OFF_THERR	0	0	OFF_SW_REQ	0	OFF_ON_PIN	0	0	0	0	0	0000_0000_0000_0000			
16400	4010	System Interrupts	PS_INT	TEMP_INT	GP_INT	ON_PIN_INT	WDOG_INT	0	0	AUXADC_INT	PRM_INT	0	RTC_INT	OTP_INT	0	0	HC_INT	UV_INT	FFFF_F00P_F0FP_F0FP				
16401	4011	Interrupt Status 1	PRM_SYSLO_ENT	0	0	ON_PIN_CNT	WDOG_TO_ENT	0	0	AUXADC_DATA_ENT	AUXADC_COMP4_ENT	AUXADC_COMP2_ENT	AUXADC_COMP1_ENT	AUXADC_COMP1_ENT	RTC_PER_ENT	RTC_ALM_ENT	TEMP_THW_CNT	0	F00P_F00P_F0FP_F0FP				
16402	4012	Interrupt Status 2	0	0	0	0	0	0	0	0	0	0	0	OTP_CVID_END_ENT	OTP_ERR_ENT	0	PS_POR_ENT	PS_SLEEP_OFF_ENT	PS_ON_WAKE_ENT	0000_0000_00FP_0FPF			
16403	4013	Interrupt Status 3	0	0	0	0	0	0	0	UV_LDO10_ENT	UV_LDO9_ENT	UV_LDO8_ENT	UV_LDO7_ENT	UV_LDO6_ENT	UV_LDO5_ENT	UV_LDO4_ENT	UV_LDO3_ENT	UV_LDO2_ENT	UV_LDO1_ENT	0000_00FP_F0FP_F0FP			
16404	4014	Interrupt Status 4	0	0	0	0	0	0	0	HC_DC2_ENT	HC_DC1_ENT	XTAL_START_ENT	XTAL_TAMPER_ENT	0	0	UV_DC4_ENT	UV_DC3_ENT	UV_DC2_ENT	UV_DC1_ENT	0000_00FP_F0FP_F0FP			
16405	4015	Interrupt Status 5	0	0	0	0	0	0	0	GP12_ENT	GP11_ENT	GP10_ENT	GP9_ENT	GP8_ENT	GP7_ENT	GP6_ENT	GP5_ENT	GP4_ENT	GP3_ENT	GP2_ENT	GP1_ENT	0000_F0FP_F0FP_F0FP	
16406	4016	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000			
16407	4017	IRQ Config	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IRQ_OD	IM_IRQ	0000_0000_0000_0010			

28 REGISTER MAP OVERVIEW

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bin Default		
16408	4018	System Interrupts Mask	IM_PS_INT	IM_TEMP_INT	IM_GP_INT	IM_ON_PIN_INT	IM_WDOG_INT	0	0	IM_AUXADC_INT	IM_PFM_INT	0	IM_RTC_INT	IM_OTP_INT	1	0	IM_HC_INT	IM_UV_INT	1111_1001_1011_1011		
16409	4019	Interrupt Status 1 Mask	IM_PFM_SY_SLO_ENT	0	0	IM_ON_PIN_CNT	IM_WDOG_TO_ENT	0	0	IM_AUXADC_DATA_ENT	IM_AUXADC_COMP1_ENT	IM_AUXADC_COMP2_ENT	IM_AUXADC_COMP3_ENT	IM_AUXADC_COMP4_ENT	IM_RTC_PERR_ENT	IM_RTC_ALM_ENT	IM_TEMP_THW_CNT	0	1001_1001_1111_1110		
16410	401A	Interrupt Status 2 Mask	0	0	0	0	0	0	0	0	0	0	IM_OTP_CMD_END_ENT	IM_OTP_ERR_ENT	0	IM_PS_POR_ENT	IM_PS_SLEEP_OFF_ENT	IM_PS_ON_WAKE_ENT	0000_0000_0011_0111		
16411	401B	Interrupt Status 3 Mask	0	0	0	0	0	0	IM_UV_LDO10_ENT	IM_UV_LDO9_ENT	IM_UV_LDO8_ENT	IM_UV_LDO7_ENT	IM_UV_LDO6_ENT	IM_UV_LDO5_ENT	IM_UV_LDO4_ENT	IM_UV_LDO3_ENT	IM_UV_LDO2_ENT	IM_UV_LDO1_ENT	0000_0011_1111_1111		
16412	401C	Interrupt Status 4 Mask	0	0	0	0	0	0	IM_HC_DC2_ENT	IM_HC_DC1_ENT	IM_XTAL_START_ENT	0	0	0	IM_UV_DC4_ENT	IM_UV_DC3_ENT	IM_UV_DC2_ENT	IM_UV_DC1_ENT	0000_0011_1000_1111		
16413	401D	Interrupt Status 5 Mask	0	0	0	0	IM_GP12_ENT	IM_GP11_ENT	IM_GP10_ENT	IM_GP9_ENT	IM_GP8_ENT	IM_GP7_ENT	IM_GP6_ENT	IM_GP5_ENT	IM_GP4_ENT	IM_GP3_ENT	IM_GP2_ENT	IM_GP1_ENT	0000_1111_1111_1111		
16414	401E	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000		
16415	401F	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000		
16416	4020	RTC Write Counter	RTC_WRT_CNT[15:0]																0000_0000_0000_0000		
16417	4021	RTC Time 1	RTC_TIME[31:16]																0000_0000_0000_0000		
16418	4022	RTC Time 2	RTC_TIME[15:0]																0000_0000_0000_0000		
16419	4023	RTC Alarm 1	RTC_ALM[31:16]																0000_0000_0000_0000		
16420	4024	RTC Alarm 2	RTC_ALM[15:0]																0000_0000_0000_0000		
16421	4025	RTC Control	RTC_VALID	RTC_SYNC_BUSY	0	0	0	RTC_ALM_BNA	0	0	0	RTC_PINT_FREQ[2:0]		0	0	0	0	0	0000_0000_0000_0000		
16422	4026	RTC Trim	0	0	0	0	0	0	RTC_TRIM[9:0]										0000_0000_0000_0000		
16423	4027	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000		
16424	4028	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000		
16425	4029	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000		
16426	402A	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000		
16427	402B	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000		
16428	402C	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000		
16429	402D	AuxADC Data	AUX_DATA_SRC[3:0]				AUX_DATA[11:0]														0000_0000_0000_0000
16430	402E	AuxADC Control	AUX_ENA	AUX_OVTR_ENA	0	AUX_SLIPENA	0	0	0	0	0	0	AUX_RATE[5:0]						0000_0000_0000_0000		
16431	402F	AuxADC Source	0	0	0	0	0	0	0	0	0	AUX_FVDD_SEL	0	AUX_CHIP_TEMP_SEL	0	AUX_GPIO12_SEL	AUX_GPIO11_SEL	AUX_GPIO10_SEL	0000_0000_0000_0000		
16432	4030	Comparator Control	0	0	0	0	DCOMP4_STS	DCOMP3_STS	DCOMP2_STS	DCOMP1_STS	0	0	0	0	DCMP4_ENA	DCMP3_ENA	DCMP2_ENA	DCMP1_ENA	0000_0000_0000_0000		
16433	4031	Comparator 1	DCMP1_SRC[2:0]			DCMP1_GT	DCMP1_THR[11:0]													0000_0000_0000_0000	
16434	4032	Comparator 2	DCMP2_SRC[2:0]			DCMP2_GT	DCMP2_THR[11:0]													0000_0000_0000_0000	
16435	4033	Comparator 3	DCMP3_SRC[2:0]			DCMP3_GT	DCMP3_THR[11:0]													0000_0000_0000_0000	
16436	4034	Comparator 4	DCMP4_SRC[2:0]			DCMP4_GT	DCMP4_THR[11:0]													0000_0000_0000_0000	
16437	4035	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000		
16438	4036	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000		
16439	4037	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000		

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bin Default
16440	4038	GPIO1 Control	GP1_DIR	GP1_PULL[1:0]	GP1_INT_M_ODE	GP1_PWR_DOM	GP1_FOL	GP1_OD	0	GP1_ENA	0	0	0	GP1_FN[3:0]				1010_0100_0000_0000	
16441	4039	GPIO2 Control	GP2_DIR	GP2_PULL[1:0]	GP2_INT_M_ODE	GP2_PWR_DOM	GP2_FOL	GP2_OD	0	GP2_ENA	0	0	0	GP2_FN[3:0]				1010_0100_0000_0000	
16442	403A	GPIO3 Control	GP3_DIR	GP3_PULL[1:0]	GP3_INT_M_ODE	GP3_PWR_DOM	GP3_FOL	GP3_OD	0	GP3_ENA	0	0	0	GP3_FN[3:0]				1010_0100_0000_0000	
16443	403B	GPIO4 Control	GP4_DIR	GP4_PULL[1:0]	GP4_INT_M_ODE	GP4_PWR_DOM	GP4_FOL	GP4_OD	0	GP4_ENA	0	0	0	GP4_FN[3:0]				1010_0100_0000_0000	
16444	403C	GPIO5 Control	GP5_DIR	GP5_PULL[1:0]	GP5_INT_M_ODE	GP5_PWR_DOM	GP5_FOL	GP5_OD	0	GP5_ENA	0	0	0	GP5_FN[3:0]				1010_0100_0000_0000	
16445	403D	GPIO6 Control	GP6_DIR	GP6_PULL[1:0]	GP6_INT_M_ODE	GP6_PWR_DOM	GP6_FOL	GP6_OD	0	GP6_ENA	0	0	0	GP6_FN[3:0]				1010_0100_0000_0000	
16446	403E	GPIO7 Control	GP7_DIR	GP7_PULL[1:0]	GP7_INT_M_ODE	GP7_PWR_DOM	GP7_FOL	GP7_OD	0	GP7_ENA	0	0	0	GP7_FN[3:0]				1010_0100_0000_0000	
16447	403F	GPIO8 Control	GP8_DIR	GP8_PULL[1:0]	GP8_INT_M_ODE	GP8_PWR_DOM	GP8_FOL	GP8_OD	0	GP8_ENA	0	0	0	GP8_FN[3:0]				1010_0100_0000_0000	
16448	4040	GPIO9 Control	GP9_DIR	GP9_PULL[1:0]	GP9_INT_M_ODE	GP9_PWR_DOM	GP9_FOL	GP9_OD	0	GP9_ENA	0	0	0	GP9_FN[3:0]				1010_0100_0000_0000	
16449	4041	GPIO10 Control	GP10_DIR	GP10_PULL[1:0]	GP10_INT_MODE	GP10_PWR_DOM	GP10_POL	GP10_OD	0	GP10_ENA	0	0	0	GP10_FN[3:0]				1010_0100_0000_0000	
16450	4042	GPIO11 Control	GP11_DIR	GP11_PULL[1:0]	GP11_INT_MODE	GP11_PWR_DOM	GP11_POL	GP11_OD	0	GP11_ENA	0	0	0	GP11_FN[3:0]				1010_0100_0000_0000	
16451	4043	GPIO12 Control	GP12_DIR	GP12_PULL[1:0]	GP12_INT_MODE	GP12_PWR_DOM	GP12_POL	GP12_OD	0	GP12_ENA	0	0	0	GP12_FN[3:0]				1010_0100_0000_0000	
16452	4044	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16453	4045	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16454	4046	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16455	4047	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16456	4048	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0001
16457	4049	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0110_0000_0010
16458	404A	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16459	404B	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16460	404C	Status LED 1	LED1_SRC[1:0]	0	0	0	0	0	LED1_MODE[1:0]	0	0	LED1_SEQ_LEN[1:0]	LED1_DUR[1:0]	LED1_DUTY_CYQ[1:0]					1100_0000_0010_0110
16461	404D	Status LED 2	LED2_SRC[1:0]	0	0	0	0	0	LED2_MODE[1:0]	0	0	LED2_SEQ_LEN[1:0]	LED2_DUR[1:0]	LED2_DUTY_CYQ[1:0]					1100_0000_0010_0110
16462	404E	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16463	404F	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16464	4050	DCDC Enable	0	0	0	0	0	0	0	EPE2_ENA	EPE1_ENA	0	0	DC4_ENA	DC3_ENA	DC2_ENA	DC1_ENA	0000_0000_UU00_UUUU	
16465	4051	LDO Enable	0	0	0	0	0	LDO11_ENA	LDO10_ENA	LDO9_ENA	LDO8_ENA	LDO7_ENA	LDO6_ENA	LDO5_ENA	LDO4_ENA	LDO3_ENA	LDO2_ENA	LDO1_ENA	0000_0UUU_UUUU_UUUU
16466	4052	DCDC Status	0	0	0	0	0	0	0	EPE2_STS	EPE1_STS	0	0	DC4_STS	DC3_STS	DC2_STS	DC1_STS	0000_0000_0000_0000	
16467	4053	LDO Status	0	0	0	0	0	LDO11_STS	LDO10_STS	LDO9_STS	LDO8_STS	LDO7_STS	LDO6_STS	LDO5_STS	LDO4_STS	LDO3_STS	LDO2_STS	LDO1_STS	0000_0000_0000_0000
16468	4054	DCDC UV Status	0	0	DC2_OV_STS	DC1_OV_STS	0	0	DC2_HC_STS	DC1_HC_STS	0	0	0	0	DC4_UV_STS	DC3_UV_STS	DC2_UV_STS	DC1_UV_STS	0000_0000_0000_0000
16469	4055	LDO UV Status	INTLDO_UV_STS	0	0	0	0	0	LDO10_UV_STS	LDO9_UV_STS	LDO8_UV_STS	LDO7_UV_STS	LDO6_UV_STS	LDO5_UV_STS	LDO4_UV_STS	LDO3_UV_STS	LDO2_UV_STS	LDO1_UV_STS	0000_0000_0000_0000
16470	4056	DC1 Control 1	DC1_RATE[1:0]	0	DC1_PHASE	0	0	0	0	0	DC1_FLT	0	DC1_SOFT_START[1:0]	0	0	0	0	0	1000_0000_0000_0000
16471	4057	DC1 Control 2	DC1_ERR_ACT[1:0]	0	DC1_HWC_SRC[1:0]	DC1_HWC_VSEL	DC1_HWC_MODE[1:0]	0	DC1_HC_THR[2:0]	0	0	0	0	DC1_FAST_DRV	DC1_HC_IN_D_ENA				0000_0011_0000_0000

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bin Default	
16472	4058	DC1 ON Config	DC1_ON_SLOT[2:0]			0	0	0	DC1_ON_MODE[1:0]			0	DC1_ON_VSEL[6:2]				DC1_ON_VSEL[1:0]		0000_0001_0000_0000	
16473	4059	DC1 SLEEP Control	DC1_SLP_SLOT[2:0]			0	0	0	DC1_SLP_MODE[1:0]			0	DC1_SLP_VSEL[6:0]						0000_0011_0000_0000	
16474	405A	DC1 DVS Control	0	0	0	DC1_DVS_SRC[1:0]		0	0	0	0	DC1_DVS_VSEL[6:0]						0000_0000_0000_0000		
16475	405B	DC2 Control 1	DC2_RATE[1:0]		0	DC2_PHASE	0	0	0	0	DC2_FLT	0	DC2_SOFT_START[1:0]		0	0	0	0	1001_0000_0000_0000	
16476	405C	DC2 Control 2	DC2_ERR_ACT[1:0]		0	DC2_HWC_SRC[1:0]		DC2_HWC_VSEL	DC2_HWC_MODE[1:0]		0	DC2_HC_THR[2:0]			0	0	DC2_FAST_DRV	DC2_HC_IN_D_ENA	0000_0011_0000_0000	
16477	405D	DC2 ON Config	DC2_ON_SLOT[2:0]			0	0	0	DC2_ON_MODE[1:0]			0	DC2_ON_VSEL[6:2]				DC2_ON_VSEL[1:0]		0000_0001_0000_0000	
16478	405E	DC2 SLEEP Control	DC2_SLP_SLOT[2:0]			0	0	0	DC2_SLP_MODE[1:0]			0	DC2_SLP_VSEL[6:0]						0000_0011_0000_0000	
16479	405F	DC2 DVS Control	0	0	0	DC2_DVS_SRC[1:0]		0	0	0	0	DC2_DVS_VSEL[6:0]						0000_0000_0000_0000		
16480	4060	DC3 Control 1	0	0	0	DC3_PHASE	0	0	0	0	DC3_FLT	0	DC3_SOFT_START[1:0]		DC3_STNBY_LIM[1:0]		0	0	0000_0000_0001_0100	
16481	4061	DC3 Control 2	DC3_ERR_ACT[1:0]		0	DC3_HWC_SRC[1:0]		DC3_HWC_VSEL	DC3_HWC_MODE[1:0]		DC3_OVP	0	0	0	0	0	0	0	0000_0011_0000_0000	
16482	4062	DC3 ON Config	DC3_ON_SLOT[2:0]			0	0	0	DC3_ON_MODE[1:0]			0	DC3_ON_VSEL[6:2]				DC3_ON_VSEL[1:0]		0000_0001_0000_0000	
16483	4063	DC3 SLEEP Control	DC3_SLP_SLOT[2:0]			0	0	0	DC3_SLP_MODE[1:0]			0	DC3_SLP_VSEL[6:0]						0000_0011_0000_0000	
16484	4064	DC4 Control 1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0000_0000_0001_0100	
16485	4065	DC4 Control 2	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0000_0011_0000_0000	
16486	4066	DC4 ON Config	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0000_0001_0000_0000	
16487	4067	DC4 SLEEP Control	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0000_0011_0000_0000	
16488	4068	LDO1 Control	LDO1_ERR_ACT[1:0]		0	LDO1_HWC_SRC[1:0]		LDO1_HWC_VSEL	LDO1_HWC_MODE[1:0]		LDO1_FLT	LDO1_SWI	0	0	0	0	0	0	LDO1_LP_MODE	0000_0010_0000_0000
16489	4069	LDO1 ON Control	LDO1_ON_SLOT[2:0]			0	0	0	0	LDO1_ON_MODE	0	0	0	LDO1_ON_VSEL[4:0]				0000_0000_0000_0000		
16490	406A	LDO1 SLEEP Control	LDO1_SLP_SLOT[2:0]			0	0	0	0	LDO1_SLP_MODE	0	0	0	LDO1_SLP_VSEL[4:0]				0000_0001_0000_0000		
16491	406B	LDO2 Control	LDO2_ERR_ACT[1:0]		0	LDO2_HWC_SRC[1:0]		LDO2_HWC_VSEL	LDO2_HWC_MODE[1:0]		LDO2_FLT	LDO2_SWI	0	0	0	0	0	0	LDO2_LP_MODE	0000_0010_0000_0000
16492	406C	LDO2 ON Control	LDO2_ON_SLOT[2:0]			0	0	0	0	LDO2_ON_MODE	0	0	0	LDO2_ON_VSEL[4:0]				0000_0000_0000_0000		
16493	406D	LDO2 SLEEP Control	LDO2_SLP_SLOT[2:0]			0	0	0	0	LDO2_SLP_MODE	0	0	0	LDO2_SLP_VSEL[4:0]				0000_0001_0000_0000		
16494	406E	LDO3 Control	LDO3_ERR_ACT[1:0]		0	LDO3_HWC_SRC[1:0]		LDO3_HWC_VSEL	LDO3_HWC_MODE[1:0]		LDO3_FLT	LDO3_SWI	0	0	0	0	0	0	LDO3_LP_MODE	0000_0010_0000_0000
16495	406F	LDO3 ON Control	LDO3_ON_SLOT[2:0]			0	0	0	0	LDO3_ON_MODE	0	0	0	LDO3_ON_VSEL[4:0]				0000_0000_0000_0000		
16496	4070	LDO3 SLEEP Control	LDO3_SLP_SLOT[2:0]			0	0	0	0	LDO3_SLP_MODE	0	0	0	LDO3_SLP_VSEL[4:0]				0000_0001_0000_0000		
16497	4071	LDO4 Control	LDO4_ERR_ACT[1:0]		0	LDO4_HWC_SRC[1:0]		LDO4_HWC_VSEL	LDO4_HWC_MODE[1:0]		LDO4_FLT	LDO4_SWI	0	0	0	0	0	0	LDO4_LP_MODE	0000_0010_0000_0000
16498	4072	LDO4 ON Control	LDO4_ON_SLOT[2:0]			0	0	0	0	LDO4_ON_MODE	0	0	0	LDO4_ON_VSEL[4:0]				0000_0000_0000_0000		
16499	4073	LDO4 SLEEP Control	LDO4_SLP_SLOT[2:0]			0	0	0	0	LDO4_SLP_MODE	0	0	0	LDO4_SLP_VSEL[4:0]				0000_0001_0000_0000		
16500	4074	LDO5 Control	LDO5_ERR_ACT[1:0]		0	LDO5_HWC_SRC[1:0]		LDO5_HWC_VSEL	LDO5_HWC_MODE[1:0]		LDO5_FLT	LDO5_SWI	0	0	0	0	0	0	LDO5_LP_MODE	0000_0010_0000_0000
16501	4075	LDO5 ON Control	LDO5_ON_SLOT[2:0]			0	0	0	0	LDO5_ON_MODE	0	0	0	LDO5_ON_VSEL[4:0]				0000_0000_0000_0000		
16502	4076	LDO5 SLEEP Control	LDO5_SLP_SLOT[2:0]			0	0	0	0	LDO5_SLP_MODE	0	0	0	LDO5_SLP_VSEL[4:0]				0000_0001_0000_0000		
16503	4077	LDO6 Control	LDO6_ERR_ACT[1:0]		0	LDO6_HWC_SRC[1:0]		LDO6_HWC_VSEL	LDO6_HWC_MODE[1:0]		LDO6_FLT	LDO6_SWI	0	0	0	0	0	0	LDO6_LP_MODE	0000_0010_0000_0000

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bin Default
16504	4078	LDO6 ON Control	LDO6_ON_SLOT[2:0]		0	0	0	0	LDO6_ON_MODE	0	0	0	LDO6_ON_VSEL[4:0]				0000_0000_0000_0000		
16505	4079	LDO6 SLEEP Control	LDO6_SLP_SLOT[2:0]		0	0	0	0	LDO6_SLP_MODE	0	0	0	LDO6_SLP_VSEL[4:0]				0000_0001_0000_0000		
16506	407A	LDO7 Control	LDO7_ERR_ACT[1:0]	0	LDO7_HWC_SRC[1:0]	LDO7_HWC_VSEL	LDO7_HWC_MODE[1:0]	LDO7_FLT	LDO7_SWI	0	0	0	0	0	0	0	0	0	0000_0010_0000_0000
16507	407B	LDO7 ON Control	LDO7_ON_SLOT[2:0]		0	0	0	0	LDO7_ON_MODE	0	0	0	LDO7_ON_VSEL[4:0]				0000_0000_0000_0000		
16508	407C	LDO7 SLEEP Control	LDO7_SLP_SLOT[2:0]		0	0	0	0	LDO7_SLP_MODE	0	0	0	LDO7_SLP_VSEL[4:0]				0000_0001_0000_0000		
16509	407D	LDO8 Control	LDO8_ERR_ACT[1:0]	0	LDO8_HWC_SRC[1:0]	LDO8_HWC_VSEL	LDO8_HWC_MODE[1:0]	LDO8_FLT	LDO8_SWI	0	0	0	0	0	0	0	0	0	0000_0010_0000_0000
16510	407E	LDO8 ON Control	LDO8_ON_SLOT[2:0]		0	0	0	0	LDO8_ON_MODE	0	0	0	LDO8_ON_VSEL[4:0]				0000_0000_0000_0000		
16511	407F	LDO8 SLEEP Control	LDO8_SLP_SLOT[2:0]		0	0	0	0	LDO8_SLP_MODE	0	0	0	LDO8_SLP_VSEL[4:0]				0000_0001_0000_0000		
16512	4080	LDO9 Control	LDO9_ERR_ACT[1:0]	0	LDO9_HWC_SRC[1:0]	LDO9_HWC_VSEL	LDO9_HWC_MODE[1:0]	LDO9_FLT	LDO9_SWI	0	0	0	0	0	0	0	0	0	0000_0010_0000_0000
16513	4081	LDO9 ON Control	LDO9_ON_SLOT[2:0]		0	0	0	0	LDO9_ON_MODE	0	0	0	LDO9_ON_VSEL[4:0]				0000_0000_0000_0000		
16514	4082	LDO9 SLEEP Control	LDO9_SLP_SLOT[2:0]		0	0	0	0	LDO9_SLP_MODE	0	0	0	LDO9_SLP_VSEL[4:0]				0000_0001_0000_0000		
16515	4083	LDO10 Control	LDO10_ERR_ACT[1:0]	0	LDO10_HWC_SRC[1:0]	LDO10_HWC_VSEL	LDO10_HWC_MODE[1:0]	LDO10_FLT	LDO10_SWI	0	0	0	0	0	0	0	0	0	0000_0010_0000_0000
16516	4084	LDO10 ON Control	LDO10_ON_SLOT[2:0]		0	0	0	0	LDO10_ON_MODE	0	0	0	LDO10_ON_VSEL[4:0]				0000_0000_0000_0000		
16517	4085	LDO10 SLEEP Control	LDO10_SLP_SLOT[2:0]		0	0	0	0	LDO10_SLP_MODE	0	0	0	LDO10_SLP_VSEL[4:0]				0000_0001_0000_0000		
16518	4086	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16519	4087	LDO11 ON Control	LDO11_ON_SLOT[2:0]		LDO11_FRC_ENA	0	0	0	0	LDO11_VSEL_SRC	0	0	0	LDO11_ON_VSEL[3:0]			0000_0000_0000_0000		
16520	4088	LDO11 SLEEP Control	LDO11_SLP_SLOT[2:0]		0	0	0	0	0	0	0	0	LDO11_SLP_VSEL[3:0]			0000_0000_0000_0000			
16521	4089	EPE1 Control	EPE1_ON_SLOT[2:0]		EPE1_HWC_SRC[1:0]	0	0	EPE1_HWC_ENA	EPE1_SLP_SLOT[2:0]		0	0	0	0	0	0	0	0	0000_0000_0000_0000
16522	408A	EPE2 Control	EPE2_ON_SLOT[2:0]		EPE2_HWC_SRC[1:0]	0	0	EPE2_HWC_ENA	EPE2_SLP_SLOT[2:0]		0	0	0	0	0	0	0	0	0000_0000_0000_0000
16523	408B	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16524	408C	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16525	408D	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16526	408E	Power Good Source 1	0	0	0	0	0	0	0	0	0	0	0	0	DC4_OK	DC3_OK	DC2_OK	DC1_OK	0000_0000_0000_0111
16527	408F	Power Good Source 2	0	0	0	0	0	0	LDO10_OK	LDO9_OK	LDO8_OK	LDO7_OK	LDO6_OK	LDO5_OK	LDO4_OK	LDO3_OK	LDO2_OK	LDO1_OK	0000_0011_1111_1111
16528	4090	Clock Control 1	CLKOUT_ENA	0	CLKOUT_OD	0	0	CLKOUT_SLOT[2:0]		0	CLKOUT_SLP_SLOT[2:0]		0	0	0	0	0	0	U000_0000_0000_0000
16529	4091	Clock Control 2	XTAL_INH	0	0	XTAL_BKUPENA	0	0	0	0	0	0	0	0	0	0	0	0	0001_0000_0000_0000
16530	4092	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16531	4093	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16532	4094	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16533	4095	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16534	4096	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16535	4097	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bin Default	
30720	7800	Unique ID 1	UNIQUE_ID[127:112]																0000_0000_0000_0000	
30721	7801	Unique ID 2	UNIQUE_ID[111:96]																0000_0000_0000_0000	
30722	7802	Unique ID 3	UNIQUE_ID[95:80]																0000_0000_0000_0000	
30723	7803	Unique ID 4	UNIQUE_ID[79:64]																0000_0000_0000_0000	
30724	7804	Unique ID 5	UNIQUE_ID[63:48]																0000_0000_0000_0000	
30725	7805	Unique ID 6	UNIQUE_ID[47:32]																0000_0000_0000_0000	
30726	7806	Unique ID 7	UNIQUE_ID[31:16]																0000_0000_0000_0000	
30727	7807	Unique ID 8	UNIQUE_ID[15:0]																0000_0000_0000_0000	
30728	7808	Factory OTP ID	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000	
30729	7809	Factory OTP 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000	
30730	780A	Factory OTP 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000	
30731	780B	Factory OTP 3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000	
30732	780C	Factory OTP 4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000	
30733	780D	Factory OTP 5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000	
30734	780E	Factory OTP 6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000	
30735	780F	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000	
30736	7810	Customer OTP ID	0	OTP_CUST_ID[13:0]															OTP_CUST_FINAL	0000_0000_0000_0000
30737	7811	DC1 OTP Control	DC2_ON_SLOT[2:0]			DC2_ON_VSEL[6:2]				DC1_ON_SLOT[2:0]			DC1_ON_VSEL[6:2]				0000_0000_0000_0000			
30738	7812	DC2 OTP Control	0	0	0	0	0	0	0	0	DC3_ON_SLOT[2:0]			DC3_ON_VSEL[6:2]				0000_0000_0000_0000		
30739	7813	DC3 OTP Control	0	DC3_PHASE	DC2_PHASE	DC1_PHASE	0	0	0	0	0	0	0	0	0	0	0	0	0	0010_0000_0000_0000
30740	7814	LDO1/2 OTP Control	LDO2_ON_SLOT[2:0]			LDO2_ON_VSEL[4:0]				LDO1_ON_SLOT[2:0]			LDO1_ON_VSEL[4:0]				0000_0000_0000_0000			
30741	7815	LDO3/4 OTP Control	LDO4_ON_SLOT[2:0]			LDO4_ON_VSEL[4:0]				LDO3_ON_SLOT[2:0]			LDO3_ON_VSEL[4:0]				0000_0000_0000_0000			
30742	7816	LDO5/6 OTP Control	LDO6_ON_SLOT[2:0]			LDO6_ON_VSEL[4:0]				LDO5_ON_SLOT[2:0]			LDO5_ON_VSEL[4:0]				0000_0000_0000_0000			
30743	7817	LDO7/8 OTP Control	LDO8_ON_SLOT[2:0]			LDO8_ON_VSEL[4:0]				LDO7_ON_SLOT[2:0]			LDO7_ON_VSEL[4:0]				0000_0000_0000_0000			
30744	7818	LDO9/10 OTP Control	LDO10_ON_SLOT[2:0]			LDO10_ON_VSEL[4:0]				LDO9_ON_SLOT[2:0]			LDO9_ON_VSEL[4:0]				0000_0000_0000_0000			
30745	7819	LDO11/EPE Control	LDO11_ON_SLOT[2:0]			0	LDO11_ON_VSEL[3:0]			EPE2_ON_SLOT[2:0]			EPE1_ON_SLOT[2:0]		0	0	0000_0000_0000_0000			
30746	781A	GPI01 OTP Control	GP1_DIR	GP1_PULL[1:0]		GP1_INT_MODE	GP1_PWR_DOM	GP1_POL	GP1_OD	GP1_ENA	GP1_FN[3:0]			0	0	XTAL_INH	0	1010_0100_0000_0000		
30747	781B	GPI02 OTP Control	GP2_DIR	GP2_PULL[1:0]		GP2_INT_MODE	GP2_PWR_DOM	GP2_POL	GP2_OD	GP2_ENA	GP2_FN[3:0]			CLKOUT_SLOT[2:0]		WDOG_ENA	0	1010_0100_0000_0001		
30748	781C	GPI03 OTP Control	GP3_DIR	GP3_PULL[1:0]		GP3_INT_MODE	GP3_PWR_DOM	GP3_POL	GP3_OD	GP3_ENA	GP3_FN[3:0]			0	0	0	0	1010_0100_0000_0000		
30749	781D	GPI04 OTP Control	GP4_DIR	GP4_PULL[1:0]		GP4_INT_MODE	GP4_PWR_DOM	GP4_POL	GP4_OD	GP4_ENA	GP4_FN[3:0]			LED1_SRC[1:0]		LED2_SRC[1:0]		1010_0100_0000_1111		
30750	781E	GPI05 OTP Control	GP5_DIR	GP5_PULL[1:0]		GP5_INT_MODE	GP5_PWR_DOM	GP5_POL	GP5_OD	GP5_ENA	GP5_FN[3:0]			0	0	0	0	1010_0100_0000_0000		
30751	781F	GPI06 OTP Control	GP6_DIR	GP6_PULL[1:0]		GP6_INT_MODE	GP6_PWR_DOM	GP6_POL	GP6_OD	GP6_ENA	GP6_FN[3:0]			SYSOK_THR[2:0]		0	1010_0100_0000_1010			

29 REGISTER BITS BY ADDRESS

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R0 (00h) Reset ID	15:0	CHIP_ID [15:0]	0000_0000 _0000_000 0	Writing to this register causes a Software Reset. The register map contents may be reset, depending on SW_RESET_CFG. Reading from this register will indicate Chip ID.	

Register 00h Reset ID

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1 (01h) Revision	15:8	PARENT_REV [7:0]	0000_0000	The revision number of the parent die	
	7:0	CHILD_REV [7:0]	0000_0000	The revision number of the child die (when present)	

Register 01h Revision

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16384 (4000h) Parent ID	15:0	PARENT_ID [15:0]	0110_0010 _0100_011 0	The ID of the parent die	

Register 4000h Parent ID

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16385 (4001h) PVDD Control	15:14	SYSLO_ERR_ACT [1:0]	00	SYSLO Error Action Selects the action taken when SYSLO is asserted 00 = Interrupt 01 = WAKE transition 10 = Reserved 11 = OFF transition	
	11	SYSLO_STS	0	SYSLO Status 0 = Normal 1 = PVDD is below SYSLO threshold	
	6:4	SYSLO_THR [2:0]	010	SYSLO threshold (falling PVDD) This is the falling PVDD voltage at which SYSLO will be asserted 000 = 2.8V 001 = 2.9V ... 111 = 3.5V	
	2:0	SYSOK_THR [2:0]	101	SYSOK threshold (rising PVDD) This is the rising PVDD voltage at which SYSOK will be asserted 000 = 2.8V 001 = 2.9V ... 111 = 3.5V	

Register 4001h PVDD Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16386 (4002h) Thermal Monitoring	3	THW_HYST	1	Thermal Warning hysteresis 0 = 8 degrees C 1 = 16 degrees C	
	1:0	THW_TEMP [1:0]	10	Thermal Warning temperature 00 = 90 degrees C 01 = 100 degrees C 10 = 110 degrees C 11 = 120 degrees C	

Register 4002h Thermal Monitoring

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16387 (4003h) Power State	15	CHIP_ON	0	Indicates whether the system is ON or OFF. 0 = OFF 1 = ON (or SLEEP) OFF can be commanded by writing CHIP_ON = 0. Note that writing CHIP_ON = 1 is not a valid 'ON' event, and will not trigger an ON transition.	
	14	CHIP_SLP	0	Indicates whether the system is in the SLEEP state. 0 = Not in SLEEP 1 = SLEEP WAKE can be commanded by writing CHIP_SLP = 0. SLEEP can be commanded by writing CHIP_SLP = 1.	
	12	REF_LP	0	Low Power Voltage Reference Control 0 = Normal 1 = Low Power Reference Mode select Note that Low Power Reference Mode is only supported when the Auxiliary ADC is disabled.	
	11:10	PWRSTATE_D LY [1:0]	10	Power State transition delay 00 = No delay 01 = No delay 10 = 1ms 11 = 10ms	
	9	SWRST_DLY	0	Software Reset Delay 0 = No delay 1 = Software Reset is delayed by PWRSTATE_DLY following the Software Reset command	

Register 4003h Power State

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16388 (4004h) Watchdog	15	WDOG_ENA	1	Watchdog Timer Enable 0 = Disabled 1 = Enabled (enables the watchdog; does not reset it) <i>Protected by security key.</i>	
	14	WDOG_DEBU G	0	Watchdog Pause 0 = Disabled 1 = Enabled (halts the Watchdog timer for system debugging) <i>Protected by security key.</i>	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	13	WDOG_RST_SRC	1	Watchdog Reset Source 0 = Hardware only 1 = Software only <i>Protected by security key.</i>	
	12	WDOG_SLPE NA	0	Watchdog SLEEP Enable 0 = Disabled 1 = Controlled by WDOG_ENA <i>Protected by security key.</i>	
	11	WDOG_RESET	0	Watchdog Software Reset 0 = Normal 1 = Watchdog Reset (resets the watchdog, if WDOG_RST_SRC = 1)	
	9:8	WDOG_SECA CT [1:0]	10	Secondary action of Watchdog timeout (taken after 2 timeout periods) 00 = No action 01 = Interrupt 10 = Device Reset 11 = WAKE transition <i>Protected by security key.</i>	
	5:4	WDOG_PRIMA CT [1:0]	01	Primary action of Watchdog timeout 00 = No action 01 = Interrupt 10 = Device Reset 11 = WAKE transition <i>Protected by security key.</i>	
	2:0	WDOG_TO [2:0]	111	Watchdog timeout period 000 = 0.256s 001 = 0.512s 010 = 1.024s 011 = 2.048s 100 = 4.096s 101 = 8.192s 110 = 16.384s 111 = 32.768s <i>Protected by security key.</i>	

Register 4004h Watchdog

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16389 (4005h) ON Pin Control	9:8	ON_PIN_SECA CT [1:0]	01	Secondary action of ON pin (taken after 1 timeout period) 00 = Interrupt 01 = ON request 10 = OFF request 11 = Reserved <i>Protected by security key.</i>	
	5:4	ON_PIN_PRIM ACT [1:0]	00	Primary action of ON pin 00 = Ignore 01 = ON request 10 = OFF request 11 = Reserved Note that an Interrupt is always raised.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				<i>Protected by security key.</i>	
	3	ON_PIN_STS	0	Current status of ON pin 0 = Asserted (logic 0) 1 = Not asserted (logic 1)	
	1:0	ON_PIN_TO [1:0]	00	ON pin timeout period 00 = 1s 01 = 2s 10 = 4s 11 = 8s <i>Protected by security key.</i>	

Register 4005h ON Pin Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16390 (4006h) Reset Control	10	SW_RESET_CFG	1	Software Reset Configuration. Selects whether the register map is reset to default values when Software Reset occurs. 0 = All registers except VPMIC domain and RTC are reset by Software Reset 1 = Register Map is not affected by Software Reset <i>Protected by security key.</i>	
	6	AUXRST_SLP_ENA	1	Sets the output status of Auxiliary Reset (GPIO) function in SLEEP 0 = Auxiliary Reset not asserted 1 = Auxiliary Reset asserted <i>Protected by security key.</i>	
	5	RST_SLP_MASK	1	Masks the RESET pin input in SLEEP mode 0 = External RESET active in SLEEP 1 = External RESET masked in SLEEP <i>Protected by security key.</i>	
	4	RST_SLPENA	1	Sets the output status of RESET pin in SLEEP 0 = RESET high (not asserted) 1 = RESET low (asserted) <i>Protected by security key.</i>	
	1:0	RST_DUR [1:0]	11	Delay period for releasing RESET after ON or WAKE sequence 00 = 3ms 01 = 11ms 10 = 51ms 11 = 101ms <i>Protected by security key.</i>	

Register 4006h Reset Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16391 (4007h) Control Interface	2	AUTOINC	1	Enable Auto-Increment function 0 = Disabled 1 = Enabled	

Register 4007h Control Interface

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16392 (4008h) Security Key	15:0	SECURITY [15:0]	0000_0000 _0000_000 0	Security Key A value of 9716h must be written to this register to access the user-keyed registers.	

Register 4008h Security Key

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16393 (4009h) Software Scratch	15:0	SW_SCRATCH [15:0]	0000_0000 _0000_000 0	Software Scratch Register for use by the host processor. Note that this register's contents are retained in the BACKUP power state.	

Register 4009h Software Scratch

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16396 (400Ch) GPIO Level	11	GP12_LVL	0	GPIO12 level. When GP12_FN = 0h and GP12_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP12_POL is 0, the register contains the opposite logic level to the external pin.	
	10	GP11_LVL	0	GPIO11 level. When GP11_FN = 0h and GP11_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP11_POL is 0, the register contains the opposite logic level to the external pin.	
	9	GP10_LVL	0	GPIO10 level. When GP10_FN = 0h and GP10_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP10_POL is 0, the register contains the opposite logic level to the external pin.	
	8	GP9_LVL	0	GPIO9 level. When GP9_FN = 0h and GP9_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP9_POL is 0, the register contains the opposite logic level to the external pin.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	7	GP8_LVL	0	GPIO8 level. When GP8_FN = 0h and GP8_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP8_POL is 0, the register contains the opposite logic level to the external pin.	
	6	GP7_LVL	0	GPIO7 level. When GP7_FN = 0h and GP7_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP7_POL is 0, the register contains the opposite logic level to the external pin.	
	5	GP6_LVL	0	GPIO6 level. When GP6_FN = 0h and GP6_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP6_POL is 0, the register contains the opposite logic level to the external pin.	
	4	GP5_LVL	0	GPIO5 level. When GP5_FN = 0h and GP5_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP5_POL is 0, the register contains the opposite logic level to the external pin.	
	3	GP4_LVL	0	GPIO4 level. When GP4_FN = 0h and GP4_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP4_POL is 0, the register contains the opposite logic level to the external pin.	
	2	GP3_LVL	0	GPIO3 level. When GP3_FN = 0h and GP3_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP3_POL is 0, the register contains the opposite logic level to the external pin.	
	1	GP2_LVL	0	GPIO2 level. When GP2_FN = 0h and GP2_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP2_POL is 0, the register contains the opposite logic level to the external pin.	
	0	GP1_LVL	0	GPIO1 level. When GP1_FN = 0h and GP1_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP1_POL is 0, the register contains the opposite logic level to the external pin.	

Register 400Ch GPIO Level

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16397 (400Dh) System Status	15	THW_STS	0	Thermal Warning status 0 = Normal 1 = Overtemperature Warning (warning temperature is set by THW_TEMP)	
	7	XTAL_OK	0	Crystal Oscillator Status 0 = Disabled or in start-up phase 1 = Enabled and verified	
	4:0	MAIN_STATE [4:0]	0_0000	Main State Machine condition 0_0000 = OFF 0_0001 = ON_CHK 0_0010 = OTP_DN 0_0011 = READ_OTP 0_0100 = UNUSED 0_0101 = UNUSED 0_0110 = BGDELAY 0_0111 = HYST 0_1000 = S_PRG_RD_OTP 0_1001 = S_PRG_OTP_DN 0_1010 = PWRDN1 0_1011 = PROGRAM 0_1100 = PROG_DN 0_1101 = PROG_OTP 0_1110 = VFY_OTP 0_1111 = VFY_DN 1_0000 = SD_RD_OTP 1_0001 = UNUSED 1_0010 = UNUSED 1_0011 = SHUTDOWN 1_0100 = STARTFAIL 1_0101 = STARTUP 1_0110 = PRACTIVE 1_0111 = XTAL_CHK 1_1000 = PWRDN2 1_1001 = SHUT_DLY 1_1010 = RESET 1_1011 = RESET_DLY 1_1100 = SLEEP 1_1101 = SLEEP_DLY 1_1110 = CHK_RST 1_1111 = ACTIVE (ON)	

Register 400Dh System Status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16398 (400Eh) ON Source	15	ON_TRANS	0	Most recent ON/WAKE event type 0 = WAKE transition 1 = ON transition <i>Reset by state machine.</i>	
	11	ON_GPIO	0	Most recent ON/WAKE event type 0 = Not caused by GPIO input 1 = Caused by GPIO input <i>Reset by state machine.</i>	
	10	ON_SYSLO	0	Most recent WAKE event type 0 = Not caused by PVDD 1 = Caused by SYSLO threshold. Note that the SYSLO threshold cannot trigger an ON event. <i>Reset by state machine.</i>	
	7	ON_WDOG_T O	0	Most recent WAKE event type 0 = Not caused by Watchdog timer 1 = Caused by Watchdog timer <i>Reset by state machine.</i>	
	6	ON_SW_REQ	0	Most recent WAKE event type 0 = Not caused by software WAKE 1 = Caused by software WAKE command (CHIP_SLP = 0) <i>Reset by state machine.</i>	
	5	ON_RTC_ALM	0	Most recent ON/WAKE event type 0 = Not caused by RTC Alarm 1 = Caused by RTC Alarm <i>Reset by state machine.</i>	
	4	ON_ON_PIN	0	Most recent ON/WAKE event type 0 = Not caused by the ON pin 1 = Caused by the ON pin <i>Reset by state machine.</i>	
	3	RESET_CNV_ UV	0	Most recent ON event type 0 = Not caused by undervoltage 1 = Caused by a Device Reset due to a Converter (LDO or DC-DC) undervoltage condition <i>Reset by state machine.</i>	
	2	RESET_SW	0	Most recent ON event type 0 = Not caused by Software Reset 1 = Caused by Software Reset <i>Reset by state machine.</i>	
	1	RESET_HW	0	Most recent ON event type 0 = Not caused by Hardware Reset 1 = Caused by Hardware Reset <i>Reset by state machine.</i>	
0	RESET_WDO G	0	Most recent ON event type 0 = Not caused by the Watchdog 1 = Caused by a Device Reset triggered by the Watchdog timer <i>Reset by state machine.</i>		

Register 400Eh ON Source

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16399 (400Fh) OFF Source	13	OFF_INTLDO_ERR	0	Most recent OFF event type 0 = Not caused by LDO13 Error condition 1 = Caused by LDO13 Error condition <i>Reset by state machine.</i>	
	12	OFF_PWR_SEQ_Q	0	Most recent OFF event type 0 = Not caused by Power Sequence Failure 1 = Caused by a Power Sequence Failure <i>Reset by state machine.</i>	
	11	OFF_GPIO	0	Most recent OFF event type 0 = Not caused by GPIO input 1 = Caused by GPIO input <i>Reset by state machine.</i>	
	10	OFF_PVDD	0	Most recent OFF event type 0 = Not caused by PVDD 1 = Caused by the SYSLO or SHUTDOWN threshold <i>Reset by state machine.</i>	
	9	OFF_THERR	0	Most recent OFF event type 0 = Not caused by temperature 1 = Caused by over-temperature <i>Reset by state machine.</i>	
	6	OFF_SW_REQ	0	Most recent OFF event type 0 = Not caused by software OFF 1 = Caused by software OFF command (CHIP_ON = 0) <i>Reset by state machine.</i>	
	4	OFF_ON_PIN	0	Most recent OFF event type 0 = Not caused by the ON pin 1 = Caused by the ON pin <i>Reset by state machine.</i>	

Register 400Fh OFF Source

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16400 (4010h) System Interrupts	15	PS_INT	0	Power State primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	14	TEMP_INT	0	Thermal primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	13	GP_INT	0	GPIO primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	12	ON_PIN_INT	0	ON Pin primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	11	WDOG_INT	0	Watchdog primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	8	AUXADC_INT	0	AUXADC primary interrupt 0 = No interrupt 1 = Interrupt is asserted	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	7	PPM_INT	0	Power Path Management primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	5	RTC_INT	0	Real Time Clock and Crystal Oscillator primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	1	HC_INT	0	High Current primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	0	UV_INT	0	Undervoltage primary interrupt 0 = No interrupt 1 = Interrupt is asserted	

Register 4010h System Interrupts

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16401 (4011h) Interrupt Status 1	15	PPM_SYSLO_EINT	0	Power Path SYSLO interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	12	ON_PIN_CINT	0	ON pin interrupt. (Rising and Falling Edge triggered) Note: Cleared when a '1' is written.	
	11	WDOG_TO_EINT	0	Watchdog timeout interrupt. (Rising Edge triggered) Note: Cleared when a '1' is written.	
	8	AUXADC_DATA_EINT	0	AUXADC Data Ready interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	7	AUXADC_DCOMP4_EINT	0	AUXADC Digital Comparator 4 interrupt (Trigger is controlled by DCMP4_GT) Note: Cleared when a '1' is written.	
	6	AUXADC_DCOMP3_EINT	0	AUXADC Digital Comparator 3 interrupt (Trigger is controlled by DCMP3_GT) Note: Cleared when a '1' is written.	
	5	AUXADC_DCOMP2_EINT	0	AUXADC Digital Comparator 2 interrupt (Trigger is controlled by DCMP2_GT) Note: Cleared when a '1' is written.	
	4	AUXADC_DCOMP1_EINT	0	AUXADC Digital Comparator 1 interrupt (Trigger is controlled by DCMP1_GT) Note: Cleared when a '1' is written.	
	3	RTC_PERIODIC_INT	0	RTC Periodic interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	2	RTC_ALARM_INT	0	RTC Alarm interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	1	TEMP_THW_CINT	0	Thermal Warning interrupt (Rising and Falling Edge triggered) Note: Cleared when a '1' is written.	

Register 4011h Interrupt Status 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16402 (4012h) Interrupt Status 2	2	PS_POR_EINT	0	Power On Reset interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	1	PS_SLEEP_O FF_EINT	0	SLEEP or OFF interrupt (Power state transition to SLEEP or OFF states) (Rising Edge triggered) Note: Cleared when a '1' is written.	
	0	PS_ON_WAKE _EINT	0	ON or WAKE interrupt (Power state transition to ON state) (Rising Edge triggered) Note: Cleared when a '1' is written.	

Register 4012h Interrupt Status 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16403 (4013h) Interrupt Status 3	9	UV_LDO10_EI NT	0	LDO10 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	8	UV_LDO9_EIN T	0	LDO9 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	7	UV_LDO8_EIN T	0	LDO8 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	6	UV_LDO7_EIN T	0	LDO7 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	5	UV_LDO6_EIN T	0	LDO6 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	4	UV_LDO5_EIN T	0	LDO5 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	3	UV_LDO4_EIN T	0	LDO4 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	2	UV_LDO3_EIN T	0	LDO3 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	1	UV_LDO2_EIN T	0	LDO2 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	0	UV_LDO1_EIN T	0	LDO1 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	

Register 4013h Interrupt Status 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16404 (4014h) Interrupt Status 4	9	HC_DC2_EINT	0	DC-DC2 High current interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	8	HC_DC1_EINT	0	DC-DC1 High current interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	7	XTAL_START_EINT	0	Crystal Oscillator Start Failure interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	6	XTAL_TAMPER_EINT	0	Crystal Oscillator Tamper interrupt (Rising and Falling Edge triggered) Note: Cleared when a '1' is written.	
	3	UV_DC4_EINT	0	DC-DC4 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	2	UV_DC3_EINT	0	DC-DC3 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	1	UV_DC2_EINT	0	DC-DC2 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	0	UV_DC1_EINT	0	DC-DC1 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	

Register 4014h Interrupt Status 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16405 (4015h) Interrupt Status 5	11	GP12_EINT	0	GPIO12 interrupt. (Trigger is controlled by GP12_INT_MODE) Note: Cleared when a '1' is written.	
	10	GP11_EINT	0	GPIO11 interrupt. (Trigger is controlled by GP11_INT_MODE) Note: Cleared when a '1' is written.	
	9	GP10_EINT	0	GPIO10 interrupt. (Trigger is controlled by GP10_INT_MODE) Note: Cleared when a '1' is written.	
	8	GP9_EINT	0	GPIO9 interrupt. (Trigger is controlled by GP9_INT_MODE) Note: Cleared when a '1' is written.	
	7	GP8_EINT	0	GPIO8 interrupt. (Trigger is controlled by GP8_INT_MODE) Note: Cleared when a '1' is written.	
	6	GP7_EINT	0	GPIO7 interrupt. (Trigger is controlled by GP7_INT_MODE) Note: Cleared when a '1' is written.	
	5	GP6_EINT	0	GPIO6 interrupt. (Trigger is controlled by GP6_INT_MODE) Note: Cleared when a '1' is written.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4	GP5_EINT	0	GPIO5 interrupt. (Trigger is controlled by GP5_INT_MODE) Note: Cleared when a '1' is written.	
	3	GP4_EINT	0	GPIO4 interrupt. (Trigger is controlled by GP4_INT_MODE) Note: Cleared when a '1' is written.	
	2	GP3_EINT	0	GPIO3 interrupt. (Trigger is controlled by GP3_INT_MODE) Note: Cleared when a '1' is written.	
	1	GP2_EINT	0	GPIO2 interrupt. (Trigger is controlled by GP2_INT_MODE) Note: Cleared when a '1' is written.	
	0	GP1_EINT	0	GPIO1 interrupt. (Trigger is controlled by GP1_INT_MODE) Note: Cleared when a '1' is written.	

Register 4015h Interrupt Status 5

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16407 (4017h) IRQ Config	1	IRQ_OD	1	IRQ pin configuration 0 = CMOS 1 = Open Drain (integrated pull-up)	
	0	IM_IRQ	0	IRQ pin output mask 0 = Normal 1 = IRQ output is masked	

Register 4017h IRQ Config

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16408 (4018h) System Interrupts Mask	15	IM_PS_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	14	IM_TEMP_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	13	IM_GP_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	12	IM_ON_PIN_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	11	IM_WDOG_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	8	IM_AUXADC_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	7	IM_PPM_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	5	IM_RTC_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	1	IM_HC_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	0	IM_UV_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

Register 4018h System Interrupts Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16409 (4019h) Interrupt Status 1 Mask	15	IM_PPM_SYSL O_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	12	IM_ON_PIN_C INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	11	IM_WDOG_TO _EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	8	IM_AUXADC_ DATA_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	7	IM_AUXADC_ DCOMP4_EIN T	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	6	IM_AUXADC_ DCOMP3_EIN T	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	5	IM_AUXADC_ DCOMP2_EIN T	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4	IM_AUXADC_DCOMP1_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	3	IM_RTC_PER_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	2	IM_RTC_ALM_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	1	IM_TEMP_THW_CINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

Register 4019h Interrupt Status 1 Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16410 (401Ah) Interrupt Status 2 Mask	2	IM_PS_POR_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	1	IM_PS_SLEEP_OFF_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	0	IM_PS_ON_WAKE_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

Register 401Ah Interrupt Status 2 Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16411 (401Bh) Interrupt Status 3 Mask	9	IM_UV_LDO10_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	8	IM_UV_LDO9_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	7	IM_UV_LDO8_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6	IM_UV_LDO7_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	5	IM_UV_LDO6_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	4	IM_UV_LDO5_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	3	IM_UV_LDO4_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	2	IM_UV_LDO3_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	1	IM_UV_LDO2_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	0	IM_UV_LDO1_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

Register 401Bh Interrupt Status 3 Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16412 (401Ch) Interrupt Status 4 Mask	9	IM_HC_DC2_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	8	IM_HC_DC1_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	7	IM_XTAL_STARRT_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	3	IM_UV_DC4_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	2	IM_UV_DC3_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1	IM_UV_DC2_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	0	IM_UV_DC1_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

Register 401Ch Interrupt Status 4 Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16413 (401Dh) Interrupt Status 5 Mask	11	IM_GP12_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	10	IM_GP11_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	9	IM_GP10_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	8	IM_GP9_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	7	IM_GP8_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	6	IM_GP7_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	5	IM_GP6_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	4	IM_GP5_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	3	IM_GP4_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	2	IM_GP3_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				Default value is 1 (masked)	
	1	IM_GP2_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	0	IM_GP1_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

Register 401Dh Interrupt Status 5 Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16416 (4020h) RTC Write Counter	15:0	RTC_WR_CNT [15:0]	0000_0000 _0000_0000 0	RTC Write Counter. This random number is updated on every write to the RTC_TIME registers.	

Register 4020h RTC Write Counter

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16417 (4021h) RTC Time 1	15:0	RTC_TIME [15:0]	0000_0000 _0000_0000 0	RTC Seconds counter (MSW) RTC_TIME increments by 1 every second. This is the 16 MSBs.	

Register 4021h RTC Time 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16418 (4022h) RTC Time 2	15:0	RTC_TIME [15:0]	0000_0000 _0000_0000 0	RTC Seconds counter (LSW) RTC_TIME increments by 1 every second. This is the 16 LSBs.	

Register 4022h RTC Time 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16419 (4023h) RTC Alarm 1	15:0	RTC_ALM [15:0]	0000_0000 _0000_0000 0	RTC Alarm time (MSW) 16 MSBs of RTC_ALM	

Register 4023h RTC Alarm 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16420 (4024h) RTC Alarm 2	15:0	RTC_ALM [15:0]	0000_0000 _0000_0000 0	RTC Alarm time (LSW) 16 LSBs of RTC_ALM	

Register 4024h RTC Alarm 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16421 (4025h) RTC Control	15	RTC_VALID	0	RTC Valid status 0 = RTC_TIME has not been set since Power On Reset 1 = RTC_TIME has been written to since Power On Reset	
	14	RTC_SYNC_BUSY	0	RTC Busy status 0 = Normal 1 = Busy The RTC registers should not be written to when RTC_SYNC_BUSY = 1.	
	10	RTC_ALM_ENA	0	RTC Alarm Enable 0 = Disabled 1 = Enabled	
	6:4	RTC_PINT_FREQ [2:0]	000	RTC Periodic Interrupt timeout period 000 = Disabled 001 = 2s 010 = 4s 011 = 8s 100 = 16s 101 = 32s 110 = 64s 111 = 128s	

Register 4025h RTC Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16422 (4026h) RTC Trim	9:0	RTC_TRIM [9:0]	00_0000_0000	RTC frequency trim. Value is a 10bit fixed point <4,6> 2's complement number. MSB Scaling = -8Hz. The register indicates the error (in Hz) with respect to the ideal 32768Hz) of the input crystal frequency. <i>Protected by security key.</i>	

Register 4026h RTC Trim

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16429 (402Dh) AuxADC Data	15:12	AUX_DATA_S RC [3:0]	0000	AUXADC Data Source 1 = GPIO10 2 = GPIO11 3 = GPIO12 5 = Chip Temperature 7 = PVDD voltage All other values are Reserved	
	11:0	AUX_DATA [11:0]	0000_0000 _0000	AUXADC Measurement Data Voltage (mV) = AUX_DATA x 1.465 ChipTemp (°C) = (498 - AUX_DATA) / 1.09	

Register 402Dh AuxADC Data

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16430 (402Eh) AuxADC Control	15	AUX_ENA	0	AUXADC Enable 0 = Disabled 1 = Enabled Note - this bit is reset to 0 when the OFF power state is entered.	
	14	AUX_CVT_EN A	0	AUXADC Conversion Enable 0 = Disabled 1 = Enabled In automatic mode, conversions are enabled by setting this bit. In manual mode (AUX_RATE = 0), setting this bit will initiate a conversion; the bit is reset automatically after each conversion.	
	12	AUX_SLPENA	0	AUXADC SLEEP Enable 0 = Disabled 1 = Controlled by AUX_ENA	
	5:0	AUX_RATE [5:0]	00_0000	AUXADC Conversion Rate 0 = Manual 1 = 2 samples/s 2 = 4 samples/s 3 = 6 samples/s ... 31 = 62 samples/s 32 = Reserved 33 = 16 samples/s 34 = 32 samples/s 35 = 48 samples/s ... 63 = 496 samples/s	

Register 402Eh AuxADC Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16431 (402Fh) AuxADC Source	6	AUX_PVDD_SEL	0	AUXADC PVDD input select 0 = Disable PVDD measurement 1 = Enable PVDD measurement	
	4	AUX_CHIP_TEMP_SEL	0	AUXADC Chip Temp input select 0 = Disable Chip Temp measurement 1 = Enable Chip Temp measurement	
	2	AUX_GPIO12_SEL	0	AUXADC GPIO12 input select 0 = Disable GPIO12 measurement 1 = Enable GPIO12 measurement	
	1	AUX_GPIO11_SEL	0	AUXADC GPIO11 input select 0 = Disable GPIO11 measurement 1 = Enable GPIO11 measurement	
	0	AUX_GPIO10_SEL	0	AUXADC GPIO10 input select 0 = Disable GPIO10 measurement 1 = Enable GPIO10 measurement	

Register 402Fh AuxADC Source

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16432 (4030h) Comparator Control	11	DCOMP4_STS	0	Digital Comparator 4 status 0 = Comparator 4 threshold not detected 1 = Comparator 4 threshold detected (Trigger is controlled by DCMP4_GT)	
	10	DCOMP3_STS	0	Digital Comparator 3 status 0 = Comparator 3 threshold not detected 1 = Comparator 3 threshold detected (Trigger is controlled by DCMP3_GT)	
	9	DCOMP2_STS	0	Digital Comparator 2 status 0 = Comparator 2 threshold not detected 1 = Comparator 2 threshold detected (Trigger is controlled by DCMP2_GT)	
	8	DCOMP1_STS	0	Digital Comparator 1 status 0 = Comparator 1 threshold not detected 1 = Comparator 1 threshold detected (Trigger is controlled by DCMP1_GT)	
	3	DCMP4_ENA	0	Digital Comparator 4 Enable 0 = Disabled 1 = Enabled	
	2	DCMP3_ENA	0	Digital Comparator 3 Enable 0 = Disabled 1 = Enabled	
	1	DCMP2_ENA	0	Digital Comparator 2 Enable 0 = Disabled 1 = Enabled	
	0	DCMP1_ENA	0	Digital Comparator 1 Enable 0 = Disabled 1 = Enabled	

Register 4030h Comparator Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16433 (4031h) Comparator 1	15:13	DCMP1_SRC [2:0]	000	Digital Comparator 1 source select 0 = Reserved 1 = GPIO10 2 = GPIO11 3 = GPIO12 4 = Reserved 5 = Chip Temperature 6 = Reserved 7 = PVDD voltage	
	12	DCMP1_GT	0	Digital Comparator 1 interrupt control 0 = interrupt when less than threshold 1 = interrupt when greater than or equal to threshold	
	11:0	DCMP1_THR [11:0]	0000_0000 _0000	Digital Comparator 1 threshold (12-bit unsigned binary number; coding is the same as AUX_DATA)	

Register 4031h Comparator 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16434 (4032h) Comparator 2	15:13	DCMP2_SRC [2:0]	000	Digital Comparator 2 source select 0 = Reserved 1 = GPIO10 2 = GPIO11 3 = GPIO12 4 = Reserved 5 = Chip Temperature 6 = Reserved 7 = PVDD voltage	
	12	DCMP2_GT	0	Digital Comparator 2 interrupt control 0 = interrupt when less than threshold 1 = interrupt when greater than or equal to threshold	
	11:0	DCMP2_THR [11:0]	0000_0000 _0000	Digital Comparator 2 threshold (12-bit unsigned binary number; coding is the same as AUX_DATA)	

Register 4032h Comparator 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16435 (4033h) Comparator 3	15:13	DCMP3_SRC [2:0]	000	Digital Comparator 3 source select 0 = Reserved 1 = GPIO10 2 = GPIO11 3 = GPIO12 4 = Reserved 5 = Chip Temperature 6 = Reserved 7 = PVDD voltage	
	12	DCMP3_GT	0	Digital Comparator 3 interrupt control 0 = interrupt when less than threshold 1 = interrupt when greater than or equal to threshold	
	11:0	DCMP3_THR [11:0]	0000_0000 _0000	Digital Comparator 3 threshold (12-bit unsigned binary number; coding is the same as AUX_DATA)	

Register 4033h Comparator 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16436 (4034h) Comparator 4	15:13	DCMP4_SRC [2:0]	000	Digital Comparator 4 source select 0 = Backup Battery voltage 1 = GPIO10 2 = GPIO11 3 = GPIO12 4 = Reserved 5 = Chip Temperature 6 = Reserved 7 = PVDD voltage	
	12	DCMP4_GT	0	Digital Comparator 4 interrupt control 0 = interrupt when less than threshold 1 = interrupt when greater than or equal to threshold	
	11:0	DCMP4_THR [11:0]	0000_0000 _0000	Digital Comparator 4 threshold (12-bit unsigned binary number; coding is the same as AUX_DATA)	

Register 4034h Comparator 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16440 (4038h) GPIO1 Control	15	GP1_DIR	1	GPIO1 pin direction 0 = Output 1 = Input	
	14:13	GP1_PULL [1:0]	01	GPIO1 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP1_INT_MOD E	0	GPIO1 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP1_POL=1) or falling edge triggered (if GP1_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP1_PWR_DO M	0	GPIO1 Power Domain select 0 = DBVDD 1 = PMICVDD (LDO12)	
	10	GP1_POL	1	GPIO1 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP1_OD	0	GPIO1 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP1_ENA	0	GPIO1 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3:0	GP1_FN [3:0]	0000	<p>GPIO1 Pin Function</p> <p>Input functions:</p> <ul style="list-style-type: none"> 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) <p>Output functions:</p> <ul style="list-style-type: none"> 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Reserved 7 = Reserved 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset 	

Register 4038h GPIO1 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16441 (4039h) GPIO2 Control	15	GP2_DIR	1	<p>GPIO2 pin direction</p> <ul style="list-style-type: none"> 0 = Output 1 = Input 	
	14:13	GP2_PULL [1:0]	01	<p>GPIO2 Pull-Up / Pull-Down configuration</p> <ul style="list-style-type: none"> 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved 	
	12	GP2_INT_MOD E	0	<p>GPIO2 Interrupt Mode</p> <ul style="list-style-type: none"> 0 = GPIO interrupt is rising edge triggered (if GP2_POL=1) or falling edge triggered (if GP2_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges 	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	11	GP2_PWR_DOMAIN	0	GPIO2 Power Domain select 0 = DBVDD 1 = PMICVDD (LDO12)	
	10	GP2_POL	1	GPIO2 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP2_OD	0	GPIO2 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP2_ENA	0	GPIO2 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP2_FN [3:0]	0000	GPIO2 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Reserved 7 = Reserved 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 4039h GPIO2 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16442 (403Ah) GPIO3 Control	15	GP3_DIR	1	GPIO3 pin direction 0 = Output 1 = Input	
	14:13	GP3_PULL [1:0]	01	GPIO3 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP3_INT_MOD E	0	GPIO3 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP3_POL=1) or falling edge triggered (if GP3_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP3_PWR_DO M	0	GPIO3 Power Domain select 0 = DBVDD 1 = PMICVDD (LDO12)	
	10	GP3_POL	1	GPIO3 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP3_OD	0	GPIO3 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP3_ENA	0	GPIO3 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP3_FN [3:0]	0000	GPIO3 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Reserved 7 = Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 403Ah GPIO3 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16443 (403Bh) GPIO4 Control	15	GP4_DIR	1	GPIO4 pin direction 0 = Output 1 = Input	
	14:13	GP4_PULL [1:0]	01	GPIO4 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP4_INT_MODE	0	GPIO4 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP4_POL=1) or falling edge triggered (if GP4_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP4_PWR_DOMAIN	0	GPIO4 Power Domain select 0 = DBVDD 1 = PVDD	
	10	GP4_POL	1	GPIO4 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP4_OD	0	GPIO4 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP4_ENA	0	GPIO4 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP4_FN [3:0]	0000	GPIO4 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Reserved 7 = Reserved 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 403Bh GPIO4 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16444 (403Ch) GPIO5 Control	15	GP5_DIR	1	GPIO5 pin direction 0 = Output 1 = Input	
	14:13	GP5_PULL [1:0]	01	GPIO5 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP5_INT_MOD E	0	GPIO5 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP5_POL=1) or falling edge triggered (if GP5_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP5_PWR_DO M	0	GPIO5 Power Domain select 0 = DBVDD 1 = PVDD	
	10	GP5_POL	1	GPIO5 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP5_OD	0	GPIO5 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP5_ENA	0	GPIO5 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3:0	GP5_FN [3:0]	0000	<p>GPIO5 Pin Function</p> <p>Input functions:</p> <ul style="list-style-type: none"> 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) <p>Output functions:</p> <ul style="list-style-type: none"> 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Reserved 7 = Reserved 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset 	

Register 403Ch GPIO5 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16445 (403Dh) GPIO6 Control	15	GP6_DIR	1	<p>GPIO6 pin direction</p> <ul style="list-style-type: none"> 0 = Output 1 = Input 	
	14:13	GP6_PULL [1:0]	01	<p>GPIO6 Pull-Up / Pull-Down configuration</p> <ul style="list-style-type: none"> 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved 	
	12	GP6_INT_MODE	0	<p>GPIO6 Interrupt Mode</p> <ul style="list-style-type: none"> 0 = GPIO interrupt is rising edge triggered (if GP6_POL=1) or falling edge triggered (if GP6_POL=0) 1 = GPIO interrupt is triggered on rising and falling 	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				edges	
	11	GP6_PWR_DOMAIN	0	GPIO6 Power Domain select 0 = DBVDD 1 = PVDD	
	10	GP6_POL	1	GPIO6 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP6_OD	0	GPIO6 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP6_ENA	0	GPIO6 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP6_FN [3:0]	0000	GPIO6 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Reserved 7 = Reserved 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 403Dh GPIO6 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16446 (403Eh) GPIO7 Control	15	GP7_DIR	1	GPIO7 pin direction 0 = Output 1 = Input	
	14:13	GP7_PULL [1:0]	01	GPIO7 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP7_INT_MOD E	0	GPIO7 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP7_POL=1) or falling edge triggered (if GP7_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP7_PWR_DO M	0	GPIO7 Power Domain select 0 = DBVDD 1 = PMICVDD (LDO12)	
	10	GP7_POL	1	GPIO7 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP7_OD	0	GPIO7 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP7_ENA	0	GPIO7 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP7_FN [3:0]	0000	GPIO7 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Reserved 7 = Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 403Eh GPIO7 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16447 (403Fh) GPIO8 Control	15	GP8_DIR	1	GPIO8 pin direction 0 = Output 1 = Input	
	14:13	GP8_PULL [1:0]	01	GPIO8 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP8_INT_MODE	0	GPIO8 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP8_POL=1) or falling edge triggered (if GP8_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP8_PWR_DOMAIN	0	GPIO8 Power Domain select 0 = DBVDD 1 = PMICVDD (LDO12)	
	10	GP8_POL	1	GPIO8 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP8_OD	0	GPIO8 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP8_ENA	0	GPIO8 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP8_FN [3:0]	0000	GPIO8 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Reserved 7 = Reserved 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 403Fh GPIO8 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16448 (4040h) GPIO9 Control	15	GP9_DIR	1	GPIO9 pin direction 0 = Output 1 = Input	
	14:13	GP9_PULL [1:0]	01	GPIO9 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP9_INT_MODE	0	GPIO9 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP9_POL=1) or falling edge triggered (if GP9_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP9_PWR_DOMAIN	0	GPIO9 Power Domain select 0 = DBVDD 1 = PMICVDD (LDO12)	
	10	GP9_POL	1	GPIO9 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP9_OD	0	GPIO9 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP9_ENA	0	GPIO9 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP9_FN [3:0]	0000	GPIO9 Pin Function Input functions:	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Reserved 7 = Reserved 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 4040h GPIO9 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16449 (4041h) GPIO10 Control	15	GP10_DIR	1	GPIO10 pin direction 0 = Output 1 = Input	
	14:13	GP10_PULL [1:0]	01	GPIO10 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP10_INT_MODE	0	GPIO10 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP10_POL=1) or falling edge triggered (if GP10_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	11	GP10_PWR_DOMAIN	0	GPIO10 Power Domain select 0 = DBVDD 1 = PVDD	
	10	GP10_POL	1	GPIO10 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP10_OD	0	GPIO10 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP10_ENA	0	GPIO10 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP10_FN [3:0]	0000	GPIO10 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Reserved 7 = Reserved 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 4041h GPIO10 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16450 (4042h) GPIO11 Control	15	GP11_DIR	1	GPIO11 pin direction 0 = Output 1 = Input	
	14:13	GP11_PULL [1:0]	01	GPIO11 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP11_INT_MODE	0	GPIO11 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP11_POL=1) or falling edge triggered (if GP11_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP11_PWR_DOMAIN	0	GPIO11 Power Domain select 0 = DBVDD 1 = PVDD	
	10	GP11_POL	1	GPIO11 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP11_OD	0	GPIO11 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP11_ENA	0	GPIO11 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP11_FN [3:0]	0000	GPIO11 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Reserved 7 = Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 4042h GPIO11 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16451 (4043h) GPIO12 Control	15	GP12_DIR	1	GPIO12 pin direction 0 = Output 1 = Input	
	14:13	GP12_PULL [1:0]	01	GPIO12 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP12_INT_MODE	0	GPIO12 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP12_POL=1) or falling edge triggered (if GP12_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP12_PWR_DOMAIN	0	GPIO12 Power Domain select 0 = DBVDD 1 = PVDD	
	10	GP12_POL	1	GPIO12 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP12_OD	0	GPIO12 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP12_ENA	0	GPIO12 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP12_FN [3:0]	0000	GPIO12 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Reserved 7 = Reserved 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 4043h GPIO12 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16460 (404Ch) Status LED 1	15:14	LED1_SRC [1:0]	11	LED1 Source (Selects the LED1 function.) 00 = Off 01 = Power State Status 10 = Reserved 11 = Manual Mode	
	9:8	LED1_MODE [1:0]	00	LED1 Mode (Controls LED1 in Manual Mode only.) 00 = Off 01 = Constant 10 = Continuous Pulsed 11 = Pulsed Sequence	
	5:4	LED1_SEQ_LEN N [1:0]	10	LED1 Pulse Sequence Length (when LED1_MODE = Pulsed Sequence) 00 = 1 pulse 01 = 2 pulses 10 = 4 pulses 11 = 7 pulses	
	3:2	LED1_DUR [1:0]	01	LED1 On time (when LED1_MODE = Continuous Pulsed or Pulsed Sequence) 00 = 1 second 01 = 250ms 10 = 125ms 11 = 62.5ms	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1:0	LED1_DUTY_CYC [1:0]	10	LED1 Duty Cycle (On:Off ratio) (when LED1_MODE = Continuous Pulsed or Pulsed Sequence) 00 = 1:1 (50% on) 01 = 1:2 (33.3% on) 10 = 1:3 (25% on) 11 = 1:7 (12.5% on)	

Register 404Ch Status LED 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16461 (404Dh) Status LED 2	15:14	LED2_SRC [1:0]	11	LED2 Source (Selects the LED2 function.) 00 = Off 01 = Power State Status 10 = Reserved 11 = Manual Mode	
	9:8	LED2_MODE [1:0]	00	LED2 Mode (Controls LED2 in Manual Mode only.) 00 = Off 01 = Constant 10 = Continuous Pulsed 11 = Pulsed Sequence	
	5:4	LED2_SEQ_LENGTH [1:0]	10	LED2 Pulse Sequence Length (when LED2_MODE = Pulsed Sequence) 00 = 1 pulse 01 = 2 pulses 10 = 4 pulses 11 = 7 pulses	
	3:2	LED2_DUR [1:0]	01	LED2 On time (when LED2_MODE = Continuous Pulsed or Pulsed Sequence) 00 = 1 second 01 = 250ms 10 = 125ms 11 = 62.5ms	
	1:0	LED2_DUTY_CYC [1:0]	10	LED2 Duty Cycle (On:Off ratio) (when LED2_MODE = Continuous Pulsed or Pulsed Sequence) 00 = 1:1 (50% on) 01 = 1:2 (33.3% on) 10 = 1:3 (25% on) 11 = 1:7 (12.5% on)	

Register 404Dh Status LED 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16464 (4050h) DCDC Enable	7	EPE2_ENA	0	EPE2 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in EPE2_STS)	
	6	EPE1_ENA	0	EPE1 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in EPE1_STS)	
	3	DC4_ENA	0	DC-DC4 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in DC4_STS)	
	2	DC3_ENA	0	DC-DC3 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in DC3_STS)	
	1	DC2_ENA	0	DC-DC2 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in DC2_STS)	
	0	DC1_ENA	0	DC_DC1 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in DC1_STS)	

Register 4050h DCDC Enable

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16465 (4051h) LDO Enable	10	LDO11_ENA	0	LDO11 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO11_STS)	
	9	LDO10_ENA	0	LDO10 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO10_STS)	
	8	LDO9_ENA	0	LDO9 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO9_STS)	
	7	LDO8_ENA	0	LDO8 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO8_STS)	
	6	LDO7_ENA	0	LDO7 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO7_STS)	
	5	LDO6_ENA	0	LDO6 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO6_STS)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4	LDO5_ENA	0	LDO5 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO5_STS)	
	3	LDO4_ENA	0	LDO4 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO4_STS)	
	2	LDO3_ENA	0	LDO3 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO3_STS)	
	1	LDO2_ENA	0	LDO2 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO2_STS)	
	0	LDO1_ENA	0	LDO1 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO1_STS)	

Register 4051h LDO Enable

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16466 (4052h) DCDC Status	7	EPE2_STS	0	EPE2 Status 0 = Disabled 1 = Enabled	
	6	EPE1_STS	0	EPE1 Status 0 = Disabled 1 = Enabled	
	3	DC4_STS	0	DC-DC4 Status 0 = Disabled 1 = Enabled	
	2	DC3_STS	0	DC-DC3 Status 0 = Disabled 1 = Enabled	
	1	DC2_STS	0	DC-DC2 Status 0 = Disabled 1 = Enabled	
	0	DC1_STS	0	DC-DC1 Status 0 = Disabled 1 = Enabled	

Register 4052h DCDC Status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16467 (4053h) LDO Status	10	LDO11_STS	0	LDO11 Status 0 = Disabled 1 = Enabled	
	9	LDO10_STS	0	LDO10 Status 0 = Disabled 1 = Enabled	
	8	LDO9_STS	0	LDO9 Status 0 = Disabled 1 = Enabled	
	7	LDO8_STS	0	LDO8 Status 0 = Disabled 1 = Enabled	
	6	LDO7_STS	0	LDO7 Status 0 = Disabled 1 = Enabled	
	5	LDO6_STS	0	LDO6 Status 0 = Disabled 1 = Enabled	
	4	LDO5_STS	0	LDO5 Status 0 = Disabled 1 = Enabled	
	3	LDO4_STS	0	LDO4 Status 0 = Disabled 1 = Enabled	
	2	LDO3_STS	0	LDO3 Status 0 = Disabled 1 = Enabled	
	1	LDO2_STS	0	LDO2 Status 0 = Disabled 1 = Enabled	
	0	LDO1_STS	0	LDO1 Status 0 = Disabled 1 = Enabled	

Register 4053h LDO Status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16468 (4054h) DCDC UV Status	13	DC2_OV_STS	0	DC-DC2 Overvoltage Status 0 = Normal 1 = Overvoltage	
	12	DC1_OV_STS	0	DC-DC1 Overvoltage Status 0 = Normal 1 = Overvoltage	
	9	DC2_HC_STS	0	DC-DC2 High Current Status 0 = Normal 1 = High Current	
	8	DC1_HC_STS	0	DC-DC1 High Current Status 0 = Normal 1 = High Current	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3	DC4_UV_STS	0	DC-DC4 Undervoltage Status 0 = Normal 1 = Undervoltage	
	2	DC3_UV_STS	0	DC-DC3 Undervoltage Status 0 = Normal 1 = Undervoltage	
	1	DC2_UV_STS	0	DC-DC2 Undervoltage Status 0 = Normal 1 = Undervoltage	
	0	DC1_UV_STS	0	DC-DC1 Undervoltage Status 0 = Normal 1 = Undervoltage	

Register 4054h DCDC UV Status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16469 (4055h) LDO UV Status	15	INTLDO_UV_STS	0	LDO13 (Internal LDO) Undervoltage Status 0 = Normal 1 = Undervoltage	
	9	LDO10_UV_STS	0	LDO10 Undervoltage Status 0 = Normal 1 = Undervoltage	
	8	LDO9_UV_STS	0	LDO9 Undervoltage Status 0 = Normal 1 = Undervoltage	
	7	LDO8_UV_STS	0	LDO8 Undervoltage Status 0 = Normal 1 = Undervoltage	
	6	LDO7_UV_STS	0	LDO7 Undervoltage Status 0 = Normal 1 = Undervoltage	
	5	LDO6_UV_STS	0	LDO6 Undervoltage Status 0 = Normal 1 = Undervoltage	
	4	LDO5_UV_STS	0	LDO5 Undervoltage Status 0 = Normal 1 = Undervoltage	
	3	LDO4_UV_STS	0	LDO4 Undervoltage Status 0 = Normal 1 = Undervoltage	
	2	LDO3_UV_STS	0	LDO3 Undervoltage Status 0 = Normal 1 = Undervoltage	
	1	LDO2_UV_STS	0	LDO2 Undervoltage Status 0 = Normal 1 = Undervoltage	
	0	LDO1_UV_STS	0	LDO1 Undervoltage Status 0 = Normal 1 = Undervoltage	

Register 4055h LDO UV Status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16470 (4056h) DC1 Control 1	15:14	DC1_RATE [1:0]	10	DC-DC1 Voltage Ramp rate 00 = 1 step every 32us 01 = 1 step every 16us 10 = 1 step every 8us 11 = Immediate voltage change	
	12	DC1_PHASE	0	DC-DC1 Clock Phase Control 0 = Normal 1 = Inverted	
	7	DC1_FLT	0	DC-DC1 Output float 0 = DC-DC1 output discharged when disabled 1 = DC-DC1 output floating when disabled	
	5:4	DC1_SOFT_START [1:0]	00	DC-DC1 Soft-Start Control (Duration in each of the 8 startup current limiting steps.) 00 = 32us steps 01 = 64us steps 10 = 128us steps 11 = 256us steps	

Register 4056h DC1 Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16471 (4057h) DC1 Control 2	15:14	DC1_ERR_ACTION [1:0]	00	DC-DC1 Error Action (Undervoltage) 00 = Ignore 01 = Shut down converter 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	DC1_HWC_SOURCE [1:0]	00	DC-DC1 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	DC1_HWC_VSEL	0	DC-DC1 Hardware Control Voltage select 0 = Set by DC1_ON_VSEL 1 = Set by DC1_SLP_VSEL	
	9:8	DC1_HWC_MODE [1:0]	11	DC-DC1 Hardware Control Operating Mode 00 = Forced Continuous Conduction Mode 01 = Disabled 10 = LDO Mode 11 = Hysteretic Mode	
	6:4	DC1_HC_THR [2:0]	000	DC-DC1 High Current threshold 000 = 125mA 001 = 250mA 010 = 375mA 011 = 500mA 100 = 625mA 101 = 750mA 110 = 875mA 111 = 1000mA	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	DC1_HC_IND_ENA	0	DC-DC1 High Current detect enable 0 = Disabled 1 = Enabled	

Register 4057h DC1 Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16472 (4058h) DC1 ON Config	15:13	DC1_ON_SLOT [2:0]	000	DC-DC1 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	9:8	DC1_ON_MODE [1:0]	01	DC-DC1 ON Operating Mode 00 = Forced Continuous Conduction Mode 01 = Auto Mode (Continuous / Discontinuous Conduction with Pulse-Skipping) 10 = LDO Mode 11 = Hysteretic Mode	
	6:2	DC1_ON_VSEL [6:2]	0_0000	DC-DC1 ON Voltage select DC1_ON_VSEL [6:0] selects the DC-DC1 output voltage from 0.6V to 1.8V in 12.5mV steps. DC1_ON_VSEL [6:2] also exist in OTP memory, controlling the voltage in 50mV steps. DC1_ON_VSEL [6:0] is coded as follows: 00h to 08h = 0.6V 09h = 0.6125V ... 67h = 1.7875V 68h to 7Fh = 1.8V	
	1:0	DC1_ON_VSEL [1:0]	00	DC-DC1 ON Voltage select DC1_ON_VSEL [6:0] selects the DC-DC1 output voltage from 0.6V to 1.8V in 12.5mV steps. See DC1_ON_VSEL [6:2] for definition.	

Register 4058h DC1 ON Config

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16473 (4059h) DC1 SLEEP Control	15:13	DC1_SLP_SLOT [2:0]	000	DC-DC1 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If DC-DC1 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the converter enters its SLEEP condition.	
	9:8	DC1_SLP_MODE [1:0]	11	DC-DC1 SLEEP Operating Mode 00 = Forced Continuous Conduction Mode 01 = Auto Mode (Continuous / Discontinuous Conduction with Pulse-Skipping) 10 = LDO Mode 11 = Hysteretic Mode	
	6:0	DC1_SLP_VOLTAGE [6:0]	000_0000	DC-DC1 SLEEP Voltage select 0.6V to 1.8V in 12.5mV steps 00h to 08h = 0.6V 09h = 0.6125V ... 67h = 1.7875V 68h to 7Fh = 1.8V	

Register 4059h DC1 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16474 (405Ah) DC1 DVS Control	12:11	DC1_DVS_SOURCE [1:0]	00	DC-DC1 DVS Control Source 00 = Disabled 01 = Enabled 10 = Controlled by Hardware DVS1 11 = Controlled by Hardware DVS2	
	6:0	DC1_DVS_VOLTAGE [6:0]	000_0000	DC-DC1 DVS Voltage select 0.6V to 1.8V in 12.5mV steps 00h to 08h = 0.6V 09h = 0.6125V ... 67h = 1.7875V 68h to 7Fh = 1.8V	

Register 405Ah DC1 DVS Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16475 (405Bh) DC2 Control 1	15:14	DC2_RATE [1:0]	10	DC-DC2 Voltage Ramp rate 00 = 1 step every 32us 01 = 1 step every 16us 10 = 1 step every 8us 11 = Immediate voltage change	
	12	DC2_PHASE	1	DC-DC2 Clock Phase Control 0 = Normal 1 = Inverted	
	7	DC2_FLT	0	DC-DC2 Output float 0 = DC-DC2 output discharged when disabled 1 = DC-DC2 output floating when disabled	
	5:4	DC2_SOFT_START [1:0]	00	DC-DC2 Soft-Start Control (Duration in each of the 8 startup current limiting steps.) 00 = 32us steps 01 = 64us steps 10 = 128us steps 11 = 256us steps	

Register 405Bh DC2 Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16476 (405Ch) DC2 Control 2	15:14	DC2_ERR_ACTION [1:0]	00	DC-DC2 Error Action (Undervoltage) 00 = Ignore 01 = Shut down converter 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	DC2_HWC_SOURCE [1:0]	00	DC-DC2 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	DC2_HWC_VSEL	0	DC-DC2 Hardware Control Voltage select 0 = Set by DC2_ON_VSEL 1 = Set by DC2_SLP_VSEL	
	9:8	DC2_HWC_MODE [1:0]	11	DC-DC2 Hardware Control Operating Mode 00 = Forced Continuous Conduction Mode 01 = Disabled 10 = LDO Mode 11 = Hysteretic Mode	
	6:4	DC2_HC_THR [2:0]	000	DC-DC2 High Current threshold 000 = 250mA 001 = 500mA 010 = 750mA 011 = 1000mA 100 = 1250mA 101 = 1500mA 110 = 1750mA 111 = 2000mA	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	DC2_HC_IND_ENA	0	DC-DC2 High Current detect enable 0 = Disabled 1 = Enabled	

Register 405Ch DC2 Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16477 (405Dh) DC2 ON Config	15:13	DC2_ON_SLOT [2:0]	000	DC-DC2 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	9:8	DC2_ON_MODE [1:0]	01	DC-DC2 ON Operating Mode 00 = Forced Continuous Conduction Mode 01 = Auto Mode (Continuous / Discontinuous Conduction with Pulse-Skipping) 10 = LDO Mode 11 = Hysteretic Mode	
	6:2	DC2_ON_VSEL [6:2]	0_0000	DC-DC2 ON Voltage select DC2_ON_VSEL [6:0] selects the DC-DC2 output voltage from 0.6V to 1.8V in 12.5mV steps. DC2_ON_VSEL [6:2] also exist in OTP memory, controlling the voltage in 50mV steps. DC2_ON_VSEL [6:0] is coded as follows: 00h to 08h = 0.6V 09h = 0.6125V ... 67h = 1.7875V 68h to 7Fh = 1.8V	
	1:0	DC2_ON_VSEL [1:0]	00	DC-DC2 ON Voltage select DC2_ON_VSEL [6:0] selects the DC-DC2 output voltage from 0.6V to 1.8V in 12.5mV steps. See DC2_ON_VSEL [6:2] for definition.	

Register 405Dh DC2 ON Config

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16478 (405Eh) DC2 SLEEP Control	15:13	DC2_SLP_SLO T [2:0]	000	DC-DC2 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If DC-DC2 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the converter enters its SLEEP condition.	
	9:8	DC2_SLP_MO DE [1:0]	11	DC-DC2 SLEEP Operating Mode 00 = Forced Continuous Conduction Mode 01 = Auto Mode (Continuous / Discontinuous Conduction with Pulse-Skipping) 10 = LDO Mode 11 = Hysteretic Mode	
	6:0	DC2_SLP_VSE L [6:0]	000_0000	DC-DC2 SLEEP Voltage select 0.6V to 1.8V in 12.5mV steps 00h to 08h = 0.6V 09h = 0.6125V ... 67h = 1.7875V 68h to 7Fh = 1.8V	

Register 405Eh DC2 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16479 (405Fh) DC2 DVS Control	12:11	DC2_DVS_SR C [1:0]	00	DC-DC2 DVS Control Source 00 = Disabled 01 = Enabled 10 = Controlled by Hardware DVS1 11 = Controlled by Hardware DVS2	
	6:0	DC2_DVS_VS EL [6:0]	000_0000	DC-DC2 DVS Voltage select 0.6V to 1.8V in 12.5mV steps 00h to 08h = 0.6V 09h = 0.6125V ... 67h = 1.7875V 68h to 7Fh = 1.8V	

Register 405Fh DC2 DVS Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16480 (4060h) DC3 Control 1	12	DC3_PHASE	0	DC-DC3 Clock Phase Control 0 = Normal 1 = Inverted	
	7	DC3_FLT	0	DC-DC3 Output float 0 = DC-DC3 output discharged when disabled 1 = DC-DC3 output floating when disabled	
	5:4	DC3_SOFT_START [1:0]	01	DC-DC3 Soft-Start Control (Duration in each of the 3 intermediate startup current limiting steps.) 00 = Immediate start-up 01 = 512us steps 10 = 4.096ms steps 11 = 32.768ms steps	
	3:2	DC3_STNBY_LIM [1:0]	01	DC-DC3 Current Limit Sets the maximum DC output current in Hysteretic Mode. Typical values shown below. 00 = 50mA 01 = 100mA 10 = 200mA 11 = 400mA <i>Protected by security key.</i>	

Register 4060h DC3 Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16481 (4061h) DC3 Control 2	15:14	DC3_ERR_ACTION [1:0]	00	DC-DC3 Error Action (Undervoltage) 00 = Ignore 01 = Shut down converter 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	DC3_HWC_SOURCE [1:0]	00	DC-DC3 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	DC3_HWC_VSEL	0	DC-DC3 Hardware Control Voltage select 0 = Set by DC3_ON_VSEL 1 = Set by DC3_SLP_VSEL	
	9:8	DC3_HWC_MODE [1:0]	11	DC-DC3 Hardware Control Operating Mode 00 = Forced Continuous Conduction Mode 01 = Disabled 10 = LDO Mode 11 = Hysteretic Mode	
	7	DC3_OVP	0	DC-DC3 Overvoltage Protection 0 = Disabled 1 = Enabled	

Register 4061h DC3 Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16482 (4062h) DC3 ON Config	15:13	DC3_ON_SLOT [2:0]	000	DC-DC3 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	9:8	DC3_ON_MODE [1:0]	01	DC-DC3 ON Operating Mode 00 = Forced Continuous Conduction Mode 01 = Forced Continuous Conduction Mode 10 = LDO Mode 11 = Hysteretic Mode	
	6:2	DC3_ON_VSEL [6:2]	0_0000	DC-DC3 ON Voltage select DC3_ON_VSEL [6:0] selects the DC-DC3 output voltage from 0.85V to 3.4V in 25mV steps. DC3_ON_VSEL [6:2] also exist in OTP memory, controlling the voltage in 100mV steps. DC3_ON_VSEL [6:0] is coded as follows: 00h = 0.85V 01h = 0.875V ... 65h = 3.375V 66h to 7Fh = 3.4V	
	1:0	DC3_ON_VSEL [1:0]	00	DC-DC3 ON Voltage select DC3_ON_VSEL [6:0] selects the DC-DC3 output voltage from 0.85V to 3.4V in 25mV steps. See DC3_ON_VSEL [6:2] for definition.	

Register 4062h DC3 ON Config

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16483 (4063h) DC3 SLEEP Control	15:13	DC3_SLP_SLO T [2:0]	000	DC-DC3 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If DC-DC3 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the converter enters its SLEEP condition.	
	9:8	DC3_SLP_MO DE [1:0]	11	DC-DC3 SLEEP Operating Mode 00 = Forced Continuous Conduction Mode 01 = Forced Continuous Conduction Mode 10 = LDO Mode 11 = Hysteretic Mode	
	6:0	DC3_SLP_VSE L [6:0]	000_0000	DC-DC3 SLEEP Voltage select 0.85V to 3.4V in 25mV steps 00h = 0.85V 01h = 0.875V ... 65h = 3.375V 66h to 7Fh = 3.4V	

Register 4063h DC3 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16488 (4068h) LDO1 Control	15:14	LDO1_ERR_A CT [1:0]	00	LDO1 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	LDO1_HWC_S RC [1:0]	00	LDO1 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	LDO1_HWC_V SEL	0	LDO1 Hardware Control Voltage select 0 = Set by LDO1_ON_VSEL 1 = Set by LDO1_SLP_VSEL	
	9:8	LDO1_HWC_M ODE [1:0]	10	LDO1 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO1_ON_MODE	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	7	LDO1_FLT	0	LDO1 Output float 0 = LDO1 output discharged when disabled 1 = LDO1 output floating when disabled	
	6	LDO1_SWI	0	LDO1 Switch Mode 0 = LDO mode 1 = Switch mode	
	0	LDO1_LP_MODE	0	LDO1 Low Power Mode Select 0 = 50mA (reduced quiescent current) 1 = 20mA (minimum quiescent current) Selects which Low Power mode is used in ON, SLEEP, or under HWC modes.	

Register 4068h LDO1 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16489 (4069h) LDO1 ON Control	15:13	LDO1_ON_SLOT [2:0]	000	LDO1 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	8	LDO1_ON_MODE	0	LDO1 ON Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO1_ON_VOLTAGE [4:0]	0_0000	LDO1 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V	

Register 4069h LDO1 ON Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16490 (406Ah) LDO1 SLEEP Control	15:13	LDO1_SLP_SLOT [2:0]	000	LDO1 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO1 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.	
	8	LDO1_SLP_MODE	1	LDO1 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO1_SLP_VSEL [4:0]	0_0000	LDO1 SLEEP Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V	

Register 406Ah LDO1 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16491 (406Bh) LDO2 Control	15:14	LDO2_ERR_ACT [1:0]	00	LDO2 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	LDO2_HWC_SRC [1:0]	00	LDO2 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	LDO2_HWC_VSEL	0	LDO2 Hardware Control Voltage select 0 = Set by LDO2_ON_VSEL 1 = Set by LDO2_SLP_VSEL	
	9:8	LDO2_HWC_MODE [1:0]	10	LDO2 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO2_ON_MODE	
	7	LDO2_FLT	0	LDO2 Output float 0 = LDO2 output discharged when disabled 1 = LDO2 output floating when disabled	
	6	LDO2_SWI	0	LDO2 Switch Mode 0 = LDO mode 1 = Switch mode	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	LDO2_LP_MODE	0	LDO2 Low Power Mode Select 0 = 50mA (reduced quiescent current) 1 = 20mA (minimum quiescent current) Selects which Low Power mode is used in ON, SLEEP, or under HWC modes.	

Register 406Bh LDO2 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16492 (406Ch) LDO2 ON Control	15:13	LDO2_ON_SLOT [2:0]	000	LDO2 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	8	LDO2_ON_MODE	0	LDO2 ON Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO2_ON_VOLTAGE [4:0]	0_0000	LDO2 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V	

Register 406Ch LDO2 ON Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16493 (406Dh) LDO2 SLEEP Control	15:13	LDO2_SLP_SLOT [2:0]	000	LDO2 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO2 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				enters its SLEEP condition.	
	8	LDO2_SLP_MODE	1	LDO2 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO2_SLP_VSEL [4:0]	0_0000	LDO2 SLEEP Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V	

Register 406Dh LDO2 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16494 (406Eh) LDO3 Control	15:14	LDO3_ERR_ACTION [1:0]	00	LDO3 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	LDO3_HWC_SRC [1:0]	00	LDO3 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	LDO3_HWC_VSEL	0	LDO3 Hardware Control Voltage select 0 = Set by LDO3_ON_VSEL 1 = Set by LDO3_SLP_VSEL	
	9:8	LDO3_HWC_MODE [1:0]	10	LDO3 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO3_ON_MODE	
	7	LDO3_FLT	0	LDO3 Output float 0 = LDO3 output discharged when disabled 1 = LDO3 output floating when disabled	
	6	LDO3_SWI	0	LDO3 Switch Mode 0 = LDO mode 1 = Switch mode	
	0	LDO3_LP_MODE	0	LDO3 Low Power Mode Select 0 = 50mA (reduced quiescent current) 1 = 20mA (minimum quiescent current) Selects which Low Power mode is used in ON, SLEEP, or under HWC modes.	

Register 406Eh LDO3 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16495 (406Fh) LDO3 ON Control	15:13	LDO3_ON_SLOT [2:0]	000	LDO3 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	8	LDO3_ON_MODE	0	LDO3 ON Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO3_ON_VOLTAGE [4:0]	0_0000	LDO3 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V	

Register 406Fh LDO3 ON Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16496 (4070h) LDO3 SLEEP Control	15:13	LDO3_SLP_SLOT [2:0]	000	LDO3 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO3 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.	
	8	LDO3_SLP_MODE	1	LDO3 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	LDO3_SLP_VSEL [4:0]	0_0000	LDO3 SLEEP Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V	

Register 4070h LDO3 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16497 (4071h) LDO4 Control	15:14	LDO4_ERR_ACTION [1:0]	00	LDO4 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	LDO4_HWC_SOURCE [1:0]	00	LDO4 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	LDO4_HWC_VOLTAGE_SELECT	0	LDO4 Hardware Control Voltage select 0 = Set by LDO4_ON_VSEL 1 = Set by LDO4_SLP_VSEL	
	9:8	LDO4_HWC_MODE [1:0]	10	LDO4 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO4_ON_MODE	
	7	LDO4_FLT	0	LDO4 Output float 0 = LDO4 output discharged when disabled 1 = LDO4 output floating when disabled	
	6	LDO4_SWI	0	LDO4 Switch Mode 0 = LDO mode 1 = Switch mode	
	0	LDO4_LP_MODE	0	LDO4 Low Power Mode Select 0 = 50mA (reduced quiescent current) 1 = 20mA (minimum quiescent current) Selects which Low Power mode is used in ON, SLEEP, or under HWC modes.	

Register 4071h LDO4 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16498 (4072h) LDO4 ON Control	15:13	LDO4_ON_SLOT [2:0]	000	LDO4 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	8	LDO4_ON_MODE	0	LDO4 ON Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO4_ON_VOLTAGE [4:0]	0_0000	LDO4 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V	

Register 4072h LDO4 ON Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16499 (4073h) LDO4 SLEEP Control	15:13	LDO4_SLP_SLOT [2:0]	000	LDO4 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO4 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.	
	8	LDO4_SLP_MODE	1	LDO4 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	LDO4_SLP_VSEL [4:0]	0_0000	LDO4 SLEEP Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V	

Register 4073h LDO4 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16500 (4074h) LDO5 Control	15:14	LDO5_ERR_ACT [1:0]	00	LDO5 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	LDO5_HWC_SRC [1:0]	00	LDO5 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	LDO5_HWC_VSEL	0	LDO5 Hardware Control Voltage select 0 = Set by LDO5_ON_VSEL 1 = Set by LDO5_SLP_VSEL	
	9:8	LDO5_HWC_MODE [1:0]	10	LDO5 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO5_ON_MODE	
	7	LDO5_FLT	0	LDO5 Output float 0 = LDO5 output discharged when disabled 1 = LDO5 output floating when disabled	
	6	LDO5_SWI	0	LDO5 Switch Mode 0 = LDO mode 1 = Switch mode	
	0	LDO5_LP_MODE	0	LDO5 Low Power Mode Select 0 = 50mA (reduced quiescent current) 1 = 20mA (minimum quiescent current) Selects which Low Power mode is used in ON, SLEEP, or under HWC modes.	

Register 4074h LDO5 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16501 (4075h) LDO5 ON Control	15:13	LDO5_ON_SLOT [2:0]	000	LDO5 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	8	LDO5_ON_MODE	0	LDO5 ON Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO5_ON_VOLTAGE [4:0]	0_0000	LDO5 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V	

Register 4075h LDO5 ON Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16502 (4076h) LDO5 SLEEP Control	15:13	LDO5_SLP_SLOT [2:0]	000	LDO5 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO5 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.	
	8	LDO5_SLP_MODE	1	LDO5 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	LDO5_SLP_VSEL [4:0]	0_0000	LDO5 SLEEP Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V	

Register 4076h LDO5 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16503 (4077h) LDO6 Control	15:14	LDO6_ERR_ACTION [1:0]	00	LDO6 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	LDO6_HWC_SOURCE [1:0]	00	LDO6 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	LDO6_HWC_VSEL	0	LDO6 Hardware Control Voltage select 0 = Set by LDO6_ON_VSEL 1 = Set by LDO6_SLP_VSEL	
	9:8	LDO6_HWC_MODE [1:0]	10	LDO6 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO6_ON_MODE	
	7	LDO6_FLT	0	LDO6 Output float 0 = LDO6 output discharged when disabled 1 = LDO6 output floating when disabled	
	6	LDO6_SWI	0	LDO6 Switch Mode 0 = LDO mode 1 = Switch mode	
	0	LDO6_LP_MODE	0	LDO6 Low Power Mode Select 0 = 50mA (reduced quiescent current) 1 = 20mA (minimum quiescent current) Selects which Low Power mode is used in ON, SLEEP, or under HWC modes.	

Register 4077h LDO6 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16504 (4078h) LDO6 ON Control	15:13	LDO6_ON_SLOT [2:0]	000	LDO6 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	8	LDO6_ON_MODE	0	LDO6 ON Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO6_ON_VOLTAGE [4:0]	0_0000	LDO6 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V	

Register 4078h LDO6 ON Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16505 (4079h) LDO6 SLEEP Control	15:13	LDO6_SLP_SLOT [2:0]	000	LDO6 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO6 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.	
	8	LDO6_SLP_MODE	1	LDO6 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	LDO6_SLP_VSEL [4:0]	0_0000	LDO6 SLEEP Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V	

Register 4079h LDO6 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16506 (407Ah) LDO7 Control	15:14	LDO7_ERR_ACT [1:0]	00	LDO7 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	LDO7_HWC_SRC [1:0]	00	LDO7 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	LDO7_HWC_VSEL	0	LDO7 Hardware Control Voltage select 0 = Set by LDO7_ON_VSEL 1 = Set by LDO7_SLP_VSEL	
	9:8	LDO7_HWC_MODE [1:0]	10	LDO7 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO7_ON_MODE	
	7	LDO7_FLT	0	LDO7 Output float 0 = LDO7 output discharged when disabled 1 = LDO7 output floating when disabled	
	6	LDO7_SWI	0	LDO7 Switch Mode 0 = LDO mode 1 = Switch mode	

Register 407Ah LDO7 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16507 (407Bh) LDO7 ON Control	15:13	LDO7_ON_SLOT [2:0]	000	LDO7 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	8	LDO7_ON_MODE	0	LDO7 ON Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO7_ON_VOLTAGE [4:0]	0_0000	LDO7 ON Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V ... 0Ch = 1.60V 0Dh = 1.70V ... 1Eh = 3.40V 1Fh = 3.50V	

Register 407Bh LDO7 ON Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16508 (407Ch) LDO7 SLEEP Control	15:13	LDO7_SLP_SLOT [2:0]	000	LDO7 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO7 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.	
	8	LDO7_SLP_MODE	1	LDO7 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	LDO7_SLP_VSEL [4:0]	0_0000	LDO7 SLEEP Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V ... 0Ch = 1.60V 0Dh = 1.70V ... 1Eh = 3.40V 1Fh = 3.50V	

Register 407Ch LDO7 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16509 (407Dh) LDO8 Control	15:14	LDO8_ERR_ACT [1:0]	00	LDO8 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	LDO8_HWC_SRC [1:0]	00	LDO8 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	LDO8_HWC_VSEL	0	LDO8 Hardware Control Voltage select 0 = Set by LDO8_ON_VSEL 1 = Set by LDO8_SLP_VSEL	
	9:8	LDO8_HWC_MODE [1:0]	10	LDO8 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO8_ON_MODE	
	7	LDO8_FLT	0	LDO8 Output float 0 = LDO8 output discharged when disabled 1 = LDO8 output floating when disabled	
	6	LDO8_SWI	0	LDO8 Switch Mode 0 = LDO mode 1 = Switch mode	

Register 407Dh LDO8 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16510 (407Eh) LDO8 ON Control	15:13	LDO8_ON_SLOT [2:0]	000	LDO8 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	8	LDO8_ON_MODE	0	LDO8 ON Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO8_ON_VOLTAGE [4:0]	0_0000	LDO8 ON Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V ... 0Ch = 1.60V 0Dh = 1.70V ... 1Eh = 3.40V 1Fh = 3.50V	

Register 407Eh LDO8 ON Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16511 (407Fh) LDO8 SLEEP Control	15:13	LDO8_SLP_SLOT [2:0]	000	LDO8 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO8 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.	
	8	LDO8_SLP_MODE	1	LDO8 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	LDO8_SLP_VSEL [4:0]	0_0000	LDO8 SLEEP Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V ... 0Ch = 1.60V 0Dh = 1.70V ... 1Eh = 3.40V 1Fh = 3.50V	

Register 407Fh LDO8 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16512 (4080h) LDO9 Control	15:14	LDO9_ERR_ACT [1:0]	00	LDO9 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	LDO9_HWC_SRC [1:0]	00	LDO9 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	LDO9_HWC_VSEL	0	LDO9 Hardware Control Voltage select 0 = Set by LDO9_ON_VSEL 1 = Set by LDO9_SLP_VSEL	
	9:8	LDO9_HWC_MODE [1:0]	10	LDO9 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO9_ON_MODE	
	7	LDO9_FLT	0	LDO9 Output float 0 = LDO9 output discharged when disabled 1 = LDO9 output floating when disabled	
	6	LDO9_SWI	0	LDO9 Switch Mode 0 = LDO mode 1 = Switch mode	

Register 4080h LDO9 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16513 (4081h) LDO9 ON Control	15:13	LDO9_ON_SLOT [2:0]	000	LDO9 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	8	LDO9_ON_MODE	0	LDO9 ON Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO9_ON_VOLTAGE [4:0]	0_0000	LDO9 ON Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V ... 0Ch = 1.60V 0Dh = 1.70V ... 1Eh = 3.40V 1Fh = 3.50V	

Register 4081h LDO9 ON Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16514 (4082h) LDO9 SLEEP Control	15:13	LDO9_SLP_SLOT [2:0]	000	LDO9 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO9 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.	
	8	LDO9_SLP_MODE	1	LDO9 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	LDO9_SLP_VSEL [4:0]	0_0000	LDO9 SLEEP Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V ... 0Ch = 1.60V 0Dh = 1.70V ... 1Eh = 3.40V 1Fh = 3.50V	

Register 4082h LDO9 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16515 (4083h) LDO10 Control	15:14	LDO10_ERR_ACT [1:0]	00	LDO10 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	LDO10_HWC_SRC [1:0]	00	LDO10 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	LDO10_HWC_VSEL	0	LDO10 Hardware Control Voltage select 0 = Set by LDO10_ON_VSEL 1 = Set by LDO10_SLP_VSEL	
	9:8	LDO10_HWC_MODE [1:0]	10	LDO10 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO10_ON_MODE	
	7	LDO10_FLT	0	LDO10 Output float 0 = LDO10 output discharged when disabled 1 = LDO10 output floating when disabled	
	6	LDO10_SWI	0	LDO10 Switch Mode 0 = LDO mode 1 = Switch mode	

Register 4083h LDO10 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16516 (4084h) LDO10 ON Control	15:13	LDO10_ON_SLOT [2:0]	000	LDO10 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	8	LDO10_ON_MODE	0	LDO10 ON Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO10_ON_VOLTAGE_SEL [4:0]	0_0000	LDO10 ON Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V ... 0Ch = 1.60V 0Dh = 1.70V ... 1Eh = 3.40V 1Fh = 3.50V	

Register 4084h LDO10 ON Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16517 (4085h) LDO10 SLEEP Control	15:13	LDO10_SLP_SLOT [2:0]	000	LDO10 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO10 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.	
	8	LDO10_SLP_MODE	1	LDO10 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	LDO10_SLP_VSEL [4:0]	0_0000	LDO10 SLEEP Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V ... 0Ch = 1.60V 0Dh = 1.70V ... 1Eh = 3.40V 1Fh = 3.50V	

Register 4085h LDO10 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16519 (4087h) LDO11 ON Control	15:13	LDO11_ON_SLOT [2:0]	000	LDO11 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	12	LDO11_FRCE NA	0	LDO11 Force Enable (allows LDO11 to be enabled at all times in the OFF, ON and SLEEP states) 0 = Disabled 1 = Enabled	
	7	LDO11_VSEL_ SRC	0	LDO11 Voltage Select source 0 = Normal (LDO11 settings) 1 = Same as DC-DC Converter 1	
	3:0	LDO11_ON_VSEL [3:0]	0000	LDO11 ON Voltage select 0.80V to 1.55V in 50mV steps 0h = 0.80V 1h = 0.85V 2h = 0.90V ... Eh = 1.50V Fh = 1.55V	

Register 4087h LDO11 ON Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16520 (4088h) LDO11 SLEEP Control	15:13	LDO11_SLP_S LOT [2:0]	000	LDO11 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO11 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.	
	3:0	LDO11_SLP_V SEL [3:0]	0000	LDO11 SLEEP Voltage select 0.80V to 1.55V in 50mV steps 0h = 0.80V 1h = 0.85V 2h = 0.90V ... Eh = 1.50V Fh = 1.55V	

Register 4088h LDO11 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16521 (4089h) EPE1 Control	15:13	EPE1_ON_S LOT [2:0]	000	EPE1 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	12:11	EPE1_HWC_S RC [1:0]	00	EPE1 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	8	EPE1_HWCEN A	0	EPE1 Hardware Control Enable 0 = EPE1 is controlled by EPE1_ENA (Hardware Control input(s) are ignored) 1 = EPE1 is controlled by HWC inputs (Hardware Control input(s) force EPE1 to be de-asserted)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	7:5	EPE1_SLP_SLOTT [2:0]	000	EPE1 SLEEP Slot select 000 = No action 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = No action 111 = No action	

Register 4089h EPE1 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16522 (408Ah) EPE2 Control	15:13	EPE2_ON_SLOTT [2:0]	000	EPE2 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	12:11	EPE2_HWC_SRC [1:0]	00	EPE2 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	8	EPE2_HWCEN A	0	EPE2 Hardware Control Enable 0 = EPE2 is controlled by EPE2_ENA (Hardware Control input(s) are ignored) 1 = EPE2 is controlled by HWC inputs (Hardware Control input(s) force EPE2 to be de-asserted)	
	7:5	EPE2_SLP_SLOTT [2:0]	000	EPE2 SLEEP Slot select 000 = No action 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = No action 111 = No action	

Register 408Ah EPE2 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16526 (408Eh) Power Good Source 1	3	DC4_OK	0	DC-DC4 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	2	DC3_OK	1	DC-DC3 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	1	DC2_OK	1	DC-DC2 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	0	DC1_OK	1	DC-DC1 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	

Register 408Eh Power Good Source 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16527 (408Fh) Power Good Source 2	9	LDO10_OK	1	LDO10 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	8	LDO9_OK	1	LDO9 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	7	LDO8_OK	1	LDO8 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	6	LDO7_OK	1	LDO7 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	5	LDO6_OK	1	LDO6 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	4	LDO5_OK	1	LDO5 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	3	LDO4_OK	1	LDO4 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	2	LDO3_OK	1	LDO3 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	1	LDO2_OK	1	LDO2 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	0	LDO1_OK	1	LDO1 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	

Register 408Fh Power Good Source 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16528 (4090h) Clock Control 1	15	CLKOUT_ENA	0	CLKOUT output enable 0 = Disabled 1 = Enabled <i>Protected by security key.</i>	
	13	CLKOUT_OD	0	CLKOUT pin configuration 0 = CMOS 1 = Open Drain	
	10:8	CLKOUT_SLOT [2:0]	000	CLKOUT output enable ON slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Do not enable 111 = Do not enable	
	6:4	CLKOUT_SLEEP_SLOT [2:0]	000	CLKOUT output SLEEP slot select 000 = Controlled by CLKOUT_ENA 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = Controlled by CLKOUT_ENA 111 = Controlled by CLKOUT_ENA	

Register 4090h Clock Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16529 (4091h) Clock Control 2	15	XTAL_INH	0	Crystal Start-Up Inhibit 0 = Disabled 1 = Enabled When XTAL_INH=0, the internal RC oscillator will provide CLKOUT until the crystal oscillator is valid. When XTAL_INH=1, the 'ON' transition is inhibited until the crystal oscillator is valid.	
	12	XTAL_BACKUP	1	Selects the RTC and 32.768kHz oscillator in BACKUP state 0 = RTC unclocked in BACKUP 1 = RTC maintained in BACKUP	

Register 4091h Clock Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30720 (7800h) Unique ID 1	15:0	UNIQUE_ID [15:0]	0000_0000_0000_0000 0	Unique ID, Word 7	

Register 7800h Unique ID 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30721 (7801h) Unique ID 2	15:0	UNIQUE_ID [15:0]	0000_0000 _0000_000 0	Unique ID, Word 6	

Register 7801h Unique ID 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30722 (7802h) Unique ID 3	15:0	UNIQUE_ID [15:0]	0000_0000 _0000_000 0	Unique ID, Word 5	

Register 7802h Unique ID 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30723 (7803h) Unique ID 4	15:0	UNIQUE_ID [15:0]	0000_0000 _0000_000 0	Unique ID, Word 4	

Register 7803h Unique ID 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30724 (7804h) Unique ID 5	15:0	UNIQUE_ID [15:0]	0000_0000 _0000_000 0	Unique ID, Word 3	

Register 7804h Unique ID 5

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30725 (7805h) Unique ID 6	15:0	UNIQUE_ID [15:0]	0000_0000 _0000_000 0	Unique ID, Word 2	

Register 7805h Unique ID 6

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30726 (7806h) Unique ID 7	15:0	UNIQUE_ID [15:0]	0000_0000 _0000_000 0	Unique ID, Word 1	

Register 7806h Unique ID 7

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30727 (7807h) Unique ID 8	15:0	UNIQUE_ID [15:0]	0000_0000 _0000_000 0	Unique ID, Word 0	

Register 7807h Unique ID 8

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30736 (7810h) Customer OTP ID	14:1	OTP_CUST_ID [13:0]	00_0000_0 000_0000	This field is checked when an 'ON' transition is requested. A non-zero value is used to confirm valid data.	
	0	OTP_CUST_FINAL	0	If OTP_CUST_FINAL is set in the OTP and also set in the DCRW, then no further Writes are possible to the OTP.	

Register 7810h Customer OTP ID

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30737 (7811h) DC1 OTP Control	15:13	DC2_ON_SLOT [2:0]	000	DC-DC2 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	12:8	DC2_ON_VSEL [6:2]	0_0000	DC-DC2 ON Voltage select DC2_ON_VSEL [6:0] selects the DC-DC2 output voltage from 0.6V to 1.8V in 12.5mV steps. DC2_ON_VSEL [6:2] controls the voltage in 50mV steps. DC2_ON_VSEL [6:0] is coded as follows: 00h to 08h = 0.6V 09h = 0.6125V ... 67h = 1.7875V 68h to 7Fh = 1.8V	
	7:5	DC1_ON_SLOT [2:0]	000	DC-DC1 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	4:0	DC1_ON_VSEL [6:2]	0_0000	DC-DC1 ON Voltage select DC1_ON_VSEL [6:0] selects the DC-DC1 output voltage from 0.6V to 1.8V in 12.5mV steps. DC1_ON_VSEL [6:2] controls the voltage in 50mV steps. DC1_ON_VSEL [6:0] is coded as follows: 00h to 08h = 0.6V 09h = 0.6125V ... 67h = 1.7875V 68h to 7Fh = 1.8V	

Register 7811h DC1 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30738 (7812h) DC2 OTP Control	15:13	DC4_ON_SLOT [2:0]	000	DC-DC4 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	12:8	DC4_ON_VSEL [6:2]	0_0000	DC-DC4 ON Voltage select DC4_ON_VSEL [6:0] selects the DC-DC3 output voltage from 0.85V to 3.4V in 25mV steps. DC4_ON_VSEL [6:2] controls the voltage in 100mV steps. DC4_ON_VSEL [6:0] is coded as follows: 00h = 0.85V 01h = 0.875V ... 65h = 3.375V 66h to 7Fh = 3.4V	
	7:5	DC3_ON_SLOT [2:0]	000	DC-DC3 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	4:0	DC3_ON_VSEL [6:2]	0_0000	DC-DC3 ON Voltage select DC3_ON_VSEL [6:0] selects the DC-DC3 output voltage from 0.85V to 3.4V in 25mV steps. DC3_ON_VSEL [6:2] controls the voltage in 100mV steps. DC3_ON_VSEL [6:0] is coded as follows: 00h = 0.85V 01h = 0.875V ... 65h = 3.375V 66h to 7Fh = 3.4V	

Register 7812h DC2 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30739 (7813h) DC3 OTP Control	15	DC4_PHASE	0	DC-DC4 Clock Phase Control 0 = Normal 1 = Inverted	
	14	DC3_PHASE	0	DC-DC3 Clock Phase Control 0 = Normal 1 = Inverted	
	13	DC2_PHASE	1	DC-DC2 Clock Phase Control 0 = Normal 1 = Inverted	
	12	DC1_PHASE	0	DC-DC1 Clock Phase Control 0 = Normal 1 = Inverted	

Register 7813h DC3 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30740 (7814h) LDO1/2 OTP Control	15:13	LDO2_ON_SL OT [2:0]	000	LDO2 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	12:8	LDO2_ON_VS EL [4:0]	0_0000	LDO2 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V	
	7:5	LDO1_ON_SL OT [2:0]	000	LDO1 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	LDO1_ON_VSEL [4:0]	0_0000	LDO1 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V	

Register 7814h LDO1/2 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30741 (7815h) LDO3/4 OTP Control	15:13	LDO4_ON_SLOT [2:0]	000	LDO4 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	12:8	LDO4_ON_VSEL [4:0]	0_0000	LDO4 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V	
	7:5	LDO3_ON_SLOT [2:0]	000	LDO3 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	LDO3_ON_VSEL [4:0]	0_0000	LDO3 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V	

Register 7815h LDO3/4 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30742 (7816h) LDO5/6 OTP Control	15:13	LDO6_ON_SLOT [2:0]	000	LDO6 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	12:8	LDO6_ON_VSEL [4:0]	0_0000	LDO6 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V	
	7:5	LDO5_ON_SLOT [2:0]	000	LDO5 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	LDO5_ON_VSEL [4:0]	0_0000	LDO5 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V ... 0Eh = 1.60V 0Fh = 1.70V ... 1Eh = 3.20V 1Fh = 3.30V	

Register 7816h LDO5/6 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30743 (7817h) LDO7/8 OTP Control	15:13	LDO8_ON_SLOT [2:0]	000	LDO8 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	12:8	LDO8_ON_VSEL [4:0]	0_0000	LDO8 ON Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V ... 0Ch = 1.60V 0Dh = 1.70V ... 1Eh = 3.40V 1Fh = 3.50V	
	7:5	LDO7_ON_SLOT [2:0]	000	LDO7 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	LDO7_ON_VSEL [4:0]	0_0000	LDO7 ON Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V ... 0Ch = 1.60V 0Dh = 1.70V ... 1Eh = 3.40V 1Fh = 3.50V	

Register 7817h LDO7/8 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30744 (7818h) LDO9/10 OTP Control	15:13	LDO10_ON_SLOT [2:0]	000	LDO10 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	12:8	LDO10_ON_VSEL [4:0]	0_0000	LDO10 ON Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V ... 0Ch = 1.60V 0Dh = 1.70V ... 1Eh = 3.40V 1Fh = 3.50V	
	7:5	LDO9_ON_SLOT [2:0]	000	LDO9 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	LDO9_ON_VSEL [4:0]	0_0000	LDO9 ON Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V ... 0Ch = 1.60V 0Dh = 1.70V ... 1Eh = 3.40V 1Fh = 3.50V	

Register 7818h LDO9/10 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30745 (7819h) LDO11/EPE Control	15:13	LDO11_ON_SLOT [2:0]	000	LDO11 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	11:8	LDO11_ON_VSEL [3:0]	0000	LDO11 ON Voltage select 0.80V to 1.55V in 50mV steps 0h = 0.80V 1h = 0.85V 2h = 0.90V ... Eh = 1.50V Fh = 1.55V	
	7:5	EPE2_ON_SLOT [2:0]	000	EPE2 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	4:2	EPE1_ON_SLOT [2:0]	000	EPE1 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	

Register 7819h LDO11/EPE Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30746 (781Ah) GPIO1 OTP Control	15	GP1_DIR	1	GPIO1 pin direction 0 = Output 1 = Input	
	14:13	GP1_PULL [1:0]	01	GPIO1 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP1_INT_MOD E	0	GPIO1 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP1_POL=1) or falling edge triggered (if GP1_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP1_PWR_DO M	0	GPIO1 Power Domain select 0 = DBVDD 1 = PMICVDD (LDO12)	
	10	GP1_POL	1	GPIO1 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP1_OD	0	GPIO1 Output pin configuration 0 = CMOS 1 = Open Drain	
	8	GP1_ENA	0	GPIO1 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	7:4	GP1_FN [3:0]	0000	GPIO1 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				7 = Reserved 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	
	1	XTAL_INH	0	Crystal Start-Up Inhibit 0 = Disabled 1 = Enabled When XTAL_INH=0, the internal RC oscillator will provide CLKOUT until the crystal oscillator is valid. When XTAL_INH=1, the 'ON' transition is inhibited until the crystal oscillator is valid.	

Register 781Ah GPIO1 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30747 (781Bh) GPIO2 OTP Control	15	GP2_DIR	1	GPIO2 pin direction 0 = Output 1 = Input	
	14:13	GP2_PULL [1:0]	01	GPIO2 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP2_INT_MOD E	0	GPIO2 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP2_POL=1) or falling edge triggered (if GP2_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP2_PWR_DO M	0	GPIO2 Power Domain select 0 = DBVDD 1 = PMICVDD (LDO12)	
	10	GP2_POL	1	GPIO2 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP2_OD	0	GPIO2 Output pin configuration 0 = CMOS 1 = Open Drain	
	8	GP2_ENA	0	GPIO2 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	7:4	GP2_FN [3:0]	0000	<p>GPIO2 Pin Function</p> <p>Input functions:</p> <ul style="list-style-type: none"> 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) <p>Output functions:</p> <ul style="list-style-type: none"> 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Reserved 7 = Reserved 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset 	
	3:1	CLKOUT_SLOT [2:0]	000	<p>CLKOUT output enable ON slot select</p> <ul style="list-style-type: none"> 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Do not enable 111 = Do not enable 	
	0	WDOG_ENA	1	<p>Watchdog Timer Enable</p> <ul style="list-style-type: none"> 0 = Disabled 1 = Enabled (enables the watchdog; does not reset it) <p><i>Protected by security key.</i></p>	

Register 781Bh GPIO2 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30748 (781Ch) GPIO3 OTP Control	15	GP3_DIR	1	GPIO3 pin direction 0 = Output 1 = Input	
	14:13	GP3_PULL [1:0]	01	GPIO3 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP3_INT_MOD E	0	GPIO3 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP3_POL=1) or falling edge triggered (if GP3_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP3_PWR_DO M	0	GPIO3 Power Domain select 0 = DBVDD 1 = PMICVDD (LDO12)	
	10	GP3_POL	1	GPIO3 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP3_OD	0	GPIO3 Output pin configuration 0 = CMOS 1 = Open Drain	
	8	GP3_ENA	0	GPIO3 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	7:4	GP3_FN [3:0]	0000	GPIO3 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Reserved 7 = Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 781Ch GPIO3 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30749 (781Dh) GPIO4 OTP Control	15	GP4_DIR	1	GPIO4 pin direction 0 = Output 1 = Input	
	14:13	GP4_PULL [1:0]	01	GPIO4 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP4_INT_MODE	0	GPIO4 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP4_POL=1) or falling edge triggered (if GP4_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP4_PWR_DOMAIN	0	GPIO4 Power Domain select 0 = DBVDD 1 = PVDD	
	10	GP4_POL	1	GPIO4 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP4_OD	0	GPIO4 Output pin configuration 0 = CMOS 1 = Open Drain	
	8	GP4_ENA	0	GPIO4 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	7:4	GP4_FN [3:0]	0000	GPIO4 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Reserved 7 = Reserved 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	
	3:2	LED1_SRC [1:0]	11	LED1 Source (Selects the LED1 function.) 00 = Off 01 = Power State Status 10 = Reserved 11 = Manual Mode	
	1:0	LED2_SRC [1:0]	11	LED2 Source (Selects the LED2 function.) 00 = Off 01 = Power State Status 10 = Reserved 11 = Manual Mode	

Register 781Dh GPIO4 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30750 (781Eh) GPIO5 OTP Control	15	GP5_DIR	1	GPIO5 pin direction 0 = Output 1 = Input	
	14:13	GP5_PULL [1:0]	01	GPIO5 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP5_INT_MODE	0	GPIO5 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP5_POL=1) or falling edge triggered (if GP5_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	11	GP5_PWR_DOM	0	GPIO5 Power Domain select 0 = DBVDD 1 = PVDD	
	10	GP5_POL	1	GPIO5 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP5_OD	0	GPIO5 Output pin configuration 0 = CMOS 1 = Open Drain	
	8	GP5_ENA	0	GPIO5 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	7:4	GP5_FN [3:0]	0000	GPIO5 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Reserved 7 = Reserved 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 781Eh GPIO5 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30751 (781Fh) GPIO6 OTP Control	15	GP6_DIR	1	GPIO6 pin direction 0 = Output 1 = Input	
	14:13	GP6_PULL [1:0]	01	GPIO6 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP6_INT_MOD E	0	GPIO6 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP6_POL=1) or falling edge triggered (if GP6_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP6_PWR_DO M	0	GPIO6 Power Domain select 0 = DBVDD 1 = PVDD	
	10	GP6_POL	1	GPIO6 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP6_OD	0	GPIO6 Output pin configuration 0 = CMOS 1 = Open Drain	
	8	GP6_ENA	0	GPIO6 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	7:4	GP6_FN [3:0]	0000	GPIO6 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Reserved 7 = Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	
	3:1	SYSOK_THR [2:0]	101	SYSOK threshold (rising PVDD) This is the rising PVDD voltage at which SYSOK will be asserted 000 = 2.8V 001 = 2.9V ... 111 = 3.5V	

Register 781Fh GPIO6 OTP Control

30 APPLICATIONS INFORMATION

30.1 EXTERNAL CONNECTIONS TO I.MX53 PROCESSOR

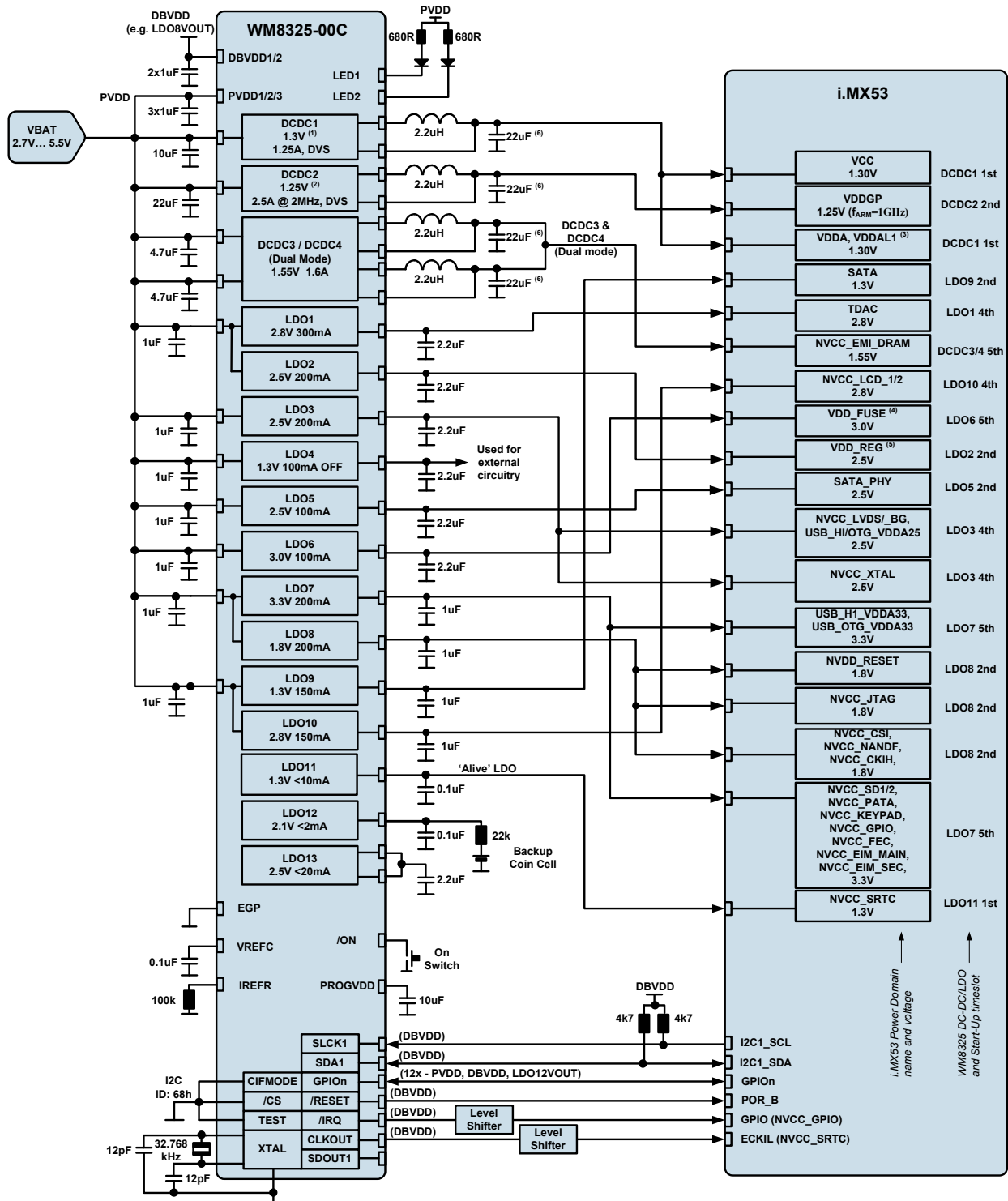


Figure 27 Typical Connections to i.MX53 Processor

Notes:

1. DC-DC1 output voltage is set accordingly to the i.MX53 performance mode, ie. High Performance Mode (HPM) or Reduced Performance Mode (RPM).
2. DC-DC2 output voltage is set according to achieve the desired fARM: 0.85 to 0.95V (fARM ≤ 160MHz), 0.9 to 1.05V (fARM ≤ 400MHz), 1.05 to 1.15V (fARM ≤ 800MHz) and 1.2 to 1.3V (fARM ≤ 1000MHz).
3. VDDA and VDDAL1 can be driven by the VDD_DIG_PLL internal regulator.
4. In read mode, VDD_FUSE should be floated or grounded.
5. VDD_REG is power supply input to VDD_ANA_PLL and VDD_DIG_PLL LDOs. VDD_REG is only used to power internal interfaces.
6. The DC-DC converter output capacitors can be increased to achieve the required load transient performance.

30.2 POWER-UP SEQUENCE

The 'ON' state transition sequence implemented on the WM8325-00C OTP program is described in Table 74. The sequence description illustrates how the i.MX53 processor requirements are achieved.

I.MX53 POWER DOMAIN	I.MX53 POWER SEQUENCE		WM8325-00C CONVERTER / REGULATOR	WM8325-00C POWER-UP TIMESLOT
NVCC_SRTC_POW	0	Always on or enabled first	LDO11	1
VCC	1	Enabled after NVCC_SRTC_POW	DC-DC1	1
NVCC_CKIH	2	Enabled after VCC	LDO8	2
<2.8V IO supplies	3	Enabled after NVCC_CKIH	LDO3	4
			LDO4	OFF
			LDO5	2
>2.8V IO supplies	3.5	Enabled when NVCC_CKIH is stable	LDO7	5
			LDO1	4
			LDO10	4
VDD_FUSE	3.5	Enabled when NVCC_CKIH is stable	LDO6	5
NVCC_REG	2	Enabled after VCC	LDO2	2
NVCC_EMI_DRAM	3	Enabled after NVCC_CKIH	DC-DC3 / DC-DC4	5
VP, VPH (ie. SATA)	1.5	Enabled when VCC is stable	LDO9	2
VDDA, VDDAL1	1	Enabled after NVCC_SRTC_POW	DC-DC1	1
VDDGP	1	Enabled after NVCC_SRTC_POW	DC-DC2	2

Table 74 WM8325-00C Power-Up Sequence

The WM8325-00C Power-Up sequence ('ON' state transition) is illustrated in Figure 28.

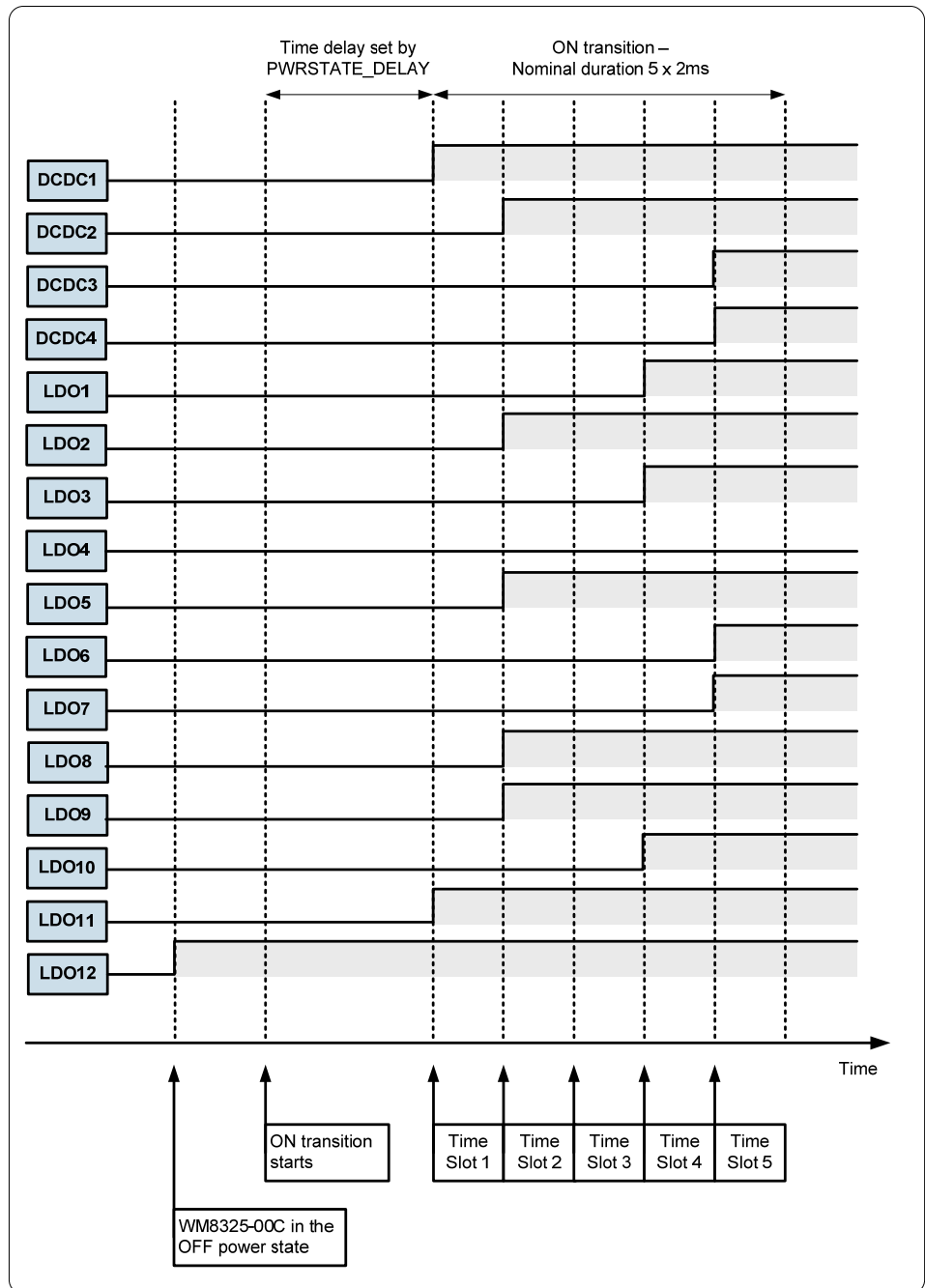


Figure 28 WM8325-00C Power-Up Sequence

30.3 OTP PROGRAM

The OTP memory program of the WM8325-00C is detailed in Figure 29. The illustration is a screenshot from Wolfson's WISCE™ evaluation board software. It shows Page 2 and Page 3 of the OTP contents only.

Note that the OTP Program shown in Figure 29 includes a control registers not described in the datasheet. The affected control registers are fields that are locked to the OTP settings on WM8325-00C and cannot be changed. Accordingly, these registers have no user function on this device.

For completeness, and to allow the same configuration settings to be implemented (or adjusted) on a user-programmable WM8325 device, the OTP Program shown here describes all of the WM8325 OTP register settings, including the registers that are not applicable to the WM8325-00C.

A register field listing is provided in Table 75.

R7810h	Customer OTP ID	Read	Write	00C1h	O_PROG=0 OTP_CUST_ID=00_0000_0110_0000												T_FINAL							
R7811h	DC1 OTP Control	Read	Write	4F30h	DC2_ON_SLOT=010			DC2_ON_VSEL=0_1111			DC1_ON_SLOT=001			DC1_ON_VSEL=1_0000										
R7812h	DC2 OTP Control	Read	Write	A7A7h	DC4_ON_SLOT=101			DC4_ON_VSEL=0_0111			DC3_ON_SLOT=101			DC3_ON_VSEL=0_0111										
R7813h	DC3 OTP Control	Read	Write	2AA5h	_PHASE=0		_PHASE=0		_PHASE=1		DC4_CAP=10		DC3_CAP=10		DC2_CAP=10		DC1_CAP=10		DC2_FREQ=01		DC1_FREQ=01			
R7814h	LDO1/2 OTP Control	Read	Write	579Ah	LDO2_ON_SLOT=010			LDO2_ON_VSEL=1_0111			LDO1_ON_SLOT=100			LDO1_ON_VSEL=1_1010										
R7815h	LDO3/4 OTP Control	Read	Write	0897h	LDO4_ON_SLOT=000			LDO4_ON_VSEL=0_1000			LDO3_ON_SLOT=100			LDO3_ON_VSEL=1_0111										
R7816h	LDO5/6 OTP Control	Read	Write	8C57h	LDO6_ON_SLOT=101			LDO6_ON_VSEL=1_1100			LDO5_ON_SLOT=010			LDO5_ON_VSEL=1_0111										
R7817h	LDO7/8 OTP Control	Read	Write	4EBDh	LDO8_ON_SLOT=010			LDO8_ON_VSEL=0_1110			LDO7_ON_SLOT=101			LDO7_ON_VSEL=1_1101										
R7818h	LDO9/10 OTP Control	Read	Write	9846h	LDO10_ON_SLOT=100			LDO10_ON_VSEL=1_1000			LDO9_ON_SLOT=010			LDO9_ON_VSEL=0_0110										
R7819h	LDO11/EPE Control	Read	Write	2A01h	LDO11_ON_SLOT=001			LDO11_ON_VSEL=1010			EPE2_ON_SLOT=000			EPE1_ON_SLOT=000			DC4_SLAVE							
R781Ah	GPIO1 OTP Control	Read	Write	A406h	GP1_DIR=1		GP1_PULL=01		T_MODE=0		VR_DOM=0		SP1_POL=1		GP1_OD=0		GP1_ENA=0		GP1_FN=0000		TAL_ENA=1		TAL_INH=1	
R781Bh	GPIO2 OTP Control	Read	Write	A402h	GP2_DIR=1		GP2_PULL=01		T_MODE=0		VR_DOM=0		SP2_POL=1		GP2_OD=0		GP2_ENA=0		GP2_FN=0000		CLKOUT_SLOT=001		DIG_ENA	
R781Ch	GPIO3 OTP Control	Read	Write	A400h	GP3_DIR=1		GP3_PULL=01		T_MODE=0		VR_DOM=0		SP3_POL=1		GP3_OD=0		GP3_ENA=0		GP3_FN=0000		0		0	
R781Dh	GPIO4 OTP Control	Read	Write	A40Fh	GP4_DIR=1		GP4_PULL=01		T_MODE=0		VR_DOM=0		SP4_POL=1		GP4_OD=0		GP4_ENA=0		GP4_FN=0000		LED1_SRC=11		LED2_SRC=11	
R781Eh	GPIO5 OTP Control	Read	Write	A400h	GP5_DIR=1		GP5_PULL=01		T_MODE=0		VR_DOM=0		SP5_POL=1		GP5_OD=0		GP5_ENA=0		GP5_FN=0000		0		0	
R781Fh	GPIO6 OTP Control	Read	Write	A40Ah	GP6_DIR=1		GP6_PULL=01		T_MODE=0		VR_DOM=0		SP6_POL=1		GP6_OD=0		GP6_ENA=0		GP6_FN=0000		SYSOK_THR=101		0	

Figure 29 WM8325-00C OTP Program (WISCE screen view)

OTP ADDRESS	BIT	LABEL	VALUE	DESCRIPTION
R16 (10h) Customer OTP ID	15	OTP_AUTO_PROG	0	Auto-programming of OTP is disabled
	14:1	OTP_CUST_ID [13:0]	0060h	OTP ID is 0060h
	0	OTP_CUST_FINAL	1	OTP contents are finalised (no further Writes are possible)
R17 (11h) DC1 OTP Control	15:13	DC2_ON_SLOT [2:0]	010	DC2 is enabled in Timeslot 2 of the ON sequence
	12:8	DC2_ON_VSEL [6:2]	0_1111	DC2 output voltage is 1.25V
	7:5	DC1_ON_SLOT [2:0]	001	DC1 is enabled in Timeslot 1 of the ON sequence
	4:0	DC1_ON_VSEL [6:2]	1_0000	DC1 output voltage is 1.3V
R18 (12h) DC2 OTP Control	15:13	DC4_ON_SLOT [2:0]	101	DC4 is enabled in Timeslot 5 of the ON sequence
	12:8	DC4_ON_VSEL [6:2]	0_0111	DC4 output voltage is 1.55V
	7:5	DC3_ON_SLOT [2:0]	101	DC3 is enabled in Timeslot 5 of the ON sequence
	4:0	DC3_ON_VSEL [6:2]	0_0111	DC3 output voltage is 1.55V
R19 (13h) DC3 OTP Control	15	DC4_PHASE	0	DC4 clock phase is Normal
	14	DC3_PHASE	0	DC3 clock phase is Normal
	13	DC2_PHASE	1	DC2 clock phase is Inverted
	12	DC1_PHASE	0	DC1 clock phase is Normal
	11:10	DC4_CAP [1:0]	10	DC4 output capacitor is 22uF to 45uF
	9:8	DC3_CAP [1:0]	10	DC3 output capacitor is 22uF to 45uF
	7:6	DC2_CAP [1:0]	10	DC2 output capacitor is 22uF to 47uF
	5:4	DC1_CAP [1:0]	10	DC1 output capacitor is 22uF to 47uF
	3:2	DC2_FREQ [1:0]	01	DC2 switching frequency is 2MHz
1:0	DC1_FREQ [1:0]	01	DC1 switching frequency is 2MHz	
R20 (14h) LDO1/2 OTP Control	15:13	LDO2_ON_SLOT [2:0]	010	LDO2 is enabled in Timeslot 2 of the ON sequence
	12:8	LDO2_ON_VSEL [4:0]	1_0111	LDO2 output voltage is 2.5V
	7:5	LDO1_ON_SLOT [2:0]	100	LDO1 is enabled in Timeslot 4 of the ON sequence
	4:0	LDO1_ON_VSEL [4:0]	1_1010	LDO1 output voltage is 2.8V
R21 (15h) LDO3/4 OTP Control	15:13	LDO4_ON_SLOT [2:0]	000	LDO4 is not enabled in the ON sequence
	12:8	LDO4_ON_VSEL [4:0]	0_1000	LDO4 output voltage is 1.3V
	7:5	LDO3_ON_SLOT [2:0]	100	LDO3 is enabled in Timeslot 4 of the ON sequence
	4:0	LDO3_ON_VSEL [4:0]	1_0111	LDO3 output voltage is 2.5V
R22 (16h) LDO5/6 OTP Control	15:13	LDO6_ON_SLOT [2:0]	101	LDO6 is enabled in Timeslot 5 of the ON sequence
	12:8	LDO6_ON_VSEL [4:0]	1_1100	LDO6 output voltage is 3.0V
	7:5	LDO5_ON_SLOT [2:0]	010	LDO5 is enabled in Timeslot 2 of the ON sequence
	4:0	LDO5_ON_VSEL [4:0]	1_0111	LDO5 output voltage is 2.5V
R23 (17h) LDO7/8 OTP Control	15:13	LDO8_ON_SLOT [2:0]	010	LDO8 is enabled in Timeslot 2 of the ON sequence
	12:8	LDO8_ON_VSEL [4:0]	0_1110	LDO8 output voltage is 1.8V
	7:5	LDO7_ON_SLOT [2:0]	101	LDO7 is enabled in Timeslot 5 of the ON sequence
	4:0	LDO7_ON_VSEL [4:0]	1_1101	LDO7 output voltage is 3.3V
R24 (18h) LDO9/10 OTP Control	15:13	LDO10_ON_SLOT [2:0]	100	LDO10 is enabled in Timeslot 4 of the ON sequence
	12:8	LDO10_ON_VSEL [4:0]	1_1000	LDO10 output voltage is 2.8V
	7:5	LDO9_ON_SLOT [2:0]	010	LDO9 is enabled in Timeslot 2 of the ON sequence
	4:0	LDO9_ON_VSEL [4:0]	0_0110	LDO9 output voltage is 1.3V
R25 (19h) LDO11/EPE OTP Control	15:13	LDO11_ON_SLOT [2:0]	001	LDO11 is enabled in Timeslot 1 of the ON sequence
	11:8	LDO11_ON_VSEL [3:0]	1010	LDO11 output voltage is 1.3V
	7:5	EPE2_ON_SLOT [2:0]	000	EPE2 output is not enabled in the ON sequence
	4:2	EPE1_ON_SLOT [2:0]	000	EPE1 output is not enabled in the ON sequence
	0	DC4_SLV	1	DC4 is Slaved to DC3 - the converters operate in Dual mode
R26 (1Ah) GPIO1 OTP Control	15	GP1_DIR	1	GPIO1 is input
	14:13	GP1_PULL [1:0]	01	GPIO1 pull-down is enabled
	12	GP1_INT_MODE	0	GPIO1 interrupt is rising-edge triggered
	11	GP1_PWR_DOM	0	GPIO1 is on DBVDD power domain
	10	GP1_POL	1	GPIO1 polarity is not inverted

OTP ADDRESS	BIT	LABEL	VALUE	DESCRIPTION
	9	GP1_OD	0	GPIO1 output is CMOS
	8	GP1_ENA	0	GPIO1 pin is tri-stated
	7:4	GP1_FN [3:0]	0000	GPIO1 pin function is GPIO
	2	XTAL_ENA	1	Crystal oscillator is enabled
	1	XTAL_INH	1	'ON' state transition is inhibited until crystal oscillator is valid
R27 (1Bh) GPIO2 OTP Control	15	GP2_DIR	1	GPIO2 is input
	14:13	GP2_PULL [1:0]	01	GPIO2 pull-down is enabled
	12	GP2_INT_MODE	0	GPIO2 interrupt is rising-edge triggered
	11	GP2_PWR_DOM	0	GPIO2 is on DBVDD power domain
	10	GP2_POL	1	GPIO2 polarity is not inverted
	9	GP2_OD	0	GPIO2 output is CMOS
	8	GP2_ENA	0	GPIO2 pin is tri-stated
	7:4	GP2_FN [3:0]	0000	GPIO2 pin function is GPIO
	3:1	CLKOUT_SLOT [2:0]	001	CLKOUT is enabled in Timeslot 1 of the ON sequence
0	WDOG_ENA	0	Watchdog Timer is enabled	
R28 (1Ch) GPIO3 OTP Control	15	GP3_DIR	1	GPIO3 is input
	14:13	GP3_PULL [1:0]	01	GPIO3 pull-down is enabled
	12	GP3_INT_MODE	0	GPIO3 interrupt is rising-edge triggered
	11	GP3_PWR_DOM	0	GPIO3 is on DBVDD power domain
	10	GP3_POL	1	GPIO3 polarity is not inverted
	9	GP3_OD	0	GPIO3 output is CMOS
	8	GP3_ENA	0	GPIO3 pin is tri-stated
	7:4	GP3_FN [3:0]	0000	GPIO3 pin function is GPIO
R29 (1Dh) GPIO4 OTP Control	15	GP4_DIR	1	GPIO4 is input
	14:13	GP4_PULL [1:0]	01	GPIO4 pull-down is enabled
	12	GP4_INT_MODE	0	GPIO4 interrupt is rising-edge triggered
	11	GP4_PWR_DOM	0	GPIO4 is on DBVDD power domain
	10	GP4_POL	1	GPIO4 polarity is not inverted
	9	GP4_OD	0	GPIO4 output is CMOS
	8	GP4_ENA	0	GPIO4 pin is tri-stated
	7:4	GP4_FN [3:0]	0000	GPIO4 pin function is GPIO
	3:2	LED1_SRC [1:0]	11	LED1 is controlled in manual mode
1:0	LED2_SRC [1:0]	11	LED2 is controlled in manual mode	
R30 (1Eh) GPIO5 OTP Control	15	GP5_DIR	1	GPIO5 is input
	14:13	GP5_PULL [1:0]	01	GPIO5 pull-down is enabled
	12	GP5_INT_MODE	0	GPIO5 interrupt is rising-edge triggered
	11	GP5_PWR_DOM	0	GPIO5 is on DBVDD power domain
	10	GP5_POL	1	GPIO5 polarity is not inverted
	9	GP5_OD	0	GPIO5 output is CMOS
	8	GP5_ENA	0	GPIO5 pin is tri-stated
7:4	GP5_FN [3:0]	0000	GPIO5 pin function is GPIO	
R31 (1Fh) GPIO6 OTP Control	15	GP6_DIR	1	GPIO6 is input
	14:13	GP6_PULL [1:0]	01	GPIO6 pull-down is enabled
	12	GP6_INT_MODE	0	GPIO6 interrupt is rising-edge triggered
	11	GP6_PWR_DOM	0	GPIO6 is on DBVDD power domain
	10	GP6_POL	1	GPIO6 polarity is not inverted
	9	GP6_OD	0	GPIO6 output is CMOS
	8	GP6_ENA	0	GPIO6 pin is tri-stated
	7:4	GP6_FN [3:0]	0000	GPIO6 pin function is GPIO
3:1	SYSOK_THR [2:0]	101	SYSOK threshold is 3.3V	

Table 75 WM8325-00C OTP Program Description

30.4 VOLTAGE AND CURRENT REFERENCE COMPONENTS

A decoupling capacitor is required between VREFC and GND; a 100nF X5R capacitor is recommended (available in 0201 package size).

A current reference resistor is required between IREFR and GND; a 100kΩ (1%) resistor is recommended.

30.5 DC-DC BUCK CONVERTER EXTERNAL COMPONENTS

The recommended connections to the DC-DC buck converters are illustrated in Figure 30.

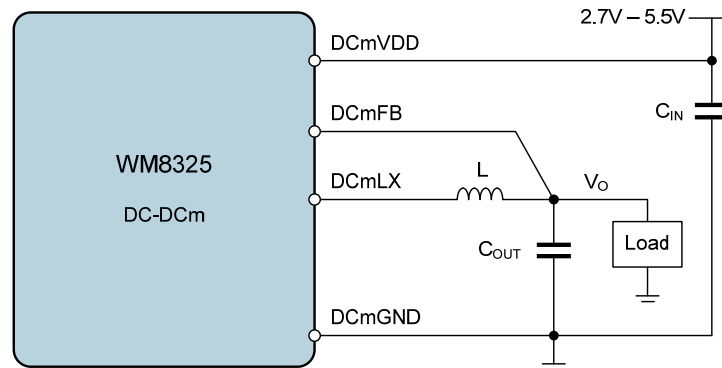


Figure 30 DC-DC Buck Converter External Components

When selecting suitable capacitors, it is imperative that the effective capacitance is within the required limits at the applicable input/output voltage of the converter. It should be noted that some components' capacitance changes significantly depending on the DC voltage applied. Ceramic X7R or X5R types are recommended.

The choice of output capacitor varies depending on the required transient response. Larger values may be required for optimum performance under large load transient conditions. Smaller values may be sufficient for a steady load, or in applications without stringent requirements on output voltage accuracy during load transients.

For layout and size reasons, users may choose to implement large values of output capacitance by connecting two or more capacitors in parallel.

When selecting a suitable output inductor, the inductance value and the saturation current must be compatible with the operating conditions of the converter.

The magnitude of the inductor current ripple is dependant on the inductor value and can be determined by the following equation:

$$\Delta I_L = \frac{V_{OUT} \cdot (1 - (V_{OUT} / V_{IN}))}{L \cdot F_{SW}}$$

ΔI_L = Inductor ripple current
 V_{OUT} = Output voltage
 V_{IN} = Input voltage
 L = Inductance
 F_{SW} = Switching frequency

As a minimum requirement, the DC current rating should be equal to the maximum load current plus one half of the inductor current ripple:

$$I_{Lpeak} = I_{OUTmax} + (\Delta I_L / 2)$$

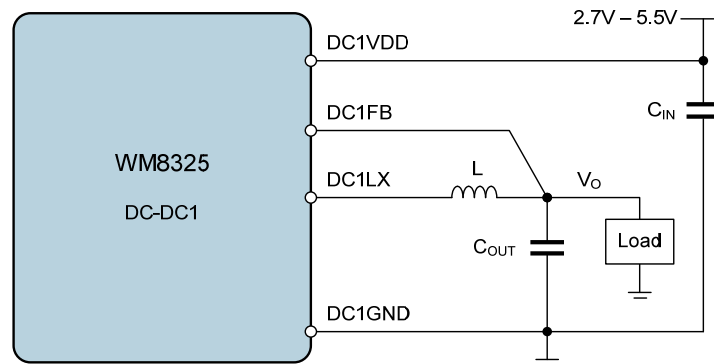
I_{Lpeak} = Inductor peak current
 I_{OUTmax} = Maximum load current
 ΔI_L = Inductor ripple current

To be suitable for the application, the chosen inductor must have a saturation current that is higher than the peak inductor current given by the above equation. To maximise the converter efficiency, the inductor should also have a low DC Resistance (DCR), resulting in minimum conduction losses. Care should also be taken to ensure that the component's inductance is valid at the applicable operating temperature.

The WM8325-00C incorporates a current-limit protection feature for all DC-DC Converter outputs. In order to achieve the benefit of this feature, the output inductor saturation current limit must be greater than or equal to the P-channel Current Limit for the applicable converter (see Section 7).

The typical connections to DC-DC Converters 1 and 2 are illustrated in Figure 31.

The input voltage connection to DC-DC Converters 1 and 2 is provided on DC1VDD and DC2VDD respectively; these pins must be connected to the PVDD power supply voltage node.



Note: Equivalent circuit applies for DC-DC2

Figure 31 DC-DC1 and DC-DC2 Synchronous Buck Converter Connections

Wolfson recommends the following external components for use with DC-DC Converter 1.

A choice of output capacitor components is supported. For best performance, the 47 μ F component is recommended. For typical applications, the 22 μ F is suitable.

COMPONENT	VALUE	PART NUMBER	SIZE
L	2.2 μ H	Coilcraft LPS3015-222ML_	3 x 3 x 1.5mm
C _{OUT}	47 μ F	MuRata GRM21BR60G476MEA1	0805
	22 μ F	MuRata GRM21BR60J226ME39	0805
C _{IN}	10 μ F	MuRata GRM188R60J106ME84	0603

Table 76 Recommended External Components - DC-DC1

Wolfson recommends the following external components for use with DC-DC Converter 2.

A choice of output capacitor components is supported. For best performance, the 47 μ F component is recommended. For typical applications, the 22 μ F is suitable.

COMPONENT	VALUE	PART NUMBER	SIZE
L	2.2 μ H	TDK VLC5045-2R2N	5 x 5 x 4.5mm
	2.2 μ H	Coilcraft XAL4030-222ME_	4 x 4 x 3.1mm
C _{OUT}	47 μ F	MuRata GRM21BR60G476MEA1	0805
	22 μ F	MuRata GRM21BR60J226ME39	0805
C _{IN}	22 μ F	MuRata GRM21BR60J226ME39	0805

Table 77 Recommended External Components - DC-DC2

DC-DC Converters 3 and 4 are configured to operate in 'Dual' mode, where the two converters are ganged together to support an increased current capability. The external component configuration is similar to DC-DC1 and DC-DC2; output load connection points (V_o) are connected together.

The typical connections to DC-DC Converters 1 and 2 are illustrated in Figure 32.

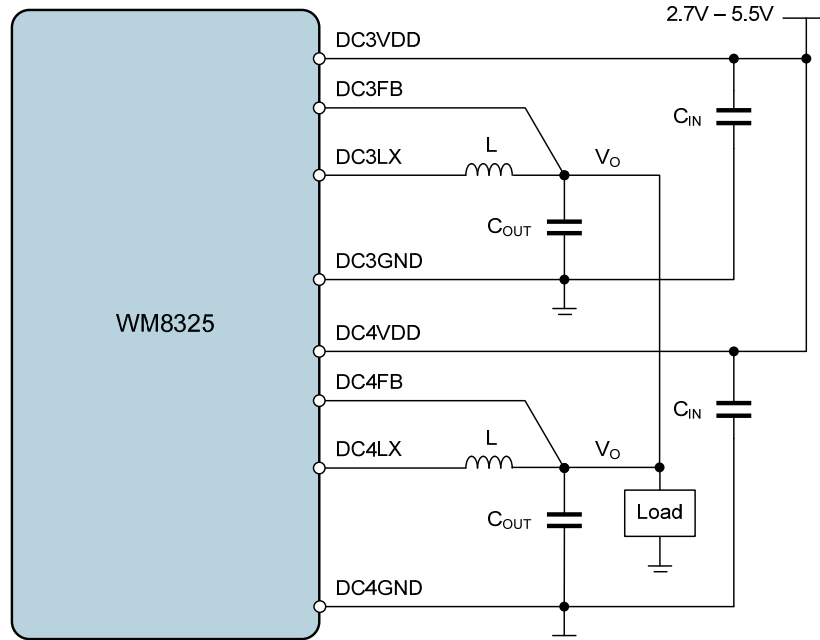


Figure 32 DC-DC3 / DC-DC4 Dual Mode Converter Connections

Wolfson recommends the following external components for use with DC-DC Converters 3 and 4 when operating in Dual Mode.

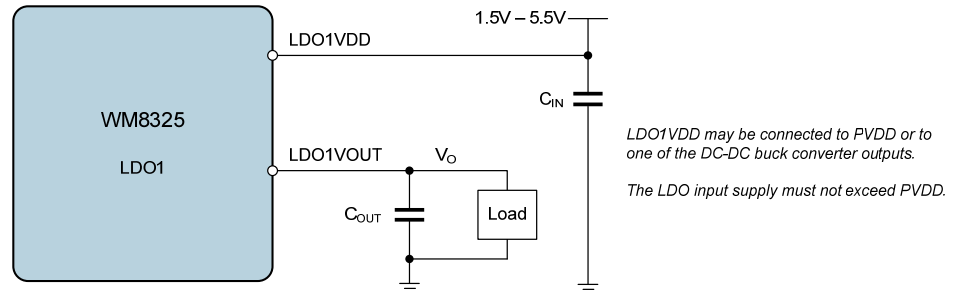
A choice of output capacitor components is supported. For best performance, the 47 μ F component is recommended. For typical applications, the 22 μ F is suitable.

COMPONENT	VALUE	PART NUMBER	SIZE
L	2.2 μ H	Coilcraft LPS3015-222ML_	3 x 3 x 1.5mm
C _{OUT}	47 μ F	MuRata GRM21BR60G476MEA1	0805
	22 μ F	MuRata GRM21BR60J226ME39	0805
C _{IN}	4.7 μ F	MuRata GRM188R60J475ME84	0603

Table 78 Recommended External Components - DC-DC3 / DC-DC4 Dual Mode

30.6 LDO REGULATOR EXTERNAL COMPONENTS

The recommended connections to the LDO Regulators are illustrated in Figure 33.



Note: Equivalent circuit applies for LDO2 through to LDO10.

Figure 33 LDO Regulators External Components

When selecting suitable capacitors, it is imperative that the effective capacitance is within the required limits at the applicable input/output voltage of the converter. Ceramic X7R or X5R types are recommended.

Wolfson recommends the following external components for use with LDO Regulators 1 to 6.

COMPONENT	VALUE	PART NUMBER	SIZE
C_{OUT}	2.2 μ F	Kemet C0402C225M9PAC	0402
C_{IN}	1.0 μ F	MuRata GRM155R61A105KE15	0402

Table 79 Recommended External Components - LDO1 to LDO6

Wolfson recommends the following external components for use with LDO Regulators 7 to 10. For these regulators, note that it is important that the output capacitance, C_{OUT} , does not exceed 4.7 μ F.

COMPONENT	VALUE	PART NUMBER	SIZE
C_{OUT}	1.0 μ F	MuRata GRM155R61A105KE15	0402
C_{IN}	1.0 μ F	MuRata GRM155R61A105KE15	0402

Table 80 Recommended External Components - LDO7 to LDO10

Wolfson recommends the following external components for use with LDO Regulators 11 to 13.

COMPONENT	VALUE	PART NUMBER	SIZE
C_{OUT} (LDO11)	0.1 μ F	MuRata GRM033R60J104KE19	0201
C_{OUT} (LDO12)	0.1 μ F	MuRata GRM033R60J104KE19	0201
C_{OUT} (LDO13)	2.2 μ F	Kemet C0402C225M9PAC	0402

Table 81 Recommended External Components - LDO11 to LDO13

30.7 PCB LAYOUT

Poor PCB layout will degrade the performance and be a contributory factor in EMI, ground bounce and resistive voltage losses. Poor regulation and instability can result.

Simple design rules can be implemented to negate these effects:

External input and output capacitors should be placed as close to the device as possible using short wide traces between the external power components. For the DC-DC Converters, the input capacitor placement takes priority on the DC-DC converters. (For the LDO Regulators, the placement of the input and output capacitors have equal priority.)

Route the DC-DC converter output voltage feedback as an independent connection to the top of the output capacitor to create a true sense of the output voltage, routing away from noisy signals such as the LX connection.

Use a local ground island for each individual DC-DC converter connected at a single point onto a fully flooded ground plane.

Current loop areas should be kept as small as possible with loop areas changing little during alternating switching cycles.

The layout in Figure 32, for example, shows DC-DC1 layout with external components C8, L1 and C1. The input capacitor, C8, is close into the IC and shares a small ground island with the output capacitor C1. The inductor, L1, is situated in close proximity to C1 in order to keep loop area small and minimise the trace resistance. Note also the use of short wide traces with all power tracking on a single (top) layer.

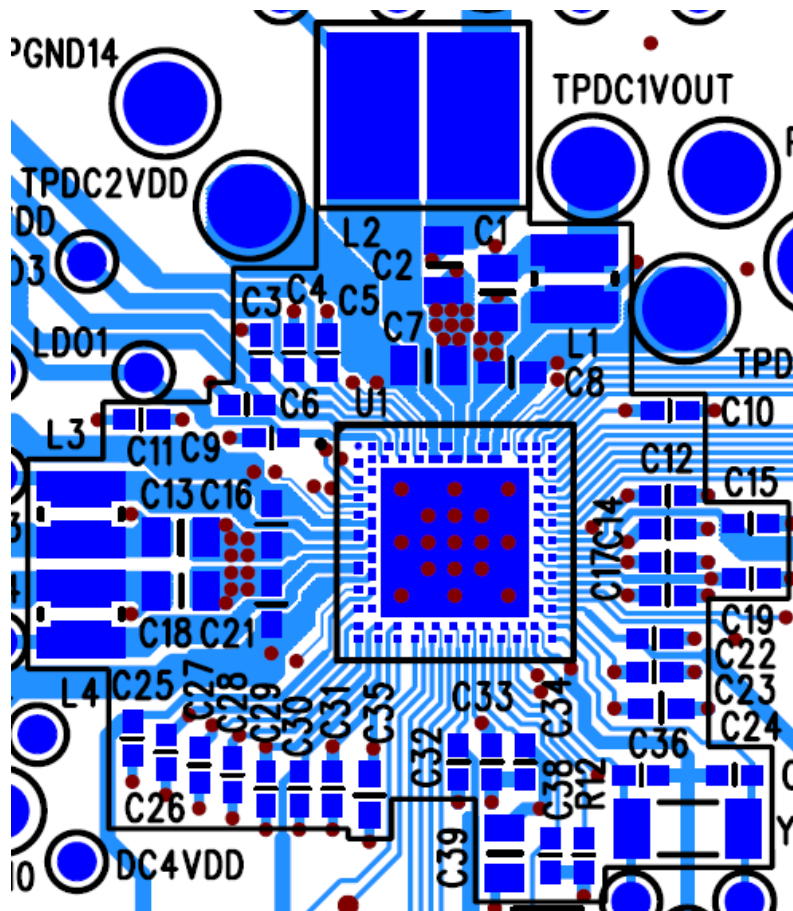
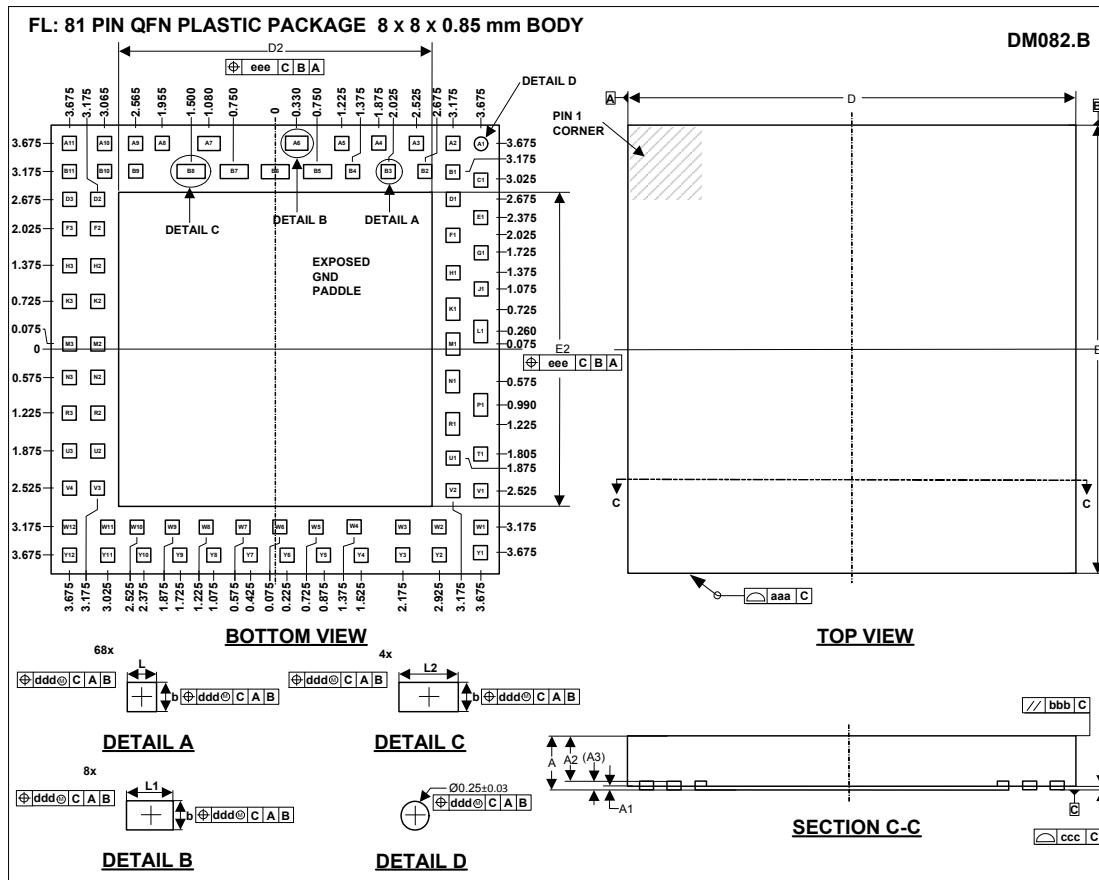


Figure 34 PCB Layout

31 PACKAGE DIAGRAM



Symbols	Dimensions (mm)			NOTE
	MIN	NOM	MAX	
A	---	---	0.85	
A1	0.02	0.05	0.08	
A2	0.64	0.675	0.71	
A3	0.12	0.13	0.14	
b	0.22	0.25	0.28	
D		8 BSC		
D2	5.55	5.60	5.65	
E		8 BSC		
E2	5.55	5.60	5.65	
L	0.22	0.25	0.28	
L1	0.37	0.4	0.43	
L2	0.47	0.5	0.53	
Tolerances of Form and Position				
aaa	0.10			
bbb	0.20			
ccc	0.05			
ddd	0.08			
eee	0.10			
REF	JEDEC, MO-220			

- NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES
 2. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-002.
 3. COPPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
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33 REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	CHANGED BY
23/11/11	3.0	First Release	PH
14/02/11	3.1	Updates to Electrical Characteristics	PH