

## Wolfson AudioPlus™ Stereo CODEC with Power Management

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### DESCRIPTION

The WM8350 is an integrated audio and power management subsystem which provides a cost effective, single-chip solution for portable audio and multimedia systems.

The integrated audio CODEC provides all the necessary functions for high-quality stereo recording and playback. Programmable on-chip amplifiers allow for the direct connection of headphones and microphones with a minimum of external components. A programmable low-noise bias voltage is available to feed one or more electret microphones. Additional audio features include programmable high-pass filter in the ADC input path.

The WM8350 includes six programmable DC-DC converters, four low-dropout (LDO) regulators and a current limit switch to generate suitable supply voltages for each part of the system, including the integrated audio CODEC as well as off-chip components such as a digital core and I/O supplies, and LED lighting. An additional on-chip regulator maintains the backup power for always-on functions. The WM8350 can be powered by a lithium battery, by a wall adaptor or USB.

An on-chip battery charger supports both trickle charging and fast (constant current, constant voltage) charging of single-cell lithium batteries. The charge current, termination voltage, and charger time-out are programmable to suit different types of batteries.

Internal power management circuitry controls the start-up and shutdown sequencing of clocks and supply voltages. It also detects and handles conditions such as under-voltage, extreme temperatures, and deeply discharged or defective batteries, with a minimum of software involvement.

Two programmable constant-current sinks are available for driving LED strings, e.g. for display backlights or photo-flash applications, in a highly power-efficient way. Additional RGB LEDs can be driven through GPIO pins.

The WM8350 includes a 32.768kHz crystal oscillator, an internal RC oscillator, a real-time clock (RTC) and an alarm function capable of waking up the system. Internal circuitry can generate all clock signals required to start up the device.

The master clock for the audio CODEC can be input directly, or may be generated internally using an integrated, low power Frequency Locked Loop (FLL).

To extend battery life, fine-grained power management enables each function in the WM8350 to be independently powered down through the control interface. The WM8350 forms part of the Wolfson AudioPlus™ series of audio and power management solutions.

### FEATURES

#### Stereo Hi-Fi CODEC

- DAC SNR 95dB ('A' weighted @ 48kHz), THD -81dB
- ADC SNR 95dB ('A' weighted @ 48kHz), THD -83dB
- 40mW on-chip headphone driver with 'capless' option
- 16Ω headphone load: THD -72dB, Po = 20mW
- 2 differential microphone inputs with low-noise bias voltage and programmable preamps
- Programmable high-pass filter for ADC
- Microphone and Headphone detection
- Auxiliary inputs for analogue signals
- Sample rates: 8, 11.025, 16, 22.05, 24, 32, 44.1 or 48kHz

#### System Control

- Support for 2-wire or 3-/4-wire Control Interface
- Handles power sequencing, reset signals and fault conditions
- Autonomous power source selection (battery, wall adaptor or USB bus)
- Total current drawn from USB bus is limited to comply with USB 2.0 standard and USB OTG supplement

#### Supply Generation

- 2 x DC-DC Buck Converters (0.85V - 3.4V, Up to 1A)
- 2 x DC-DC Buck Converters (0.85V - 3.4V, Up to 500mA)
- 2 x DC-DC Boost Converters (5V - 20V, 40 to 200mA)
- 4 x LDO voltage regulators (0.9V - 3.3V, 150mA)

#### LED Drivers

- 2 programmable constant-current sinks, suitable for screen backlight or white LED photo flash
- 3 open-drain outputs for RGB LEDs

#### Battery Charger

- Single-cell Li-Ion / Li-Pol battery charger
- Thermal protection for charge control; temperature monitoring available for thermal regulation
- LED outputs to indicate charge status and fault conditions

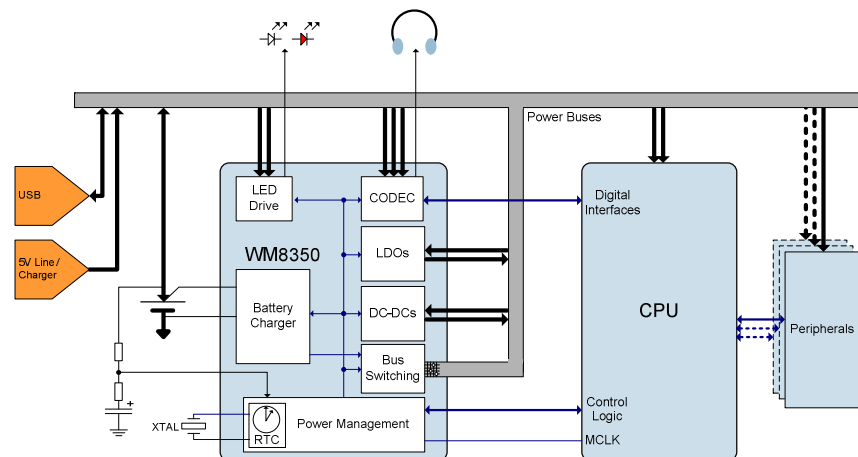
#### Additional Features

- "Always on" RTC with wake-up alarm
- Watchdog timer
- Up to 13 configurable GPIO pins
- On-chip crystal oscillator and internal RC oscillator
- Low power FLL supporting wide range of input clocks
- 7x7mm, 129 BGA package, 0.5mm ball pitch

### APPLICATIONS

- Portable Audio and Media players
- Portable Navigation Devices
- Portable systems powered by single-cell lithium batteries

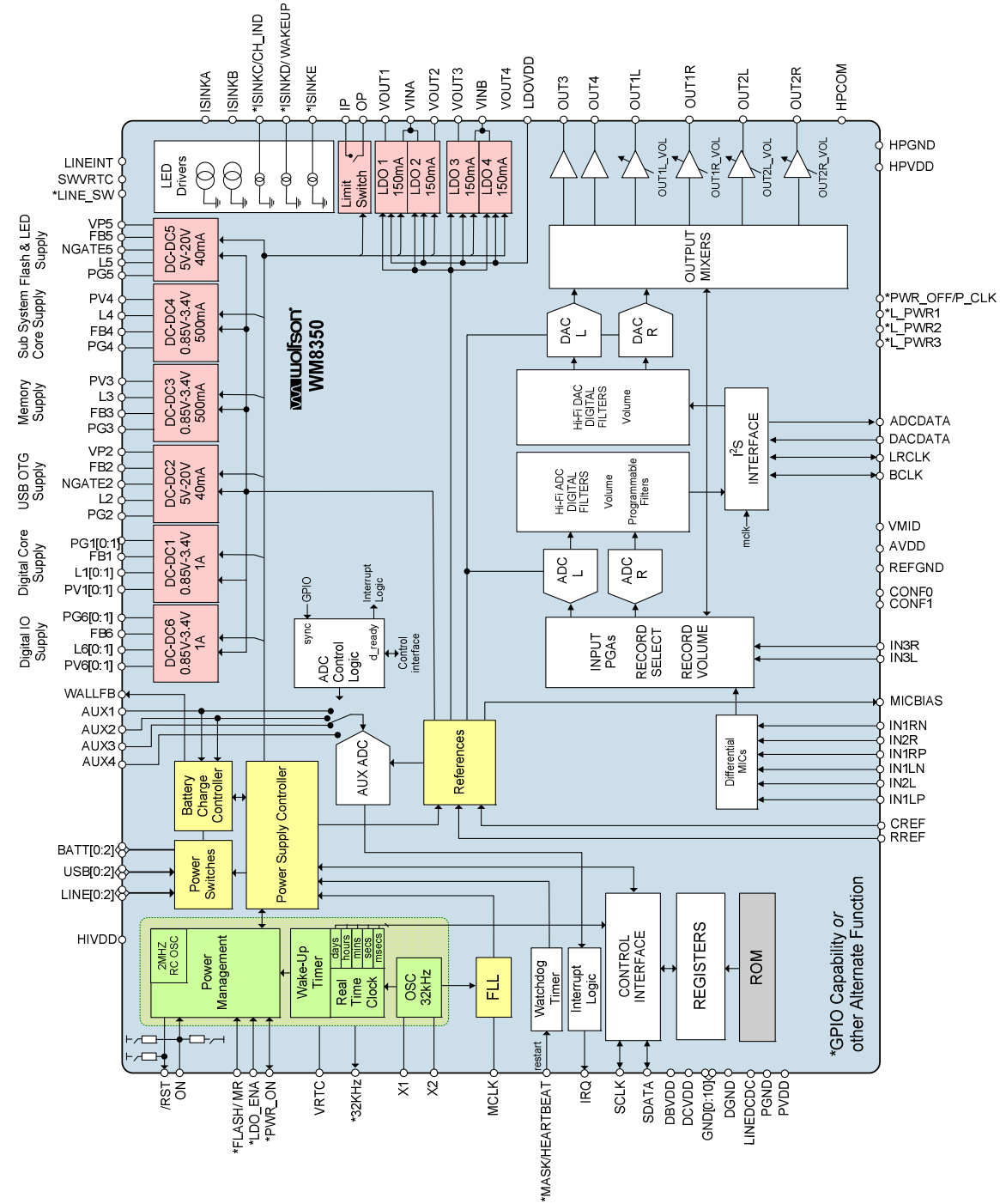
## TYPICAL APPLICATIONS



The WM8350 is a complete audio and power management solution for portable media devices. The device incorporates four programmable step-down switching regulators, two step-up switching regulators, a full-featured battery charger, four Low Drop-Out (LDO) voltage regulators which can also serve as hot-swap outputs, a backup supply regulator, two programmable white LED drivers, a Real-Time Clock (RTC) alongside a 32.768kHz (32kHz) oscillator capable of operating from a backup battery, a 12-bit auxiliary ADC for precise measurements, a ROM-programmable power management state machine and numerous protection features all in a single 7x7mm BGA package. When only battery power is available, a battery switch provides power to all switching regulators (and some other internal modules). When external power is applied (eg. from USB or Wall adapter), the WM8350 seamlessly transitions from battery power (a single-cell Lithium battery) to the applicable external supply. The battery charger is then activated, all internal power for the device is drawn from the appropriate external power source and the battery is disconnected from the load. Maximum battery charge current and charge time are programmable. The USB power manager provides accurate current limiting for the USB pin under all conditions. The hot-swap outputs (LDOs in current-limited 'Switch Mode' operation) are ideal for powering memory cards and other devices that can be inserted while the system is fully powered.

The integrated Hi-Fi stereo CODEC incorporates preamps and a low-noise bias voltage for differential microphones, and flexible pseudo-differential drivers for headphone and differential/single-ended line outputs. External component requirements are reduced as no separate microphone or headphone amplifiers are required. Digital filter options are available in the ADC and DAC paths, to cater for application filtering. The WM8350 is capable of operating without any external clock, as it can derive all required clocks from its internal crystal oscillator, RC clock, and Frequency Locked Loop. An external low jitter clock may be required in some applications for high performance audio.

**BLOCK DIAGRAM**



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








## 1 PIN CONFIGURATION

|   | 1     | 2       | 3      | 4     | 5            | 6     | 7       | 8      | 9     | 10     | 11      | 12     | 13      |
|---|-------|---------|--------|-------|--------------|-------|---------|--------|-------|--------|---------|--------|---------|
| A | VP5   | PG5     | OP     | PV1   | L1           | PG1   | PG6     | L6     | PV6   | FB6    | GPIO12  | FB2    | PG2     |
| B | L5    | NGATE5  | IP     | PV1   | L1           | PG1   | PG6     | L6     | PV6   | PVDD   | GPIO10  | NGATE2 | VP2     |
| C | L4    | PG4     | FB4    | FB5   | LINEDCD<br>C | FB1   | GND     | GND    | AUX4  | GPIO11 | PGND    | PG3    | L2      |
| D | PV4   | BATT    | HIVDD  | N/A   | N/A          | N/A   | N/A     | N/A    | N/A   | N/A    | FB3     | PV3    | L3      |
| E | BATT  | BATT    | WALLFB | N/A   | N/A          | N/A   | N/A     | N/A    | N/A   | N/A    | ISINKA  | ISINKB | SINKGND |
| F | LINE  | LINE    | LINE   | N/A   | N/A          | GND   | GND     | GND    | N/A   | N/A    | VOUT4   | LDOVDD | VINB    |
| G | USB   | USB     | USB    | N/A   | N/A          | GND   | GND     | GND    | N/A   | N/A    | VOUT2   | VOUT3  | VINA    |
| H | VRTC  | LINEINT | CREF   | N/A   | N/A          | GND   | GND     | GND    | N/A   | N/A    | AUX1    | VOUT1  | AUX3    |
| J | CONF0 | X1      | RREF   | N/A   | N/A          | N/A   | N/A     | N/A    | N/A   | N/A    | OUT1R   | HPCOM  | AUX2    |
| K | CONF1 | ON      | X2     | N/A   | N/A          | N/A   | N/A     | N/A    | N/A   | N/A    | OUT1L   | OUT4   | HPVDD   |
| L | GPIO0 | /RST    | SWVRTC | IRQ   | GPIO5        | GPIO8 | GPIO9   | BCLK   | LRCLK | IN3L   | IN1LN   | OUT3   | HPGND   |
| M | GPIO2 | GPIO1   | SDA    | GPIO6 | DGND         | MCLK  | ADCDATA | AVDD   | IN3R  | INL2   | MICBIAS | OUT2R  | OUT2L   |
| N | GPIO3 | SCL     | GPIO4  | GPIO7 | DCVDD        | DBVDD | DACDATA | REFGND | VMID  | IN1LP  | INR2    | IN1RP  | IN1RN   |

### 7mm x 7mm BGA1Z

Notes: Pin names beginning with a lower-case "n" indicate that the pin is active low.  
Colour coding indicates function of pins in typical usage:

|   |                               |
|---|-------------------------------|
|  | DC-DC converters              |
|  | LDO voltage regulators        |
|  | Power management functions    |
|  | Analogue pins for audio codec |
|  | Digital pins for audio codec  |
|  | Quiet ground                  |
|  | Others                        |

## 2 ORDERING INFORMATION

| ORDER CODE   | TEMPERATURE RANGE | PACKAGE   | MOISTURE SENSITIVITY LEVEL | PEAK SOLDERING TEMPERATURE |
|--------------|-------------------|---|----------------------------|----------------------------|
| WM8350GEB/V  | -25°C to +85°C    | 129-ball BGA (7 x 7 mm)<br>(Pb-free)                | MSL3                       | 260°C                      |
| WM8350GEB/RV | -25°C to +85°C    | 129-ball BGA (7 x 7 mm)<br>(Pb-free, tape and reel) | MSL3                       | 260°C                      |

### Note:

Reel quantity = 2,200

### 3 PIN DESCRIPTION

**Notes:**

Pins are listed in alphabetical order by name.

| NAME    | LOCATION(S)                                | TYPE            | POWER DOMAIN | DESCRIPTION   |
|---------|--|-----------------|--------------|---|
| ADCDATA | M7   | Digital Output  | DBVDD        | Digital audio output (typically from on-chip audio ADC to external IC)  |
| AUX1    | H11  | Analogue Input  | LINE         | Auxiliary ADC input AUX1<br>(Special function for connection to temperature-sensing NTC resistor in battery pack) |
| AUX2    | J13  | Analogue Input  | LINE         | Auxiliary ADC input AUX2  |
| AUX3    | H13  | Analogue Input  | LINE         | Auxiliary ADC input AUX3  |
| AUX4    | C9   | Analogue Input  | LINE         | Auxiliary ADC input AUX4  |
| AVDD    | M8   | Supply          |              | Analogue supply for audio CODEC   |
| BATT    | E1, E2, D2                                 | Analogue I/O    |              | Main battery power connection (can draw power or charge battery)  |
| BCLK    | L8   | Digital I/O     | DBVDD        | Bit clock signal for digital audio interface  |
| CREF    | H3   | Analogue Output | VRTC         | Decoupling for VREF reference voltage (connect capacitor here)  |
| CONF0   | J1   | Digital Input   | VRTC         | Start-up configuration pin 0  |
| CONF1   | K1   | Digital Input   | VRTC         | Start-up configuration pin 1  |
| DACDATA | N7   | Digital Input   | DBVDD        | Digital audio input (typically from external IC to on-chip audio DAC)   |
| DCVDD   | N5   | Supply          |              | Digital core supply; powers digital core of audio CODEC   |
| DBVDD   | N6   | Supply          |              | Digital I/O buffer supply; powers digital audio interface, control interface and pins GPIO4 to GPIO9              |
| DGND    | M5   | Supply          |              | Digital ground; return path for DCVDD and DBVDD supplies  |
| FB1     | C6   | Analogue Input  | PV1          | DC-DC1 feedback pin   |
| FB2     | A12  | Analogue Input  | VP2          | DC-DC2 feedback pin   |
| FB3     | D11  | Analogue Input  | PV3          | DC-DC3 feedback pin   |
| FB4     | C3   | Analogue Input  | PV4          | DC-DC4 feedback pin   |
| FB5     | C4   | Analogue Input  | VP5          | DC-DC5 feedback pin   |
| FB6     | A10  | Analogue Input  | PV6          | DC-DC6 feedback pin   |
| GND     | F6, F7, F8, G6, G7, G8, H6, H7, H8, C7, C8 | Supply          |              | Quiet ground connection for audio CODEC.<br>Note that DC-DC Converters use a separate ground connection.          |
| GPIO0   | L1   | Digital I/O     | VRTC         | General Purpose Input/Output pin 0  |
| GPIO1   | M2   | Digital I/O     | VRTC         | General Purpose Input/Output pin 1  |
| GPIO2   | M1   | Digital I/O     | VRTC         | General Purpose Input/Output pin 2  |
| GPIO3   | N1   | Digital I/O     | VRTC         | General Purpose Input/Output pin 3  |
| GPIO4   | N3   | Digital I/O     | DBVDD        | General Purpose Input/Output pin 4  |
| GPIO5   | L5   | Digital I/O     | DBVDD        | General Purpose Input/Output pin 5  |
| GPIO6   | M4   | Digital I/O     | DBVDD        | General Purpose Input/Output pin 6  |
| GPIO7   | N4   | Digital I/O     | DBVDD        | General Purpose Input/Output pin 7  |
| GPIO8   | L6   | Digital I/O     | DBVDD        | General Purpose Input/Output pin 8  |
| GPIO9   | L7   | Digital I/O     | DBVDD        | General Purpose Input/Output pin 9  |
| GPIO10  | B11  | Digital I/O     | LINE         | General Purpose Input/Output pin 10   |
| GPIO11  | C10  | Digital I/O     | LINE         | General Purpose Input/Output pin 11   |
| GPIO12  | A11  | Digital I/O     | LINE         | General Purpose Input/ Output pin 12  |
| HIVDD   | D3   | Analogue Output |              | Analogue output from power management unit which determines highest supply from Line, Battery or USB.             |
| HPCOM   | J12  | Analogue Input  | HPVDD        | Headphone output amplifier noise compensation input   |
| HPGND   | L13  | Supply          | HPVDD        | Headphone ground; return path for HPVDD supply  |

| NAME     | LOCATION(S) | TYPE                      | POWER DOMAIN | DESCRIPTION  |
|----------|-------------|---------------------------|--------------|--|
| HPVDD    | K13         | Supply                    |              | Headphone supply – powers the analogue outputs OUT1L, OUT1R, OUT2L, OUT2R, OUT3 and OUT4 |
| IN1LN    | L11         | Analogue Input            | AVDD         | Inverting input for left microphone channel  |
| IN1LP    | N10         | Analogue Input            | AVDD         | Non-inverting input 1 for left microphone channel  |
| IN1RN    | N13         | Analogue Input            | AVDD         | Inverting input for right microphone channel   |
| IN1RP    | N12         | Analogue Input            | AVDD         | Non-inverting input 1 for right microphone channel                                       |
| IN2L     | M10         | Analogue Input            | AVDD         | Non-inverting input 2 for left microphone channel  |
| IN2R     | N11         | Analogue Input            | AVDD         | Non-inverting input 2 for right microphone channel                                       |
| IN3L     | L10         | Analogue Input            | AVDD         | Auxiliary input for analogue audio signals (left channel)                                |
| IN3R     | M9          | Analogue Input            | AVDD         | Auxiliary input for analogue audio signals (right channel)                               |
| IP       | B3          | Analogue Input            |              | Power input to current limit switch  |
| ISINKA   | E11         | Analogue Output           | LDOVDD       | Constant-current LED driver A  |
| ISINKB   | E12         | Analogue Output           | LDOVDD       | Constant-current LED driver B  |
| L1       | A5, B5      | Analogue I/O              | PV1          | DC-DC1 inductor connection   |
| L2       | C13         | Analogue I/O              | VP2          | DC-DC2 inductor connection   |
| L3       | D13         | Analogue I/O              | PV3          | DC-DC3 inductor connection   |
| L4       | C1          | Analogue I/O              | PV4          | DC-DC4 inductor connection   |
| L5       | B1          | Analogue I/O              | VP5          | DC-DC5 inductor connection   |
| L6       | A8, B8      | Analogue I/O              | PV6          | DC-DC6 inductor connection   |
| LDOVDD   | F12         | Supply                    |              | LDO amplifier supply voltage   |
| LINEDCDC | C5          | Supply                    |              | Supply connection for DC-DC 1, 4 and 5 control circuits                                  |
| LINEINT  | H2          | Supply                    |              | Supply connection for Internal Reference circuits  |
| LINE     | F1, F2, F3  | Supply                    |              | LINE supply connection   |
| LRCLK    | L9          | Digital I/O               | DBVDD        | Word clock (left/right clock) signal for digital audio interface                         |
| MCLK     | M6          | Digital I/O               | DBVDD        | Master Clock (may be generated internally or externally)                                 |
| MICBIAS  | M11         | Analogue Output           | AVDD         | Low-noise bias voltage for condenser microphones (connect decoupling capacitor here)     |
| NGATE2   | B12         | Analogue Output           | VP2          | DC-DC2 connection to gate of external power FET  |
| NGATE5   | B2          | Analogue Output           | VP5          | DC-DC5 connection to gate of external power FET  |
| IRQ      | L4          | Digital Output open-drain | DBVDD        | Interrupt signal from WM8350 to host processor   |
| ON       | K2          | Digital Input             | VRTC         | Connection for power-on switch   |
| /RST     | L2          | Digital Output open-drain | DBVDD        | System Reset Signal (active low)   |
| OP       | A3          | Analogue Output           |              | Power output from current limit switch   |
| OUT1L    | K11         | Analogue Output           | AVDD         | Left channel analogue audio output 1   |
| OUT2L    | M13         | Analogue Output           | AVDD         | Left channel analogue audio output 2   |
| OUT1R    | J11         | Analogue Output           | AVDD         | Right channel analogue audio output 1  |
| OUT2R    | M12         | Analogue Output           | AVDD         | Right channel analogue audio output 2  |
| OUT3     | L12         | Analogue Output           | AVDD         | Analogue audio output 3 (or pseudo-ground output for capacitor-less headphone outputs)   |
| OUT4     | K12         | Analogue Output           | AVDD         | Analogue audio output 4  |
| PG1      | A6, B6      | Supply                    |              | DC-DC1 power ground  |
| PG2      | A13         | Supply                    |              | DC-DC2 power ground  |
| PG3      | C12         | Supply                    |              | DC-DC3 power ground  |
| PG4      | C2          | Supply                    |              | DC-DC4 power ground  |
| PG5      | A2          | Supply                    |              | DC-DC5 power ground  |
| PG6      | A7, B7      | Supply                    |              | DC-DC6 power ground  |
| PGND     | C11         | Supply                    |              | Ground connection  |
| PV1      | A4, B4,     | Supply                    |              | DC-DC1 line or battery power input   |
| PV3      | D12         | Supply                    |              | DC-DC3 line or battery power input   |
| PV4      | D1          | Supply                    |              | DC-DC4 line or battery power input   |

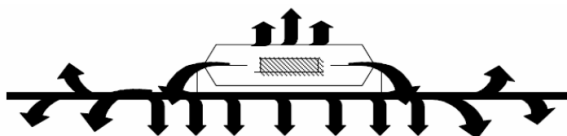
| NAME    | LOCATION(S) | TYPE            | POWER DOMAIN | DESCRIPTION  |
|---------|-------------|-----------------|--------------|--|
| PV6     | A9, B9      | Supply          |              | DC-DC6 power input   |
| PVDD    | B10         | Supply          |              | Supply connection for DC-DC 2, 3 and 6 control circuits  |
| REFGND  | N8          | Supply          |              | Reference ground for audio ADC and DAC   |
| RREF    | J3          | Analogue Output |              | Connection for external 100kΩ current reference resistor   |
| SCLK    | N2          | Digital Input   | DBVDD        | Clock signal for 2-wire serial control interface (5V Tolerant)   |
| SDATA   | M3          | Digital I/O     | DBVDD        | Data line for 2-wire serial control interface (5V Tolerant)  |
| SINKGND | E13         | Supply          |              | Ground connection for ISINKA and ISINKB  |
| SWVRTC  | L3          | Analogue Output | VRTC         | Switchable VRTC output. Typically used for battery temperature monitoring  |
| USB     | G1, G2, G3  | Supply          |              | Connection to USB power rail   |
| VINA    | G13         | Supply          |              | Input to voltage regulators LDO1 and LDO2  |
| VINB    | F13         | Supply          |              | Input to voltage regulators LDO3 and LDO4  |
| VMID    | N9          | Analogue I/O    | AVDD         | Reference voltage (normally AVDD/2) for audio CODEC (connect capacitor here)   |
| VOUT1   | H12         | Analogue Output | VINA         | Output of voltage regulator LDO1   |
| VOUT2   | G11         | Analogue Output | VINA         | Output of voltage regulator LDO2   |
| VOUT3   | G12         | Analogue Output | VINB         | Output of voltage regulator LDO3   |
| VOUT4   | F11         | Analogue Output | VINB         | Output of voltage regulator LDO4   |
| VP2     | B13         | Supply          |              | DC-DC2 power input   |
| VP5     | A1          | Supply          |              | DC-DC5 power input   |
| VRTC    | H1          | Supply          |              | Backup power connection (WM8350 can draw power from this pin or re-charge the backup power source)                             |
| WALLFB  | E3          | Analogue Input  | LINE         | Connection to Wall feedback  |
| X1      | J2          | Analogue Input  | VRTC         | Connection for 32.768kHz crystal (input to oscillator from crystal) or 32.768kHz external clock input (when not using crystal) |
| X2      | K3          | Analogue Output | VRTC         | Connection for 32.768kHz crystal (output from oscillator to crystal)   |

## 4 THERMAL CHARACTERISTICS

Thermal analysis must be performed in the intended application to prevent the WM8350 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the nine central GND balls through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air:

- Package top to air (radiation).
- Package bottom to PCB (radiation).
- Package leads to PCB (conduction).



The temperature rise  $T_R$  is given by  $T_R = P_D * \Theta_{JA}$

- $P_D$  is the power dissipated by the device.
- $\Theta_{JA}$  is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air.
- For WM8350,  $\Theta_{JA} = 32^\circ\text{C/W}$

The junction temperature  $T_J$  is given by  $T_J = T_A + T_R$

- $T_A$ , is the ambient temperature.

The worst case conditions are when the WM8350 is operating in a high ambient temperature, with low supply voltage, high duty cycle and high output current. Under such conditions, it is possible that the heat dissipated could exceed the maximum junction temperature of the device. Care must be taken to avoid this situation. An example calculation of the junction temperature is given below.

- $P_D = 1\text{W}$  (example figure)
- $\Theta_{JA} = 32^\circ\text{C/W}$
- $T_R = P_D * \Theta_{JA} = 32^\circ\text{C}$
- $T_A = 85^\circ\text{C}$  (example figure)
- $T_J = T_A + T_R = 117^\circ\text{C}$

The minimum and maximum operating junction temperatures for the WM8350 are quoted in Section 5. The maximum junction temperature is  $125^\circ\text{C}$ . Therefore, the junction temperature in the above example is within the operating limits of the WM8350.

## 5 ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The WM8350 has been classified as MSL3.

| CONDITION   | MIN                   | MAX          |
|---|-----------------------|--------------|
| BATT, LINE and USB voltage  | -0.3V                 | +7V          |
| Input voltage for LDO regulators (pins VINA, VINB)                | -0.3V                 | +7V          |
| Analogue supply voltages (AVDD, HPVDD)                            | -0.3V                 | +4.5V        |
| Digital supply voltages (DCVDD, DBVDD)                            | -0.3V                 | +4.5V        |
| Voltage range for CODEC analogue inputs                           | -0.3V                 | AVDD + 0.3V  |
| Voltage range for digital inputs                                  | -0.3V                 | DBVDD + 0.3V |
| Master Clock Frequency<br>(When MCLK_DIV set to divide by 2)      |                       | 37MHz        |
| Operating Temperature Range, T <sub>A</sub>                       | -25°C                 | +85°C        |
| Junction Temperature, T <sub>J</sub>                              | -20°C                 | +125°C       |
| Thermal Impedance Junction to Ambient, θ <sub>JA</sub>            |                       | 32°C/W       |
| Storage temperature prior to soldering                            | 30°C max / 60% RH max |              |
| Storage temperature after soldering                               | -65°C                 | +150°C       |
| Soldering temperature (10 seconds)                                |                       | +260°C       |
| <b>Note:</b> These ratings assume that all ground pins are at 0V. |                       |              |

## 6 RECOMMENDED OPERATING CONDITIONS

| PARAMETER                     | SYMBOL   | MIN  | TYP | MAX  | UNITS |
|-------------------------------|--|------|-----|------|-------|
| Digital Supply Range (Core)   | DCVDD  | 1.71 |     | 3.6  | V     |
| Digital Supply Range (Buffer) | DBVDD  | 1.71 |     | 3.6  | V     |
| Headphone Supply Range        | HPVDD  | 2.5  |     | 3.6  | V     |
| Analogue Supply Range         | AVDD   | 2.5  |     | 3.6  | V     |
| Line Input Source             | LINE   | 2.95 |     | 5.5  | V     |
| Battery Input Source          | BATT   | 2.95 |     | 4.2  | V     |
| USB Input Source              | USB  | 4.75 |     | 5.25 | V     |
| LDO Input Source              | VINA, VINB   | 0    |     | 5.5  | V     |
| Ground                        | GND, PGND, DGND, HPGND,<br>REFGND, PG1, PG2, PG3,<br>PG4, PG5, PG6 |      | 0   |      | V     |

## 7 ELECTRICAL CHARACTERISTICS

### 7.1 HI-FI AUDIO CODEC

#### Test Conditions

DCVDD = 1.8V, AVDD = HPVDD = 3.3V, T<sub>A</sub> = +25°C, 1kHz signal, f<sub>s</sub> = 48kHz, 24-bit audio data unless otherwise stated.

| PARAMETER   | SYMBOL                | TEST CONDITIONS                            | MIN | TYP       | MAX   | UNIT         |
|---|-----------------------|--|-----|-----------|-------|--------------|
| <b>Microphone Preamp Inputs (IN1LP, IN1LN, IN1RP, IN1RN)</b>                                |                       |  |     |           |       |              |
| Full-scale Input Signal Level (0dB) – note this changes with AVDD                           | V <sub>INFS</sub>     |  |     | 1<br>0    |       | V rms<br>dBV |
| Mic preamp equivalent input noise   | At<br>35.25dB<br>gain |  |     | 150       |       | μV           |
| Input resistance  | R <sub>MICIN</sub>    | Gain set to 35.25dB                        |     | 2.3       |       | kΩ           |
| Input resistance  | R <sub>MICIN</sub>    | Gain set to 0dB                            |     | 64        |       | kΩ           |
| Input resistance  | R <sub>MICIN</sub>    | Gain set to -12dB                          |     | 101       |       | kΩ           |
| Input Capacitance   | C <sub>MICIN</sub>    |  |     | 2         |       | pF           |
| Recommended decoupling cap  | C <sub>DECOUP</sub>   |  |     | 0.33      |       | μF           |
| <b>MIC Programmable Gain Amplifier (PGA)</b>  |                       |  |     |           |       |              |
| Programmable Gain   |                       |  | -12 |           | 35.25 | dB           |
| Programmable Gain Step Size   |                       | Monotonic                                  |     | 0.75      |       | dB           |
| Mute Attenuation  |                       |  |     | -90       |       | dB           |
| <b>Selectable Input Gain Boost (0/+20dB)</b>  |                       |  |     |           |       |              |
| Gain Boost  |                       |  | 0   |           | 20    | dB           |
| <b>Auxiliary Analogue Inputs (IN3L, IN3R)</b>   |                       |  |     |           |       |              |
| Full-scale Input Signal Level (0dB) – note this changes with AVDD                           | V <sub>INFS</sub>     |  |     | 1.0<br>0  |       | V rms<br>dBV |
| PGA gain range to summer  |                       |  | -12 |           | +6    | dB           |
| PGA step size to summer   |                       |  |     | 3         |       | dB           |
| Input Resistance  | R <sub>AUXIN</sub>    |  |     | 32        |       | kΩ           |
| Input Capacitance   | C <sub>AUXIN</sub>    |  |     | 10        |       | pF           |
| <b>Analogue to Digital Converter (ADC)</b>  |                       |  |     |           |       |              |
| Signal to Noise Ratio (Note 1, 2)   |                       | A-weighted, 0dB gain                       | 86  | 95        |       | dB           |
| Total Harmonic Distortion (Note 4)  |                       | -2dBV Input                                | -75 | -83       |       | dB           |
| <b>Digital to Analogue Converter (DAC) to Line-Out (OUT1L, OUT1R with 10kΩ / 50pF load)</b> |                       |  |     |           |       |              |
| Full-scale output   |                       | PGA gains set to 0dB                       |     | HPVDD/3.3 |       | V rms        |
| Signal to Noise Ratio (Note 1, 2)   | SNR                   | A-weighted                                 | 90  | 95        |       | dB           |
| Total Harmonic Distortion (Note 3)  | THD+N                 | R <sub>L</sub> = 10kΩ<br>full-scale signal | -75 | -81       |       | dB           |
| Channel Separation (Note 4)   |                       | 1kHz signal                                |     | 89        |       | dB           |
| <b>Output Mixers</b>  |                       |  |     |           |       |              |
| PGA gain range into mixer   |                       |  | -15 | 0         | +6    | dB           |
| PGA gain step into mixer  |                       |  |     | 3         |       | dB           |
| <b>Analogue Output PGAs (OUT1L, OUT1R, OUT2L, OUT2R)</b>                                    |                       |  |     |           |       |              |
| Programmable Gain range   |                       |  | -57 | 0         | +6    | dB           |
| Programmable Gain step size   |                       | Monotonic                                  |     | 1         |       | dB           |
| Mute attenuation  |                       | 1KHz, full scale signal                    |     | 78        |       | dB           |



**Test Conditions**DCVDD = 1.8V, AVDD = HPVDD = 3.3V, T<sub>A</sub> = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

| PARAMETER  | SYMBOL               | TEST CONDITIONS   | MIN       | TYP       | MAX       | UNIT             |
|--|----------------------|---|-----------|-----------|-----------|------------------|
| <b>Headphone Output (OUT1L, OUT1R, OUT2L, OUT2R)</b> |                      |   |           |           |           |                  |
| 0dB full scale output voltage                        |                      |   |           | HPVDD/3.3 |           | V <sub>rms</sub> |
| Signal to Noise Ratio                                | SNR                  | A-weighted  | 87        | 96        |           | dB               |
| Total Harmonic Distortion (Note 3)                   | THD+N                | R <sub>L</sub> = 16Ω,<br>P <sub>o</sub> =20mW<br>HPVDD=3.3V | -65       | -72       |           | dB               |
|  |                      | R <sub>L</sub> = 32Ω,<br>P <sub>o</sub> =20mW<br>HPVDD=3.3V |           | -71       |           | dB               |
| <b>OUT3/OUT4 outputs (with 10kΩ / 50pF load)</b>     |                      |   |           |           |           |                  |
| Full-scale output                                    |                      |   |           | HPVDD/3.3 |           | V <sub>rms</sub> |
| Signal to Noise Ratio (Note 1, 2)                    | SNR                  | A-weighted  | 90        | 97        |           | dB               |
| Total Harmonic Distortion (Note 3)                   | THD                  | R <sub>L</sub> = 10kΩ<br>full-scale signal                  | -77       | -83       |           | dB               |
| Channel Separation (Note 4)                          |                      | 5kHz signal   |           | 80        |           | dB               |
| <b>Microphone Bias</b>                               |                      |   |           |           |           |                  |
| Bias Voltage   | V <sub>MICBIAS</sub> | MBVSEL=0  |           | 0.9*AVDD  |           | V                |
|  |                      | MBVSEL=1  |           | 0.75*AVDD |           | V                |
| Bias Current Source                                  | I <sub>MICBIAS</sub> |   |           | 3         |           | mA               |
| Output Noise Voltage                                 | V <sub>n</sub>       | 1kHz to 20kHz   |           | 24        |           | nV/√Hz           |
| <b>Digital Input / Output</b>                        |                      |   |           |           |           |                  |
| Input HIGH Level                                     | V <sub>IH</sub>      |   | 0.7×DBVDD |           |           | V                |
| Input LOW Level                                      | V <sub>IL</sub>      |   |           |           | 0.3×DBVDD | V                |
| Output HIGH Level                                    | V <sub>OH</sub>      | I <sub>OL</sub> =1mA  | 0.9×DBVDD |           |           | V                |
| Output LOW Level                                     | V <sub>OL</sub>      | I <sub>OH</sub> =1mA  |           |           | 0.1×DBVDD | V                |
| <b>Frequency Locked Loop (FLL)</b>                   |                      |   |           |           |           |                  |
| Reference clock frequency                            | F <sub>REF</sub>     |   | 0.032     |           | 22        | MHz              |
| <b>Jack Detect</b>                                   |                      |   |           |           |           |                  |
| Detection switch threshold                           | V <sub>IH</sub>      |   | 0.7×AVDD  |           |           | V                |
|  | V <sub>IL</sub>      |   |           |           | 0.3×AVDD  | V                |
| <b>HPCOM</b>   |                      |   |           |           |           |                  |
| Ground noise rejection                               | V <sub>IH</sub>      |   |           | 40        |           | dB               |
|  | V <sub>IL</sub>      |   |           | 40        |           | dB               |

**TERMINOLOGY**

1. Signal-to-noise ratio (dB) = SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) = DR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (E.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) = THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Channel Separation (dB) = Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.

## 7.2 DC-DC STEP UP CONVERTER ELECTRICAL CHARACTERISTICS

### Test Conditions

T<sub>A</sub> = +25°C unless otherwise noted.

| PARAMETER                     | SYMBOL               | CONDITIONS   | MIN             | TYP  | MAX          | UNITS |
|-------------------------------|----------------------|--|-----------------|------|--------------|-------|
| <b>DC-DC2 and DC-DC5</b>      |                      |  |                 |      |              |       |
| Input voltage range           | V <sub>IN</sub>      | when used as converter   | 2.7             | 3.7  | 5.5          | V     |
|                               |                      | when used as switch  | 1.2             |      |              |       |
| Output voltage range          | V <sub>OUT</sub>     | by default<br>(needs external component configuration)                 | V <sub>IN</sub> |      | 20<br>(30)   | V     |
| USB OTG output voltage        | V <sub>OUT,USB</sub> | V <sub>IN</sub> <4.5V; I <sub>OUT</sub> <100mA;<br>DCn_FBSRC [1:0]=11  |                 | 5.0  |              | V     |
| Output current                | I <sub>OUT</sub>     | V <sub>OUT</sub> =30V  | 0               |      | 25           | mA    |
|                               |                      | V <sub>OUT</sub> =20V<br>(DCn_ILIM_=1)                                 |                 |      | 40<br>(18)   |       |
|                               |                      | V <sub>OUT</sub> =5.0V<br>(DCn_ILIM_=1)                                |                 |      | 170<br>(100) |       |
| Switch resistance             | R <sub>ON</sub>      | V <sub>IN</sub> =3.3V; V <sub>OUT</sub> =3.2V; +25°C                   |                 | 0.26 |              | Ω     |
|                               |                      | V <sub>IN</sub> =1.8V; V <sub>OUT</sub> =1.7V; +25°C                   |                 | 0.41 |              |       |
|                               |                      | V <sub>IN</sub> =1.2V; V <sub>OUT</sub> =1.1V; +25°C                   |                 | 0.84 |              |       |
| Maximum switch current        | I <sub>SW,MAX</sub>  |  |                 |      | 700          | mA    |
| Switching frequency           | f <sub>CLK</sub>     |  |                 | 1.0  |              | MHz   |
| Maximum duty cycle            | D <sub>MAX</sub>     | V <sub>IN</sub> =3V; f <sub>CLK</sub> =1.0MHz                          |                 | 90   |              | %     |
| Efficiency                    | H                    | V <sub>IN</sub> =3.8V; V <sub>OUT</sub> =20V; I <sub>OUT</sub> =20mA   |                 | 75   |              | %     |
|                               |                      | V <sub>IN</sub> =3.8V; V <sub>OUT</sub> =5.0V; I <sub>OUT</sub> =100mA |                 | 88   |              |       |
| Quiescent current             | I <sub>DD</sub>      | Shutdown or switch configuration                                       |                 | 0.1  |              | μA    |
|                               |                      | active; no switching   |                 | 260  |              |       |
|                               |                      | active; pulse skipping   |                 | 260  |              |       |
| Regulated feedback voltage    | V <sub>FB</sub>      | DCn_FBSRC [1:0] = 00   |                 | 0.5  |              | V     |
|                               | V <sub>CURR</sub>    | DCn_FBSRC [1:0] = 01 or 10   |                 | 0.5  |              |       |
| Undervoltage detect           | V <sub>FB,UV</sub>   | below feedback voltage   |                 | 12   |              | %     |
|                               | V <sub>USB,UV</sub>  | DCn_FBSRC [1:0] = 11   |                 | 4.6  |              |       |
| Overvoltage detect            | V <sub>FB,OV</sub>   | above feedback voltage   |                 | 8    |              | %     |
|                               | V <sub>USB,OV</sub>  | DCn_FBSRC [1:0] = 11   |                 | 5.4  |              |       |
| Peak inductor current limit   | I <sub>PK</sub>      | V <sub>IN</sub> =3V; V <sub>OUT</sub> =90%;<br>DCn_ILIM_=1             |                 | 700  |              | mA    |
|                               |                      |  |                 | 450  |              |       |
| On resistance of NGATE driver | R <sub>NGATE</sub>   | P-Channel FET (I <sub>PFET</sub> =100mA)                               |                 | 4.6  |              | Ω     |
|                               |                      | N-Channel FET (I <sub>NFET</sub> =100mA)                               |                 | 4.9  |              |       |
| Input capacitor               | C <sub>IN</sub>      | X5R/X7R dielectric   | 1.0             | 2.2  |              | μF    |
| Inductor                      | L <sub>F</sub>       |  | -30%            | 10   | +30%         | μH    |
| Inductor current rating       | I <sub>SAT,Lf</sub>  |  | 500             |      |              | mA    |
|                               |                      | DCn_ILIM_=1  | 320             |      |              |       |
| Output capacitor              | C <sub>OUT</sub>     | DCn_FBSRC [1:0]= 00 or 11; V <sub>OUT</sub> =5V                        | 3.7             | 10   | 22           | μF    |
|                               |                      | DCn_FBSRC [1:0]= 00; V <sub>OUT</sub> =10V                             | 0.84            | 2.2  | 4.7          |       |
|                               |                      | DCn_FBSRC [1:0]= 00; V <sub>OUT</sub> =20V                             | 0.18            | 0.47 | 1.0          |       |
|                               |                      | DCn_FBSRC [1:0]= 01 or 10; V <sub>OUT</sub> =10V                       | 2.0             | 4.7  | 10           |       |
|                               |                      | DCn_FBSRC [1:0]= 01 or 10; V <sub>OUT</sub> =15V                       | 1.5             | 2.2  | 10           |       |
|                               |                      | DCn_FBSRC [1:0]= 01 or 10; V <sub>OUT</sub> =20V                       | 0.9             | 1.5  | 4.7          |       |

### 7.3 DC-DC STEP DOWN CONVERTER ELECTRICAL CHARACTERISTICS

#### Test Conditions

$V_{IN} = 3.7$ ,  $V_{OUT} = 1.8$ V,  $T_A = +25^\circ\text{C}$  unless otherwise noted.

| PARAMETER                 | SYMBOL           | CONDITIONS   |                     | MIN     | TYP   | MAX                | UNITS    |
|---------------------------|------------------|--|---------------------|---------|-------|--------------------|----------|
| <b>DC-DC1 and DC-DC6</b>  |                  |  |                     |         |       |                    |          |
| Input Voltage             | $V_{IN}$         |  |                     | 2.7     | 3.7   | 5.5                | V        |
| Output Voltage            | $V_{OUT}$        |  |                     | 0.85    |       | 3.4                | V        |
| VOUT Accuracy             | $V_{OUT}$        | $V_{IN} = 3.7$ V<br>$V_{OUT} = 0.85$ V / 1.8V<br>/ 3.4V                          | $I_{OUT} = 0.5$ A   | Active  |       | +/- 3.0            | %        |
|                           |                  |  | $I_{OUT} = 0.005$ A | Sleep   |       | -1.5<br>+4.5       |          |
| Line Regulation           | $V_{OUT\ LINE}$  | $V_{IN} = 2.7$ V to<br>5.5V<br>$V_{OUT} = 1.8$ V                                 | $I_{OUT} = 0.5$ A   | Active  |       | +/- 0.5            | %        |
|                           |                  |  | $I_{OUT} = 0.1$ A   | Standby |       | +/-<br>0.25        |          |
|                           |                  |  | $I_{OUT} = 0.005$ A | Sleep   |       | +/- 0.4<br>+/- 0.5 |          |
| Load Regulation           | $V_{OUT\ LOAD}$  | $I_{OUT} = 0.001$ A to 1A<br>$I_{OUT} = 0$ A to 0.1A<br>$I_{OUT} = 0$ A to 0.01A |                     | Active  |       | +/- 0.2            | %        |
|                           |                  |  |                     | Standby |       | +/- 0.2            |          |
|                           |                  |  |                     | Sleep   |       | +/- 0.3<br>+/- 0.5 |          |
| Quiescent Current         | $I_{Q\ ACTIVE}$  | Active (excluding switching losses)  |                     |         | 265   |                    | $\mu$ A  |
|                           | $I_{Q\ STANDBY}$ | Standby (excluding switching losses)   |                     |         | 115   |                    |          |
|                           | $I_{Q\ SLEEP}$   | Sleep  |                     |         | 25    |                    |          |
| Shutdown current          | $I_{SD}$         |  |                     |         | 0.01  |                    | $\mu$ A  |
| P-channel On Resistance   | $R_{DSP}$        | $V_{IN} = 3.7$ V, $I_{L(n)} = 100$ mA  |                     |         | 0.09  |                    | $\Omega$ |
| N-channel On Resistance   | $R_{DSN}$        | $V_{IN} = 3.7$ V, $I_{L(n)} = 100$ mA  |                     |         | 0.167 |                    | $\Omega$ |
| P-channel leakage current | $I_{LXP}$        | $V_{IN} = 3.7$ V, L(n) = GND   |                     |         | 0.01  |                    | $\mu$ A  |
| N-channel leakage current | $I_{LXN}$        | $V_{IN} = 3.7$ V, L(n) = 3.7V  |                     |         | 2.8   |                    | $\mu$ A  |
| Switching Frequency       | $f_{SW}$         |  |                     |         | 2.0   |                    | MHz      |

## Test Conditions

$V_{IN} = 3.7$ ,  $V_{OUT} = 1.8$ V,  $T_A = +25^\circ\text{C}$  unless otherwise noted.

| PARAMETER                 | SYMBOL           | CONDITIONS   |                                    | MIN     | TYP                | MAX                | UNITS    |
|---------------------------|------------------|--|------------------------------------|---------|--------------------|--------------------|----------|
| <b>DC-DC3 and DC-DC4</b>  |                  |  |                                    |         |                    |                    |          |
| Input Voltage             | $V_{IN}$         |  |                                    | 2.7     | 3.7                | 5.5                | V        |
| Output Voltage            | $V_{OUT}$        |  |                                    | 0.85    |                    | 3.4                | V        |
| VOU Accuracy              | $V_{OUT}$        | $V_{IN} = 3.7$ V<br>$V_{OUT} = 0.85$ V / 1.8V / 3.4V                               | $I_{OUT} = 0.5$ A                  | Active  |                    | +/- 3.0            | %        |
|                           |                  |  | $I_{OUT} = 0.005$ A                | Sleep   |                    | -1.5<br>+4.5       |          |
| Line Regulation           | $V_{OUT\ LINE}$  | $V_{IN} = 2.7$ V to 5.5V<br>$V_{OUT} = 1.8$ V                                      | $I_{OUT} = 0.25$ A                 | Active  |                    | +/- 0.4            | %        |
|                           |                  |  | $I_{OUT} = 0.025$ A<br>(100mA lim) | Standby |                    | +/- 0.18           |          |
|                           |                  |  | $I_{OUT} = 0.005$ A                | Sleep   |                    | +/- 0.4<br>+/- 0.5 |          |
| Load Regulation           | $V_{OUT\ LOAD}$  | $I_{OUT} = 1$ mA to 500mA<br>$I_{OUT} = 0$ A to 0.05A<br>$I_{OUT} = 0$ A to 0.010A | Active                             |         | +/- 0.5            | %                  |          |
|                           |                  |  | Standby                            |         | +/- 0.2            |                    |          |
|                           |                  |  | Sleep                              |         | +/- 0.3<br>+/- 0.5 |                    |          |
| Quiescent Current         | $I_{Q\ ACTIVE}$  | Active (excluding switching losses)  |                                    |         | 318                |                    | $\mu$ A  |
|                           | $I_{Q\ STANDBY}$ | Standby (excluding switching losses)   |                                    |         | 120                |                    |          |
|                           | $I_{Q\ SLEEP}$   | Sleep  |                                    |         | 25                 |                    |          |
| Shutdown current          | $I_{SD}$         |  |                                    |         | 0.01               |                    | $\mu$ A  |
| P-channel On Resistance   | $R_{DSP}$        | $V_{IN} = 3.7$ V, $I_{L(n)} = 100$ mA  |                                    |         | 0.29               |                    | $\Omega$ |
| N-channel On Resistance   | $R_{DSN}$        | $V_{IN} = 3.7$ V, $I_{L(n)} = 100$ mA  |                                    |         | 0.2                |                    | $\Omega$ |
| P-channel leakage current | $I_{LXP}$        | $V_{IN} = 3.7$ V, $L(n) = GND$   |                                    |         | 0.02               |                    | $\mu$ A  |
| N-channel leakage current | $I_{LXN}$        | $V_{IN} = 3.7$ V, $L(n) = 3.7$ V   |                                    |         | 1.4                |                    | $\mu$ A  |
| Switching Frequency       | $f_{SW}$         |  |                                    |         | 2.0                |                    | MHz      |

## 7.4 LDO REGULATOR ELECTRICAL CHARACTERISTICS

### Test Conditions

$V_{IN} = 3.7$ ,  $V_{OUT} = 1.8V$ ,  $T_A = +25^\circ C$  unless otherwise noted.

| PARAMETER                                    | SYMBOL     | TEST CONDITIONS                       | MIN | TYP                              | MAX        | UNIT     |
|--|------------|---------------------------------------|-----|----------------------------------|------------|----------|
| <b>LDO1 to LDO4 (WM8350 in ACTIVE State)</b> |            |                                       |     |                                  |            |          |
| Input Voltage                                | $V_{IN}$   | After start-up                        | 1.6 | 3.7                              | 5.5        | V        |
| Output voltage                               | $V_{OUTn}$ |                                       | 0.9 |                                  | 3.3        | V        |
| Regulation Accuracy                          |            |                                       |     | +/-3.3                           |            | %        |
| Dropout Voltage                              |            | 100mA, $V_{IN} < 1.8V$                |     | 200                              |            | mV       |
|  |            | 100mA, $V_{IN} < 2.7V$                |     | 700                              |            |          |
| Load current                                 |            |                                       |     | 100                              | 150        | mA       |
| Quiescent Current                            |            |                                       | 27  |                                  | 1% of load | $\mu A$  |
| Leakage Current                              |            |                                       |     | <2.5                             |            | $\mu A$  |
| Power Supply Rejection Ratio                 | PSRR       | 1kHz, $V_{OUT} = 1.8V$ ,<br>25mA load |     | -50                              |            | dB       |
|  |            | 100Hz                                 |     |                                  |            |          |
| ON Resistance in switch mode                 | $R_{ON}$   | LDO <sub>n</sub> _SWI = 1             |     | 2                                | 3.5        | $\Omega$ |
| <b>LDO1 (WM8350 in OFF State)</b>            |            |                                       |     |                                  |            |          |
| Output Voltage                               | $V_{OUT1}$ |                                       |     | $0.95 \times V_{OUT1}$ in ACTIVE |            | V        |

## 7.5 BATTERY CHARGER

### Test Conditions

T<sub>A</sub> = +25°C unless otherwise noted.

| PARAMETER  | SYMBOL           | TEST CONDITIONS                                   | MIN  | TYP              | MAX  | UNIT |
|--|------------------|---|------|------------------|------|------|
| <b>General</b>   |                  |   |      |                  |      |      |
| Wall adaptor voltage   | LINE             | When charging from wall adaptor                   | 4.0  |                  | 5.5  | V    |
| USB voltage  | USB              | When charging from USB power rail                 | 4.0  |                  | 5.5  | V    |
| Target voltage   |                  | CHG_VSEL=00                                       | 4.0  | 4.05             | 4.1  | V    |
|  |                  | CHG_VSEL=01                                       | 4.05 | 4.1              | 4.15 |      |
|  |                  | CHG_VSEL=10                                       | 4.1  | 4.15             | 4.2  |      |
|  |                  | CHG_VSEL=11                                       | 4.15 | 4.2              | 4.25 |      |
| Defective battery threshold  |                  |   |      | 2.85             |      | V    |
| End of Charge Current  | EOC              | Programmable in register R168<br>CHG_EOC_SEL bits |      | 20 to 90         |      | mA   |
| <b>Trickle Charging</b>  |                  |   |      |                  |      |      |
| Trickle charge initiation threshold (WM8350 starts trickle charging when battery is below this threshold)  |                  |   |      | CHG_VSEL - 100mV |      | V    |
| 50mA trickle charge current  |                  | CHG_TRICKLE_SEL = 0 (default)                     |      | 36.6             |      | mA   |
| 100mA trickle charge current   |                  | CHG_TRICKLE_SEL = 1                               |      | 79.5             |      | mA   |
| <b>Fast Charging</b>   |                  |   |      |                  |      |      |
| Fast charge threshold (WM8350 can only fast-charge if battery is above this threshold)                     |                  |   |      | 3.1              |      | V    |
| Maximum fast-charge current  | I <sub>MAX</sub> |   |      | 750              |      | mA   |
| <b>Backup Battery (VRTC)</b>   |                  |   |      |                  |      |      |
| Backup battery charger output. (Note that this backup charger voltage also determines the UVLO threshold.) |                  |   | 2.5  | 2.7              | 2.9  | V    |

## 7.6 CURRENT LIMIT SWITCH

### Test Conditions

T<sub>A</sub> = +25°C unless otherwise noted.

| PARAMETER                         | CONDITION | MIN | TYP | MAX  | UNITS |
|-----------------------------------|-----------|-----|-----|------|-------|
| Maximum input voltage             |           | 2.7 |     | LINE | V     |
| On resistance (at 3.3V)           |           |     | 2.0 |      | Ω     |
| Current limit flag threshold      |           |     | 180 |      | mA    |
| Current limit                     |           |     | 215 |      | mA    |
| Quiescent current (EN but not ON) |           |     | 7   |      | μA    |
| Quiescent current (EN and ON)     |           |     |     |      | μA    |

## 7.7 LED DRIVERS

### Test Conditions

T<sub>A</sub> = +25°C unless otherwise noted.

| PARAMETER                     | SYMBOL | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|-------------------------------|--------|------------------|-----|-----|-----|------|
| <b>ISINKA, ISINKB</b>         |        |                  |     |     |     |      |
| Sink Current                  |        | duty cycle = 20% |     |     | 200 | mA   |
|                               |        | continuous       |     |     | 40  |      |
| <b>ISINKC, ISINKD, ISINKE</b> |        |                  |     |     |     |      |
| Sink Current                  |        |                  |     |     | 20  | mA   |
| Output voltage drop           |        | 10mA load        |     | 0.8 |     | V    |

## 7.8 GENERAL PURPOSE INPUTS / OUTPUTS (GPIO)

### Test Conditions

T<sub>A</sub> = +25°C unless otherwise noted.

| PARAMETER                              | SYMBOL          | TEST CONDITIONS | MIN                  | TYP | MAX                  | UNIT |
|--|-----------------|-----------------|----------------------|-----|----------------------|------|
| <b>GPIO0 to GPIO3</b>                  |                 |                 |                      |     |                      |      |
| Input HIGH Level                       | V <sub>IH</sub> |                 | 0.7×V <sub>RTC</sub> |     |                      | V    |
| Input LOW Level                        | V <sub>IL</sub> |                 |                      |     | 0.3×V <sub>RTC</sub> | V    |
| Output HIGH Level                      | V <sub>OH</sub> | sinking 2 mA    | 0.9×V <sub>RTC</sub> |     |                      | V    |
| Output LOW Level                       | V <sub>OL</sub> | sourcing 2 mA   |                      |     | 0.1×V <sub>RTC</sub> | V    |
| Sink / source current                  |                 |                 |                      |     |                      | mA   |
| Pull-up resistance to V <sub>RTC</sub> | R <sub>PU</sub> | GPn_PU = 1      |                      | 310 |                      | kΩ   |
| Pull-down resistance                   | R <sub>PD</sub> | GPn_PD = 1      |                      | 225 |                      | kΩ   |
| <b>GPIO4 to GPIO9</b>                  |                 |                 |                      |     |                      |      |
| Logic levels                           |                 | See Section 7.9 |                      |     |                      |      |
| Sink / source current                  |                 |                 |                      |     |                      | mA   |
| Pull-up resistance to DBVDD            | R <sub>PU</sub> | GPn_PU = 1      |                      | 220 |                      | kΩ   |
| Pull-down resistance                   | R <sub>PD</sub> | GPn_PD = 1      |                      | 144 |                      | kΩ   |
| <b>GPIO10 to GPIO12</b>                |                 |                 |                      |     |                      |      |
| Input HIGH Level                       | V <sub>IH</sub> |                 | 2.0                  |     |                      | V    |
| Input LOW Level                        | V <sub>IL</sub> |                 |                      |     | 0.9                  | V    |
| Output HIGH Level                      | V <sub>OH</sub> | sinking 2 mA    | 0.9×<br>LINE         |     |                      | V    |
| Output LOW Level                       | V <sub>OL</sub> | sourcing 2 mA   |                      |     | 0.1×<br>GPIO_VD<br>D | V    |
| Sink / source current                  |                 |                 |                      |     |                      | mA   |
| Pull-up resistance to LINE             | R <sub>PU</sub> | GPn_PU = 1      |                      | 250 |                      | kΩ   |
| Pull-down resistance                   | R <sub>PD</sub> | GPn_PD = 1      |                      | 135 |                      | kΩ   |

## 7.9 DIGITAL INTERFACES

### Test Conditions

T<sub>A</sub> = +25°C unless otherwise noted.

| PARAMETER   | SYMBOL          | TEST CONDITIONS | MIN       | TYP | MAX       | UNIT |
|---|-----------------|-----------------|-----------|-----|-----------|------|
| <b>SDA, SCLK, MCLK, BCLK, LRCLK, ADCDATA, DACDATA, GPIO4 to GPIO9</b> |                 |                 |           |     |           |      |
| Input HIGH Level  | V <sub>IH</sub> |                 | 0.7×DBVDD |     |           | V    |
| Input LOW Level   | V <sub>IL</sub> |                 |           |     | 0.3×DBVDD | V    |
| Output HIGH Level   | V <sub>OH</sub> | sinking 1mA     | 0.9×DBVDD |     |           | V    |
| Output LOW Level  | V <sub>OL</sub> | sourcing 1mA    |           |     | 0.1×DBVDD | V    |

## 7.10 AUXILIARY ADC

### Test Conditions

T<sub>A</sub> = +25°C unless otherwise noted.

| PARAMETER  | CONDITIONS  | SYMBOL              | MIN | TYP     | MAX                  | UNITS       |
|--|---|---------------------|-----|---------|----------------------|-------------|
| Input resistance<br>(AUX1,2,3,4, USB, LINE, BATT and CHIPTEMP)   | AUXADC_SCALEn [1:0] = 00  |                     | ∞   | ∞       | ∞                    | Ω           |
|  | AUXADC_SCALEn [1:0] = 01  |                     |     | 2.2     |                      | kΩ          |
|  | AUXADC_SCALEn [1:0] = 10  |                     | 330 |         | 660                  | kΩ          |
|  | AUXADC_SCALEn [1:0] = 11  |                     | 330 |         | 440                  | kΩ          |
| Input Voltage range.<br>AUX1,2,3,4,USB,LINE,BATT and CHIPTEMP<br>(V <sub>RTC</sub> = 2.7V & V <sub>LINE</sub> (max)= 5.5V, V <sub>BG</sub> =1.25V) | AUXADC_SCALEn [1:0] = 01<br>AUXADC_REF = 0  |                     |     |         | V <sub>BG</sub>      | V           |
|  | AUXADC_SCALEn [1:0] = 01<br>AUXADC_REF = 1  |                     |     |         | V <sub>RTC</sub>     | V           |
|  | AUXADC_SCALEn [1:0] = 10<br>AUXADC_REF = 0  |                     |     |         | 2 x V <sub>BG</sub>  | V           |
|  | AUXADC_SCALEn [1:0] = 10<br>AUXADC_REF = 1  |                     |     |         | 2 x V <sub>RTC</sub> | V           |
|  | AUXADC_SCALEn [1:0] = 11<br>AUXADC_REF = 0  |                     |     |         | V <sub>LINE</sub>    | V           |
|  | AUXADC_SCALEn [1:0] = 11<br>AUXADC_REF = 1  |                     |     |         | 4 x V <sub>BG</sub>  | V           |
| Input capacitance<br>(AUX1,2,3,4, USB, LINE, BATT and CHIPTEMP)  | Input is selected<br>(INPUT_SELECT) and<br>AUXADC_SCALEn [1:0] not = 00   |                     |     | 2.08    |                      | pF          |
| V <sub>RTC</sub> quiescent current   | AUX_RBMODE = 0,<br>AUXADC_ENA = 1   |                     |     | 140     |                      | μA          |
| V <sub>RTC</sub> quiescent current   | AUX_RBMODE = 1<br>AUXADC_ENA = 1  |                     |     | 151     |                      | μA          |
| LINE_INT quiescent current   |   |                     |     |         | <<1                  | mA          |
| ADCCLK frequency   |   | f <sub>AUXCLK</sub> | 400 | 470/512 | 800                  | kHz         |
| ADC Resolution   |   |                     |     | 12      |                      | bits        |
| ADC Conversion Time  |   |                     |     | 13      |                      | CLK periods |
| Aux ADC accuracy   | Non-calibrated (calibration possible using the VBG input on AUX3). 1% of this variation due to BG variation over temperature. |                     |     | 2.2     |                      | %           |



## 8 TYPICAL POWER CONSUMPTION

### ADC Master Mode

#### 48kHz

| AVDD<br>(V) | HPVDD<br>(V) | DBVDD<br>(V) | DCVDD<br>(V) | IAVDD<br>(mA) | IHPVDD<br>(mA) | IDB<br>(mA) | IDC<br>(mA) | Power Consumption<br>(mW) |
|-------------|--------------|--------------|--------------|---------------|----------------|-------------|-------------|---------------------------|
| 2.5         | 2.5          | 1.71         | 1.71         | 3.6           | 0.000014       | 0.55        | 2.3         | 13.87                     |
| 3.3         | 3.3          | 3.3          | 1.8          | 4.46          | 0.00003        | 1.085       | 2.4         | 22.62                     |
| 3.6         | 3.6          | 3.6          | 3.6          | 4.79          | 0.000028       | 1.18        | 5.67        | 41.90                     |

### ADC Master Mode

#### 1kHz Tone 100mVpk-pk

| AVDD<br>(V) | HPVDD<br>(V) | DBVDD<br>(V) | DCVDD<br>(V) | IAVDD<br>(mA) | IHPVDD<br>(mA) | IDB<br>(mA) | IDC<br>(mA) | Power Consumption<br>(mW) |
|-------------|--------------|--------------|--------------|---------------|----------------|-------------|-------------|---------------------------|
| 2.5         | 2.5          | 1.71         | 1.71         | 3.6           | 0.00009        | 0.5         | 2.14        | 13.51                     |
| 3.3         | 3.3          | 3.3          | 1.8          | 4.4           | 0.00016        | 1.02        | 2.3         | 22.03                     |
| 3.6         | 5.5          | 3.6          | 3.6          | 4.8           | 0.00008        | 1.12        | 5.3         | 40.39                     |

### ADC Master Mode

#### Pink Noise

| AVDD<br>(V) | HPVDD<br>(V) | DBVDD<br>(V) | DCVDD<br>(V) | IAVDD<br>(mA) | IHPVDD<br>(mA) | IDB<br>(mA) | IDC<br>(mA) | Power Consumption<br>(mW) |
|-------------|--------------|--------------|--------------|---------------|----------------|-------------|-------------|---------------------------|
| 2.5         | 2.5          | 1.71         | 1.71         | 3.58          | 0.000004       | 0.51        | 2.1         | 13.41                     |
| 3.3         | 3.3          | 3.3          | 1.8          | 4.43          | 0.00026        | 1           | 2.2         | 21.88                     |
| 3.6         | 5.5          | 3.6          | 3.6          | 4.8           | 0.000085       | 1.1         | 5.2         | 39.96                     |

### ADC Slave Mode

#### 44.1kHz

| AVDD<br>(V) | HPVDD<br>(V) | DBVDD<br>(V) | DCVDD<br>(V) | IAVDD<br>(mA) | IHPVDD<br>(mA) | IDB<br>(mA) | IDC<br>(mA) | Power Consumption<br>(mW) |
|-------------|--------------|--------------|--------------|---------------|----------------|-------------|-------------|---------------------------|
| 2.5         | 2.5          | 1.71         | 1.71         | 3.4           | 0.00002        | 0.02        | 2.2         | 12.30                     |
| 3.3         | 3.3          | 3.3          | 1.8          | 4.2           | 0.00041        | 0.05        | 2.3         | 18.17                     |
| 3.6         | 3.6          | 3.6          | 3.6          | 4.4           | 0.0004         | 0.05        | 5.33        | 35.21                     |

### DAC OUT1 Master Mode

#### 44.1kHz, 10kΩ Load

| AVDD<br>(V) | HPVDD<br>(V) | DBVDD<br>(V) | DCVDD<br>(V) | IAVDD<br>(mA) | IHPVDD<br>(mA) | IDB<br>(mA) | IDC<br>(mA) | Power Consumption<br>(mW) |
|-------------|--------------|--------------|--------------|---------------|----------------|-------------|-------------|---------------------------|
| 2.5         | 2.5          | 1.71         | 1.71         | 2.97          | 0.299          | 0.193       | 1.69        | 11.39                     |
| 3.3         | 3.3          | 3.3          | 1.8          | 4.14          | 0.432          | 0.39        | 1.78        | 19.58                     |
| 3.6         | 3.6          | 3.6          | 3.6          | 4.54          | 0.486          | 0.461       | 4.28        | 35.16                     |

#### 48kHz, 10kΩ Load

| AVDD<br>(V) | HPVDD<br>(V) | DBVDD<br>(V) | DCVDD<br>(V) | IAVDD<br>(mA) | IHPVDD<br>(mA) | IDB<br>(mA) | IDC<br>(mA) | Power Consumption<br>(mW) |
|-------------|--------------|--------------|--------------|---------------|----------------|-------------|-------------|---------------------------|
| 2.5         | 2.5          | 1.71         | 1.71         | 2.82          | 0.3            | 0.2         | 2           | 11.56                     |
| 3.3         | 3.3          | 3.3          | 1.8          | 3.94          | 0.45           | 0.42        | 2.12        | 19.69                     |
| 3.6         | 3.6          | 3.6          | 3.6          | 4.33          | 0.51           | 0.46        | 4.9         | 36.72                     |

## DAC OUT1 Master Mode

## Pink Noise

| AVDD<br>(V) | HPVDD<br>(V) | DBVDD<br>(V) | DCVDD<br>(V) | IAVDD<br>(mA) | IHPVDD<br>(mA) | IDB<br>(mA) | IDC<br>(mA) | Power Consumption<br>(mW) |
|-------------|--------------|--------------|--------------|---------------|----------------|-------------|-------------|---------------------------|
| 2.5         | 2.5          | 1.71         | 1.71         | 2.97          | 2              | 0.192       | 2.2         | 16.52                     |
| 3.3         | 3.3          | 3.3          | 1.8          | 4.13          | 2.6            | 0.39        | 2.3         | 27.64                     |
| 3.6         | 5.5          | 3.6          | 3.6          | 4.5           | 2.9            | 0.45        | 5.5         | 53.57                     |

## DAC OUT1 Master Mode

## 1kHz Tone, 16Ω Load

| AVDD<br>(V) | HPVDD<br>(V) | DBVDD<br>(V) | DCVDD<br>(V) | IAVDD<br>(mA) | IHPVDD<br>(mA) | IDB<br>(mA) | IDC<br>(mA) | Power Consumption<br>(mW) |
|-------------|--------------|--------------|--------------|---------------|----------------|-------------|-------------|---------------------------|
| 2.5         | 2.5          | 1.71         | 1.71         | 2.9           | 2.97           | 0.19        | 2.2         | 18.76                     |
| 3.3         | 3.3          | 3.3          | 1.8          | 4.1           | 3.8            | 0.4         | 2.3         | 31.53                     |
| 3.6         | 5.5          | 3.6          | 3.6          | 4.5           | 4.1            | 0.44        | 5.4         | 59.77                     |

## 1kHz Tone, 10kΩ Load

| AVDD<br>(V) | HPVDD<br>(V) | DBVDD<br>(V) | DCVDD<br>(V) | IAVDD<br>(mA) | IHPVDD<br>(mA) | IDB<br>(mA) | IDC<br>(mA) | Power Consumption<br>(mW) |
|-------------|--------------|--------------|--------------|---------------|----------------|-------------|-------------|---------------------------|
| 2.5         | 2.5          | 1.71         | 1.71         | 2.97          | 0.3            | 0.2         | 2.17        | 12.23                     |
| 3.3         | 3.3          | 3.3          | 1.8          | 4.14          | 0.43           | 0.4         | 2.3         | 20.54                     |
| 3.6         | 3.6          | 3.6          | 3.6          | 4.5           | 0.5            | 0.46        | 5.4         | 39.10                     |

## DAC OUT1 Slave Mode

## 44.1 kHz, 10kΩ Load

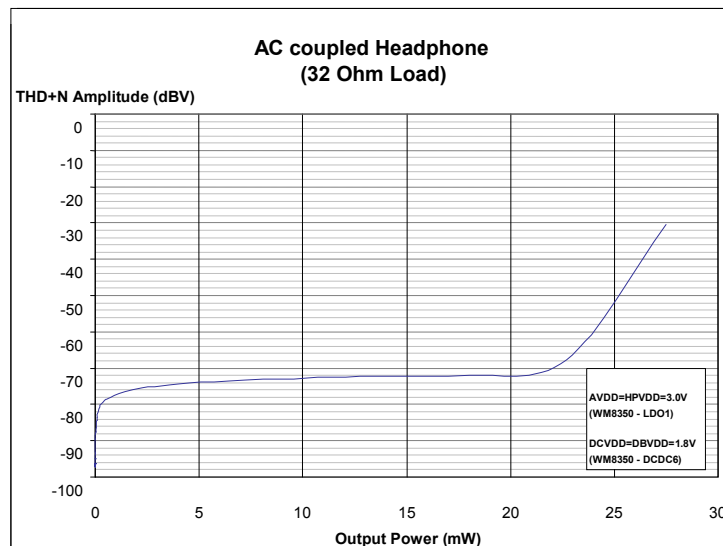
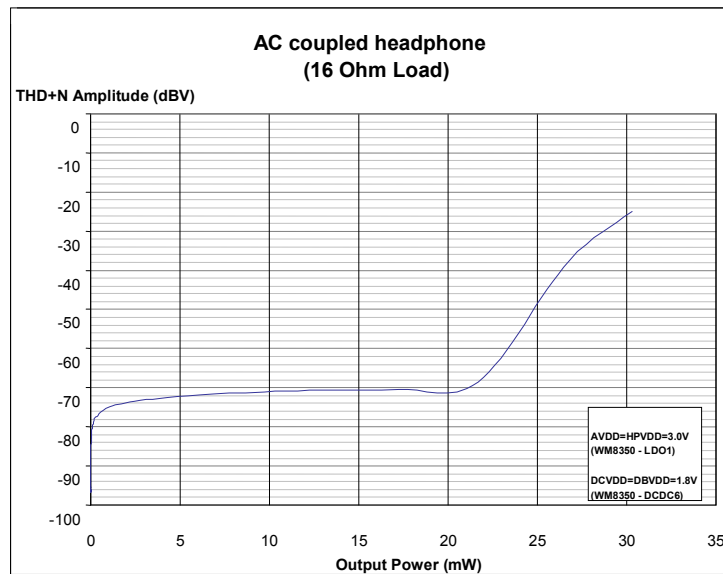
| AVDD<br>(V) | HPVDD<br>(V) | DBVDD<br>(V) | DCVDD<br>(V) | IAVDD<br>(mA) | IHPVDD<br>(mA) | IDB<br>(mA) | IDC<br>(mA) | Power Consumption<br>(mW) |
|-------------|--------------|--------------|--------------|---------------|----------------|-------------|-------------|---------------------------|
| 2.5         | 2.5          | 1.71         | 1.71         | 2.8           | 0.27           | 0.009       | 2.1         | 11.28                     |
| 3.3         | 3.3          | 3.3          | 1.8          | 3.6           | 0.38           | 0.02        | 2.3         | 17.34                     |
| 3.6         | 3.6          | 3.6          | 3.6          | 4.1           | 0.43           | 0.02        | 5.2         | 35.10                     |

## 9 TYPICAL PERFORMANCE DATA

### 9.1 AUDIO CODEC

Typical THD+N performance of the Headphone Drivers is shown below for 16Ω and 32Ω headphone loads. These graphs are derived whilst using the WM8350 Power Management to generate the power supply rails for the audio CODEC. The supply conditions are as follows:

- AVDD = HPVDD = 3.0V, generated by WM8350 LDO1
- DCVDD = DBVDD = 1.8V, generated by WM8350 DC-DC6



9.2 DC-DC CONVERTERS

9.2.1 POWER EFFICIENCY

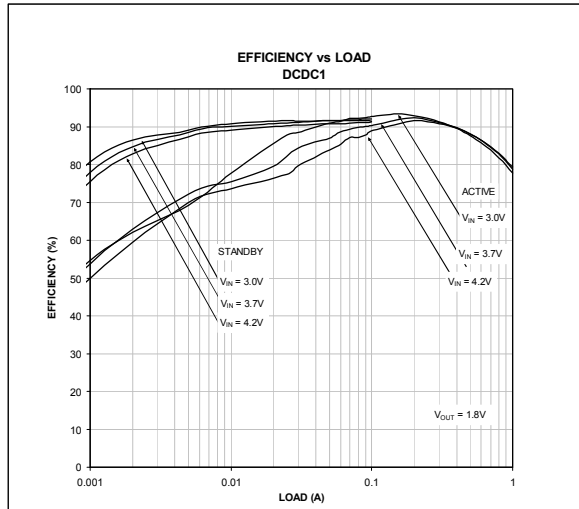


Figure 1 DC-DC1 Efficiency Vs Load Current Vo=1.8V

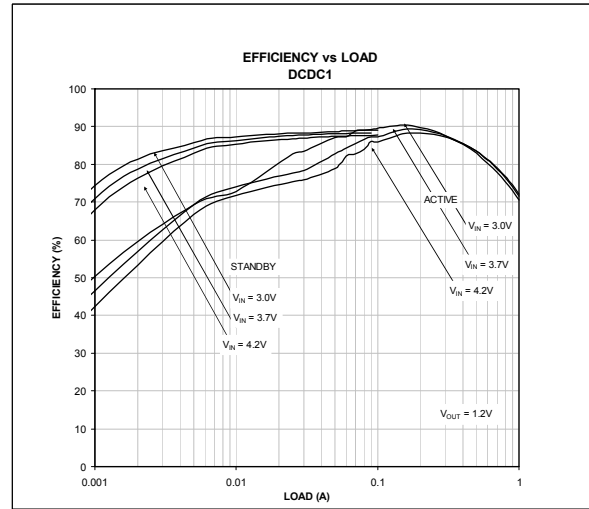


Figure 2 DC-DC1 Efficiency Vs Load Current Vo=1.2V

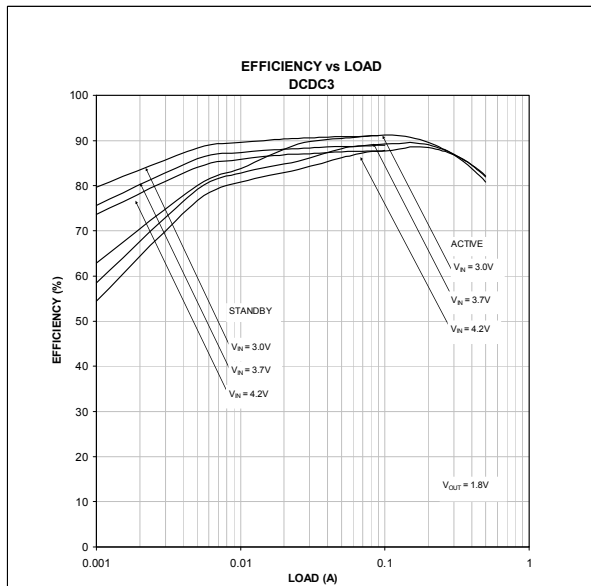


Figure 3 DC-DC3 Efficiency Vs Load Current Vo=1.8V

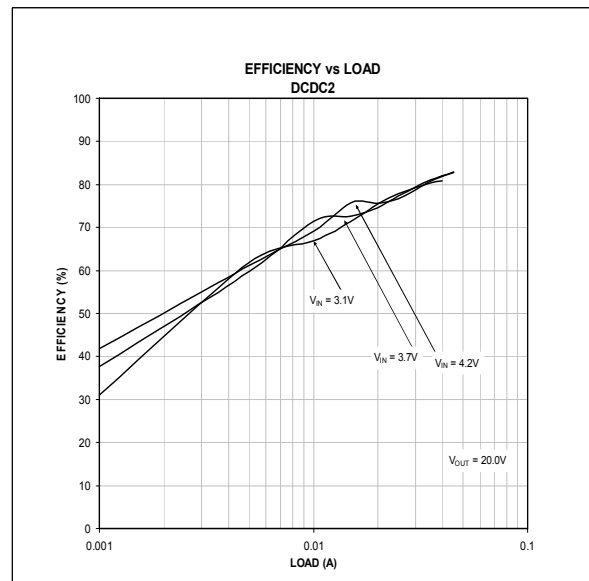


Figure 4 DC-DC2 Efficiency Vs Load Current Vo=20V

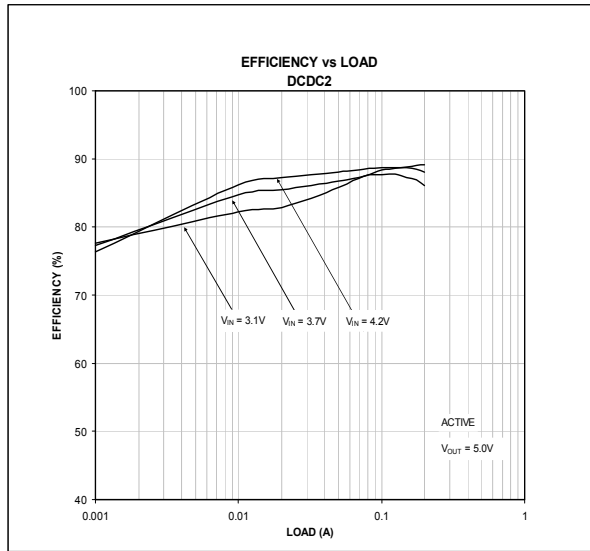


Figure 5 DC-DC2 Efficiency Vs Load Current  $V_o=5V$

### 9.2.2 OUTPUT VOLTAGE REGULATION

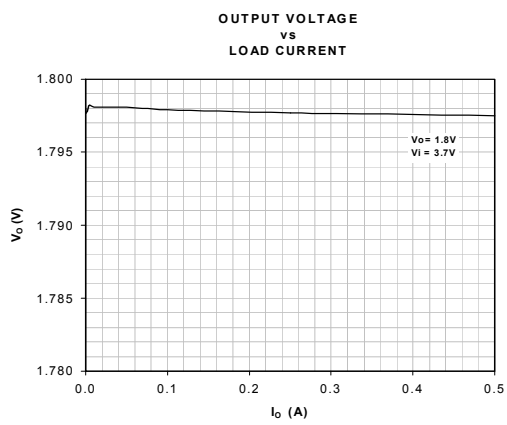


Figure 6 DC-DC1 Output Voltage Vs Output Current

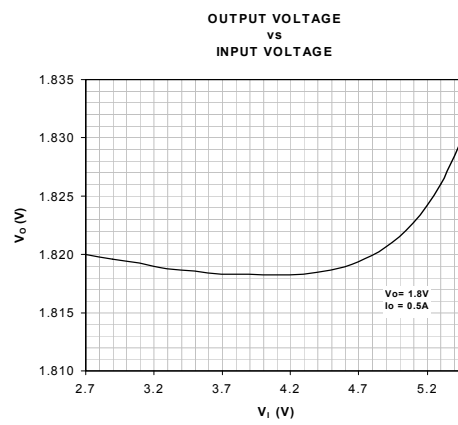


Figure 7 DC-DC1 Output Voltage Vs Input Voltage

9.2.3 DYNAMIC OUTPUT VOLTAGE

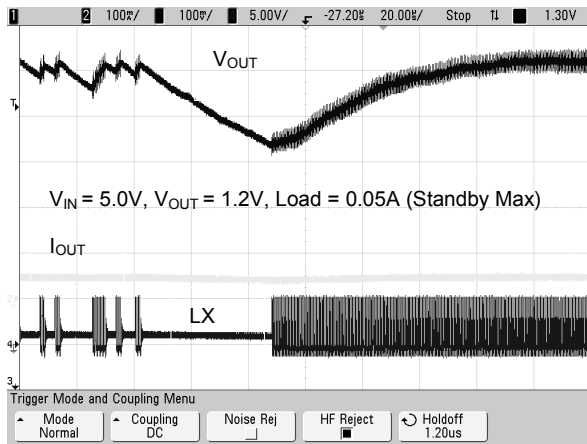


Figure 8 DC-DC1 STANDBY to ACTIVE Handover at Maximum Standby Current

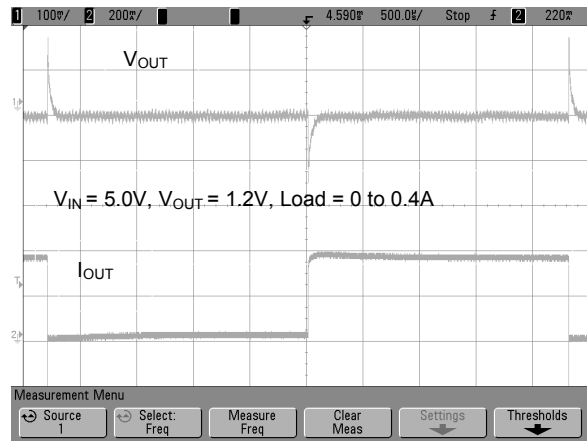


Figure 9 DC-DC1 Transient Load

### 9.3 LDO REGULATORS

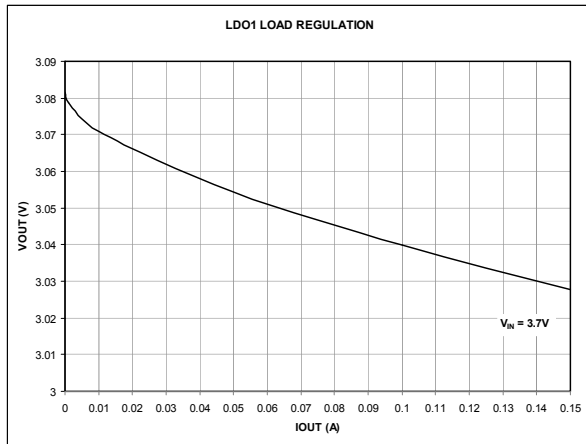


Figure 10 LDO1 Output Voltage Versus Output Current

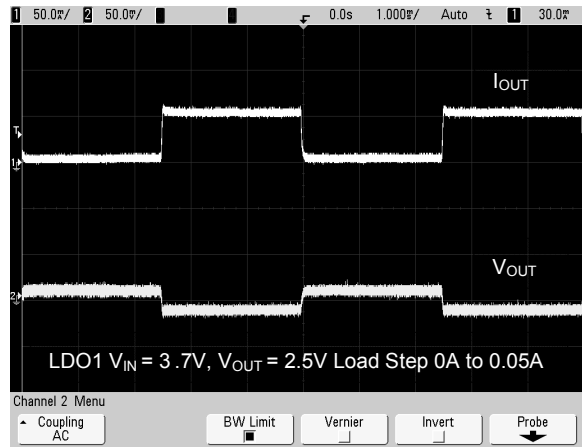


Figure 11 LDO1 Load Transient Response

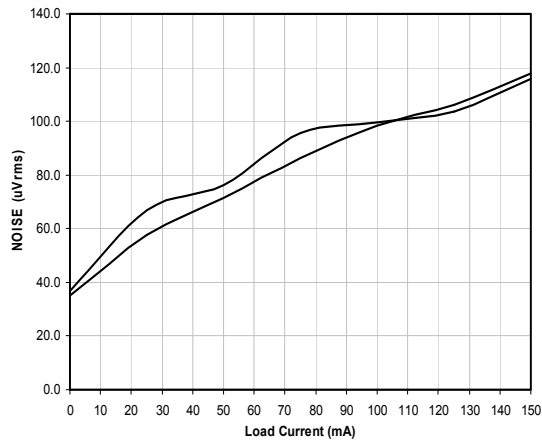


Figure 12 LDO1 Output Noise versus Output Current

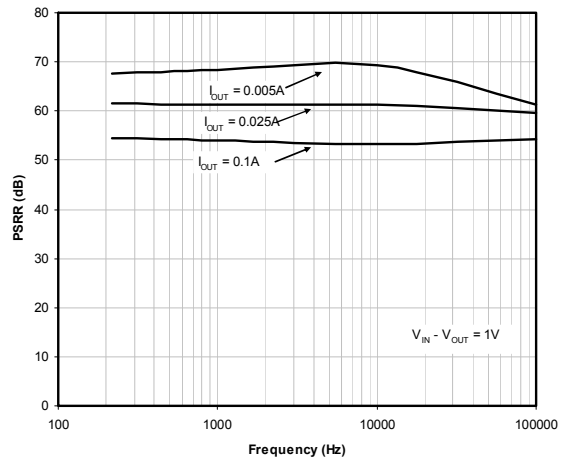


Figure 13 Power Supply Ripple Rejection versus Frequency 217Hz GSM to 100kHz

## 10 SIGNAL TIMING REQUIREMENTS

### 10.1 SYSTEM CLOCK TIMING

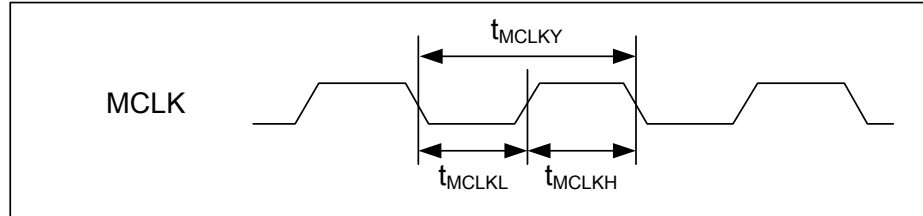


Figure 14 Master Clock Timing

| Master Clock Timing |             |                        |       |     |       |      |
|---------------------|-------------|------------------------|-------|-----|-------|------|
| PARAMETER           | SYMBOL      | TEST CONDITIONS        | MIN   | TYP | MAX   | UNIT |
| MCLK cycle time     | $T_{MCLKY}$ |                        | 40    |     |       | ns   |
| MCLK duty cycle     |             | = high time / low time | 60:40 |     | 40:60 |      |

### 10.2 AUDIO INTERFACE TIMING - MASTER MODE

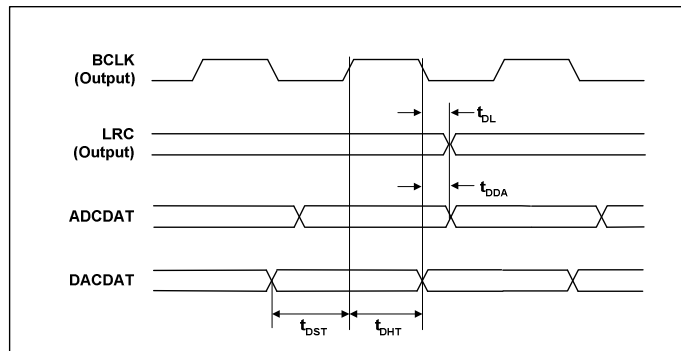


Figure 15 Digital Audio Data Timing – Master Mode

#### Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, DGND = 0V,  $T_A = +25^\circ\text{C}$ , Master Mode,  $f_s = 48\text{kHz}$ , 24-bit data, unless otherwise stated.

| PARAMETER                                       | SYMBOL       | MIN   | TYP | MAX   | UNIT |
|---|--------------|-------|-----|-------|------|
| BCLK rise time (10pF load)                      | $t_{BCLKR}$  |       |     | 3     | ns   |
| BCLK fall time (10pF load)                      | $t_{BCLKF}$  |       |     | 3     | ns   |
| BCLK duty cycle                                 | $t_{BCLKDS}$ | 60:40 |     | 40:60 |      |
| LRC propagation delay from BCLK falling edge    | $t_{DL}$     |       |     | 10    | ns   |
| ADCDAT propagation delay from BCLK falling edge | $t_{DDA}$    |       |     | 10    | ns   |
| DACDAT setup time to BCLK rising edge           | $t_{DST}$    | 10    |     |       | ns   |
| DACDAT hold time from BCLK rising edge          | $t_{DHT}$    | 10    |     |       | ns   |



### 10.3 AUDIO INTERFACE TIMING - SLAVE MODE

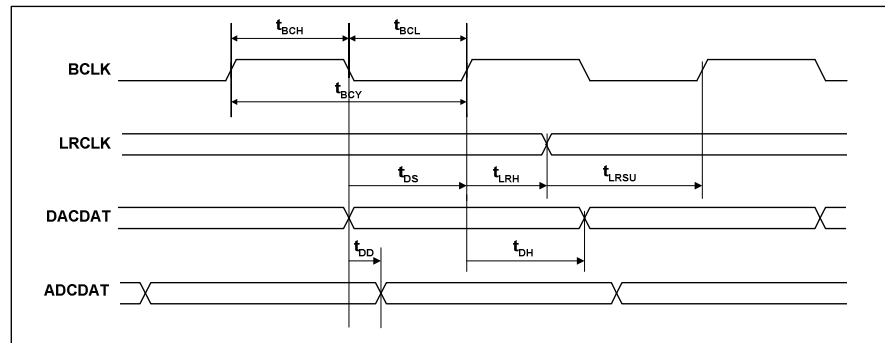


Figure 16 Digital Audio Data Timing – Slave Mode

#### Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, DGND = 0V, T<sub>A</sub> = +25°C, Slave Mode, fs = 48kHz, 24-bit data, unless otherwise stated.

| PARAMETER                                       | SYMBOL            | MIN | TYP | MAX | UNIT |
|---|-------------------|-----|-----|-----|------|
| BCLK cycle time                                 | t <sub>BCY</sub>  | 50  |     |     | ns   |
| BCLK pulse width high                           | t <sub>BCH</sub>  | 20  |     |     | ns   |
| BCLK pulse width low                            | t <sub>BCL</sub>  | 20  |     |     | ns   |
| LRCLK set-up time to BCLK rising edge           | t <sub>LRSU</sub> | 10  |     |     | ns   |
| LRCLK hold time from BCLK rising edge           | t <sub>LRH</sub>  | 10  |     |     | ns   |
| DACDAT hold time from BCLK rising edge          | t <sub>DH</sub>   | 10  |     |     | ns   |
| DACDAT set-up time to BCLK rising edge          | t <sub>DS</sub>   | 10  |     |     | ns   |
| ADCDAT propagation delay from BCLK falling edge | t <sub>DD</sub>   |     |     | 10  | ns   |

## 10.4 AUDIO INTERFACE TIMING - TDM MODE

In TDM mode, it is important that two ADC devices do not attempt to drive the ADCDAT pin simultaneously. The timing of the WM8350 ADCDAT tri-stating at the start and end of the data transmission is described in Figure 17 and the table below.

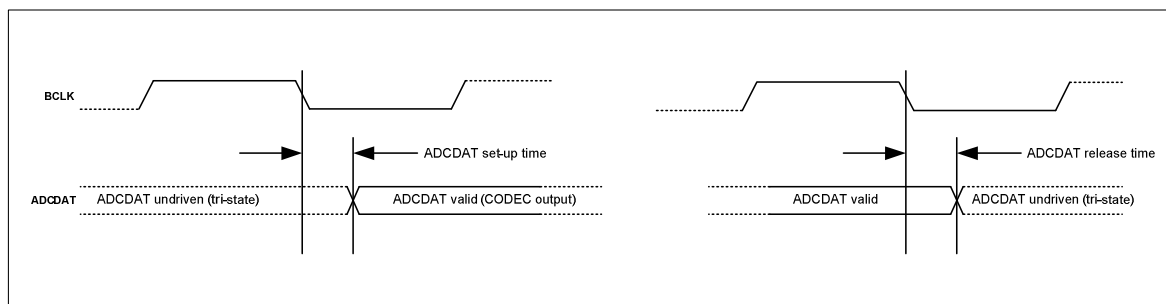


Figure 17 Digital Audio Data Timing - TDM Mode

### Test Conditions

DBVDD = 3.3V, DGND = 0V,  $T_A = +25^\circ\text{C}$ , Master Mode,  $f_s = 48\text{kHz}$ , 24-bit data, unless otherwise stated.

| PARAMETER                                  | CONDITIONS   | MIN | TYP | MAX | UNIT |
|--|--------------|-----|-----|-----|------|
| <b>Audio Data Timing Information</b>       |              |     |     |     |      |
| ADCDAT setup time from BCLK falling edge   | DCVDD = 3.6V |     | 5   |     | ns   |
|  | DCVDD = 1.8V |     | 15  |     | ns   |
| ADCDAT release time from BCLK falling edge | DCVDD = 3.6V |     | 5   |     | ns   |
|  | DCVDD = 1.8V |     | 15  |     | ns   |

## 10.5 CONTROL INTERFACE TIMING

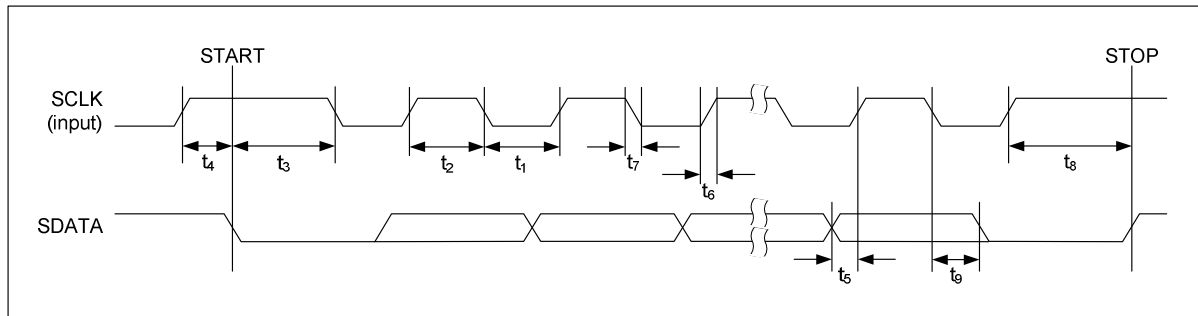


Figure 18 Control Interface Timing - 2-wire Control Mode

### Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, DGND = 0V,  $T_A = +25^\circ\text{C}$ , unless otherwise stated.

| PARAMETER                                     | SYMBOL   | MIN | TYP | MAX | UNIT |
|---|----------|-----|-----|-----|------|
| SCLK Frequency                                |          | 0   |     | 526 | kHz  |
| SCLK Low Pulse-Width                          | $t_1$    | 1.3 |     |     | us   |
| SCLK High Pulse-Width                         | $t_2$    | 600 |     |     | ns   |
| Hold Time (Start Condition)                   | $t_3$    | 600 |     |     | ns   |
| Setup Time (Start Condition)                  | $t_4$    | 600 |     |     | ns   |
| Data Setup Time                               | $t_5$    | 100 |     |     | ns   |
| SDATA, SCLK Rise Time                         | $t_6$    |     |     | 300 | ns   |
| SDATA, SCLK Fall Time                         | $t_7$    |     |     | 300 | ns   |
| Setup Time (Stop Condition)                   | $t_8$    | 600 |     |     | ns   |
| Data Hold Time                                | $t_9$    |     |     | 900 | ns   |
| Pulse width of spikes that will be suppressed | $t_{ps}$ | 0   |     | 5   | ns   |

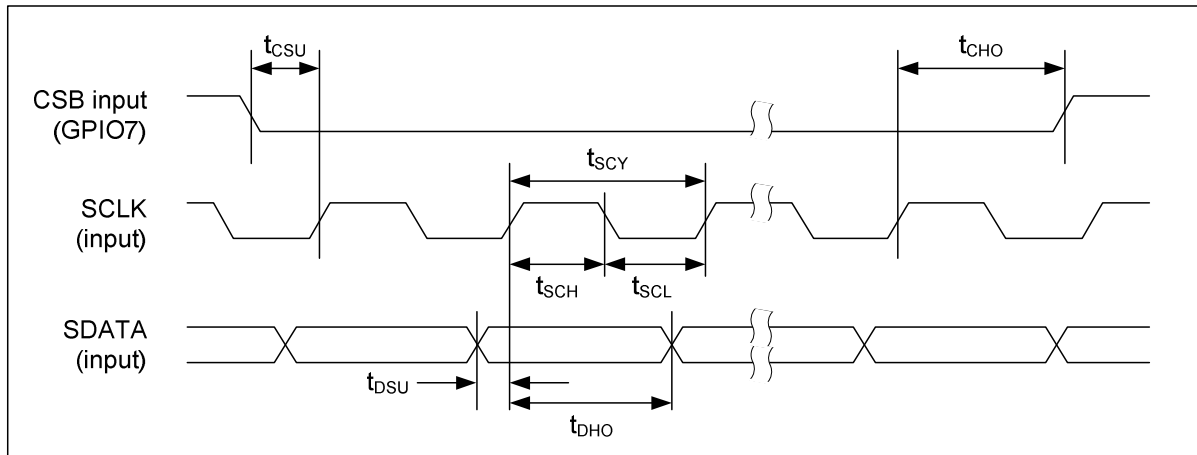


Figure 19 Control Interface Timing - 3-wire Control Mode (Write Cycle)

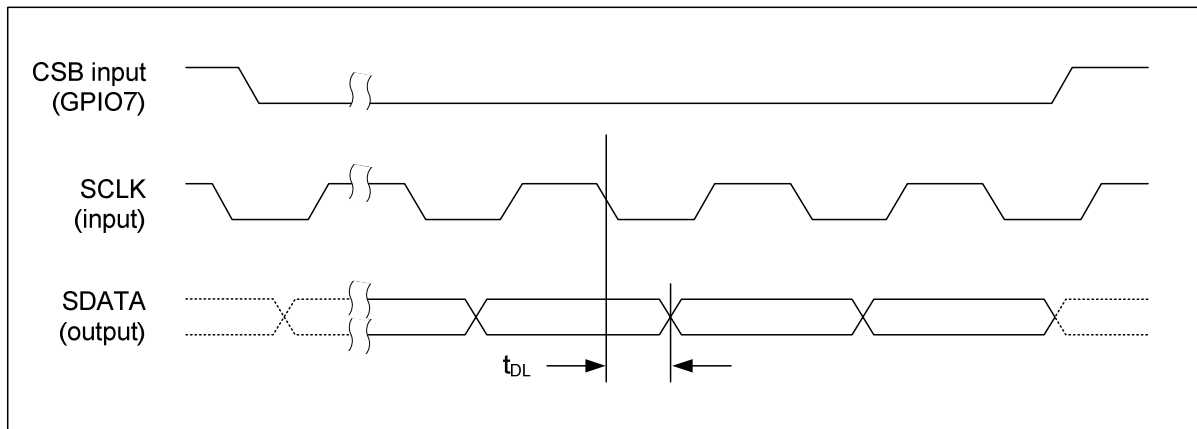


Figure 20 Control Interface Timing - 3-wire Control Mode (Read Cycle)

**Test Conditions**

DBVDD = 3.3V, DGND = 0V, T<sub>A</sub> = +25°C, unless otherwise stated.

| PARAMETER                                     | SYMBOL           | MIN | TYP | MAX | UNIT |
|---|------------------|-----|-----|-----|------|
| CSB falling edge to SCLK rising edge          | t <sub>CSU</sub> | 40  |     |     | ns   |
| SCLK rising edge to CSB rising edge           | t <sub>CHO</sub> | 10  |     |     | ns   |
| SCLK pulse cycle time                         | t <sub>SCY</sub> | 200 |     |     | ns   |
| SCLK pulse width low                          | t <sub>SCL</sub> | 80  |     |     | ns   |
| SCLK pulse width high                         | t <sub>SCH</sub> | 80  |     |     | ns   |
| SDATA to SCLK set-up time                     | t <sub>DSU</sub> | 40  |     |     | ns   |
| SDATA to SCLK hold time                       | t <sub>DHO</sub> | 10  |     |     | ns   |
| Pulse width of spikes that will be suppressed | t <sub>ps</sub>  | 0   |     | 5   | ns   |
| SCLK falling edge to SDATA output transition  | t <sub>DL</sub>  |     |     | 40  | ns   |

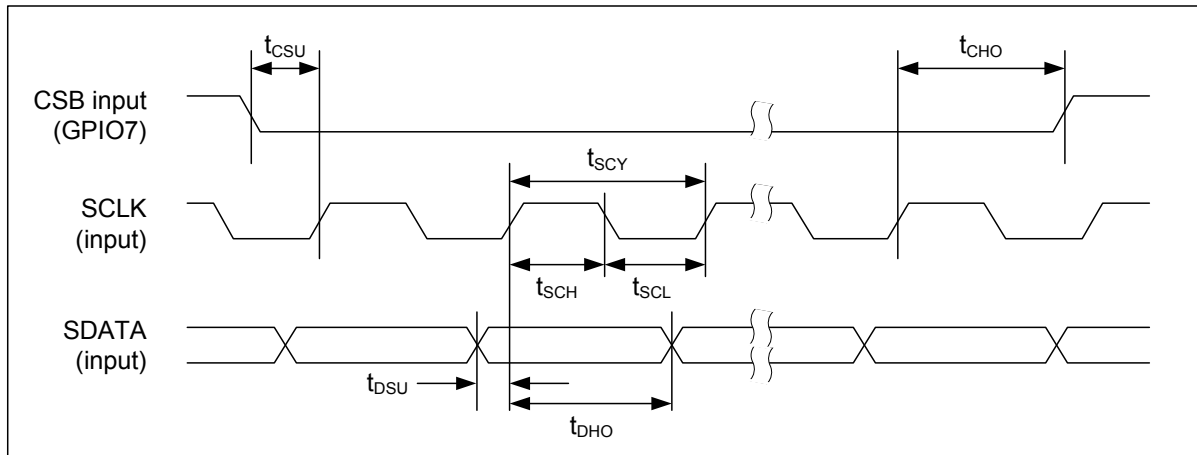


Figure 21 Control Interface Timing - 4-wire Control Mode (Write Cycle)

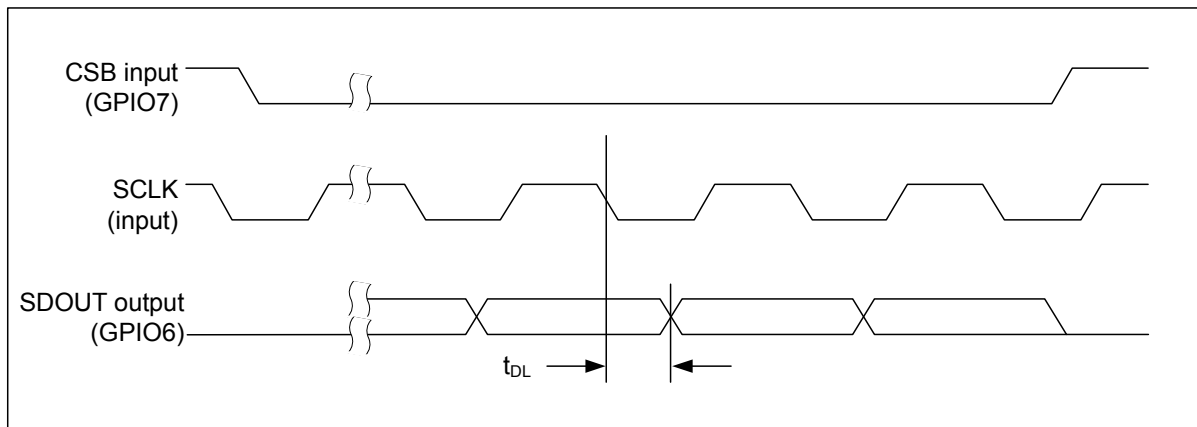


Figure 22 Control Interface Timing - 4-wire Control Mode (Read Cycle)

**Test Conditions**

DBVDD = 3.3V, DGND = 0V, T<sub>A</sub> = +25°C, unless otherwise stated.

| PARAMETER                                     | SYMBOL           | MIN | TYP | MAX | UNIT |
|---|------------------|-----|-----|-----|------|
| CSB falling edge to SCLK rising edge          | t <sub>CSU</sub> | 40  |     |     | ns   |
| SCLK rising edge to CSB rising edge           | t <sub>CHO</sub> | 10  |     |     | ns   |
| SCLK pulse cycle time                         | t <sub>SCY</sub> | 200 |     |     | ns   |
| SCLK pulse width low                          | t <sub>SCL</sub> | 80  |     |     | ns   |
| SCLK pulse width high                         | t <sub>SCH</sub> | 80  |     |     | ns   |
| SDATA to SCLK set-up time                     | t <sub>DSU</sub> | 40  |     |     | ns   |
| SDATA to SCLK hold time                       | t <sub>DHO</sub> | 10  |     |     | ns   |
| Pulse width of spikes that will be suppressed | t <sub>ps</sub>  | 0   |     | 5   | ns   |
| SCLK falling edge to SDOUT transition         | t <sub>DL</sub>  |     |     | 40  | ns   |

## 11 CONTROL INTERFACE

### 11.1 GENERAL DESCRIPTION

The WM8350 is controlled by writing to its control registers. Readback is available for most registers. Most aspects of the WM8350 operation can be controlled via this interface. The control interface can operate as either a 2-, 3- or 4-wire control interface:

- 2-wire mode uses pins SCLK and SDATA.
- 3-wire mode uses pins CSB, SCLK and SDATA.
- 4-wire mode uses pins CSB, SCLK, SDATA and SDOUT.

GPIO7 is automatically enabled as CSB in 3-wire and 4-wire control modes. GPIO6 is automatically enabled as SDOUT in 4-wire control mode. Register readback is provided on the bi-directional pin SDATA in 2-/3-wire modes and on SDOUT (GPIO6) in 4-wire mode.

In 2-wire mode, the control interface supports single register access as well as multiple access with or without address auto-increment.

In Development Mode (see Section 14.4), the WM8350 initially selects the secondary 2-wire control interface, using pins GPIO10 and GPIO11. This enables configuration of the WM8350 via a separate interface prior to selecting the normal system operation. Note that, in Custom modes, the secondary interface is not supported.

### 11.2 CONTROL INTERFACE MODES

The WM8350 control interface can be configured for 2-, 3- or 4-wire operation using the following register bits:

| ADDRESS                          | BIT | LABEL     | DEFAULT | DESCRIPTION  |
|----------------------------------|-----|-----------|---------|--|
| R6 (06h)<br>Interface<br>Control | 3   | SPI_CFG   | 0       | Controls the SDOUT (GPIO6) pin operation in 4 wire mode<br>0 = SDOUT output is CMOS<br>1 = SDOUT output is open drain<br>Note: SPI_4WIRE must be set for this to take effect.      |
|                                  | 2   | SPI_4WIRE | 0       | Selects 3-wire or 4-wire SPI mode<br>0 = 3 wire mode using bi-directional SDATA pin<br>1 = 4 wire mode using SDOUT (GPIO6)<br>Note: SPI_3WIRE must be set for this to take effect. |
|                                  | 1   | SPI_3WIRE | 0       | Selects 2- or 3-/4-wire mode.<br>0 = 2-wire mode<br>1 = 3-/4-wire mode   |

Table 1 Control Interface Modes

### 11.3 2-WIRE SERIAL CONTROL MODE

The 2-wire control interface normally uses the SCLK and SDATA pins, which are referenced to the digital buffer supply, DBVDD. (In Development mode, the interface is initially redirected, with GPIO10 and GPIO11 effectively replacing SCLK and SDATA - see Section 14.4.1).

2-wire control mode is selected by setting SPI\_3WIRE = 0. This is the default setting for this field.

In 2-wire mode, the WM8350 is a slave device on the control interface; SCLK (or GPIO10) is a clock input, while SDATA (or GPIO11) is a bi-directional data pin. To allow arbitration of multiple slaves (and/or multiple masters) on the same interface, the WM8350 transmits logic 1 by tri-stating the SDATA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDATA line high so that the logic 1 can be recognised by the master.

Many devices can be controlled by the same bus, and each device has a unique 7-bit device ID (this is not the same as the 8-bit address of each register in the WM8350). The default device ID is 0011 0100 (0x34h). The LSB of the device ID is the Read/Write bit; this bit is set to logic 1 for "Read" and logic 0 for "Write". In Development Mode, the device ID may be changed to other values.

The controller indicates the start of data transfer with a high to low transition on SDATA while SCLK remains high. This indicates that a device ID, register address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDATA (7-bit device ID + Read/Write bit, MSB first). If the device ID received matches the device ID of the WM8350, then the WM8350 responds by pulling SDATA low on the next clock pulse (ACK). If the device ID is not recognised or the R/W bit is '1' when operating in write only mode, the WM8350 returns to the idle condition and waits for a new start condition and valid address.

If the device ID matches the device ID of the WM8350, the data transfer continues as described below. The controller indicates the end of data transfer with a low to high transition on SDATA while SCLK remains high. After receiving a complete address and data sequence the WM8350 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDATA changes while SCLK is high), the device returns to the idle condition.

The WM8350 supports the following read and write operations:

- Single write
- Single read
- Multiple write using auto-increment
- Multiple read using auto-increment

The sequence of signals associated with a single register write operation is illustrated in Figure 23.

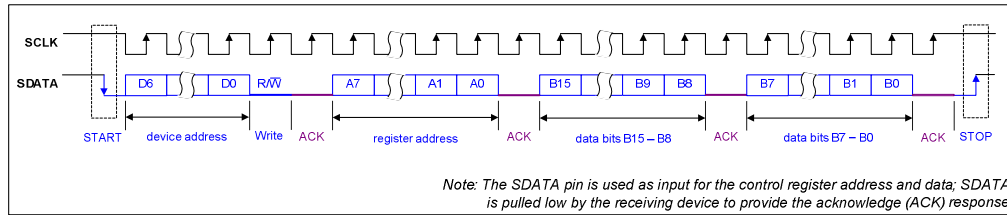


Figure 23 Control Interface 2-wire Register Write

The sequence of signals associated with a single register read operation is illustrated in Figure 24.

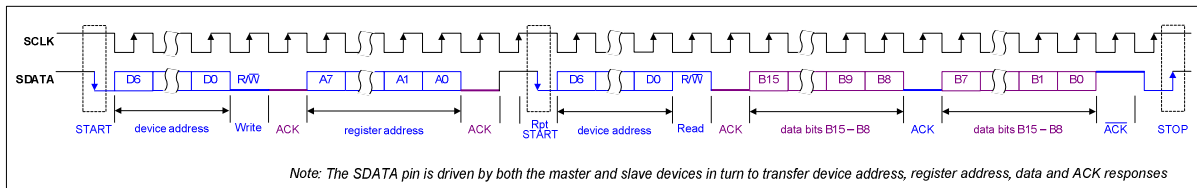


Figure 24 Control Interface 2-wire Register Read

The Control Interface also supports other register operations, as listed above. The interface protocol for these operations is summarised below. The terminology used in the following figures is detailed in Table 2.

| TERMINOLOGY   | DESCRIPTION                         |                       |
|---------------|-------------------------------------|-----------------------|
| S             | Start Condition                     |                       |
| Sr            | Repeated start                      |                       |
| A             | Acknowledge                         |                       |
| P             | Stop Condition                      |                       |
| R/W           | ReadNotWrite                        | 0 = Write<br>1 = Read |
| [White field] | Data flow from bus master to WM8350 |                       |
| [Grey field]  | Data flow from WM8350 to bus master |                       |

Table 2 Control Interface Terminology

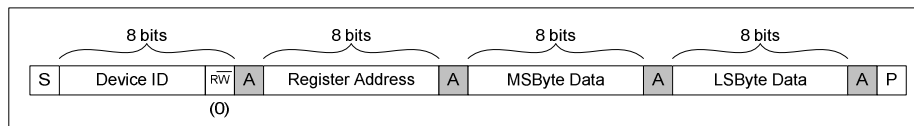


Figure 25 Single Register Write to Specified Address

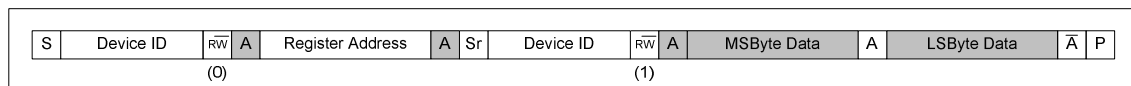


Figure 26 Single Register Read from Specified Address



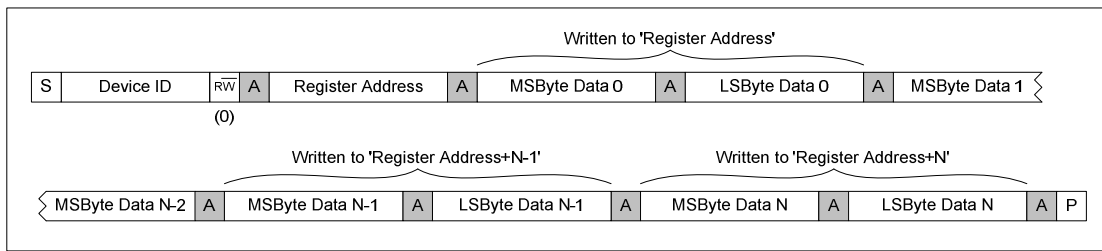


Figure 27 Multiple Register Write to Specified Address using Auto-increment

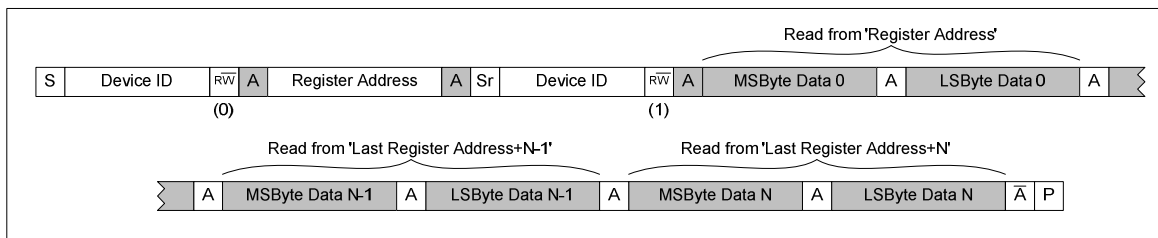


Figure 28 Multiple Register Read from Specified Address using Auto-increment

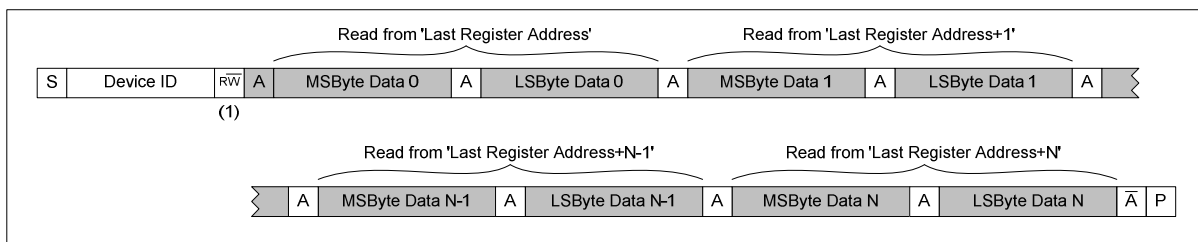


Figure 29 Multiple Register Read from Last Address using Auto-increment

Multiple Write and Multiple Read operations enable the host processor to access sequential blocks of the data in the WM8350 register map faster than is possible with single register operations. The Auto-Increment function is enabled by default; this is controlled by the AUTOINC register bit as described in Table 3.

| ADDRESS                       | BIT | LABEL   | DEFAULT | DESCRIPTION   |
|-------------------------------|-----|---------|---------|---|
| R6 (06h)<br>Interface Control | 9   | AUTOINC | 1       | Enables address auto-increment<br>0 = disabled<br>1 = enabled |

Table 3 Enabling Address Auto-Increment

## 11.4 3-WIRE SERIAL CONTROL MODE

The 3-wire control interface uses the CSB, SCLK and SDATA pins, which are referenced to the digital buffer supply, DBVDD. (In 3-wire mode, CSB is provided on GPIO7.)

3-wire control mode is selected by setting SPI\_3WIRE = 1 and SPI\_4WIRE = 0.

In 3-wire control mode, a control word consists of 24 bits. The first bit is the read/write bit (R/W), which is followed by 7 address bits (A6 to A0) that determine which control register is accessed. The remaining 16 bits (B15 to B0) are data bits, corresponding to the 16 bits in each control register.

In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDATA pin. A rising edge on CSB latches in a complete control word consisting of the last 24 bits.

In Write operations (R/W=0), all SDATA bits are driven by the controlling device.

In Read operations (R/W=1), the SDATA pin is driven by the controlling device to clock in the register address, after which the WM8350 drives the SDATA pin to output the applicable data bits.

Similarly to 2-wire control mode, the WM8350 transmits logic 1 by tri-stating the SDATA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDATA line high so that the logic 1 can be recognised by the master.

The 3-wire control mode timing is illustrated in Figure 30.

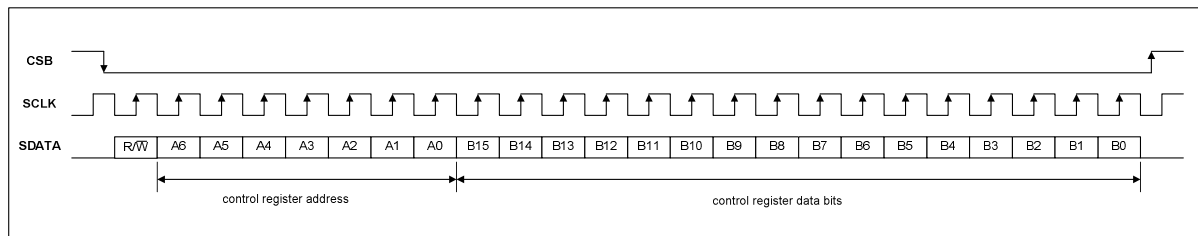


Figure 30 3-Wire Serial Control Interface

### 11.5 4-WIRE SERIAL CONTROL MODE

The 4-wire control interface uses the CSB, SCLK, SDATA and SDOUT pins, which are referenced to the digital buffer supply, DBVDD. (In 4-wire mode, SDOUT is provided on GPIO6; CSB is provided on GPIO7.)

4-wire control mode is selected by setting SPI\_3WIRE = 1 and SPI\_4WIRE = 1.

The Data Output pin, SDOUT, can be configured as CMOS or Open Drain, as described in Table 1. In CMOS mode, SDOUT is driven low when not outputting register data bits. In Open Drain mode, SDOUT is undriven when not outputting register data bits.

In Write operations (R/W=0), this mode is the same as 3-wire mode described above.

In Read operations (R/W=1), the SDATA pin is ignored following receipt of the valid register address. SDOUT is driven by the WM8350.

The 4-wire control mode timing is illustrated in Figure 31 and Figure 32.

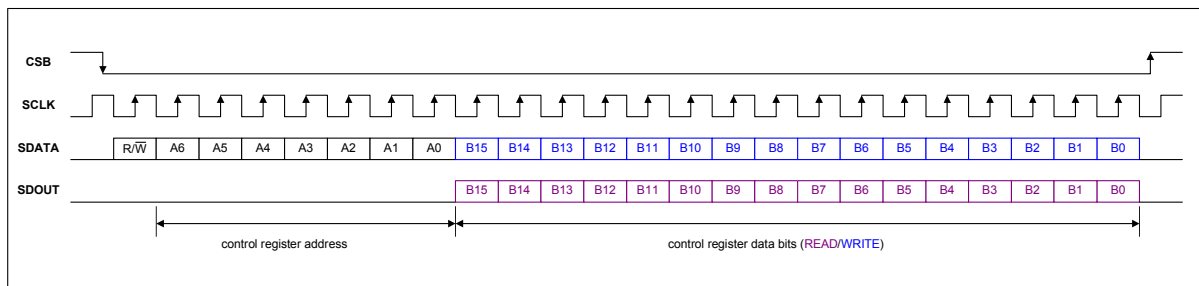


Figure 31 4-Wire Readback (CMOS)

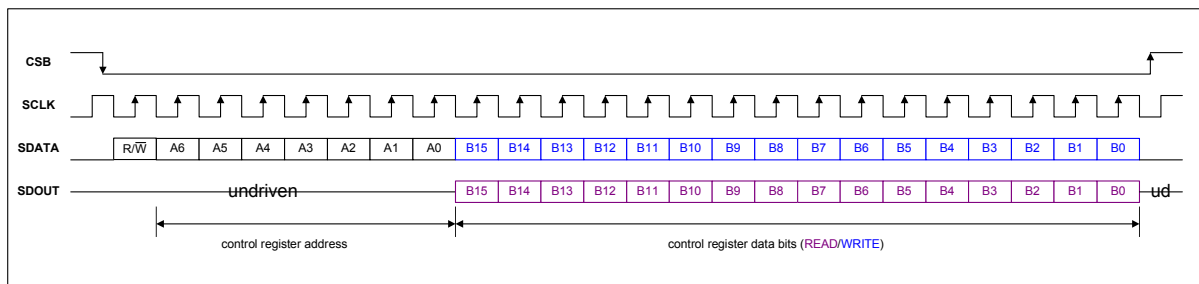


Figure 32 4-Wire Readback (Open Drain)

## 11.6 REGISTER LOCKING

Certain control fields are protected against accidental overwriting. This includes:

- Watchdog timer and system control settings in Registers R3, R4, R6 and R12 (03h, 04h, 06h and 0Ch).
- Battery charger control fields in Registers R168, R169 and R170 (A8h, A9h and AAh).

By default, these registers are locked, i.e. writing to them has no effect. However, they can be unlocked by writing a value of 0013h to Register R219.

| ADDRESS                | BIT      | LABEL              | DEFAULT | DESCRIPTION  |
|------------------------|----------|--------------------|---------|--|
| R219 (DBh)<br>Security | 15:<br>0 | SECURITY<br>[15:0] | 0000h   | The value 0013h needs to be set in this register to allow write access to the security locked registers. |

**Table 4 Locking and Unlocking Protected Registers**

It is recommended to re-lock the protected registers immediately after writing to them. This helps protect the system against accidental overwriting of register values.

It is recommended to contact Wolfson Applications support for guidance on features that are affected by Register Locking.

## 11.7 SPECIAL REGISTERS

### 11.7.1 CHIP ID

A read instruction from register R0 can be used to confirm that the chip is a WM8350.

| ADDRESS              | BIT  | LABEL                       | DEFAULT | DESCRIPTION                          |
|----------------------|------|-----------------------------|---------|--------------------------------------|
| R0 (00h)<br>Reset/ID | 15:0 | SW_RESET/C<br>HIP_ID [15:0] | 6143h   | Reading this register returns 6143h. |

**Table 5 Chip ID**

### 11.7.2 DEVICE INFORMATION

The read-only register R1 provides additional information about the WM8350 device.

| ADDRESS              | BIT       | LABEL             | DEFAULT | DESCRIPTION  |
|----------------------|-----------|-------------------|---------|--|
| R1 (01h)<br>ID       | 15:1<br>2 | CHIP_REV<br>[3:0] |         | The functional silicon revision - this tracks changes in functionality which are separate from ROM mask settings |
|                      | 11:1<br>0 | CONF_STS<br>[1:0] |         | The state of the configuration pins. This selects what register defaults should be.                              |
|                      | 7:0       | CUST_ID [7:0]     |         | The Chip Revision Number   |
| R2 (02h)<br>Revision | 7:0       | MASK_REV<br>[7:0] |         | The ROM mask ID  |

**Table 6 Reading Device Information**

## 12 CLOCKING, TIMING AND SAMPLE RATES

### 12.1 GENERAL DESCRIPTION

The WM8350 includes clocking circuitry for the on-chip audio CODEC, the DC-DC converters and the auxiliary ADC. It provides the following capabilities:

The WM8350 has two internal clock generators: a 2MHz RC oscillator and a 32kHz crystal oscillator. Clocks are required for system start-up and also for the DC-DC converter clocks; these are derived from the internal 2MHz RC oscillator. The 32kHz crystal oscillator (or external 32kHz source) is used to drive the internal Real Time Clock (RTC), and may also be used as a reference source for the CODEC clock generators.

The CODEC clocks may be derived either directly from MCLK, or else via an on-chip Frequency Locked Loop (FLL) to generate the required clocking from a wide range of reference inputs. The FLL can take as input the external MCLK, or ADCLRCLK / DACLRCLK (in Slave modes), or the 32kHz crystal oscillator (or external 32kHz source), and generates (typically) a 12.288MHz clock for the CODEC.

The flexible clocking arrangements are illustrated in Figure 33.

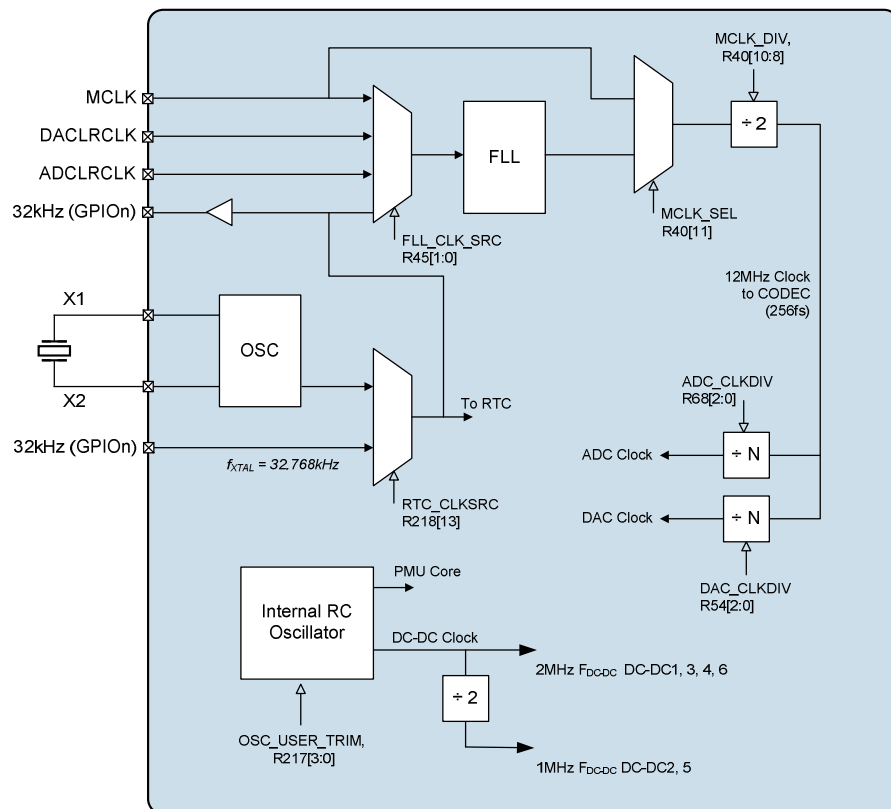


Figure 33 Clock Generation and Distribution Scheme

### 12.1.1 CLOCKING THE AUDIO CODEC

The WM8350 audio CODEC core requires an accurate, low-jitter clock. Clocks for the ADCs, DACs, DSP core functions, and the digital audio interface are all derived from a common internal clock source, SYSCLK. This clock may be derived directly from MCLK, or may be generated from an FLL using MCLK or alternate sources as an external reference. The SYSCLK source is selected by MCLK\_SEL. Many commonly-used audio sample rates can be derived directly from typical MCLK frequencies.

The ADC and DAC sample rates are independently selectable, relative to SYSCLK, using ADC\_CLKDIV and DAC\_CLKDIV. Refer to Section 12.3 for more details

### 12.1.2 CLOCKING THE DC-DC CONVERTERS

During a system start-up, no external clock signals are available. The WM8350 therefore generates all internal clocks required for the DC-DC converters, system control and housekeeping functions. These clocks are derived from the on-chip RC oscillator. The DC-DC converters' nominal switching rate is 2.0MHz and 1.0MHz.

### 12.1.3 INTERNAL RC OSCILLATOR

The internal RC Oscillator generates the system clock 2.0MHz as well as the clock for the DCDC converters. The period of the generated clock is defined by the time needed for a fixed value capacitor to be charged up to the reference voltage by a constant current source.

## 12.2 CRYSTAL OSCILLATOR

The on-chip crystal oscillator generates a 32.768kHz reference clock, which can be used to provide reference clock for the Real Time Clock (RTC) in the WM8350. It may also be used as a reference input to the FLL, for the purpose of generating the CODEC clocks. The oscillator is powered from VRTC, so that it can keep running when no other power source is available. It requires an external crystal on the X1 and X2 pins, as well as two capacitors and a resistor, connected as shown in Figure 34.

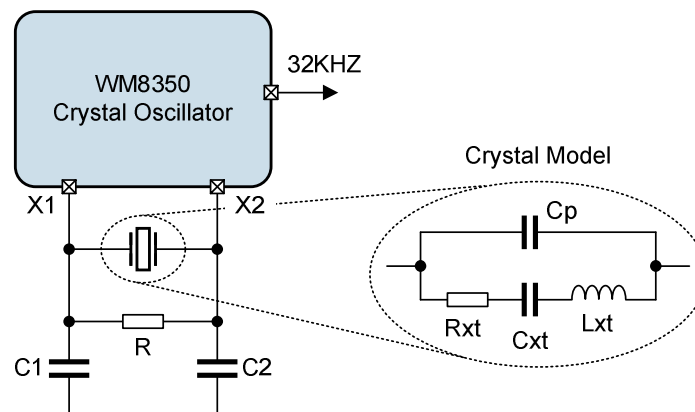


Figure 34 WM8350 Crystal Oscillator

The oscillator is enabled by the OSC32K\_ENA field, as described in Table 7. It is enabled by default and remains enabled when the WM8350 is in the OFF or BACKUP state.

| ADDRESS   | BIT | LABEL      | DEFAULT | DESCRIPTION   |
|---|-----|------------|---------|---|
| R12 (0Ch)<br>Power<br>Mgmt (5)  | 10  | OSC32K_ENA | 1       | 32kHz crystal oscillator control<br>0 = 32kHz OSC is disabled<br>1 = 32kHz OSC is enabled |
| R218 (DAh)<br>RTC Tick<br>Control   | 12  |            |         |   |
| <b>Note:</b> OSC32K_ENA can be accessed through R12 or through R218. Reading from or writing to either register location has the same effect. |     |            |         |   |

**Table 7 Enabling the 32kHz Oscillator**

If a suitable 32.768kHz clock is already present elsewhere in the system, then it is possible for the WM8350 to use this clock instead. An external clock can be provided to the WM8350 on pin X1 (with pin X2 left floating) or else on a GPIO pin configured as a 32kHz input (see Section 20).

In addition to driving the RTC, the 32kHz oscillator signal can be output to a GPIO pin configured as a 32kHz output; this is possible on GPIO pins 2, 3, 5 and 12 (see Section 20.2).

## 12.3 CLOCKING AND SAMPLE RATES

Clocks for the ADCs, DACs, DSP core functions, and the digital audio interface are all derived from a common internal clock source, SYSCLK.

SYSCLK can either be derived directly from MCLK (with a selectable divide by two option, controlled by MCLK\_DIV), or may be generated by the FLL using MCLK or alternate sources as an external reference. The SYSCLK source is selected by MCLK\_SEL. Many commonly-used audio sample rates can be derived directly from typical MCLK frequencies.

The ADC and DAC sample rates are independently selectable, relative to SYSCLK, using ADC\_CLKDIV and DAC\_CLKDIV. These fields must be set according to the required sampling frequency and depending upon the selected clocking mode. Two clocking modes are provided as follows. Normal mode allows selection of the commonly used sample rates from typical audio system clocking frequencies (eg. 12.288MHz); USB mode allows many of these sample rates to be generated from a 12MHz USB clock. Depending on the available clock sources, USB mode may be used to save power by supporting 44.1kHz operation.

In Normal mode,

- $ADC\_SYSCLK = 256 \times \text{ADC Sampling Frequency}$
- $DAC\_SYSCLK = 256 \times \text{DAC Sampling Frequency}$

In USB mode,

- $ADC\_SYSCLK = 272 \times \text{ADC Sampling Frequency}$
- $DAC\_SYSCLK = 272 \times \text{DAC Sampling Frequency}$

The above equations determine the required values for ADC\_CLKDIV and DAC\_CLKDIV. The clocking mode is selected via the AIF\_LRCLKRATE field.

In master mode, BCLK is also derived from SYSCLK via a programmable division set by BCLK\_DIV. In the case where the ADCs and DACs are operating at different sample rates, BCLK must be set according to whichever is the faster rate. In Master Mode, internal clock divide and phase control mechanisms ensure that the BCLK, ADCLRCLK and DACLRCLK edges will occur in a predictable and repeatable position relative to each other and to the data for a given combination of ADC/DAC sample rates and BCLK settings. In Slave Mode, the host processor must ensure that BCLK, ADCLRCLK and DACLRCLK are fully synchronised; if these inputs are not synchronised, unpredictable pops and noise may result.

When the GPIO5 pin is configured as CODEC\_OPCLK, a clock derived from SYSCLK may be output on this pin to provide clocking for other parts of the system. The frequency of this signal is set by OPCLK\_DIV.

Alternate GPIO pins can be used to provide ADCLRCLK and ADCBCLK as described in Section 20. An inverted L/R clock signal ADCLRCLKB can also be generated. When this feature is used, the LRCLK and BCLK pins support the DAC only, and the alternate GPIO pins support the ADC only. Limited capability can be provided to support mixed sample rates by this method. (The selection of USB mode and the supported values of the various SYSCLK dividers impose restrictions on what combinations of clocking and sample rates may be configured.)

A slow clock derived from SYSCLK may be used to provide de-bouncing of the headphone detect function, and to set the timeout period for volume updates when zero-cross functions are used. This clock is enabled by TOCLK\_ENA and its frequency is set by TOCLK\_RATE.

The overall CODEC clocking scheme is illustrated in Figure 35.

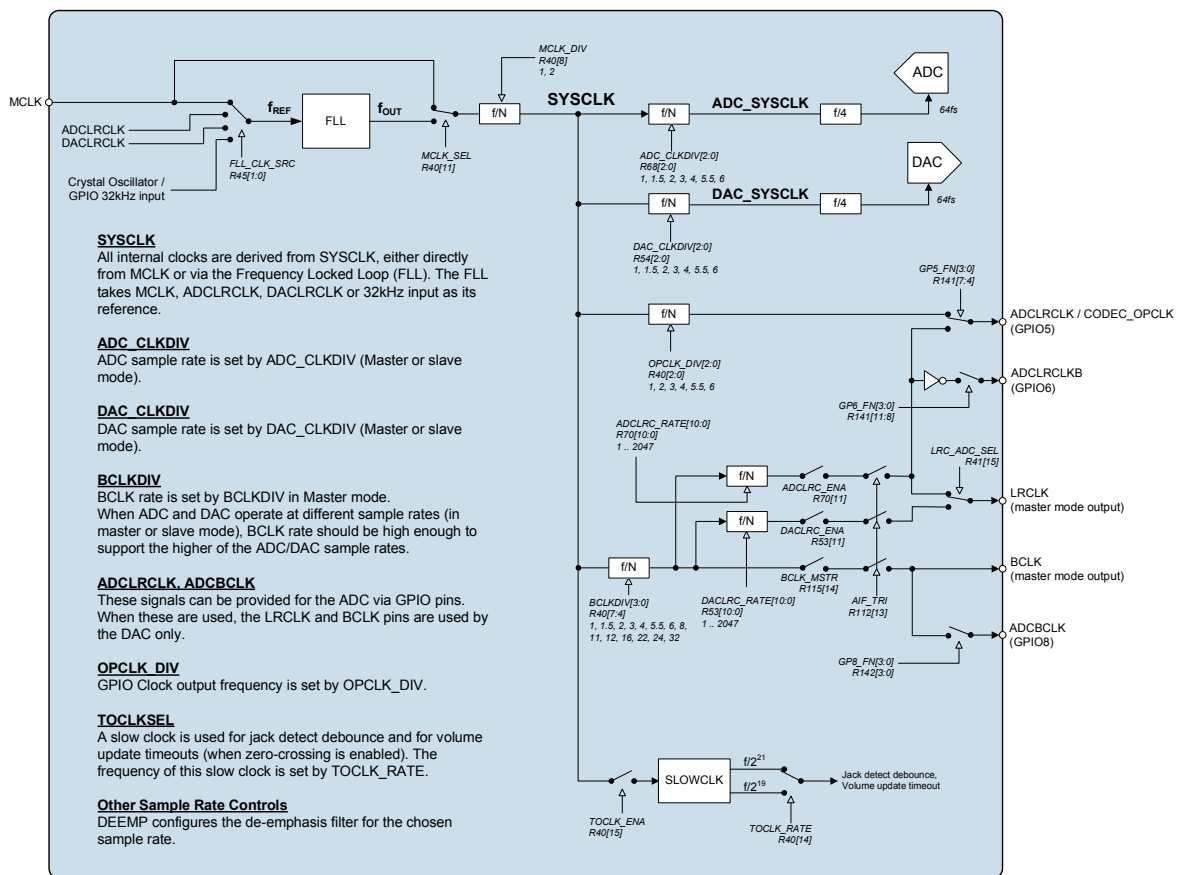


Figure 35 Audio CODEC Clocking



### 12.3.1 SYSCLOCK CONTROL

The MCLK\_SEL bit is used to select the source for SYSCLOCK. The source may be either directly from the MCLK input or may be from the output of the FLL. If required, the selected source may be divided by two, as determined by MCLK\_DIV, as described in Table 8. For further details of the FLL, see Section 12.4.

When the internal clock source is switched from one value to another using MCLK\_SEL, the change of source will only occur following a falling edge of the source signal that was originally selected. In the case where the clock source is switched from FLL to MCLK, a suitable falling edge can be ensured by disabling the FLL after selection of MCLK as the source.

The recommended sequence of actions to switch from FLL to MCLK source is as follows:

- Select MCLK as source (MCLK\_SEL = 0)
- Disable FLL (FLL\_ENA = 0)
- Disable FLL oscillator (FLL\_OSC\_ENA = 0)

Note that, as an alternative to the above sequence, a software reset may be used to re-select MCLK as the default SYSCLOCK source.

The recommended sequence of actions to switch from MCLK to FLL source is as follows:

- Enable FLL oscillator (FLL\_OSC\_ENA = 1)
- Enable FLL (FLL\_ENA = 1)
- Select FLL as source (MCLK\_SEL = 1)

| REGISTER ADDRESS                | BIT | LABEL    | DEFAULT | DESCRIPTION   |
|---------------------------------|-----|----------|---------|---|
| R40 (28h)<br>Clock Control<br>1 | 11  | MCLK_SEL | 0       | Selects source for SYSCLOCK to CODEC<br>0 = MCLK pin<br>1 = FLL                                   |
|                                 | 8   | MCLK_DIV | 0       | Selects MCLK division in slave (MCLK input) mode:<br>0 = divide MCLK by 1<br>1 = divide MCLK by 2 |

Table 8 SYSCLOCK Control

### 12.3.2 ADC / DAC SAMPLE RATES

The ADC and DAC sample rates are independently selectable, relative to SYSCLK, by setting the register fields ADC\_CLKDIV and DAC\_CLKDIV. These fields must be set according to the SYSCLK frequency, and according to the selected mode of operation (Normal or USB). The applicable fields are described in Table 9.

Selection of USB mode enables a 12MHz USB clock to be used to generate the required internal clock signals. Table 10 describes the available sample rates using four different common MCLK frequencies. The AIF\_LRCLKRATE field must be set as described in Table 9.

In Normal mode, the programmable division set by ADC\_CLKDIV must ensure that ADC\_SYSCLK is  $256 * \text{ADC Sampling Frequency}$ . DAC\_CLKDIV must ensure that DAC\_SYSCLK is  $256 * \text{DAC Sampling Frequency}$ .

In USB mode, ADC\_CLKDIV must ensure that ADC\_SYSCLK is  $272 * \text{ADC Sampling Frequency}$ . DAC\_CLKDIV must ensure that DAC\_SYSCLK is  $272 * \text{DAC Sampling Frequency}$ .

| REGISTER ADDRESS               | BIT | LABEL            | DEFAULT | DESCRIPTION   |
|--------------------------------|-----|------------------|---------|---|
| R48 (30h)<br>DAC Control       | 12  | AIF_LRCLKRATE    | 0       | Mode Select<br>1 = USB mode ( $272 * F_s$ )<br>0 = Normal mode ( $256 * F_s$ )  |
| R68 (44h)<br>ADC Clock Control | 2:0 | ADC_CLKDIV [2:0] | 000     | ADC Sample rate divider<br>000 = SYSCLK / 1.0<br>001 = SYSCLK / 1.5<br>010 = SYSCLK / 2<br>011 = SYSCLK / 3<br>100 = SYSCLK / 4<br>101 = SYSCLK / 5.5<br>110 = SYSCLK / 6<br>111 = Reserved |
| R54 (36h)<br>DAC Clock Control | 2:0 | DAC_CLKDIV [2:0] | 000     | DAC Sample rate divider<br>000 = SYSCLK / 1.0<br>001 = SYSCLK / 1.5<br>010 = SYSCLK / 2<br>011 = SYSCLK / 3<br>100 = SYSCLK / 4<br>101 = SYSCLK / 5.5<br>110 = SYSCLK / 6<br>111 = Reserved |

Table 9 ADC / DAC Sample Rate Control

| SYSCLK      | ADC / DAC SAMPLE RATE DIVIDER | CLOCKING MODE        | ADC / DAC SAMPLE RATE |
|-------------|-------------------------------|----------------------|-----------------------|
| 12.2880 MHz | 000 = SYSCLK / 1              | Normal<br>(256 * Fs) | 48 kHz                |
|             | 001 = SYSCLK / 1.5            |                      | 32 kHz                |
|             | 010 = SYSCLK / 2              |                      | 24 kHz                |
|             | 011 = SYSCLK / 3              |                      | 16 kHz                |
|             | 100 = SYSCLK / 4              |                      | 12 kHz                |
|             | 101 = SYSCLK / 5.5            |                      | Not used              |
|             | 110 = SYSCLK / 6              |                      | 8 kHz                 |
|             | 111 = Reserved                |                      | Reserved              |
| 11.2896 MHz | 000 = SYSCLK / 1              | Normal<br>(256 * Fs) | 44.1 kHz              |
|             | 001 = SYSCLK / 1.5            |                      | Not used              |
|             | 010 = SYSCLK / 2              |                      | 22.05 kHz             |
|             | 011 = SYSCLK / 3              |                      | Not used              |
|             | 100 = SYSCLK / 4              |                      | 11.025 kHz            |
|             | 101 = SYSCLK / 5.5            |                      | 8.018 kHz             |
|             | 110 = SYSCLK / 6              |                      | Not used              |
|             | 111 = Reserved                |                      | Reserved              |
| 12.0000 MHz | 000 = SYSCLK / 1              | USB<br>(272 * Fs)    | 44.118 kHz            |
|             | 001 = SYSCLK / 1.5            |                      | Not used              |
|             | 010 = SYSCLK / 2              |                      | 22.059 kHz            |
|             | 011 = SYSCLK / 3              |                      | Not used              |
|             | 100 = SYSCLK / 4              |                      | 11.029 kHz            |
|             | 101 = SYSCLK / 5.5            |                      | 8.021 kHz             |
|             | 110 = SYSCLK / 6              |                      | Not used              |
|             | 111 = Reserved                |                      | Reserved              |
| 2.0480 MHz  | 000 = SYSCLK / 1              | Normal<br>(256 * Fs) | 8 kHz                 |
|             | 001 = SYSCLK / 1.5            |                      | Not used              |
|             | 010 = SYSCLK / 2              |                      | Not used              |
|             | 011 = SYSCLK / 3              |                      | Not used              |
|             | 100 = SYSCLK / 4              |                      | Not used              |
|             | 101 = SYSCLK / 5.5            |                      | Not used              |
|             | 110 = SYSCLK / 6              |                      | Not used              |
|             | 111 = Reserved                |                      | Reserved              |

**Table 10 Derivation of Sample Rates in Normal / USB Modes**

Note that, in USB mode, the ADC / DAC sample rates do not match exactly with the commonly used sample rates (eg. 44.118 kHz instead of 44.100 kHz). At most, the difference is less than 0.5%, which is within normal accepted tolerances. Data recorded at 44.100 kHz sample rate and replayed at 44.118 kHz will experience a slight (sub 0.5%) pitch shift as a result of this difference.

**Note:** USB mode cannot be used to generate a 48kHz samples rate from a 12MHz MCLK; the FLL should be used in this case.

The user must ensure correct synchronisation of data across the digital interfaces. This is particularly important when different sample rates are used, as described above.

### 12.3.3 BCLK CONTROL

In Master Mode, BCLK is derived from SYSCLK via a programmable division set by BCLK\_DIV, as described in Table 11. BCLK\_DIV must be set to an appropriate value to ensure that there are sufficient BCLK cycles to transfer the complete data words from the ADCs and to the DACs. When the GPIO8 pin is used to provide ADCBCLK in Master mode, the clock rate on this pin is also controlled by BCLK\_DIV.

In Slave Mode, BCLK is generated externally and appears as an input to the CODEC. The host device must provide sufficient BCLK cycles to transfer complete data words to the ADCs and DACs.

Note that, although the ADC and DAC can run at different sample rates, they share the same bit clock BCLK in Master Mode. In the case where different ADC / DAC sample rates are used, the BCLK frequency should be set according to the higher of the ADC / DAC bit rates. When the GPIO8 pin is used to provide ADCBCLK, and either the ADC or DAC is in Slave mode, then this restriction does not apply.

Master/Slave operation for BCLK is controlled by the BCLK\_MSTR register field.

| REGISTER ADDRESS                       | BIT | LABEL          | DEFAULT | DESCRIPTION  |
|--|-----|----------------|---------|--|
| R40 (28h)<br>Clock Control<br>1        | 7:4 | BCLK_DIV [3:0] | 0000    | Sets BCLK rate for Master mode<br>0000 = SYSCLK<br>0001 = SYSCLK / 1.5<br>0010 = SYSCLK / 2<br>0011 = SYSCLK / 3<br>0100 = SYSCLK / 4<br>0101 = SYSCLK / 5.5<br>0110 = SYSCLK / 6<br>0111 = SYSCLK / 8<br>1000 = SYSCLK / 11<br>1001 = SYSCLK / 12<br>1010 = SYSCLK / 16<br>1011 = SYSCLK / 22<br>1100 = SYSCLK / 24<br>1101 = SYSCLK / 32<br>1110 = SYSCLK / 32<br>1111 = SYSCLK / 32 |
| R115 (73h)<br>Audio I/F<br>DAC Control | 14  | BCLK_MSTR      | 0       | Enables the Audio Interface BCLK generation and enables the BCLK pin for Master mode<br>0 = BCLK Slave Mode<br>1 = BCLK Master Mode  |

Table 11 BCLK Control

Table 12 shows the maximum word lengths supported for a given SYSCLK and BCLK\_DIV, assuming that one or both the ADCs and DACs are running at maximum rate.

| SYSCLK             | BCLK DIVIDER<br>BCLK_DIV | BCLK RATE (MASTER<br>MODE) (MHZ) | MAXIMUM WORD<br>LENGTH |
|--------------------|--------------------------|----------------------------------|------------------------|
| 12.288 MHz         | 0000 = SYSCLK / 1        | 12.288                           | 32                     |
|                    | 0001 = SYSCLK / 1.5      | 8.192                            | 32                     |
|                    | 0010 = SYSCLK / 2        | 6.144                            | 32                     |
|                    | 0011 = SYSCLK / 3        | 4.096                            | 32                     |
|                    | 0100 = SYSCLK / 4        | 3.072                            | 32                     |
|                    | 0101 = SYSCLK / 5.5      | 2.2341818                        | 20                     |
|                    | 0110 = SYSCLK / 6        | 2.048                            | 20                     |
|                    | 0111 = SYSCLK / 8        | 1.536                            | 16                     |
|                    | 1000 = SYSCLK / 11       | 1.117091                         | 8                      |
|                    | 1001 = SYSCLK / 12       | 1.024                            | 8                      |
|                    | 1010 = SYSCLK / 16       | 0.768                            | 8                      |
|                    | 1011 = SYSCLK / 22       | 0.558545                         | N/A                    |
|                    | 1100 = SYSCLK / 24       | 0.512                            | N/A                    |
|                    | 1101 = SYSCLK / 32       | 0.384                            | N/A                    |
|                    | 1110 = SYSCLK / 32       | 0.384                            | N/A                    |
| 1111 = SYSCLK / 32 | 0.384                    | N/A                              |                        |
| 11.2896 MHz        | 0000 = SYSCLK / 1        | 11.2896                          | 32                     |
|                    | 0001 = SYSCLK / 1.5      | 7.5264                           | 32                     |
|                    | 0010 = SYSCLK / 2        | 5.6448                           | 32                     |
|                    | 0011 = SYSCLK / 3        | 3.7632                           | 32                     |
|                    | 0100 = SYSCLK / 4        | 2.8224                           | 32                     |
|                    | 0101 = SYSCLK / 5.5      | 2.052655                         | 20                     |
|                    | 0110 = SYSCLK / 6        | 1.8816                           | 20                     |
|                    | 0111 = SYSCLK / 8        | 1.4112                           | 16                     |
|                    | 1000 = SYSCLK / 11       | 1.026327                         | 8                      |
|                    | 1001 = SYSCLK / 12       | 0.9408                           | 8                      |
|                    | 1010 = SYSCLK / 16       | 0.7056                           | 8                      |
|                    | 1011 = SYSCLK / 22       | 0.513164                         | N/A                    |
|                    | 1100 = SYSCLK / 24       | 0.4704                           | N/A                    |
|                    | 1101 = SYSCLK / 32       | 0.3528                           | N/A                    |
|                    | 1110 = SYSCLK / 32       | 0.3528                           | N/A                    |
| 1111 = SYSCLK / 32 | 0.3528                   | N/A                              |                        |

Table 12 BCLK Divider in Master Mode

### 12.3.4 ADCLRCLK / DACLRCLK CONTROL

In Master Mode, ADCLRCLK and DACLRCLK are derived from BCLK via programmable dividers set by ADCLRC\_RATE and DACLRC\_RATE. The BCLK frequency is derived from SYSCLK according to BCLK\_DIV, as described earlier in Table 11.

In Slave Mode, ADCLRCLK and DACLRCLK are generated externally and are input to the CODEC.

By default, the LRCLK pin provides the L/R Clock signal for the ADC and the DAC. If a separate L/R Clock is required for the ADC and the DAC, then a GPIO pin must be configured as ADCLRCLK (or ADCLRCB) as described in Section 20. The LRCLK pin can be driven by either ADCLRCLK or by DACLRCLK in Master Mode; this is selected by the LRC\_ADC\_SEL bit as described in Table 13.

Master/Slave operation for ADCLRCLK is controlled by the ADCLRC\_ENA register field.

Master/Slave operation for DACLRCLK is controlled by the DACLRC\_ENA register field.

| REGISTER ADDRESS             | BIT  | LABEL              | DEFAULT                 | DESCRIPTION   |
|------------------------------|------|--------------------|-------------------------|---|
| R70 (46h)<br>ADC LRC Rate    | 11   | ADCLRC_ENA         | 0                       | Enables the LRC generation for the ADC<br>0 = disabled<br>1 = enabled   |
|                              | 10:0 | ADCLRC_RATE [10:0] | 040h<br>(64 BCLK / LRC) | Determines the number of bit clocks per LRC phase (when enabled)<br>0000000000 = invalid<br>...<br>0000000111 = invalid<br>0000001000 = 8 BCPS<br>...<br>1111111111 = 2047 BCPS |
| R53 (35h)<br>DAC LRC Rate    | 11   | DACLRC_ENA         | 0                       | Enables DAC LRC generation in Master mode<br>0 = disabled<br>1 = enabled  |
|                              | 10:0 | DACLRC_RATE [10:0] | 040h<br>(64 BCLK / LRC) | Determines the number of bit clocks per LRC phase (when enabled)<br>0000000000 = invalid<br>...<br>0000000111 = invalid<br>0000001000 = 8 BCPS<br>...<br>1111111111 = 2047 BCPS |
| R41 (29h)<br>Clock Control 2 | 15   | LRC_ADC_SEL        | 0                       | Selects either ADCLRCLK or DACLRCLK to drive LRCLK pin in Master Mode<br>0 = DACLRCLK<br>1 = ADCLRCLK   |

Table 13 ADCLRCLK / DACLRCLK Control

### 12.3.5 OPCLK CONTROL

When the GPIO5 pin is configured as CODEC\_OPCLK, a clock derived from SYSCLK may be output on this pin to provide clocking for other parts of the system. The frequency of this signal is derived from SYSCLK and determined by OPCLK\_DIV, as described in Table 14.

| REGISTER ADDRESS                | BIT | LABEL              | DEFAULT | DESCRIPTION   |
|---------------------------------|-----|--------------------|---------|---|
| R40 (28h)<br>Clock Control<br>1 | 2:0 | OPCLK_DIV<br>[2:0] | 000     | OPCLK Frequency (GPIO function)<br>000 = SYSCLK<br>001 = SYSCLK / 2<br>010 = SYSCLK / 3<br>011 = SYSCLK / 4<br>100 = SYSCLK / 5.5<br>101 = SYSCLK / 6<br>110 = Reserved<br>111 = Reserved |

Table 14 OPCLK Control

### 12.3.6 SLOWCLK CONTROL

A slow clock derived from SYSCLK may be generated for de-bouncing of the Headphone Jack Detect function or to set the timeout period for volume updates when zero-cross functions are used. This clock is enabled by TOCLK\_ENA and its frequency is set by TOCLK\_RATE, as described in Table 15.

| REGISTER ADDRESS                | BIT | LABEL      | DEFAULT | DESCRIPTION   |
|---------------------------------|-----|------------|---------|---|
| R11 (0Bh)<br>Power Mgmt<br>4    | 8   | TOCLK_ENA  | 0       | Slow clock enable. Used for both the jack insert detect debounce circuit and the zero cross timeout.<br>0 = slow clock disabled<br>1 = slow clock enabled                               |
| R40 (28h)<br>Clock Control<br>1 | 15  |            |         |   |
|                                 | 14  | TOCLK_RATE | 0       | Slow Clock Selection (Used for volume update timeouts and for jack detect debounce)<br>0 = SYSCLK / 2 <sup>21</sup> (Slower Response)<br>1 = SYSCLK / 2 <sup>19</sup> (Faster Response) |

**Note:** TOCLK\_ENA can be accessed through R11 or through R40. Reading from or writing to either register location has the same effect.

Table 15 SLOWCLK Control

## 12.4 FLL

The integrated FLL can be used to generate SYSCLK from a wide variety of different reference sources and frequencies. The FLL can accept a wide range of reference frequencies, which may be high frequency (eg. 12.288MHz) or low frequency (eg. 32.768kHz). The FLL is tolerant of jitter and may be used to generate a stable SYSCLK from a less stable input signal.

The FLL can take as input the external MCLK, or ADCLRCLK / DACLRCLK (in Slave modes), or the 32kHz crystal oscillator (or external 32kHz source). The FLL input reference source is selected using the FLL\_CLK\_SRC, as described in Table 17. Choosing the 32kHz source as an input selects either the 32kHz GPIO input or the internal 32kHz oscillator, as illustrated in Figure 33. For best audio performance, it is recommended that a high frequency input clock (above 1MHz) is used.

The analogue and digital portions of the FLL may be enabled independently via FLL\_OSC\_ENA and FLL\_ENA. When initialising the FLL, the analogue circuit must be enabled first by setting FLL\_OSC\_ENA. The digital circuit may then be enabled on the next register write or later. When changing FLL settings, it is recommended that the digital circuit be disabled via FLL\_ENA and then re-enabled after the other register settings have been updated. When changing the input reference frequency  $F_{REF}$ , it is recommended that the FLL be reset by setting FLL\_ENA to 0.

The field FLL\_RATE controls internal functions within the FLL; it is recommended that only the default setting be used for this parameter. FLL\_RSP\_RATE controls the internal loop gain and should be set to the recommended value.

The FLL output frequency is directly determined from FLL\_RATIO, FLL\_OUTDIV and the real number represented by FLL\_N and FLL\_K. The field FLL\_N is an integer (LSB = 1); FLL\_K is the fractional portion of the number (MSB = 0.5). The fractional portion is only valid when enabled by the field FLL\_FRAC. It is recommended that FLL\_FRAC is enabled at all times.

The FLL frequency is determined according to the following equation:

$$F_{OUT} = (F_{VCO} / FLL\_OUTDIV)$$

$$F_{VCO} = (F_{REF} \times N.K \times FLL\_RATIO)$$

$F_{VCO}$  must be in the range 90-100 MHz. The value of FLL\_OUTDIV should be selected as follows according to the desired output  $F_{OUT}$ .

| OUTPUT FREQUENCY $F_{OUT}$ | FLL_OUTDIV        |
|----------------------------|-------------------|
| 2.8125 MHz - 3.125 MHz     | 4h (divide by 32) |
| 5.625 MHz - 6.25 MHz       | 3h (divide by 16) |
| 11.25 MHz - 12.5 MHz       | 2h (divide by 8)  |
| 22.5 MHz - 25 MHz          | 1h (divide by 4)  |

**Table 16 Choice of FLL\_OUTDIV**

Note that the output frequencies that do not lie within the ranges quoted above cannot be guaranteed across the full range of device operating temperatures.

Once  $F_{VCO}$  has been determined, the value of FLL\_RATIO should be selected in accordance with the recommendations in Table 17. The value of N.K can then be determined using the equation above. FLL\_REF\_FREQ should be set as described in Table 17.

For best performance, FLL Fractional Mode should always be used. Therefore, if the calculations yield an integer value of N.K, then it is recommended to adjust FLL\_RATIO in order to obtain a non-integer value of N.K.

The register fields that control the FLL are described in Table 17. Example settings for a variety of reference frequencies and output frequencies are shown in Table 18.

| REGISTER ADDRESS           | BIT  | LABEL            | DEFAULT | DESCRIPTION  |
|----------------------------|------|------------------|---------|--|
| R42 (2Ah)<br>FLL Control 1 | 15   | FLL_ENA          | 0       | Digital Enable for FLL<br>0 = disabled<br>1 = enabled<br><br>Note that FLL_OSC_ENA must be enabled before enabling FLL_ENA.  |
|                            | 14   | FLL_OSC_ENA      | 0       | Analogue Enable for FLL<br>0 = FLL disabled<br>1 = FLL enabled<br><br>Note that FLL_OSC_ENA must be enabled before enabling FLL_ENA.   |
|                            | 10:8 | FLL_OUTDIV [2:0] | 010     | $F_{OUT}$ clock divider<br>000 = $F_{VCO} / 2$<br>001 = $F_{VCO} / 4$<br>010 = $F_{VCO} / 8$<br>011 = $F_{VCO} / 16$<br>100 = $F_{VCO} / 32$<br>101 = Reserved<br>110 = Reserved |



| REGISTER ADDRESS           | BIT   | LABEL             | DEFAULT     | DESCRIPTION  |
|----------------------------|-------|-------------------|-------------|--|
|                            |       |                   |             | 111 = Reserved   |
|                            | 7:4   | FLL_RSP_RATE      | 0000        | FLL Loop Gain<br>0000 = x 1 (Recommended value)<br>0001 = x 2<br>0010 = x 4<br>0011 = x 8<br>0100 = x 16<br>0101 = x 32<br>0110 = x 64<br>0111 = x 128<br>1000 = x 256<br><br>Recommended that these are not changed from default.                             |
|                            | 2:0   | FLL_RATE [2:0]    | 000         | Frequency of the FLL control block<br>000 = $F_{VCO} / 1$ (Recommended value)<br>001 = $F_{VCO} / 2$<br>010 = $F_{VCO} / 4$<br>011 = $F_{VCO} / 8$<br>100 = $F_{VCO} / 16$<br>101 = $F_{VCO} / 32$<br><br>Recommended that these are not changed from default. |
| R43 (2Bh)<br>FLL Control 2 | 15:11 | FLL_RATIO [4:0]   | 14<br>(0Eh) | CLK_VCO is divided by this integer, valid from 1 .. 31.<br>1 recommended for high freq reference<br>8 recommended for low freq reference   |
|                            | 9:0   | FLL_N [9:0]       | 086h        | FLL integer multiplier N for CLK_REF   |
| R44 (2Ch)<br>FLL Control 3 | 15:0  | FLL_K [15:0]      | C226h       | FLL fractional multiplier K for CLK_REF. This is only used if FLL_FRAC is set.   |
| R45 (2Dh)<br>FLL Control 4 | 7     | FLL_REF_FREQ      | 0           | Low frequency reference locking<br>0 = High frequency reference locking (recommended for reference clock > 48kHz)<br>1 = Lock frequency reference locking (recommended for reference clock <= 48kHz)   |
|                            | 5     | FLL_FRAC          | 0           | Fractional enable<br>0 = Integer Mode<br>1 = Fractional Mode<br><br>1 recommended in all cases   |
|                            | 1:0   | FLL_CLK_SRC [1:0] | 00          | Select FLL input clock Source<br>00 = MCLK<br>01 = DACLRCLK<br>10 = ADCLRCLK<br>11 = CLK_32K_REF   |

Table 17 FLL Control Registers

### 12.4.1 EXAMPLE FLL CALCULATION

To generate 12.288 MHz output ( $F_{OUT}$ ) from a 12.000 MHz reference clock ( $F_{REF}$ ):

- Determine FLL\_OUTDIV for the required output frequency as given by Table 16:  
For  $F_{OUT} = 12.288$  MHz, FLL\_OUTDIV = 2h (divide by 8)
- Calculate  $F_{VCO}$  for the given FLL\_OUTDIV:  
 $F_{VCO} = F_{OUT} * FLL\_OUTDIV = 12.288 \text{ MHz} * 8 = 98.304 \text{ MHz}$
- Calculate the required N.K x FLL\_RATIO for the given  $F_{REF}$  and  $F_{VCO}$ :  
 $N.K * FLL\_RATIO = F_{VCO} / F_{REF} = 8.192$
- Determine FLL\_REF\_FREQ for the given  $F_{REF}$  as given by Table 17:  
For  $F_{REF} = 12\text{MHz}$ , FLL\_REF\_FREQ = 0
- Determine FLL\_RATIO as given by Table 17:  
For High Frequency Reference, FLL\_RATIO = 1
- Calculate N.K for the given FLL\_RATIO:  
 $N.K = 8.192 / 1 = 8.192$
- Determine FLL\_N and FLL\_K from the integer and fractional portions of N.K:  
FLL\_N is 8. FLL\_K is 0.192
- Set FLL\_FRAC according to whether fractional mode is required:  
FLL\_K is 0.192, so fractional mode is required; FLL\_FRAC = 1

Note that, for best performance, FLL Fractional Mode should always be used. If the calculations yield an integer value of N.K, then it is recommended to adjust FLL\_RATIO in order to obtain a non-integer value of N.K.

### 12.4.2 EXAMPLE FLL SETTINGS

Table 18 provides example FLL settings for generating common SYSCLK frequencies from a variety of low and high frequency reference inputs.

| F <sub>REF</sub> | F <sub>OUT</sub> | F <sub>VCO</sub> | FLL_N      | FLL_K             | FLL_RATIO | FLL_OUTDIV       | FLL_FRAC | FLL_REF_FREQ |
|------------------|------------------|------------------|------------|-------------------|-----------|------------------|----------|--------------|
| 32.000 kHz       | 12.288 MHz       | 98.304 MHz       | 438 (1B6h) | 0.857143 (DB6Eh)  | 7         | 2h (divide by 8) | 1        | 1            |
| 32.000 kHz       | 11.2896 MHz      | 90.3168 MHz      | 352 (160h) | 0.8 (CCCCCh)      | 8         | 2h (divide by 8) | 1        | 1            |
| 32.768 kHz       | 12.288 MHz       | 98.304 MHz       | 428 (1ACh) | 0.571429 (9249 h) | 7         | 2h (divide by 8) | 1        | 1            |
| 32.768 kHz       | 11.288576 MHz    | 90.308608 MHz    | 344 (158h) | 0.500000 (8000 h) | 8         | 2h (divide by 8) | 1        | 1            |
| 32.768 kHz       | 11.2896 MHz      | 90.3168 MHz      | 344 (158h) | 0.53125 (8800h)   | 8         | 2h (divide by 8) | 1        | 1            |
| 48 kHz           | 12.288 MHz       | 98.304 MHz       | 292 (124h) | 0.571429 (9249 h) | 7         | 2h (divide by 8) | 1        | 1            |
| 11.3636 MHz      | 12.368544 MHz    | 98.948354 MHz    | 8 (008h)   | 0.707483 (B51Dh)  | 1         | 2h (divide by 8) | 1        | 0            |
| 12.000 MHz       | 12.288 MHz       | 98.3040 MHz      | 8 (008h)   | 0.192 (3127h)     | 1         | 2h (divide by 8) | 1        | 0            |
| 12.000 MHz       | 11.289597 MHz    | 90.3168 MHz      | 7 (007h)   | 0.526398 (86C2h)  | 1         | 2h (divide by 8) | 1        | 0            |
| 12.288 MHz       | 12.288 MHz       | 98.304 MHz       | 2 (002h)   | 0.666667 (AAABh)  | 3         | 2h (divide by 8) | 1        | 0            |
| 12.288 MHz       | 11.2896 MHz      | 90.3168 MHz      | 7 (007h)   | 0.35 (599Ah)      | 1         | 2h (divide by 8) | 1        | 0            |
| 13.000 MHz       | 12.287990 MHz    | 98.3040 MHz      | 7 (007h)   | 0.56184 (8FD5h)   | 1         | 2h (divide by 8) | 1        | 0            |
| 13.000 MHz       | 11.289606 MHz    | 90.3168 MHz      | 6 (006h)   | 0.94745 (F28Ch)   | 1         | 2h (divide by 8) | 1        | 0            |
| 19.200 MHz       | 12.287988 MHz    | 98.3040 MHz      | 5 (005h)   | 0.119995 (1EB8h)  | 1         | 2h (divide by 8) | 1        | 0            |
| 19.200 MHz       | 11.289588 MHz    | 90.3168 MHz      | 4 (004h)   | 0.703995 (B439h)  | 1         | 2h (divide by 8) | 1        | 0            |

Table 18 Example FLL Settings

## 13 AUDIO CODEC SUBSYSTEM

### 13.1 GENERAL DESCRIPTION

The WM8350 includes a high-performance stereo CODEC. Analogue output buffers and input amplifiers are integrated on-chip, enabling the WM8350 to connect directly to headphones and microphones as well as line-in and line-out sockets.

The CODEC handles analogue-to-digital and digital-to-analogue conversion for audio signals, and integrates programmable filtering. Analogue mixing capabilities are also provided.

Digital audio data is transferred to and from the audio CODEC through a dedicated audio interface that supports a number of industry-standard data formats.

Electrical power is provided to the CODEC through the following pins:

- DBVDD and DGND – for the CODEC's audio interface
- DCVDD and DGND – for the CODEC's digital core
- HPVDD and HPGND – for the analogue outputs
- AVDD and REF\_GND – for ADC and DAC references
- AVDD and GND – for all other analogue functions (including input amplifiers and buffers, ADC, DAC, and analogue mixers)



### 13.3 ENABLING THE AUDIO CODEC

Before the audio CODEC can be used, it must be enabled by writing to the CODEC\_ENA, SYSCLK\_ENA and BIAS\_ENA register bits.

| ADDRESS                      | BIT | LABEL         | DEFAULT | DESCRIPTION  |
|------------------------------|-----|---------------|---------|--|
| R12 (0Ch)<br>Power<br>Mgmt 5 | 12  | CODEC_EN<br>A | 0       | Master codec enable bit. Until this bit is set, all codec registers are held in reset.<br>0 = All codec registers held in reset<br>1 = Codec registers operate normally. |
| R11 (0Bh)<br>Power<br>Mgmt 4 | 14  | SYSCLK_ENA    | 0       | CODEC SYSCLK enable<br>0 = disabled<br>1 = enabled   |
| R8 (08h)<br>Power<br>Mgmt 1  | 5   | BIAS_ENA      | 0       | Enables bias to analogue audio CODEC circuitry<br>0 = disabled<br>1 = enabled  |

**Table 19 Enabling the Audio CODEC**

Each individual part of the audio CODEC (e.g. left/right ADC, left/right DAC, each analogue output pin, mic bias etc.) also has its own enable bit, which must be set before that part of the CODEC can be used. These enable bits are described in the sections that follow.

In order to minimize output pop and click noise, it is recommended that the WM8350 device is powered up and down under control using the following sequences:

#### Power Up:

1. Ensure the CODEC power supplies are available before the CODEC is enabled (CODEC\_ENA = 1). The order in which this is done should be DCVDD, DBVDD then HPVDD And/Or AVDD
2. Mute all outputs
3. Enable the anti-pop circuits by setting ANTI\_POP. There are three Anti-pop setting options. Recommended value is ANTI\_POP = 01.
4. Ensure external capacitors are fully discharged on all outputs that are used by delaying 250ms
5. Set the mixers and DAC volume to required settings
6. Enable VMID by setting VMID\_ENA = 1. VMID should raise in a controlled fashion and charge the output capacitors
7. Wait approx 500ms to allow VMID to charge.
8. Disable the anti-pop circuits by setting ANTI\_POP = 00.
9. Un-mute all outputs

**Power Down:**

1. Mute all outputs
2. Enable anti-pop circuits by setting ANTI\_POP = 01.
3. Disable circuits down-stream on outputs
4. Disable VMID by setting VMID\_ENA = 0.
5. Wait for VMID to discharge (typically 500ms)
6. Disable the anti-pop circuits by setting ANTI\_POP = 00.
7. Disable all outputs

## 13.4 INPUT SIGNAL PATH

The WM8350 has multiple analogue inputs. There are two input channels, Left and Right, each of which consists of an input PGA stage followed by a boost/mix stage switch into the hi-fi ADC. Each input PGA path has three input pins which can be configured in a variety of ways to accommodate single-ended, differential or dual differential microphones. There are two auxiliary input pins which can be fed into the input boost/mix stage as well as driving into the output path. A bypass path exists from the output of the boost/mix stage into the output left/right mixers.

### 13.4.1 MICROPHONE INPUTS

The microphone inputs of the WM8350 are designed to accommodate electret condenser microphones or analogue line-in signals. They comprise the following pins:

- IN1LP: first non-inverting input, left channel
- IN2L: second non-inverting input, left channel
- IN1LN: inverting input, left channel
- IN1RP: first non-inverting input, right channel
- IN2R: second non-inverting input, right channel
- IN1RN: inverting input, right channel

The non-inverting inputs have constant input impedance to VMID, whereas the inverting input's impedance varies with the pre-amplifier's gain. (Note: the terms "inverting" and "non-inverting" refer to the microphone pre-amplifiers only. For overall behaviour, the inverting record mixer and the ADC, whose output can optionally be inverted in the digital domain, must also be taken into account.)

Each channel has a programmable pre-amplifier, which supports single-ended or pseudo-differentially connected microphones. The amplified signal for each channel can be digitised in the audio ADC and/or mixed into the output signal path.

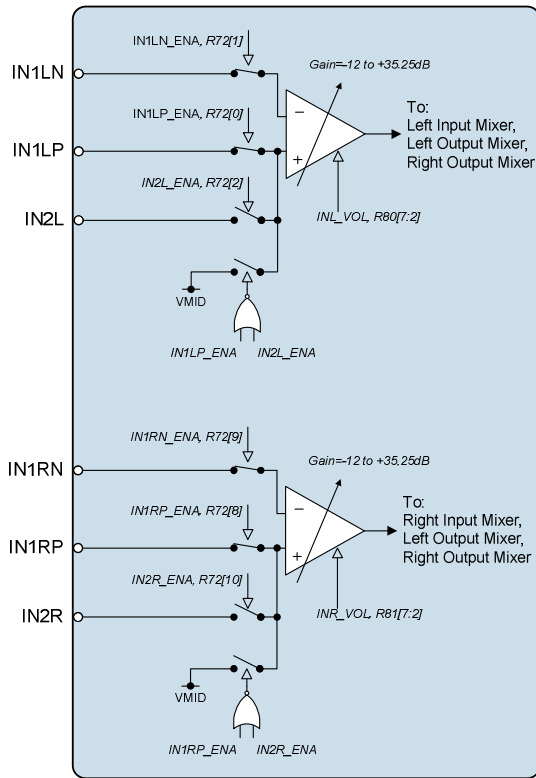


Figure 37 Microphone Inputs and Pre-amplifiers

13.4.2 ENABLING THE PRE-AMPLIFIERS

| ADDRESS                            | BIT | LABEL   | DEFAULT | DESCRIPTION   |
|------------------------------------|-----|---------|---------|---|
| R9 (09h)<br>Power Mgmt<br>2        | 9   | INR_ENA | 0       | Right input PGA enable<br>0 = disabled<br>1 = enabled |
|                                    | 8   | INL_ENA | 0       | Left input PGA enable<br>0 = disabled<br>1 = enabled  |
| R80 (50h)<br>Left Input<br>Volume  | 15  | INL_ENA | 0       | Left input PGA enable<br>0 = disabled<br>1 = enabled  |
| R81 (51h)<br>Right Input<br>Volume | 15  | INR_ENA | 0       | Right input PGA enable<br>0 = disabled<br>1 = enabled |

**Note:** These bits can be accessed through R9 or through R80/R81. Reading from or writing to either register location has the same effect.

Table 20 Enabling the Microphone Pre-amplifiers



## 13.4.3 SELECTING INPUT SIGNALS

| ADDRESS                           | BIT | LABEL     | DEFAULT | DESCRIPTION  |
|-----------------------------------|-----|-----------|---------|--|
| R72 (48h)<br>Mic Input<br>Control | 0   | IN1LP_ENA | 1       | Connect IN1LP pin to left channel input PGA amplifier positive terminal.<br>0 = IN1LP not connected to input PGA<br>1 = input PGA amplifier positive terminal connected to IN1LP (constant input impedance)                |
|                                   | 1   | IN1LN_ENA | 1       | Connect IN1LN pin to left channel input PGA negative terminal.<br>0 = IN1LN not connected to input PGA<br>1 = IN1LN connected to input PGA amplifier negative terminal.  |
|                                   | 2   | IN2L_ENA  | 0       | Connect IN2L pin to left channel input PGA amplifier<br>0 = IN2L not connected to input PGA amplifier<br>1 = IN2L connected to input PGA amplifier   |
|                                   | 8   | IN1RP_ENA | 1       | Connect IN1RP pin to right channel input PGA amplifier positive terminal.<br>0 = IN1RP not connected to input PGA<br>1 = right channel input PGA amplifier positive terminal connected to IN1RP (constant input impedance) |
|                                   | 9   | IN1RN_ENA | 1       | Connect IN1RN pin to right channel input PGA negative terminal.<br>0 = IN1RN not connected to input PGA<br>1 = IN1RN connected to right channel input PGA amplifier negative terminal.                                     |
|                                   | 10  | IN2R_ENA  | 0       | Connect IN2R pin to right channel input PGA<br>0 = IN2R not connected to input PGA amplifier<br>1 = IN2R connected to input PGA amplifier  |

Table 21 Selecting Input Pins for the Microphone Pre-amplifiers

### 13.4.4 CONTROLLING THE PRE-AMPLIFIER GAINS

The gain of each microphone pre-amplifier is controlled by writing to the appropriate control registers. The gain of each pre-amplifier applies to all three inputs associated with that pre-amplifier, whether inverting or non-inverting. Although the gain settings for each pre-amplifier are in two separate registers, both gains can be changed simultaneously using the IN\_VU bit (see Table 22). Additionally, it is also possible to control the gain updates to only occur when the respective signal crosses through zero. This feature reduces clicking noise caused by gain changes.

| ADDRESS                            | BIT | LABEL            | DEFAULT | DESCRIPTION   |
|------------------------------------|-----|------------------|---------|---|
| R80 (50h)<br>Left Input<br>Volume  | 14  | INL_MUTE         | 0       | Mute control for left channel input PGA:<br>0 = Input PGA not muted, normal operation<br>1 = Input PGA muted (and disconnected from the following input record mixer).  |
|                                    | 13  | INL_ZC           | 0       | Left channel input PGA zero cross enable:<br>0 = Update gain when gain register changes<br>1 = Update gain on 1st zero cross after gain register write.                 |
|                                    | 8   | IN_VU            | 0       | Input left PGA and input right PGA volume do not update until a 1 is written to either IN_VU register bit.  |
|                                    | 7:2 | INL_VOL<br>[5:0] | 01_0000 | Left channel input PGA volume<br>000000 = -12dB<br>000001 = -11.25dB<br>.<br>010000 = 0dB<br>.<br>111111 = 35.25dB  |
| R81 (51h)<br>Right Input<br>Volume | 14  | INR_MUTE         | 0       | Mute control for right channel input PGA:<br>0 = Input PGA not muted, normal operation<br>1 = Input PGA muted (and disconnected from the following input record mixer). |
|                                    | 13  | INR_ZC           | 0       | Right channel input PGA zero cross enable:<br>0 = Update gain when gain register changes<br>1 = Update gain on 1st zero cross after gain register write.                |
|                                    | 8   | IN_VU            | 0       | Input left PGA and input right PGA volume do not update until a 1 is written to either IN_VU register bit.  |
|                                    | 7:2 | INR_VOL<br>[5:0] | 01_0000 | Right channel input PGA volume<br>000000 = -12dB<br>000001 = -11.25dB<br>.<br>010000 = 0dB<br>.<br>111111 = 35.25dB   |

Table 22 Controlling the Microphone Pre-amplifier Gain

### 13.4.5 MICROPHONE BIASING

The WM8350 provides a programmable, low-noise bias voltage for condenser electret microphones on the MICBIAS pin.

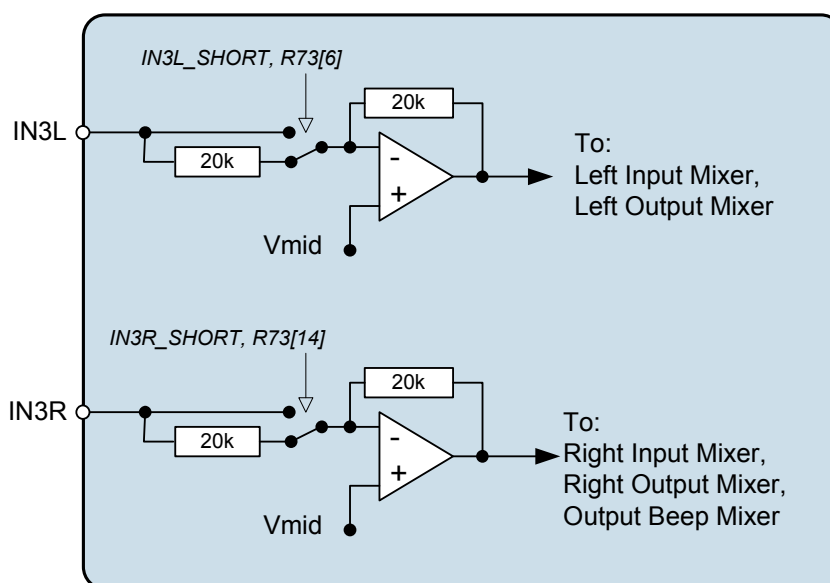
| ADDRESS                  | BIT | LABEL    | DEFAULT | DESCRIPTION   |
|--------------------------|-----|----------|---------|---|
| R8 (08h)<br>Power Mgmt 1 | 4   | MICB_ENA | 0       | Microphone bias enable<br>0 = OFF (high impedance output)<br>1 = ON       |
| R74 (4Ah)                | 15  | MICB_ENA |         |   |
| Mic Bias<br>Control      | 14  | MICB_SEL | 0       | Microphone bias voltage control:<br>0 = $0.9 * AVDD$<br>1 = $0.75 * AVDD$ |

**Note:** MICB\_ENA can be accessed through R8 or through R74. Reading from or writing to either register location has the same effect.

**Table 23 Controlling the Microphone Bias Voltage**

### 13.4.6 AUXILIARY INPUTS (IN3L AND IN3R)

The WM8350 provides two additional analogue input pins, IN3L and IN3R, for line-level audio or "beep" signals. Each pin has a simple input buffer whose output signal can be digitised in the audio ADC and/or mixed into the output signal path. The Right input IN3R may also be connected to the Output Beep Mixer, for output on OUT2R (see Table 43). The input buffers have a nominal default gain of -1 (0dB).



**Figure 38 Auxiliary Input Buffers**

| REGISTER ADDRESS   | BIT | LABEL      | DEFAULT | DESCRIPTION  |
|--|-----|------------|---------|--|
| R9 (09h)<br>Power Mgmt 2   | 10  | IN3L_ENA   | 0       | IN3L Amplifier enable<br>0 = disabled<br>1 = enabled   |
|  | 11  | IN3R_ENA   | 0       | IN3R Amplifier enable<br>0 = disabled<br>1 = enabled   |
| R73 (49h)<br>IN3 Input Control   | 7   | IN3L_ENA   | 0       | IN3L Amplifier enable<br>0 = disabled<br>1 = enabled   |
|  | 15  | IN3R_ENA   | 0       | IN3R Amplifier enable<br>0 = disabled<br>1 = enabled   |
|  | 6   | IN3L_SHORT | 0       | Short circuit internal input resistor for IN3L amplifier.<br>0 = Internal resistor in circuit<br>1 = Internal resistor shorted |
|  | 14  | IN3R_SHORT | 0       | Short circuit internal input resistor for IN3R amplifier.<br>0 = Internal resistor in circuit<br>1 = Internal resistor shorted |
| <b>Note:</b> IN3L_ENA and IN3R_ENA can be accessed through R9 or through R73. Reading from or writing to either register location has the same effect. |     |            |         |  |

Table 24 Controlling the Auxiliary Input Buffers

### 13.4.7 INPUT MIXERS

The WM8350 has mixers in the input signal paths. This allows each ADC to record either a single input signal or a mix of several signals, as desired. The gain for the different input signals can also be adjusted. Each input mixer has four inputs:

- the output of the respective (left/right) microphone pre-amplifier
- the IN2L and IN2R pins (used as a line input, bypassing the microphone pre-amplifiers)
- the output of the respective (left/right) auxiliary input buffer (ie. inputs IN3L or IN3R)
- the output of the OUT4 amplifier (only one input mixer at a time can take this signal)

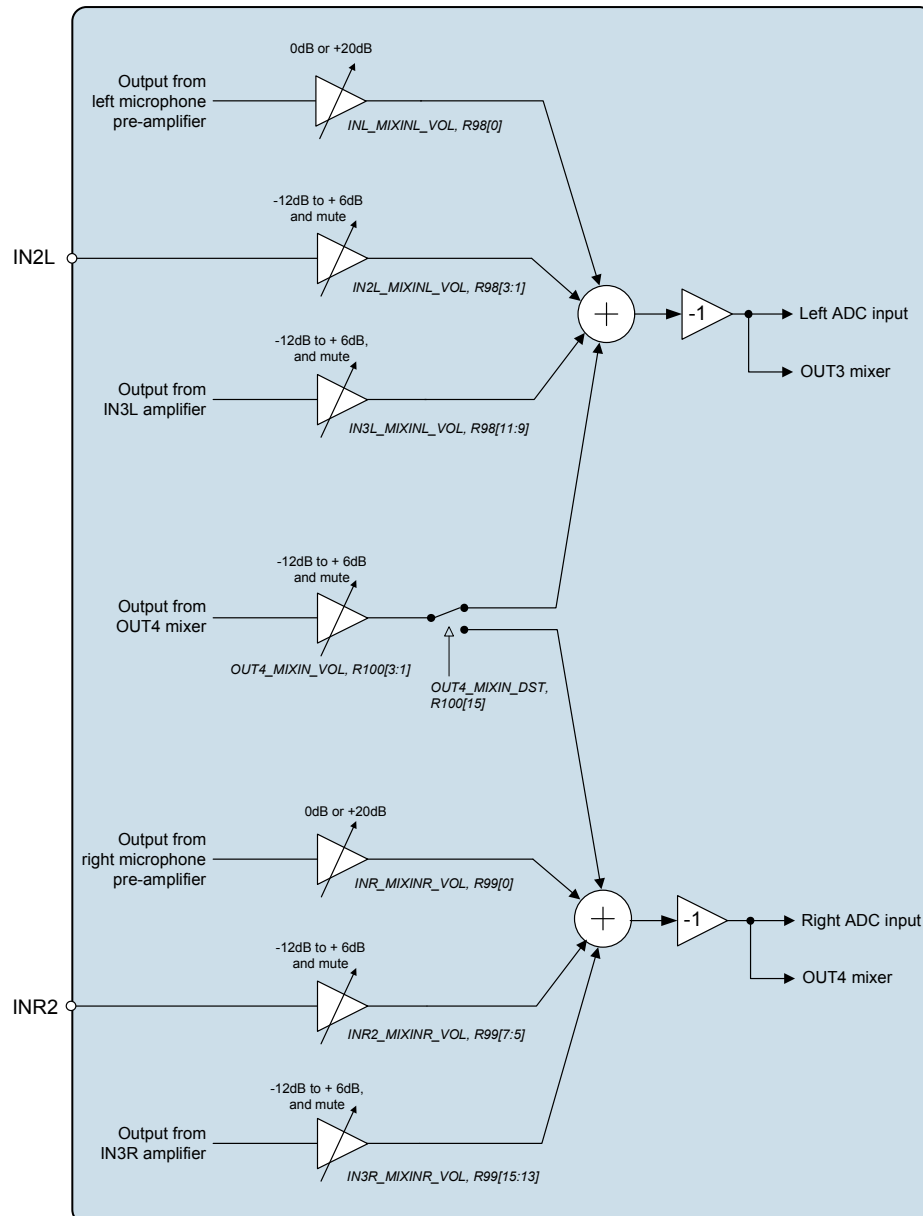


Figure 39 Input Mixers

| ADDRESS   | BIT   | LABEL                     | DEFAULT | DESCRIPTION  |
|---|-------|---------------------------|---------|--|
| R9 (09h)<br>Power Mgmt<br>2                             | 7     | MIXINR_ENA                | 0       | Right input mixer enable<br>0 = disabled<br>1 = enabled  |
|   | 6     | MIXINL_ENA                | 0       | Left input mixer enable<br>0 = disabled<br>1 = enabled   |
| R98 (62h)<br>Input mixer<br>volume for left<br>channel  | 0     | INL_MIXINL_V<br>OL        | 0       | Boost enable for left channel input PGA:<br>0 = PGA output has +0dB gain through<br>input record mixer.<br>1 = PGA output has +20dB gain through<br>input record mixer.  |
|   | 3:1   | IN2L_MIXINL_<br>VOL [2:0] | 000     | IN2L amplifier volume control to right input<br>mixer.<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer                                    |
|   | 11:9  | IN3L_MIXINL_<br>VOL       | 000     | IN3L amplifier volume control to right input<br>mixer.<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer                                    |
| R99 (63h)<br>Input mixer<br>volume for<br>right channel | 0     | INR_MIXINR_<br>VOL        | 1       | Boost enable for right channel input PGA:<br>0 = PGA output has +0dB gain through<br>input record mixer.<br>1 = PGA output has +20dB gain through<br>input record mixer.   |
|   | 7:5   | IN2R_MIXINR_<br>VOL [2:0] | 000     | IN2R amplifier volume control to right<br>input mixer.<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer                                    |
|   | 15:13 | IN3R_MIXINR_<br>VOL [2:0] | 000     | IN3R amplifier volume control to right<br>input mixer.<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer                                    |
| R100 (64h)<br>OUT4 Mixer<br>Control                     | 15    | OUT4_MIXIN_<br>DST        | 0       | Select routing of OUT4 to input mixers.<br>0 = OUT4 to left input mixer.<br>1 = OUT4 to right input mixer.   |
|   | 3:1   | OUT4_MIXIN_<br>VOL [2:0]  | 000     | Controls the gain of OUT4 to left and right<br>input mixers:<br>000 = Path disabled (left and right mute)<br>001 = -12dB gain through boost stages<br>010 = -9dB gain through boost stages<br>....<br>111 = +6dB gain through boost stages |

Table 25 Input Mixer Control

## 13.5 ANALOGUE TO DIGITAL CONVERTER (ADC)

The high-performance stereo ADC within the WM8350 converts analogue input signals to the digital domain. It uses a multi-bit, over-sampled sigma-delta architecture. The ADC's over-sampling rate is selectable to control the trade-off between best audio performance and lowest power consumption. A variety of digital filtering stages process the ADC's digital output signal before it is sent to the WM8350 audio interface. These include:

- digital decimation and filtering needed for the ADC
- digital volume control
- A programmable high-pass filter

The audio ADC supports all commonly used audio sampling rates between 8kHz and 48kHz (see Figure 40).

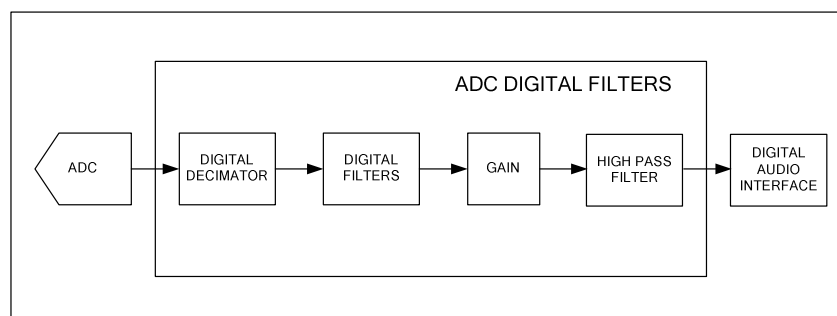


Figure 40 ADC Digital Filter Path

| ADDRESS                           | BIT | LABEL       | DEFAULT | DESCRIPTION  |
|-----------------------------------|-----|-------------|---------|--|
| R11 (0Bh)<br>Power Mgmt 4         | 2   | ADCL_ENA    | 0       | Left ADC enable<br>0 = disabled<br>1 = enabled<br>When ADCL and ADCL are used together as a stereo pair, then both ADCs must be enabled together using a single register write to Register R11 (0Bh).  |
| R66 (42h)<br>ADC Digital Volume L | 15  |             |         |  |
| R11 (0Bh)<br>Power Mgmt 4         | 3   | ADCR_ENA    | 0       | Right ADC enable<br>0 = disabled<br>1 = enabled<br>When ADCR and ADCL are used together as a stereo pair, then both ADCs must be enabled together using a single register write to Register R11 (0Bh). |
| R67 (43h)<br>ADC Digital Volume R | 15  |             |         |  |
| R64 (40h)<br>ADC Control          | 1   | ADCL_DATINV | 0       | ADC Left channel polarity:<br>0 = Normal<br>1 = Inverted   |
|                                   | 0   | ADCR_DATINV | 0       | ADC Right Channel Polarity<br>0 = Normal<br>1 = Inverted   |

**Note:** ADCL\_ENA and ADCR\_ENA can be accessed through R11 or through R66/R67. Reading from or writing to either register location has the same effect.

Table 26 Enabling the ADC Left and Right Channels

When ADCR and ADCL are used together as a stereo pair, then it is important that ADCR\_ENA and ADCL\_ENA are enabled at the same time using a single register write. This must be implemented by writing to the bits in Register R11 (0Bh). This ensures that the system starts up both channels in a synchronous manner.

### 13.5.1 ADC VOLUME CONTROL

Programmable digital volume control is provided to attenuate the ADC's output signal.

| ADDRESS                              | BIT | LABEL              | DEFAULT       | DESCRIPTION   |
|--------------------------------------|-----|--------------------|---------------|---|
| R66 (42h)<br>ADC Digital<br>Volume L | 8   | ADC_VU             | 0             | ADC left and ADC right volume do not update until a 1 is written to either ADC_VU register bit.   |
|                                      | 7:0 | ADCL_VO<br>L [7:0] | 1100_000<br>0 | Left ADC Digital Volume Control<br>0000 0000 = Digital Mute<br>0000 0001 = -71.625dB<br>0000 0010 = -71.25dB<br>... 0.375dB steps up to<br>1110 1111 = +17.625dB  |
| R67 (43h)<br>ADC Digital<br>Volume R | 8   | ADC_VU             | 0             | ADC left and ADC right volume do not update until a 1 is written to either ADC_VU register bit.   |
|                                      | 7:0 | ADCR_VO<br>L [7:0] | 1100_000<br>0 | Right ADC Digital Volume Control<br>0000 0000 = Digital Mute<br>0000 0001 = -71.625dB<br>0000 0010 = -71.25dB<br>... 0.375dB steps up to<br>1110 1111 = +17.625dB |

Table 27 ADC Volume Control

### 13.5.2 ADC HIGH-PASS FILTER

A digital high-pass filter is provided to remove DC offsets from the ADC signal.

| ADDRESS  | BIT | LABEL                 | DEFAULT | DESCRIPTION   |
|--|-----|-----------------------|---------|---|
| R11 (0Bh)<br>Power<br>Mgmt 4   | 13  | ADC_HPF_EN<br>A       | 0       | High Pass Filter enable<br>0 = disabled<br>1 = enabled  |
| R64 (40h)<br>ADC<br>Control  | 15  |                       |         |   |
|  | 9:8 | ADC_HPF_CU<br>T [1:0] | 00      | Select cut-off frequency for high-pass filter<br>00 = $2^{-11}$ (first order) = 3.7Hz @<br>fs=44.1kHz<br>01 = $2^{-5}$ (2nd order) = ~250Hz @ fs=8kHz<br>10 = $2^{-4}$ (2nd order) = ~250Hz @ fs=16kHz<br>11 = $2^{-3}$ (2nd order) = ~250Hz @ fs=32kHz |
| <p><b>Note:</b> ADC_HPF_ENA can be accessed through R11 or through R64. Reading from or writing to either register location has the same effect.</p> |     |                       |         |   |

Table 28 Controlling the ADC High-pass Filter



## 13.6 DIGITAL MIXING

### 13.6.1 DIGITAL SIDETONE

A digital sidetone is available when ADCs and DACs are operating at the same sample rate. Digital data from either left or right ADC can be mixed with the audio interface data on the left and right DAC channels. Sidetone data is taken from the ADC high pass filter output, to reduce low frequency noise in the sidetone (e.g. wind noise or mechanical vibration).

The digital sidetone will not function when ADCs and DACs are operating at different sample rates.

When using the digital sidetone, it is recommended that the ADCs are enabled before un-muting the DACs to prevent pop noise. The DAC volumes and sidetone volumes should be set to an appropriate level to avoid clipping at the DAC input.

The digital sidetone is controlled as shown Table 29.

| REGISTER ADDRESS                             | BIT   | LABEL                  | DEFAULT | DESCRIPTION   |
|--|-------|------------------------|---------|---|
| R68 (44h)<br>ADC<br>Divider                  | 11:8  | ADCL_DAC_SVOL<br>[3:0] | 0000    | Controls left digital side tone volume from -36dB to 0dB in 3dB steps.<br>0000 = -36dB<br>0001 = -33dB<br>... (3dB steps)<br>1011 = -3dB<br>1100 = 0dB<br>11XX = 0dB      |
|  | 7:4   | ADCR_DAC_SVOL<br>[3:0] | 0000    | Controls right digital side tone volume from -36dB to 0dB in 3dB steps.<br><br>0000 = -36dB<br>0001 = -33dB<br>... (3dB steps)<br>1011 = -3dB<br>1100 = 0dB<br>11XX = 0dB |
| R60 (3Ch)<br>Digital Side<br>Tone<br>Control | 13:12 | ADC_TO_DACL<br>[1:0]   | 00      | DAC Left Side-tone Control<br>11 = Unused<br>10 = Mix ADCR into DACL<br>01 = Mix ADCL into DACL<br>00 = No Side-tone mix into DACL  |
|  | 11:10 | ADC_TO_DACR<br>[1:0]   | 00      | DAC Right Side-tone Control<br>11 = Unused<br>10 = Mix ADCR into DACR<br>01 = Mix ADCL into DACR<br>00 = No Side-tone mix into DACR                                       |

**Table 29 Digital Side Tone Control**

The coding of ADCL\_DAC\_SVOL and ADCR\_DAC\_SVOL is described in Table 30.

| ADCL_DAC_SVOL or<br>ADCR_DAC_SVOL | SIDETONE<br>VOLUME |
|-----------------------------------|--------------------|
| 0000                              | -36                |
| 0001                              | -33                |
| 0010                              | -30                |
| 0011                              | -27                |
| 0100                              | -24                |
| 0101                              | -21                |
| 0110                              | -18                |
| 0111                              | -15                |
| 1000                              | -12                |
| 1001                              | -9                 |
| 1010                              | -6                 |
| 1011                              | -3                 |
| 1100                              | 0                  |
| 1101                              | 0                  |
| 1110                              | 0                  |
| 1111                              | 0                  |

Table 30 Digital Side Tone Control

### 13.7 DIGITAL TO ANALOGUE CONVERTER (DAC)

The WM8350 contains a high-performance stereo DAC to convert digital audio signals to the analogue domain. Audio data is passed to the WM8350 via the audio interface, and passes through a variety of digital filtering stages before reaching the DAC. These include:

- Digital volume control
- Digital filtering, interpolation and sigma-delta modulation functions needed for the DAC

The audio DAC supports all commonly used audio sampling rates between 8kHz and 48kHz.

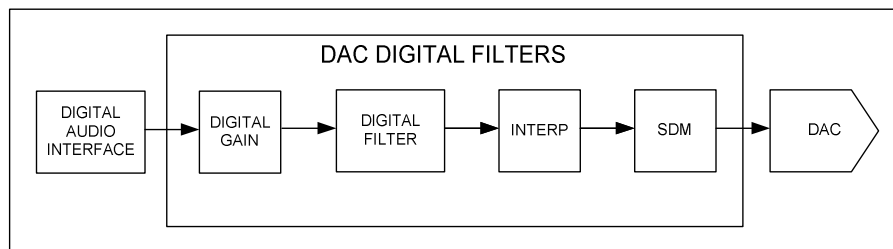


Figure 41 DAC Overview

| ADDRESS  | BIT | LABEL        | DEFAULT | DESCRIPTION                                     |
|--|-----|--------------|---------|---|
| R11 (0Bh)<br>Power Mgmt<br>4   | 4   | DACL_EN<br>A | 0       | Left DAC enable<br>0 = disabled<br>1 = enabled  |
| R50 (32h)<br>DAC Digital<br>Volume Left  | 15  |              |         |   |
| R11 (0Bh)<br>Power Mgmt  | 5   | DACR_EN<br>A | 0       | Right DAC enable<br>0 = disabled<br>1 = enabled |
| R51 (33h)<br>DAC Digital<br>Volume Right   | 15  |              |         |   |
| <b>Note:</b> These bits can be accessed through R11 or through R50/R51. Reading from or writing to either register location has the same effect. |     |              |         |   |

Table 31 DAC Enable

13.7.1 DAC PLAYBACK VOLUME CONTROL

| REGISTER ADDRESS                      | BIT | LABEL          | DEFAULT   | DESCRIPTION  |
|---------------------------------------|-----|----------------|-----------|--|
| R50 (32h)<br>DAC Digital Volume Left  | 8   | DAC_VU         | 0         | DAC left and DAC right volume do not update until a 1 is written to either DAC_VU register bit.  |
|                                       | 7:0 | DACL_VOL [7:0] | 1100_0000 | Left DAC digital volume control:<br>0000_0000 = Digital mute<br>0000_0001 = -71.625dB<br>0000_0010 = -71.25dB<br>... (0.375dB steps)<br>1100_0000 = 0dB  |
| R51 (33h)<br>DAC Digital Volume Right | 8   | DAC_VU         | 0         | DAC left and DAC right volume do not update until a 1 is written to either DAC_VU register bit.  |
|                                       | 7:0 | DACR_VOL [7:0] | 1100_0000 | Right DAC digital volume control:<br>0000_0000 = Digital mute<br>0000_0001 = -71.625dB<br>0000_0010 = -71.25dB<br>... (0.375dB steps)<br>1100_0000 = 0dB |

Table 32 DAC Volume Control

13.7.2 DAC SOFT MUTE AND SOFT UN-MUTE

The WM8350 has a soft mute function which, when enabled, gradually attenuates the volume of the DAC output. When soft mute is disabled, the gain will either gradually ramp back up to the digital gain setting, or return instantly to the digital gain setting, depending on the DAC\_MUTEMODE register bit.

The DAC is soft-muted by default (DAC\_MUTE = 1). To play back an audio signal, this function must first be disabled by setting DAC\_MUTE to 0.

Soft Mute Mode would typically be enabled (DAC\_MUTEMODE = 1) when using DAC\_MUTE during playback of audio data so that when DAC\_MUTE is subsequently disabled, the sudden volume increase will not create pop noise by jumping immediately to the previous volume level (e.g. resuming playback after pausing during a track).

Soft Mute Mode would typically be disabled (DAC\_MUTEMODE = 0) when un-muting at the start of a music file, in order that the first part of the track is not attenuated (e.g. when starting playback of a new track, or resuming playback after pausing between tracks).

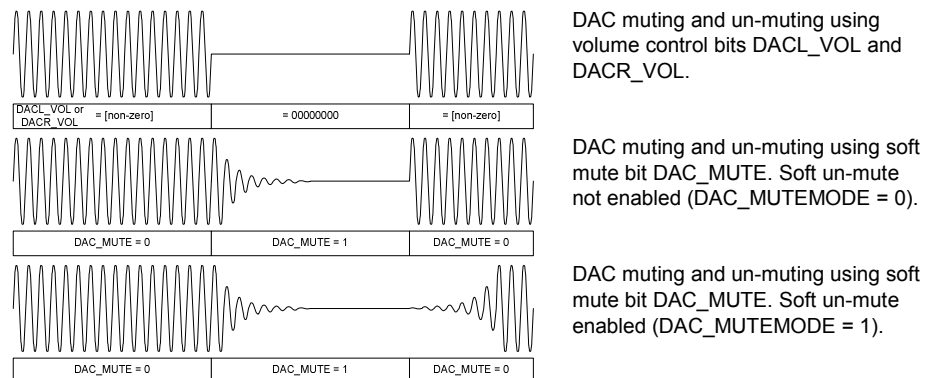


Figure 42 DAC Mute Control

The volume ramp rate during soft mute and un-mute is controlled by the DAC\_MUTERATE bit. Ramp rates of fs/32 and fs/2 are selectable as shown

| REGISTER ADDRESS                | BIT | LABEL            | DEFAULT | DESCRIPTION   |
|---------------------------------|-----|------------------|---------|---|
| R58 (3Ah)<br>DAC Mute           | 14  | DAC_MUTE         | 1       | DAC Mute<br>0 = disabled<br>1 = enabled   |
| R59 (3Bh)<br>DAC Mute<br>Volume | 14  | DAC_MUTEM<br>ODE | 0       | DAC Soft Mute Mode<br>0 = Disabling soft-mute<br>(DAC_MUTE=0) will cause the volume to change immediately to the DACL_VOL / DACR_VOL settings<br>1 = Disabling soft-mute<br>(DAC_MUTE=0) will cause the volume to ramp up gradually to the DACL_VOL / DACR_VOL settings |
|                                 | 13  | DAC_MUTER<br>ATE | 0       | DAC Soft Mute Ramp Rate<br>0 = Fast ramp (24kHz at fs=48k, providing maximum delay of 10.7ms)<br>1 = Slow ramp (1.5kHz at fs=48k, providing maximum delay of 171ms)   |

Table 33 DAC Soft-Mute Control

### 13.7.3 DAC DE-EMPHASIS

Digital de-emphasis can be applied to the DAC playback data (e.g. when the data comes from a CD with pre-emphasis used in the recording). De-emphasis filtering is available for sample rates of 48kHz, 44.1kHz and 32kHz.

| REGISTER ADDRESS         | BIT | LABEL       | DEFAULT | DESCRIPTION  |
|--------------------------|-----|-------------|---------|--|
| R48 (30h)<br>DAC Control | 5:4 | DEEMP [1:0] | 00      | De-Emphasis Control<br>11 = 48kHz sample rate<br>10 = 44.1kHz sample rate<br>01 = 32kHz sample rate<br>00 = No de-emphasis |

Table 34 DAC De-Emphasis Control

### 13.7.4 DAC OUTPUT PHASE AND MONO MIXING

The digital audio data is converted to oversampled bit streams in the on-chip 24-bit digital interpolation filters. The bitstream data enters two multi-bit, sigma-delta DACs, which convert them to high quality analogue audio signals. The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter. It also uses a Dynamic Element Matching technique for high linearity and low distortion.

In normal operation, the left and right channel digital audio data is converted to analogue in two separate DACs. It is also possible for the DACs to output a mono mix of left and right channels, using DAC\_MONO. Both DACs must be enabled for this mono mix to function.

| REGISTER ADDRESS      | BIT | LABEL       | DEFAULT | DESCRIPTION   |
|-----------------------|-----|-------------|---------|---|
| R48 (30h) DAC Control | 13  | DAC_MONO    | 0       | Adds left and right channel and halves the resulting output to create a mono output |
|                       | 1   | DACL_DATINV | 0       | DAC data left channel polarity<br>0 = Normal<br>1 = Inverted                        |
|                       | 0   | DACR_DATINV | 0       | DAC data right channel polarity<br>0 = Normal<br>1 = Inverted                       |

Table 35 DAC Mono Mix and Phase Invert Select

### 13.7.5 DAC STOPBAND ATTENUATION

The DAC digital filter type is selected by the DAC\_SB\_FILT register bit as shown in Table 36.

| REGISTER ADDRESS              | BIT | LABEL       | DEFAULT | DESCRIPTION  |
|-------------------------------|-----|-------------|---------|--|
| R59 (3Bh) DAC Digital Control | 12  | DAC_SB_FILT | 0       | Selects DAC filter characteristics<br>0 = Normal mode<br>1 = Sloping stopband mode |

Table 36 DAC Filter Selection

## 13.8 OUTPUT SIGNAL PATH

The analogue output pins produce audio signals to drive headphones, line-out connections and/or external loudspeaker amplifiers. These pins include:

- OUT1L and OUT1R
- OUT2L and OUT2R
- OUT3 and OUT4

OUT1L, OUT1R, OUT2L and OUT2R have individual analogue volume PGAs with -57dB to +6dB ranges. AC-coupled and Capless headphone drive modes are available. Common mode noise rejection is possible using the HPCOM connection.

OUT3 and OUT4 can be configured as a stereo line out (OUT3 is left output and OUT4 is right output). OUT3 and OUT4 can also be used as a Vmid buffer to provide a "ground" reference for headphone outputs, eliminating the need for DC blocking capacitors.

Alternatively, OUT4 can be used to provide a mono mix of left and right channels.

All analogue output pins are powered through the HPVDD and HPGND pins.

Each output can drive a headphone load down to 16Ω.

There are four output mixers in the output signal path: the left and right channel mixers which control the signals to headphone (and optionally the line outputs) and also dedicated OUT3 and OUT4 mixers.

### 13.8.1 ENABLING THE ANALOGUE OUTPUTS

Each output can be individually enabled or disabled via dedicated control bits.

| ADDRESS  | BIT | LABEL     | DEFAULT | DESCRIPTION                 |
|--|-----|-----------|---------|-----------------------------|
| R10 (0Ah)  | 0   | OUT1L_ENA | 0       | OUT1L enable                |
| R104 (68h)   | 15  |           |         | 0 = disabled<br>1 = enabled |
| R10 (0Ah)  | 1   | OUT1R_ENA | 0       | OUT1R enable                |
| R105 (69h)   | 15  |           |         | 0 = disabled<br>1 = enabled |
| R10 (0Ah)  | 2   | OUT2L_ENA | 0       | OUT2L enable                |
| R106 (70h)   | 15  |           |         | 0 = disabled<br>1 = enabled |
| R10 (0Ah)  | 3   | OUT2R_ENA | 0       | OUT2R enable                |
| R107 (71h)   | 15  |           |         | 0 = disabled<br>1 = enabled |
| R9 (09h)   | 4   | OUT3_ENA  | 0       | OUT3 enable                 |
| R92 (5Ch)  | 15  |           |         | 0 = disabled<br>1 = enabled |
| R9 (09h)   | 5   | OUT4_ENA  | 0       | OUT4 enable                 |
| R93 (5Dh)  | 15  |           |         | 0 = disabled<br>1 = enabled |
| <b>Note:</b> Each bit can be accessed through two separate control registers. Reading from or writing to either register location has the same effect. |     |           |         |                             |

**Table 37 Enabling the Analogue Outputs**

13.8.2 OUTPUT MIXERS

The left and right output channel mixers are shown in Figure 43. These mixers allow the AUX inputs, the ADC bypass and the DAC left and right channels to be combined as desired. This allows a mono mix of the DAC channels to be done as well as mixing in external line-in from the IN3.

The IN3L/IN3R and PGA inputs have individual volume control from -15dB to +6dB. The DAC channel volumes can be adjusted in the digital domain if required. The outputs of these mixers are routed to OUT1L/OUT1R or OUT2L/OUT2R. They can also optionally be routed to the OUT3 and OUT4 mixers.

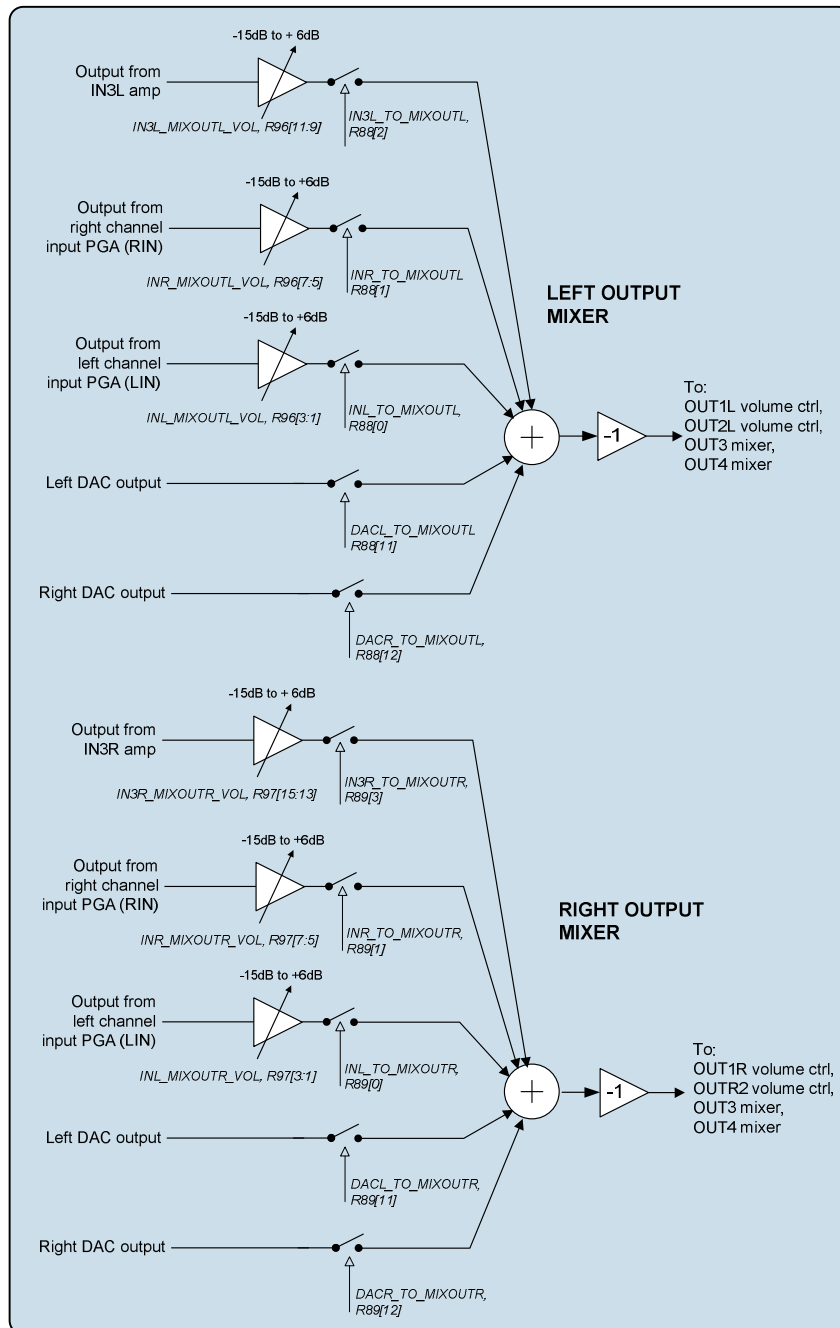


Figure 43 Output Mixers



Each output mixer can be enabled or disabled by writing either to the power management control register or to the respective mixer's own control register. Each analogue signal going into the output mixers can be independently enabled or muted for each mixer.

| ADDRESS   | BIT | LABEL               | DEFAULT | DESCRIPTION  |
|---|-----|---------------------|---------|--|
| R88 (58h)<br>Left Mixer<br>Control  | 0   | INL_TO_MIXOU<br>TL  | 0       | Left input PGA output to left output mixer<br>0 = not selected<br>1 = selected   |
|   | 1   | INR_TO_MIXOU<br>TL  | 0       | Right input PGA output to left output mixer<br>0 = not selected<br>1 = selected  |
|   | 2   | IN3L_TO_MIXO<br>UTL | 0       | IN3L amplifier output to left output mixer:<br>0 = not selected<br>1 = selected  |
|   | 11  | DACL_TO_MIX<br>OUTL | 0       | Left DAC output to left output mixer<br>0 = not selected<br>1 = selected         |
|   | 12  | DACR_TO_MIX<br>OUTL | 0       | Right DAC output to left output mixer<br>0 = not selected<br>1 = selected        |
|   | 15  | MIXOUTL_ENA         | 0       | Left output mixer enable<br>0 = disabled<br>1 = enabled                          |
| R9 (09h)<br>Power Mgmt 2  | 0   |                     |         |  |
| R89 (59h)<br>Right Mixer<br>Control   | 0   | INL_TO_MIXOU<br>TR  | 0       | Left input PGA output to right output mixer<br>0 = not selected<br>1 = selected  |
|   | 1   | INR_TO_MIXOU<br>TR  | 0       | Right input PGA output to right output mixer<br>0 = not selected<br>1 = selected |
|   | 3   | IN3L_TO_MIXO<br>UTR | 0       | IN3L amplifier output to right output mixer:<br>0 = not selected<br>1 = selected |
|   | 11  | DACL_TO_MIX<br>OUTR | 0       | Left DAC output to right output mixer<br>0 = not selected<br>1 = selected        |
|   | 12  | DACR_TO_MIX<br>OUTR | 0       | Right DAC output to right output mixer<br>0 = not selected<br>1 = selected       |
|   | 15  | MIXOUTR_ENA         | 0       | Right output mixer enable<br>0 = disabled<br>1 = enabled                         |
| R9 (09h)<br>Power Mgmt 2  | 1   |                     |         |  |
| <b>Note:</b> MIXOUTL_ENA and MIXOUTR_ENA can be accessed through two separate control registers. Reading from or writing to either register location has the same effect. |     |                     |         |  |

**Table 38 Selecting Signals into the Output Mixers**

The gain for microphone pre-amp and auxiliary input (IN3L/IN3R) signals can be independently adjusted for each output mixer. This does not affect the volume of the same signals going into the separate record mixer. The level of the DAC output signals can be adjusted using the DAC's digital volume control function (see Table 32).

| ADDRESS                                      | BIT       | LABEL                      | DEFAULT | DESCRIPTION  |
|--|-----------|----------------------------|---------|--|
| R96 (60h)<br>Output Left<br>Mixer<br>Volume  | 3:1       | INL_MIXOUTL_VOL<br>[2:0]   | 000     | Left input PGA volume control to left output mixer.<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer   |
|  | 7:5       | INR_MIXOUTL_VO<br>L [2:0]  | 000     | Right input PGA volume control to left output mixer.<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer  |
|  | 11:9      | IN3L_MIXOUTL_VO<br>L [2:0] | 000     | IN3L amplifier volume control to left output mixer<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer    |
| R97 (61h)<br>Output Right<br>Mixer<br>Volume | 3:1       | INL_MIXOUTR_VO<br>L [2:0]  | 000     | Left input PGA volume control to right output mixer.<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer  |
|  | 7:5       | INR_MIXOUTR_VO<br>L [2:0]  | 000     | Right input PGA volume control to right output mixer.<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer |
|  | 15:1<br>3 | IN3R_MIXOUTR_V<br>OL [2:0] | 000     | IN3R amplifier volume control to right output mixer.<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer  |

**Table 39 Controlling the Gain of Signals Going into the Output Mixers**

## 13.9 ANALOGUE OUTPUTS

### 13.9.1 OUT1L AND OUT1R

The headphone outputs, OUT1L and OUT1R can drive a 16Ω or 32Ω headphone load, either through DC blocking capacitors, or DC coupled without any capacitor. Each output has an analogue volume control PGA with a gain range of -57dB to +6dB as shown in Figure 44.

Common mode noise rejection is also possible on the OUT1L and OUT1R outputs, using HPCOM as the return path. The HPCOM feature must be enabled via the OUT1\_FB register field and the HPCOM connection must be AC coupled to the headphone output. A 4.7μF coupling capacitor is required between the noisy ground connection the HPCOM pin.

The control register fields for the OUT1L and OUT1R outputs are described in Table 40. The available output configurations are shown in Section 13.9.3.

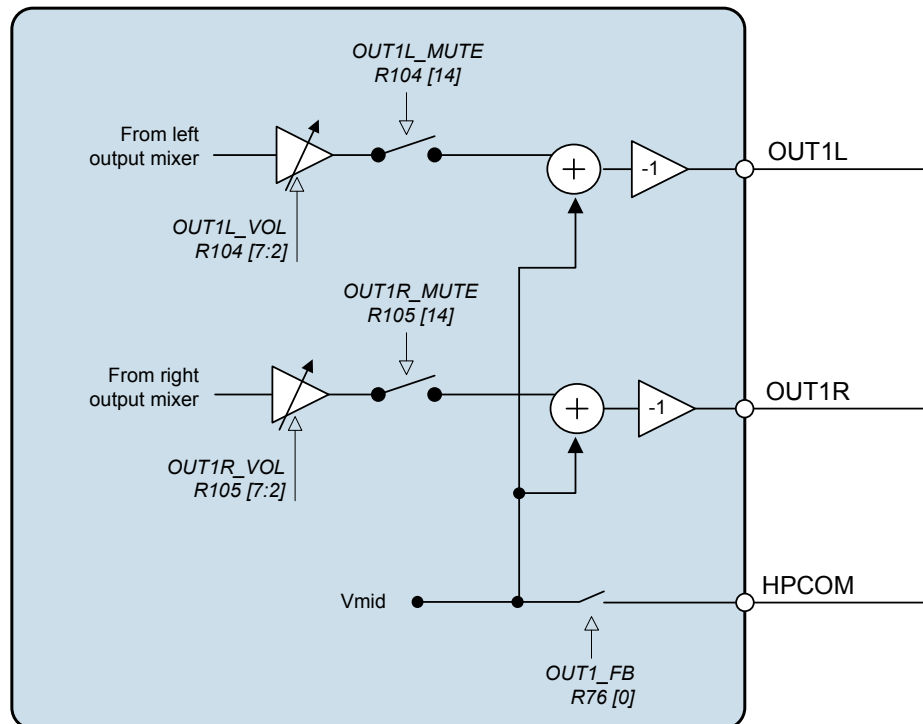


Figure 44 Headphone Outputs OUT1L and OUT1R

| ADDRESS                        | BIT | LABEL              | DEFAULT | DESCRIPTION  |
|--------------------------------|-----|--------------------|---------|--|
| R104 (68h)<br>OUT1L<br>Volume  | 14  | OUT1L_MUTE         | 0       | OUT1L mute:<br>0 = normal operation<br>1 = mute  |
|                                | 13  | OUT1L_ZC           | 0       | OUT1L volume zero cross enable<br>0 = Change gain immediately<br>1 = Change gain on zero cross only  |
|                                | 8   | OUT1_VU            | 0       | OUT1L and OUT1R volumes do not<br>update until a 1 is written to either<br>OUT1_VU.  |
|                                | 7:2 | OUT1L_VOL<br>[5:0] | 11_1001 | OUT1L volume:<br>000000 = -57dB<br>...<br>111001 = 0dB<br>...<br>111111 = +6dB   |
| R105 (69h)<br>OUT1R<br>Volume  | 14  | OUT1R_MUTE         | 0       | OUT1R mute:<br>0 = normal operation<br>1 = mute  |
|                                | 13  | OUT1R_ZC           | 0       | OUT1R volume zero cross enable<br>0 = Change gain immediately<br>1 = Change gain on zero cross only  |
|                                | 8   | OUT1_VU            | 0       | OUT1L and OUT1R volumes do not<br>update until a 1 is written to either<br>OUT1_VU.  |
|                                | 7:2 | OUT1R_VOL<br>[5:0] | 11_1001 | OUT1R volume:<br>000000 = -57dB<br>...<br>111001 = 0dB<br>...<br>111111 = +6dB   |
| R76 (4Ch)<br>Output<br>Control | 0   | OUT1_FB            | 0       | Enable Headphone common mode<br>ground feedback for OUT1<br>0 = disabled (HPCOM unused)<br>1 = enabled (common mode feedback<br>through HPCOM) |

Table 40 Controlling OUT1L and OUT1R

### 13.9.2 OUT2L AND OUT2R

OUT2L and OUT2R are designed as a stereo pair and can drive a headphone, a line load or a loudspeaker amplifier. Each output has an analogue volume control PGA with a gain range of -57dB to +6dB as shown in Figure 45.

Common mode noise rejection is also possible on the OUT2L and OUT2R outputs, using HPCOM as the return path. The HPCOM feature must be enabled via the OUT2\_FB register field and the HPCOM connection must be AC coupled to the headphone output. A 4.7uF coupling capacitor is required between the noisy ground connection the HPCOM pin.

The signal path from the right output mixer to OUT2R can be inverted, using the OUT2R\_INV and OUT2R\_INV\_MUTE register bits. Table 41 describes the required settings of these register bits for inverted and non-inverted configurations. Note that the OUT2R\_MUTE mutes the OUT2R signal path in both cases.

| OUT2R_INV | OUT2R_INV_MUTE | DESCRIPTION                              |
|-----------|----------------|--|
| 0         | 1              | Non-inverting path from MIXOUTR to OUT2R |
| 1         | 0              | Inverting path from MIXOUTR to OUT2R     |

Table 41 OUT2R Signal Path Polarity

The control register fields for the OUT2L and OUT2R outputs are described in Table 42. The available output configurations are shown in Section 13.9.3.

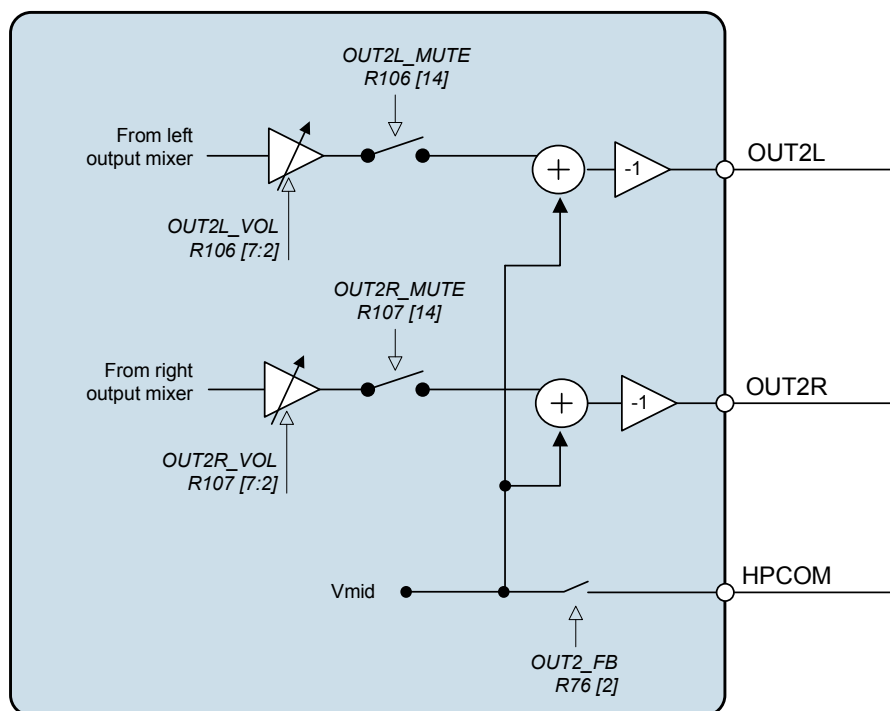


Figure 45 Headphone Outputs OUT2L and OUT2R

| ADDRESS                           | BIT | LABEL              | DEFAULT | DESCRIPTION  |
|-----------------------------------|-----|--------------------|---------|--|
| R106 (6Ah)<br>for OUT2L<br>Volume | 14  | OUT2L_MUTE         | 0       | OUT2L mute:<br>0 = normal operation<br>1 = mute  |
|                                   | 13  | OUT2L_ZC           | 0       | OUT2L volume zero cross enable<br>0 = Change gain immediately<br>1 = Change gain on zero cross only  |
|                                   | 8   | OUT2_VU            | 0       | OUT2L and OUT2R volumes do not update until a 1 is written to either OUT2_VU register bits.  |
|                                   | 7:2 | OUT2L_VOLUME [5:0] | 11_1001 | OUT2L volume:<br>000000 = -57dB<br>...<br>111001 = 0dB<br>...<br>111111 = +6dB   |
| R107 (6Bh)<br>for OUT2R           | 14  | OUT2R_MUTE         | 0       | OUT2R mute:<br>0 = normal operation<br>1 = mute  |
|                                   | 13  | OUT2R_ZC           | 0       | OUT2R volume zero cross enable<br>0 = Change gain immediately<br>1 = Change gain on zero cross only  |
|                                   | 10  | OUT2R_INV          | 0       | Enable OUT2R inverting amplifier<br>0 = disabled<br>1 = enabled<br>This register must be set to 0 when using the non-inverting MIXOUT2R to OUT2R path.<br>This register must be set to 1 when using the inverting MIXOUT2R to OUT2R path.  |
|                                   | 9   | OUT2R_INV_MUTE     | 1       | Mute output of PGA to inverting amplifier.<br>0 = PGA output goes to inverting amplifier<br>1 = PGA output goes to output driver<br>This register must be set to 0 when using the inverting MIXOUT2R to OUT2R path.<br>This register must be set to 1 when using the non-inverting MIXOUT2R to OUT2R path. |
|                                   | 8   | OUT2_VU            | 0       | OUT2L and OUT2R volumes do not update until a 1 is written to either OUT2_VU register bits.  |
|                                   | 7:2 | OUT2R_VOLUME [5:0] | 11_1001 | OUT2R volume:<br>000000 = -57dB<br>...<br>111001 = 0dB<br>...<br>111111 = +6dB   |
| R76 (4Ch)<br>Output<br>Control    | 2   | OUT2_FB            | 0       | Enable Headphone common mode ground feedback for OUT2<br>0 = disabled (HPCOM unused)<br>1 = enabled (common mode feedback through HPCOM)   |

Table 42 Controlling OUT2L and OUT2R

A beep signal on the IN3R pin (see Table 43) can be mixed into OUT2R independently of the right output mixer (i.e. without mixing the same beep signal into OUT1R).

Note that this feature is only possible when the inverting path configuration (MIXOUTR to OUT2R) is selected. See Table 41 for the required register settings.

| ADDRESS                      | BIT | LABEL                | DEFAULT | DESCRIPTION  |
|------------------------------|-----|----------------------|---------|--|
| R111 (6Fh)<br>Beep<br>Volume | 15  | IN3R_TO_OUT2R        | 0       | Beep mixer enable<br>0 = disabled<br>1 = enabled                     |
|                              | 7:5 | IN3R_OUT2R_VOL [2:0] | 000     | Beep mixer volume:<br>000 = -15dB<br>... in +3dB steps<br>111 = +6dB |

Table 43 Controlling the “Beep” Path (IN3R to OUT2R)

### 13.9.3 HEADPHONE OUTPUTS EXTERNAL CONNECTIONS

Some example headphone output configurations are shown below.

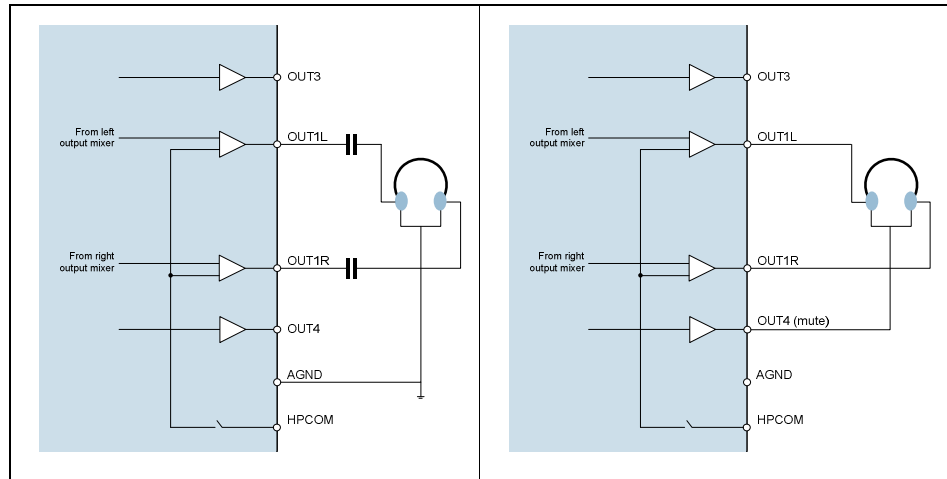


Figure 46 AC-Coupled Headphone Drive

Figure 47 DC-Coupled (Capless) Mode Headphone Drive

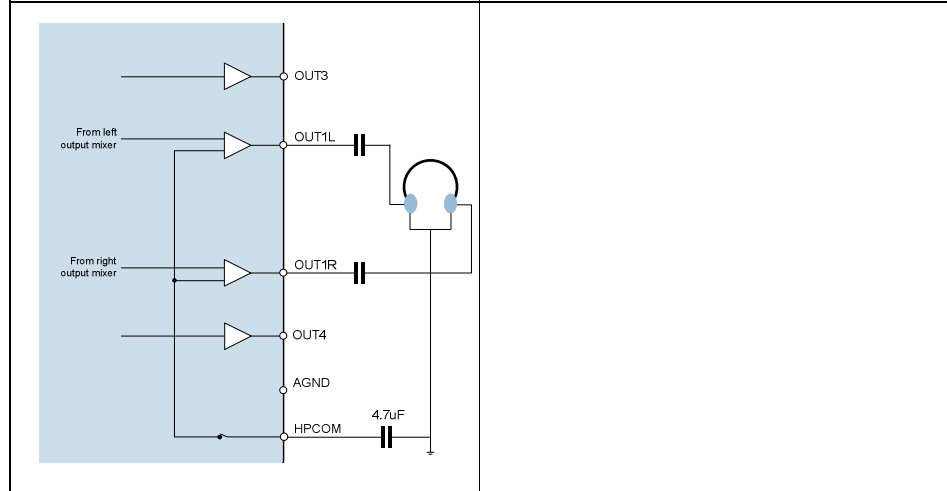


Figure 48 AC-Coupled Headphone Drive with Common Mode Noise Rejection

**Notes:**

The above figures illustrate the headphone connections to outputs OUT1L and OUT1R. The equivalent configurations apply equally to OUT2L and OUT2R.

The DC-coupled configuration illustrated in Figure 47 shows OUT4 (muted) being used as the Ground Return connection. The same capability may alternatively be provided using OUT3.

Twin headphone output (OUT1L, OUT1R, OUT2L and OUT2R) is possible, using a shared Ground Return connection via any of OUT3, OUT4, HPCOM or AGND.

Capless operation is not possible when using the HPCOM feature.

When DC blocking capacitors are used their capacitance and the load resistance together determine the lower cut-off frequency,  $f_c$ . Increasing the capacitance lowers  $f_c$ , improving the bass response. Smaller capacitance values will diminish the bass response. For a  $16\Omega$  load and a capacitance of  $220\mu\text{F}$ , the following derivation of cut-off frequency applies:

$$f_c = 1 / 2\pi R_L C_1 = 1 / (2\pi \times 16\Omega \times 220\mu\text{F}) = 45 \text{ Hz}$$

In the DC coupled configuration, the headphone "ground" is connected to VMID. The OUT3 or OUT4 pins can be configured as DC output drivers by de-selecting all inputs to the OUT3 or OUT4 mixers. The DC voltage on VMID in this configuration is equal to the DC offset on the OUT1L and OUT2L pins therefore no DC blocking capacitors are required. This saves space and material cost in portable applications.

It is recommended to only use the DC coupled configuration to drive headphones, and not to use this configuration to drive the line input of another device.



### 13.9.4 OUT3 AND OUT4

The additional analogue outputs OUT3 and OUT4 have independent mixers and can be used in a number of different ways:

- OUT3 and OUT4 as a stereo pair (OUT3 = left, OUT4 = right) to drive a headphone or line load
- OUT3 or OUT4 as pseudo-ground outputs for headphones connected directly (without DC blocking capacitors) to OUT1L/OUT1R or OUT2L/OUT2R
- OUT4 as a mono mix of left and right signals

The OUT3 and OUT4 output stages are powered from HPVDD and HPGND.

If OUT4 is providing a mono mix, it is recommended to reduce the level of OUT4 by 6dB to avoid clipping in the event of 2 full-scale signals being combined. This is implemented via the OUT4\_ATT register field. When OUT4\_ATT is asserted, then  $OUT4 = (L+R) / 2$ .

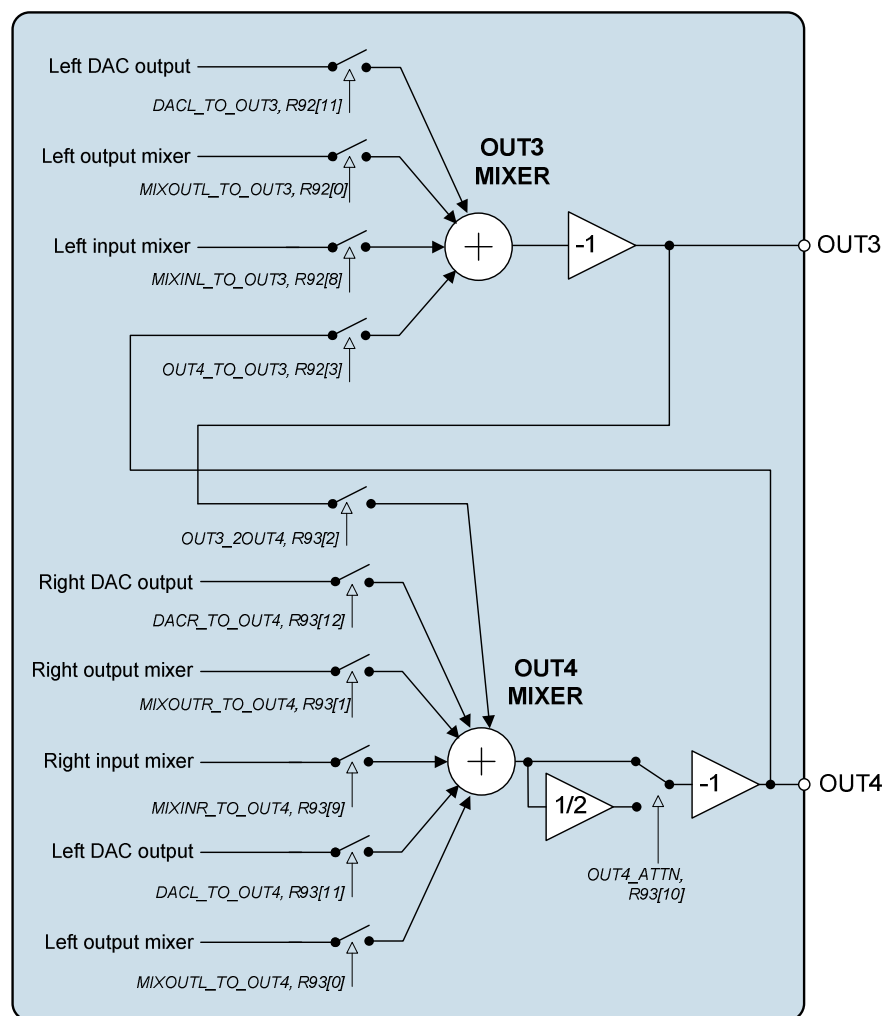


Figure 49 OUT 3 and OUT4 Mixers

OUT3 can provide a buffered midrail headphone pseudo-ground, or a left line output. It can also be a common mode input for OUT2L/OUT2R. OUT4 can provide a buffered midrail headphone pseudo-ground, a right line output, or a mono mix output. It can also be mixed into the input boost mixer for recording.

| ADDRESS   | BIT | LABEL           | DEFAULT | DESCRIPTION  |
|---|-----|-----------------|---------|--|
| R92 (5Ch)<br>OUT3 Mixer   | 11  | DACL_TO_OUT3    | 0       | Left DAC output to OUT3<br>0 = disabled<br>1 = enabled   |
|   | 8   | MIXINL_TO_OUT3  | 0       | Left input mixer to OUT3<br>0 = disabled<br>1 = enabled  |
|   | 3   | OUT4_TO_OUT3    | 0       | OUT4 mixer to OUT3<br>0 = disabled<br>1 = enabled        |
|   | 0   | MIXOUTL_TO_OUT3 | 0       | Left output mixer to OUT3<br>0 = disabled<br>1 = enabled |
| R92 (5Ch)<br>OUT3 Mixer   | 15  | OUT3_ENA        | 0       | OUT3 enable<br>0 = disabled<br>1 = enabled               |
| R9 (09h)<br>Power Mgmt 2  | 4   |                 |         |  |
| <b>Note:</b> OUT3_ENA can be accessed through R92 or R9. Reading from or writing to either register location has the same effect. |     |                 |         |  |

**Table 44 Controlling the OUT3 Mixer**

| ADDRESS   | BIT | LABEL           | DEFAULT | DESCRIPTION  |
|---|-----|-----------------|---------|--|
| R93 (5Dh)<br>OUT4 Mixer   | 12  | DACR_TO_OUT4    | 0       | Right DAC output to OUT4<br>0 = disabled<br>1 = enabled                              |
|   | 11  | DACL_TO_OUT4    | 0       | Left DAC output to OUT4<br>0 = Disabled<br>1 = Enabled                               |
|   | 10  | OUT4_ATT        | 0       | Reduce OUT4 output by 6dB<br>0 = Output at normal level<br>1 = Output reduced by 6dB |
|   | 9   | MIXINR_TO_OUT4  | 0       | Right input mixer to OUT4<br>0 = disabled<br>1 = enabled                             |
|   | 2   | OUT3_TO_OUT4    | 0       | OUT3 mixer to OUT4<br>This function is not supported                                 |
|   | 1   | MIXOUTR_TO_OUT4 | 0       | Right output mixer to OUT4<br>0 = disabled<br>1 = enabled                            |
|   | 0   | MIXOUTL_TO_OUT4 | 0       | Left output mixer to OUT4<br>0 = disabled<br>1 = enabled                             |
| R93 (5Dh)<br>OUT4 Mixer   | 15  | OUT4_ENA        | 0       | OUT4 enable<br>0 = disabled<br>1 = enabled   |
| R9 (09h)<br>Power Mgmt 2  | 5   |                 |         |  |
| <b>Note:</b> OUT4_ENA can be accessed through R93 or R9. Reading from or writing to either register location has the same effect. |     |                 |         |  |

**Table 45 Controlling the OUT4 Mixer**

## 13.10 DIGITAL AUDIO INTERFACE

The audio interface enables the WM8350 to exchange audio data with other system components. It is separate from the control interface and has four dedicated pins:

- ADCDAT: Output pin for data coming from the audio ADC
- DACDAT: Input pin for audio data going to the audio DAC
- LRCLK: Data Left/Right alignment clock (also known as “word clock”)
- BCLK: Bit clock, for synchronisation

The LRCLK and BCLK pins are outputs when the WM8350 operates as a master device and are inputs when it is a slave device.

In order to allow the ADC and DAC to run at different sampling rates, separate ADCLRCLK and ADCBCLK signals are both available through GPIO pins: GPIO5 (ADCLRCLK) and GPIO6 or GPIO8 (ADCBCLK). This feature also allows mixed Master/Slave operation between the ADC and DAC.

### 13.10.1 AUDIO DATA FORMATS

The audio interface supports six different audio data formats:

- Left justified
- Right justified
- I<sup>2</sup>S
- DSP mode A
- DSP mode B
- TDM Mode

In all of these formats, the MSB (most significant bit) of each data sample is transferred first and the LSB (least significant bit) last.

| ADDRESS                       | BIT   | LABEL         | DEFAULT         | DESCRIPTION  |
|-------------------------------|-------|---------------|-----------------|--|
| R112 (70h)<br>Audio Interface | 15    | AIF_BCLK_INV  | 0               | BCLK polarity<br>0 = normal<br>1 = inverted  |
|                               | 13    | AIF_TRI       | 0               | Sets Output enables for LRCLK and BCLK and ADCDAT to inactive state<br>0 = normal<br>1 = forces pins to Hi-Z   |
|                               | 12    | AIF_LRCLK_INV | 0               | LRCLK clock polarity<br>0 = normal<br>1 = inverted<br><br>DSP Mode – mode A/B select<br>0 = MSB is available on 2 <sup>nd</sup> BCLK rising edge after LRCLK rising edge (mode A)<br>1 = MSB is available on 1 <sup>st</sup> BCLK rising edge after LRCLK rising edge (mode B) |
|                               | 11:10 | AIF_WL [1:0]  | 10<br>(24 bits) | Data word length<br>11 = 32 bits<br>10 = 24 bits<br>01 = 20 bits<br>00 = 16 bits<br><br>Note: When using the Right-Justified data format (AIF_FMT=00), the maximum word length is 24 bits.   |

| ADDRESS                                   | BIT | LABEL           | DEFAULT                  | DESCRIPTION   |
|---|-----|-----------------|--------------------------|---|
|   | 8:9 | AIF_FMT [1:0]   | 10<br>(I <sup>2</sup> S) | Data format<br>00 = Right Justified<br>01 = Left Justified<br>10 = I <sup>2</sup> S<br>11 = DSP / PCM mode<br>Note - see Section 13.11 for the selection of 8-bit mode. |
| R114 (72h)<br>Audio Interface ADC Control | 7   | AIFADC_PD       | 0                        | Enables a pull down on ADC data pin<br>0 = disabled<br>1 = enabled  |
|   | 6   | AIFADCL_SRC     | 0                        | Selects Left channel ADC output.<br>0 = ADC Left channel<br>1 = ADC Right channel   |
|   | 5   | AIFADCR_SRC     | 1                        | Selects Right channel ADC output.<br>0 = ADC Left channel<br>1 = ADC Right channel  |
|   | 4   | AIFADC_TDM_CHAN | 0                        | ADCDAT TDM Channel Select<br>0 = ADCDAT outputs data on slot 0<br>1 = ADCDAT outputs data on slot 1   |
|   | 3   | AIFADC_TDM      | 0                        | ADC TDM Enable<br>0 = Normal ADCDAT operation<br>1 = TDM enabled on ADCDAT  |
| R115 (73h)<br>Audio Interface DAC Control | 7   | AIFDAC_PD       | 0                        | Enables a pull down on DAC data pin<br>0 = disabled<br>1 = enabled  |
|   | 6   | DACL_SRC        | 0                        | Selects Left channel DAC input.<br>0 = DAC Left channel<br>1 = DAC Right channel  |
|   | 5   | DACR_SRC        | 1                        | Selects Right channel DAC input.<br>0 = DAC Left channel<br>1 = DAC Right channel   |
|   | 4   | AIFDAC_TDM_CHAN | 0                        | DACDAT TDM Channel Select<br>0 = DACDAT outputs data on slot 0<br>1 = DACDAT outputs data on slot 1   |
|   | 3   | AIFDAC_TDM      | 0                        | DAC TDM Enable<br>0 = Normal DACDAT operation<br>1 = TDM enabled on DACDAT  |

Table 46 Selecting the Audio Data Format

In Left Justified mode, the MSB is available on the first rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

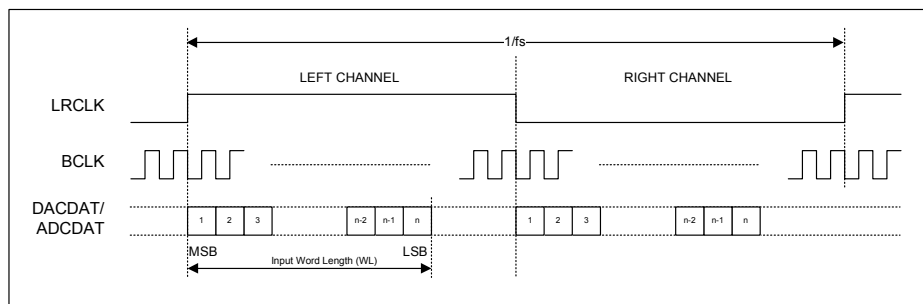


Figure 50 Left Justified Audio Interface (assuming n-bit word length)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.

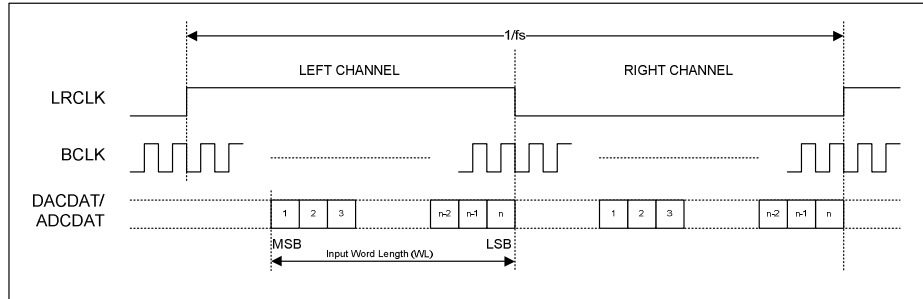


Figure 51 Right Justified Audio Interface (assuming n-bit word length)

In I2S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

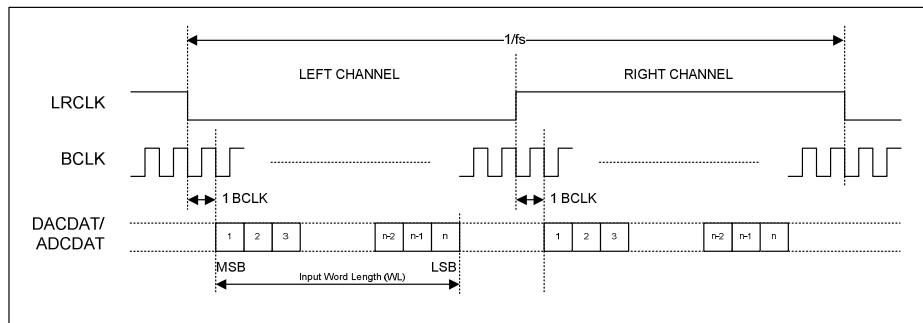


Figure 52 I2S Audio Interface (assuming n-bit word length)

In DSP/PCM mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by AIF\_LRCLK\_INV) following a rising edge of LRCLK. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

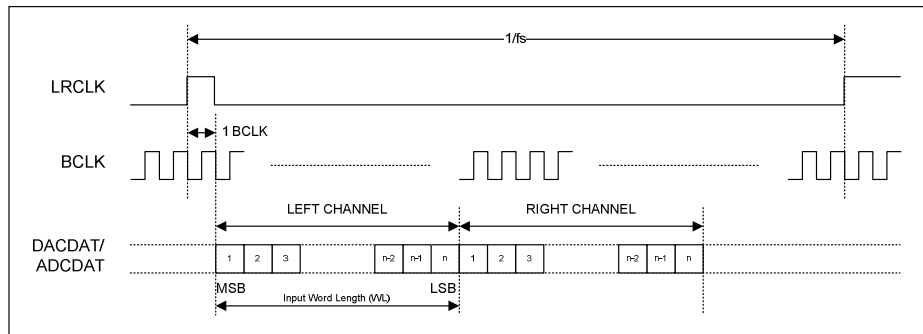


Figure 53 DSP/PCM Mode Audio Interface (mode A, AIF\_LRCLK\_INV=0)

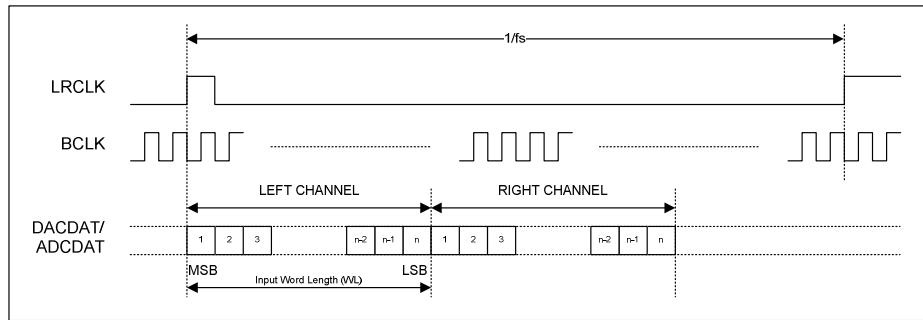


Figure 54 DSP/PCM Mode Audio Interface (mode B, AIF\_LRCLK\_INV=1)

### 13.10.2 AUDIO INTERFACE TDM MODE

The digital audio interface on WM8350 has the facility of tri-stating the ADCDAT pin to allow multiple data sources to operate on the same bus. Time division multiplexing (TDM) is also supported, allowing audio output data to be transferred simultaneously from two different sources.

TDM mode is enabled for the ADC and DAC by register bits AIFADC\_TDM and AIFDAC\_TDM respectively. TDM slot selection for the WM8350 is set for the ADC and DAC by register bits AIFADC\_TDM\_CHAN and AIFDAC\_TDM\_CHAN respectively, as defined in Table 46. When not actively transmitting data, the ADCDAT pin will be tristated in TDM mode, to allow other devices to transmit data.

### 13.10.3 TDM DATA FORMATS

All selectable data formats support TDM. The allocation of time slots is controlled by register bits AIFADC\_TDM\_CHAN and AIFDAC\_TDM\_CHAN. Two possible slots (SLOT0 and SLOT1) are available for the ADC and for the DAC.

Timing signals for the various interface formats in TDM mode are shown below for the ADC. Similar slot allocation will exist for the DAC.

**Left Justified Mode:** SLOT0 and SLOT1 are defined as shown below. The number of BCLK cycles from the start of SLOT0 to the start of SLOT1 is determined by the selected word length of the interface of the WM8350.

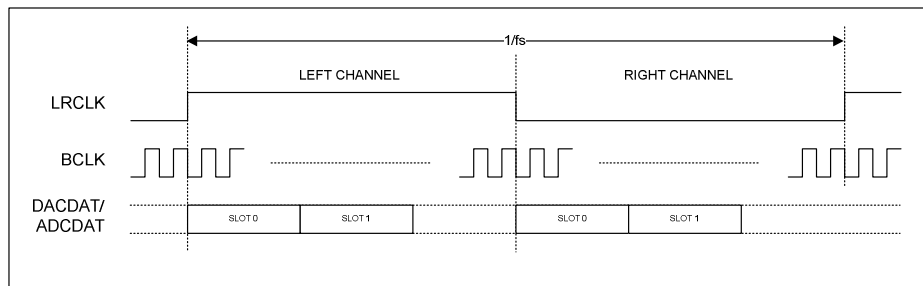


Figure 55 Left Justified Mode with TDM

**Right Justified Mode:** SLOT0 and SLOT1 are defined as shown below. The number of BCLK cycles from the end of SLOT1 to the end of SLOT0 is determined by the selected word length of the interface of the WM8350.

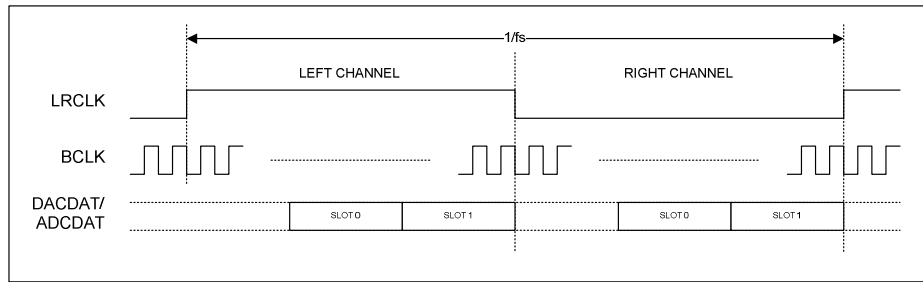


Figure 56 Right Justified Mode with TDM

**I2S Mode:** SLOT0 and SLOT1 are defined as shown below. The number of BCLK cycles from the start of SLOT0 to the start of SLOT1 is determined by the selected word length of the interface of the WM8350.

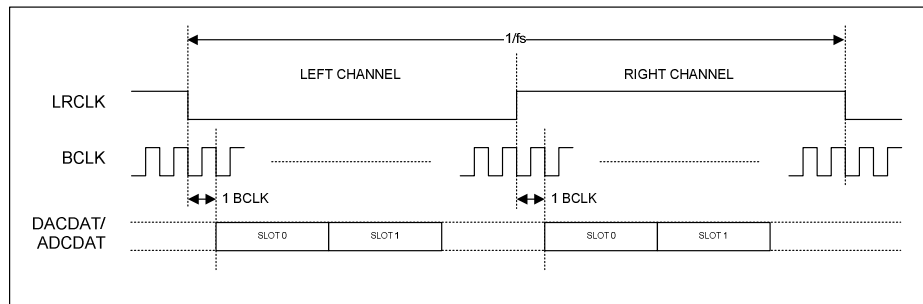


Figure 57 I2S Mode with TDM

**DSP/PCM Mode A, Master Mode:** SLOT0 and SLOT1 are defined as shown below. The number of BCLK cycles from the start of SLOT0 (left) to the start of SLOT1 (left) is determined by the selected word length of the interface of the WM8350.

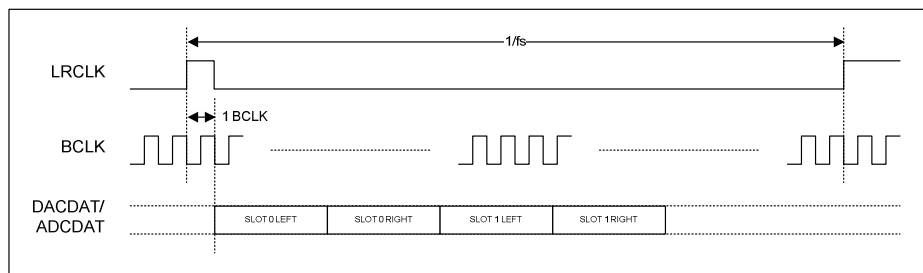


Figure 58 DSP/PCM Mode A, Master Mode with TDM

**DSP/PCM Mode B, Master Mode:** SLOT0 and SLOT1 are defined as shown below. The number of BCLK cycles from the start of SLOT0 (left) to the start of SLOT1 (left) is determined by the selected word length of the interface of the WM8350.

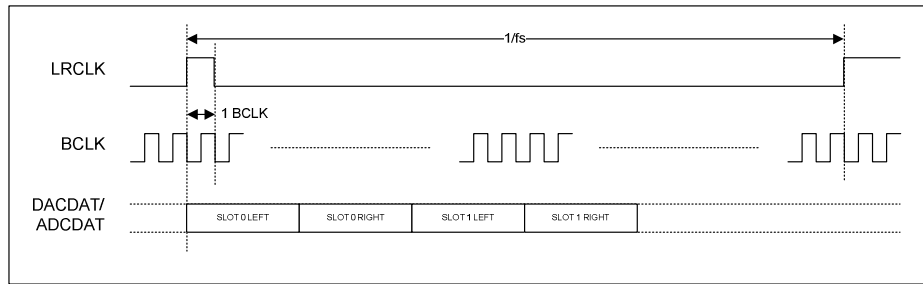


Figure 59 DSP/PCM Mode B, Master Mode, with TDM

**DSP/PCM Mode A, Slave Mode:** SLOT0 and SLOT1 are defined as shown below. The number of BCLK cycles from the start of SLOT0 (left) to the start of SLOT1 (left) is determined by the selected word length of the interface of the WM8350.

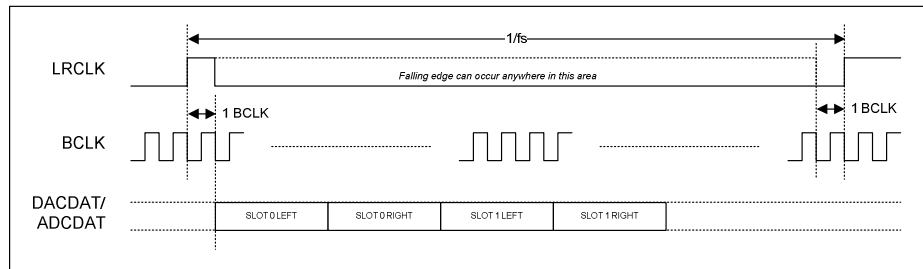


Figure 60 DSP/PCM Mode A, Slave Mode with TDM

**DSP/PCM Mode B, Slave Mode:** SLOT0 and SLOT1 are defined as shown below. The number of BCLK cycles from the start of SLOT0 (left) to the start of SLOT1 (left) is determined by the selected word length of the interface of the WM8350.

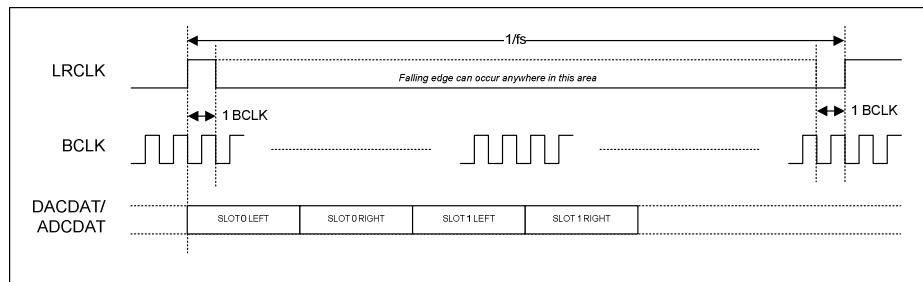


Figure 61 DSP/PCM Mode B, Slave Mode, with TDM

**13.10.4 LOOPBACK**

When the loopback feature is enabled, the audio ADC’s digital output data is looped back to the audio DAC and converted back into an analogue signal. This is often useful for test and evaluation purposes.

| ADDRESS                   | BIT | LABEL    | DEFAULT | DESCRIPTION   |
|---------------------------|-----|----------|---------|---|
| R113 (71h)<br>ADC Control | 0   | LOOPBACK | 0       | Digital Loopback Function<br>0 = No loopback.<br>1 = Loopback enabled, ADC data output is fed directly into DAC data input. |

Table 47 Enabling loopback



## 13.11 COMPANDING

The WM8350 supports A-law and  $\mu$ -law companding on both transmit (ADC) and receive (DAC) sides. Companding can be enabled on the DAC or ADC audio interfaces by writing the appropriate value to the DAC\_COMP or ADC\_COMP register bits respectively.

| REGISTER ADDRESS                 | BIT | LABEL        | DEFAULT | DESCRIPTION  |
|----------------------------------|-----|--------------|---------|--|
| R113 (71h)<br>Companding Control | 4   | ADC_COMPMODE | 0       | ADC Companding mode select:<br>0 = $\mu$ -law<br>1 = A-law<br>(Note: Setting ADC_COMPMODE=1 selects 8-bit mode when DAC_COMP=0 and ADC_COMP=0) |
|                                  | 5   | ADC_COMP     | 0       | ADC Companding enable<br>0 = disabled<br>1 = enabled   |
|                                  | 6   | DAC_COMPMODE | 0       | DAC Companding mode select:<br>0 = $\mu$ -law<br>1 = A-law<br>(Note: Setting DAC_COMPMODE=1 selects 8-bit mode when DAC_COMP=0 and ADC_COMP=0) |
|                                  | 7   | DAC_COMP     | 0       | DAC Companding enable<br>0 = disabled<br>1 = enabled   |

**Table 49 Companding Control**

Companding involves using a piecewise linear approximation of the following equations (as set out by ITU-T G.711 standard) for data compression:

$\mu$ -law (where  $\mu=255$  for the U.S. and Japan):

$$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu) \quad -1 \leq x \leq 1$$

law (where  $A=87.6$  for Europe):

$$F(x) = A|x| / (1 + \ln A) \quad \text{for } x \leq 1/A$$

$$F(x) = (1 + \ln A|x|) / (1 + \ln A) \quad \text{for } 1/A \leq x \leq 1$$

The companded data is also inverted as recommended by the G.711 standard (all 8 bits are inverted for  $\mu$ -law, all even data bits are inverted for A-law). The data will be transmitted as the first 8 MSBs of data.

Companding converts 13 bits ( $\mu$ -law) or 12 bits (A-law) to 8 bits using non-linear quantization. This provides greater precision for low amplitude signals than for high amplitude signals, resulting in a greater usable dynamic range than 8 bit linear quantization. The companded signal is an 8-bit word comprising sign (1 bit), exponent (3 bits) and mantissa (4-bits).

8-bit mode is selected whenever DAC\_COMP=1 or ADC\_COMP=1. The use of 8-bit data allows samples to be passed using as few as 8 BCLK cycles per LRCLK frame. When using DSP mode B, 8-bit data words may be transferred consecutively every 8 BCLK cycles.

8-bit mode (without Companding) may be enabled by setting DAC\_COMPMODE=1 or ADC\_COMPMODE=1 when DAC\_COMP=0 and ADC\_COMP=0.

| BIT7 | BIT[6:4] | BIT[3:0] |
|------|----------|----------|
| SIGN | EXPONENT | MANTISSA |

**Table 50 8-bit Companded Word Composition**

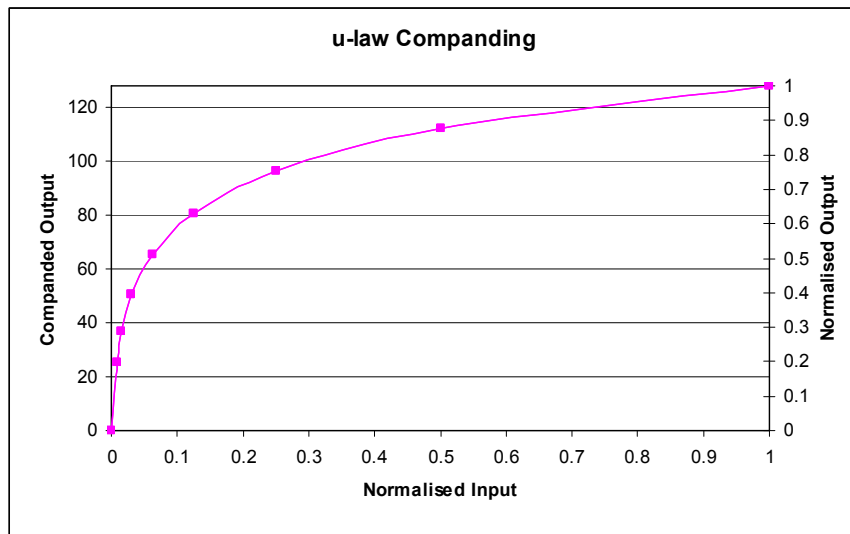


Figure 39  $\mu$ -Law Comanding

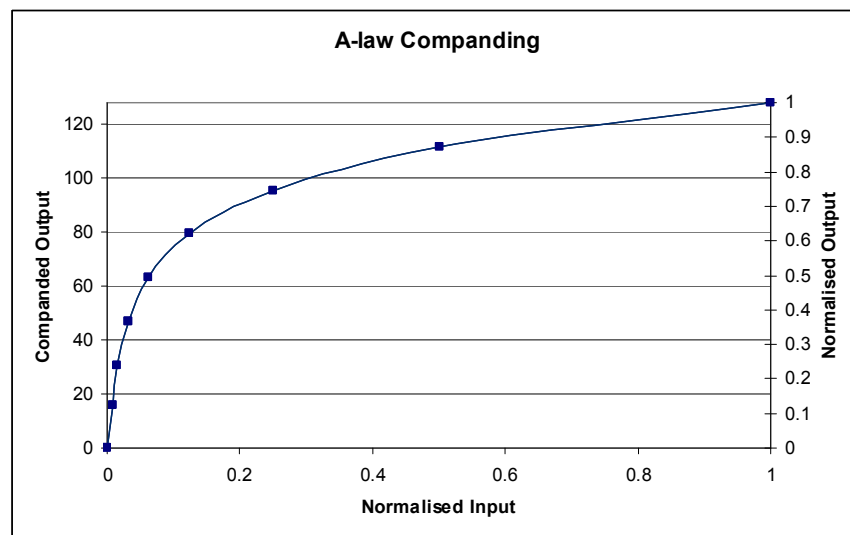


Figure 40 A-Law Comanding

## 13.12 ADDITIONAL CODEC FUNCTIONS

### 13.12.1 HEADPHONE JACK DETECT

The IN2L and IN2R pins can be selected as headphone jack detect inputs, to enable automatic control of the analogue outputs when a headphone is plugged into a jack socket.

Jack Detection on the IN2L or IN2R pins is enabled by register bits JDL\_ENA or JDR\_ENA respectively. When Jack Detection is enabled, the associated second level interrupts CODEC\_JCK\_DET\_L\_EINT and CODEC\_JCK\_DET\_R\_EINT indicate the status of the jack socket. See Section 13.12.7 for further details.

The Headphone Jack Detect function requires the internal slow clock to be enabled - see Section 12.3.6.

| REGISTER ADDRESS         | BIT | LABEL   | DEFAULT | DESCRIPTION  |
|--------------------------|-----|---------|---------|--|
| R77 (4Dh)<br>Jack Detect | 15  | JDL_ENA | 0       | Jack Detect Enable for inputs connected to IN2L<br>0 = disabled<br>1 = enabled |
|                          | 14  | JDR_ENA | 0       | Jack Detect Enable for input connected to IN2R<br>0 = disabled<br>1 = enabled  |

**Table 48 Headphone Jack Detect**

### 13.12.2 MICROPHONE DETECTION

The WM8350 can detect when a microphone has been plugged in, and/or when the microphone is short-circuited. It detects these events by comparing the current drawn from the MICBIAS pin against two thresholds. The thresholds for plug-in detection and short-circuit detection are programmable.

A MICBIAS current above the MCDTHR threshold level is used to indicate that a microphone is plugged in, and is associated with the CODEC\_MICD\_EINT interrupt. If the bias current exceeds the MCDSCTHR limit, this indicates a microphone short-circuit condition, and the WM8350 raises a CODEC\_MICSCD\_EINT interrupt. See Section 13.12.7 for further details. Note that the MICBIAS current thresholds are subject to a wide tolerance - up to +/-50% of the specified value.

Microphone detection requires the internal slow clock to be enabled - see Section 12.3.6.

| ADDRESS  | BIT | LABEL          | DEFAULT | DESCRIPTION   |
|--|-----|----------------|---------|---|
| R8 (08h)<br>Power Mgmt 1   | 8   | MIC_DET_ENA    | 0       | Enable MIC detect:<br>0 = disabled<br>1 = enabled   |
| R74 (4Ah)<br>Mic Bias<br>Control   | 7   | MIC_DET_ENA    | 0       | 1 = enabled   |
|  | 4:2 | MCDTHR [2:0]   | 000     | Threshold for bias current detection<br>000 = 160µA<br>001 = 330µA<br>010 = 500µA<br>011 = 680µA<br>100 = 850µA<br>101 = 1000µA<br>110 = 1200µA<br>111 = 1400µA<br>These threshold currents scale proportionally with AVDD. The values given are for AVDD=3.3V. |
|  | 1:0 | MCDSCTHR [1:0] | 00      | Threshold for microphone short-circuit detection<br>00 = 400µA<br>01 = 900µA<br>10 = 1350µA<br>11 = 1800µA<br>These threshold currents scale proportionally with AVDD. The values given are for AVDD=3.3V.  |
| <b>Note:</b> MIC_DET_ENA can be accessed through R8 or through R74. Reading from or writing to either register location has the same effect. |     |                |         |   |

**Table 49 Controlling Microphone Bias Current Detection**

### 13.12.3 MID-RAIL REFERENCE (VMID)

VMID provides a potential mid-way between AVDD and GND, used in many parts of the audio CODEC. It is generated from AVDD using on-chip potential dividers. Different resistor values can be selected for this purpose. A medium resistance should be used when the CODEC is active. A high resistance option provides a more power-efficient way to maintain the VMID voltage when the CODEC is in “Standby” (i.e. inactive but ready to start immediately, without needing to wait for the VMID capacitor to be charged). For startup and shutdown the VMID generator provides soft VMID ramping to reduce pops and clicks. The speed of this ramp is selectable using the anti-pop controls and can be tuned to the application.

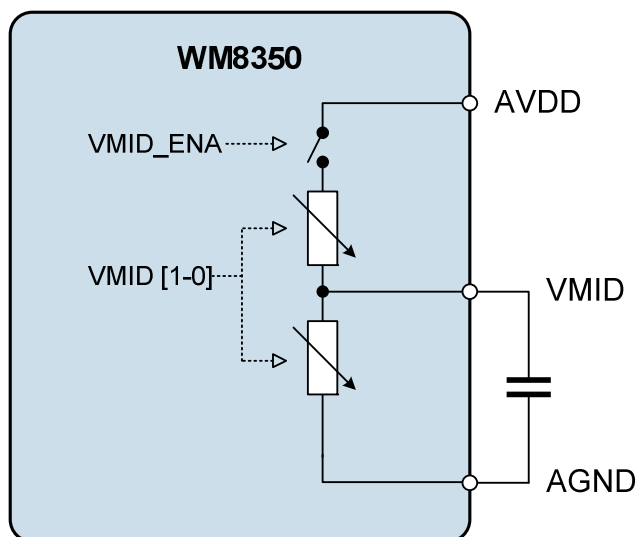


Figure 62 Generating the Mid-rail Reference

| ADDRESS                           | BIT | LABEL        | DEFAULT     | DESCRIPTION   |
|-----------------------------------|-----|--------------|-------------|---|
| R8 (08h)<br>Power<br>Management 1 | 2   | VMID_EN<br>A | 0           | Enables VMID resistor string<br>0 = disabled<br>1 = enabled   |
|                                   | 1:0 | VMID [1:0]   | 00<br>(off) | Resistor selection for VMID potential divider<br>00 = off<br>01 = Vmid comes from 300kΩ R-string<br>10 = Vmid comes from 50kΩ R-string<br>11 = Vmid comes from 5kΩ R-string |

Table 50 Controlling the Mid-rail Reference

## 13.12.4 ANTI-POP CONTROL

| ADDRESS                          | BIT | LABEL             | DEFAULT | DESCRIPTION   |
|----------------------------------|-----|-------------------|---------|---|
| R78 (4Eh)<br>Anti pop<br>control | 9:8 | ANTI_POP [1:0]    | 00      | Reduces pop when VMID is enabled by setting the speed of the S-ramp for VMID.<br>00 = no S-ramp (will pop)<br>01 = fastest S-curve<br>10 = medium S-curve<br>11 = slowest S-curve |
|                                  | 7:6 | DIS_OP_LN4 [1:0]  | 00      | Sets the Discharge rate for OUT4<br>00 = discharge path OFF<br>01 = fastest discharge<br>10 = medium discharge<br>11 = slowest discharge  |
|                                  | 5:4 | DIS_OP_LN3 [1:0]  | 00      | Sets the Discharge rate for OUT3<br>00 = discharge path OFF<br>01 = fastest discharge<br>10 = medium discharge<br>11 = slowest discharge  |
|                                  | 3:2 | DIS_OP_OUT2 [1:0] | 00      | Sets the discharge rate for OUT2L and OUT2R<br>00 = discharge path OFF<br>01 = fastest discharge<br>10 = medium discharge<br>11 = slowest discharge                               |
|                                  | 1:0 | DIS_OP_OUT1 [1:0] | 00      | Sets the discharge rate for OUT1L and OUT1R<br>00 = discharge path OFF<br>01 = fastest discharge<br>10 = medium discharge<br>11 = slowest discharge                               |

Table 51 Control Registers for Anti-pop

### 13.12.5 UNUSED ANALOGUE INPUTS/OUTPUTS

Whenever an analogue input/output is disabled, it remains connected to AVDD/2 through a resistor. This helps to prevent pop noise when the output is re-enabled. The resistance between the voltage buffer and the output pins can be controlled using the VROI control bits. The default impedance is low, so that any capacitors on the outputs can charge up quickly at start-up. If high impedance is desired for disabled outputs, VROI can then be set to 1, increasing the resistance to about 30k $\Omega$ .

There are individual VROI bits for each output or output pair. This allows matching of the rise times of the outputs if they are driving different capacitors. Using the small resistance with a capacitor for headphone outputs (typically 220uF) and the larger resistance with a line load capacitance (10uF for example); will allow both sets of outputs to power up in around the same time, around 200ms.

| REGISTER ADDRESS               | BIT | LABEL     | DEFAULT | DESCRIPTION   |
|--------------------------------|-----|-----------|---------|---|
| R8 (08h)<br>Power Mgmt<br>1    | 13  | VBUF_ENA  | 0       | Forces ON the tie-off amplifiers<br>0 = disabled<br>1 = enabled                                   |
| R76 (4Ch)<br>Output<br>Control | 8   | OUT1_VROI | 0       | VREF (AVDD/2) to OUT1L/OUT1R<br>resistance<br>0 = approx 500 $\Omega$<br>1 = approx 30 k $\Omega$ |
|                                | 9   | OUT2_VROI | 0       | VREF (AVDD/2) to OUT2L/OUT2R<br>resistance<br>0 = approx 500 $\Omega$<br>1 = approx 30 k $\Omega$ |
|                                | 10  | OUT3_VROI | 0       | VREF (AVDD/2) to OUT3 resistance<br>0 = approx 500 $\Omega$<br>1 = approx 30 k $\Omega$           |
|                                | 11  | OUT4_VROI | 0       | VREF (AVDD/2) to OUT4 resistance<br>0 = approx 500 $\Omega$<br>1 = approx 30 k $\Omega$           |

**Table 52 Disabled Outputs to VREF Resistance**

A dedicated buffer is available for tying off unused analogue I/O pins as shown below. This buffer can be enabled using the VBUF\_ENA register bit.

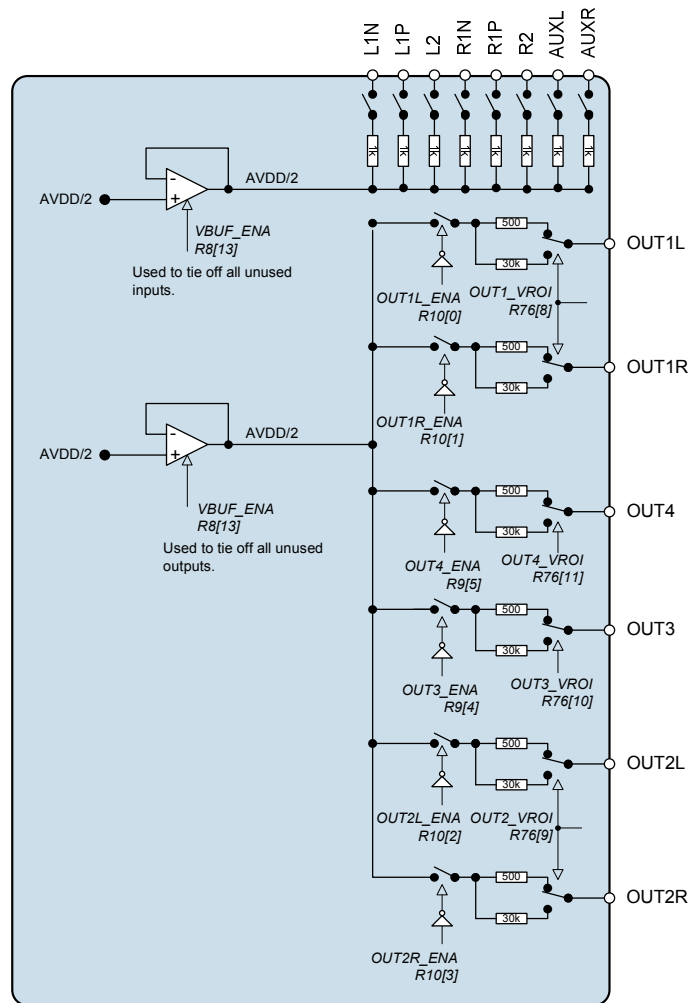


Figure 63 Unused Input/Output Pin Tie-off Buffers

| OUT1R/L_ENA/<br>OUT2R/L_ENA<br>OUT3/4_ENA | VROI | OUTPUT CONFIGURATION                     |
|---|------|--|
| 0   | 0    | 500Ω tie-off to AVDD/2                   |
| 0   | 1    | 30kΩ tie-off to AVDD/2                   |
| 1   | X    | Output enabled (DC level = AVDD/2)       |
| 1   | X    | Output enabled (DC level = 1.5 x AVDD/2) |

Table 53 Unused Output Pin Tie-off Options



### 13.12.6 ZERO CROSS TIMEOUT

A zero-cross timeout function is also provided so that if zero cross is enabled on the input or output PGAs the gain will automatically update after a timeout period if a zero cross has not occurred.

The zero-cross timeout function requires the internal slow clock to be enabled - see Section 12.3.6.

### 13.12.7 INTERRUPTS AND FAULT PROTECTION

The CODEC has its own first-level interrupt, CODEC\_INT (see Section 24). This comprises four second-level interrupts which indicate Jack detect and Microphone current conditions. These interrupts can be individually masked by setting the applicable mask bit(s) as described in Table 54.

| ADDRESS   | BIT  | LABEL                                    | DESCRIPTION  |
|---|------|--|--|
| R31 (1Fh)<br>Comparator<br>Interrupt<br>Status      | 11   | CODEC_JCK_DET_L_EINT                     | Left channel Jack detection interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.  |
|   | 10   | CODEC_JCK_DET_R_EINT                     | Right channel Jack detection interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 9    | CODEC_MICSCD_EINT                        | Mic short-circuit detect interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 8    | CODEC_MICD_EINT                          | Mic detect interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.   |
| R39 (27h)<br>Comparator<br>Interrupt<br>Status Mask | 11:8 | "IM_" + name of respective<br>bit in R31 | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br>Each bit in R39 enables or masks the<br>corresponding bit in R31. The default<br>value for these bits is 0 (unmasked). |

**Table 54** CODEC Interrupts

## 14 POWER MANAGEMENT SUBSYSTEM

### 14.1 GENERAL DESCRIPTION

The WM8350 provides 6 DC-DC Converters and 4 LDO Regulators which each deliver high efficiency across a wide range of line and load conditions. These power management components are designed to support application processors and associated peripherals. They are also suitable for providing power to the analogue and digital functions of the on-board CODEC and GPIO features. The output voltage of each of the converters and regulators is programmable in software through control registers.

The WM8350 has a number of operating states which are either selected by software control or are selected autonomously according to the available power supply conditions. A low power active 'Hibernate' state is provided, with programmable characteristics. The 'Backup' and 'Zero' states are selected autonomously when the available supply voltages do not permit full operation of the WM8350.

Four configuration modes are provided, selected by hardware control. Development Mode gives complete control over the configuration and start-up behaviour of the WM8350. Three different Custom Modes each have a defined set of configuration parameters, which determine the start-up timing and output voltage of each of the DC-DC Converters and LDO Regulators. The configuration of each of the GPIO pins is also contained with the configuration modes definitions.

### 14.2 POWER MANAGEMENT OPERATING STATES

The WM8350 autonomously controls the power-up and power-down sequencing for itself and for other connected devices. It also selects the most appropriate power source available at any given time (see Section 17). The stable states of the WM8350 are:

**ACTIVE** - All WM8350 functions can be used. The WM8350 enters the ACTIVE state after a valid start-up event (see Section 14.3.1), provided that no fault condition occurred during start-up.

**HIBERNATE** - This is an alternative active state with programmable characteristics, allowing an optional low power system condition. The internally generated supply voltages can be individually enabled or disabled as desired. The WM8350 enters the HIBERNATE state from ACTIVE by setting the HIBERNATE register bit or when commanded via a GPIO pin configured as a HIBERNATE alternate function.

**OFF** - All DC-DC converters and regulators LDO2, LDO3 and LDO4 are disabled. LDO1 may remain active (See Section 14.7.4). The VRTC regulator remains active and powers the always-on functions (such as crystal oscillator and RTC.) Register settings are restored to default settings. Trickle charging for the main battery is enabled by default. The WM8350 enters the OFF state from ACTIVE if a shutdown event occurs (see Section 14.3.3), or if the power source falls below the shutdown threshold (see Section 18). The WM8350 enters the OFF state from BACKUP if a power source greater than the UVLO threshold becomes available.

**BACKUP** - The crystal oscillator and RTC are enabled, powered from the backup power (VRTC) supply. All other functions are disabled. The WM8350 enters the BACKUP state from OFF if the power source falls below the UVLO threshold (see Section 18), and provided that backup power (VRTC) is available (i.e. LINE falls below the UVLO level but VRTC remains above the Power-On Reset threshold).

**ZERO** - All functions are disabled and all data in registers is lost. The WM8350 goes into this state when no power source is available and VRTC falls below the Power-On Reset threshold.

The Active state can only be entered via the **PRE-ACTIVE** state. In Development Mode, the Pre-Active state is the state in which the WM8350 start-up parameters may be defined, prior to the start-up sequence being triggered. The **ACTIVE** state is only entered on completion of the start-up sequence.

The WM8350 operating states and valid transitions are illustrated in Figure 64.

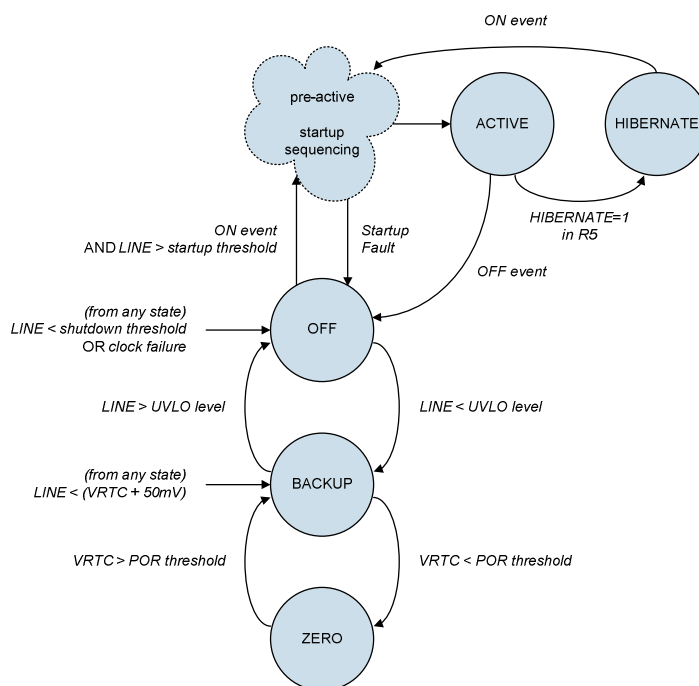


Figure 64 WM8350 Operating State Diagram

14.2.1 HIBERNATE STATE SELECTION

The WM8350 moves from the ACTIVE to the HIBERNATE state when the HIBERNATE register bit is set. It can also move to hibernate using the Hibernate Edge or the Hibernate Level function from the GPIOs.

It returns to the ACTIVE state when the Hibernate Level GPIO function is reset and the HIBERNATE bit is set to 0. It can also return to ACTIVE via the Hibernate Edge function or when a wake-up event (see Section 14.3.1) occurs.

If a fault condition occurs in the HIBERNATE state, the WM8350 moves to the OFF state.

| ADDRESS                         | BIT | LABEL     | DEFAULT | DESCRIPTION   |
|---------------------------------|-----|-----------|---------|---|
| R5 (05h)<br>System<br>Hibernate | 15  | HIBERNATE | 0       | Determines what state the chip should operate in.<br>0 = Active state<br>1 = Hibernate state<br>The register bit defaults to 0 when a reset happens |

Table 55 Invoking HIBERNATE State

The behaviour of the WM8350 in the HIBERNATE state is programmable in terms of supply voltage generation, interrupts and resets. Fast battery charging is disabled in the HIBERNATE state, but trickle charging is possible.

## 14.3 POWER SEQUENCING AND CONTROL

### 14.3.1 STARTUP

The WM8350 moves from OFF or HIBERNATE states to the ACTIVE state when a startup event occurs. Startup events include:

- A trigger signal on the ON pin lasting more than 40ms. The active polarity of this input is set by the register field ON\_POL.
- A trigger signal on a GPIO pin configured as /WAKEUP lasting more than 40ms. The active polarity of this input is set by GPn\_CFG for the applicable GPIO pin (see Section 20).
- A trigger signal on a GPIO pin configured as PWR\_ON input lasting more than 40ms. The active polarity of this input is set by GPn\_CFG for the applicable GPIO pin (see Section 20).
- Programmed ALARM from RTC module, if enabled (see Section 22).
- Wall adaptor plug-in (WALL\_FB rises above 4.0V).
- USB plug-in (USB pin rises above 4.0V).

The start-up events are only valid provided also that the available supply voltage, sensed on the LINE pin, is greater than the start-up threshold set by PCCMP\_ON\_THR, as defined in Section 18.

Start-Up by Wall adaptor plug-in occurs when the Wall Adapter feedback pin detects a voltage greater than 4.0V. See Section 17.1 for a description of the WALL\_FB pin function.

Start-Up by USB plug-in occurs when the USB voltage rises above the LINE voltage. If USB Suspend mode is invoked, then USB plug-in starts the WM8350 on battery power, if available. When USB Suspend Mode is not invoked, this start-up event will lead to starting the WM8350 on USB power, and USB 100mA trickle charging of the battery is enabled.

Note that applying a battery voltage is not a start-up event, i.e. connecting a battery pack does not start the WM8350. The WM8350 starts up on battery power if a startup event occurs and battery power is the only power source available, provided the battery voltage is above the startup threshold. (The start-up threshold is set by PCCMP\_ON\_THR, as defined in Section 18.

In the ACTIVE state, the host processor can read the Interrupt status fields in Register R31 in order to determine what action initiated the start-up. These fields indicate, for example, if the start-up was due to a reset caused by an error condition, or if the start-up was caused by a PWR\_ON input, or if the start-up was caused by an RTC alarm. The first-level interrupt WKUP\_INT is triggered whenever any of the second-level interrupt events described in Table 56 is set. See Section 24 for further details of Interrupt.

| ADDRESS   | BIT | LABEL                                 | DESCRIPTION  |
|---|-----|---------------------------------------|--|
| R31 (1Fh)<br>Comparator<br>Interrupt<br>Status      | 6   | WKUP_OFF_STATE_EINT                   | Indicates that the chip started from the OFF state.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 5   | WKUP_HIB_STATE_EINT                   | Indicated the chip started up from the hibernate state.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 4   | WKUP_CONV_FAULT_EINT                  | Indicates the wakeup was caused by a converter fault leading to the chip being reset.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                                 |
|   | 3   | WKUP_WDOG_RST_EINT                    | Indicates the wakeup was caused by a watchdog heartbeat being missed, and hence the chip being reset.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                 |
|   | 2   | WKUP_GP_PWR_ON_EINT                   | PWR_ON (Alternate GPIO function) pin has been pressed for longer than specified time.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                                 |
|   | 1   | WKUP_ONKEY_EINT                       | ON key has been pressed for longer than specified time.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 0   | WKUP_GP_WAKEUP_EINT                   | WAKEUP (Alternate GPIO function) pin has been pressed for longer than specified time.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                                 |
| R39 (27h)<br>Comparator<br>Interrupt<br>Status Mask | 6:0 | "IM_" + name of respective bit in R31 | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br>Each bit in R39 enables or masks the corresponding bit in R31. The default value for these bits is 0 (unmasked). |

Table 56 Wake-Up Interrupts

### 14.3.2 POWER-UP SEQUENCING

The WM8350 power supply blocks can be commanded to start up according to a defined sequence when the WM8350 is commanded into the ACTIVE state. This sequence comprises fourteen timeslots, where the enabling of each DC-DC converter, LDO voltage regulator and the current limit switch is associated with one timeslot. In order to minimise supply in-rush current at power-up time, the start-up of these power supply blocks should be staggered in time by the use of this feature.

The WM8350 proceeds from one time slot to the next after a delay of approximately 1.28ms, provided that all power supply blocks started up in the current time slot (if any) have reached 90% of their programmed output voltage. See Section 14.3.4 for details of the WM8350 behaviour if any power supply block fails to achieve 90% of its programmed output voltage.

### 14.3.3 SHUTDOWN

The WM8350 goes from ACTIVE or HIBERNATE to the OFF state when a shutdown event occurs. Shutdown events include:

- Software shutdown (setting CHIP\_ON = 0)
- A trigger signal on a GPIO pin configured as PWR\_OFF lasting more than 5ms. The active polarity of this input is set by GPn\_CFG for the applicable GPIO pin (see Section 20).
- A trigger signal on the ON pin lasting more than 10 seconds. The active polarity of this input is set by the register field ON\_POL. If required, the de-bounce time can be set to 5 seconds using the ON\_DEB\_T register bit.
- Watchdog time-out (see Section 23) after 7 previous faults.
- Fault conditions programmed to trigger a shutdown (see Section 18).
- Thermal shutdown (see Section 25)

As part of the start-up sequence, the CHIP\_ON bit is set to 1. The software shutdown is commanded by writing 0 to the CHIP\_ON register field as described in Table 57.

| ADDRESS                         | BIT | LABEL    | DEFAULT | DESCRIPTION  |
|---------------------------------|-----|----------|---------|--|
| R3 (03h)<br>System<br>Control 1 | 15  | CHIP_ON  | 0       | Indicates whether the system is on or off. Writing 0 to this bit powers down the whole chip. Registers which are affected by state machine reset will get reset. Once the system is turned OFF it can be restarted by any of the valid ON event. |
|                                 | 3   | ON_DEB_T | 0       | ON pin Shutdown function debounce time<br>0 = 10s<br>1 = 5s  |
|                                 | 1   | ON_POL   | 1       | ON pin polarity:<br>0 = Active high (ON)<br>1 = Active low (/ON)   |

**Table 57 Software Shutdown**

As part of the shutdown sequence, the WM8350 asserts the /RST and /MEMRST reset signals, resets its internal control registers, disables most of its functions, resets the CHIP\_ON bit to 0 and moves to the OFF state. (Note that /MEMRST is an optional output available on GPIO pins only.)

#### 14.3.4 POWER CYCLING

If an undervoltage fault or a limit switch overcurrent fault is detected (eg. during start-up, or when exiting the HIBERNATE state), the WM8350 will respond according to various configurable options. The Limit Switch and each of the DC Converters and LDO Regulators may be programmed to shutdown the system in the event of a fault condition. In these events (where a system shutdown is selected), the WM8350 will either shut down or will attempt to re-start, depending on the state of the POWERCYCLE register bit.

If POWERCYCLE = 0, then a fault condition will result in the shutdown of the WM8350, reverting to the OFF state. If POWERCYCLE = 1, then the WM8350 will make a maximum of 8 attempts to re-start. Each attempt will be scheduled at 200ms intervals. After 8 consecutive failed attempts, the WM8350 reverts to the OFF state and resets the power cycling counter. Any subsequent start-up event again has a maximum of 8 attempts to start up (provided that POWERCYCLE = 1).

| ADDRESS                       | BIT | LABEL          | DEFAULT | DESCRIPTION   |
|-------------------------------|-----|----------------|---------|---|
| R3 (03h)<br>System<br>Control | 13  | POWERCYCL<br>E | 0       | Action to take on a fault (if fault response is set to shutdown system):<br>0 = Shut down<br>1 = Shutdown everything then go through startup sequence. ie. Reboot the system. |

Table 58 Controlling Power Cycling

#### 14.3.5 REGISTER RESET

The control registers of the WM8350 are reset when it goes into the OFF state. Under default conditions, the control registers are also reset when exiting the HIBERNATE state; this behaviour is selectable using the REG\_RESET\_HIB\_MODE control bit.

In Development mode, the register reset in OFF can be disabled using the RECONFIG\_AT\_ON register field. See Section 14.4 for a definition of this field.

| ADDRESS                         | BIT | LABEL                      | DEFAULT | DESCRIPTION   |
|---------------------------------|-----|----------------------------|---------|---|
| R5 (05h)<br>System<br>Hibernate | 5   | REG_RESE<br>T_HIB_MOD<br>E | 0       | Action of the internal register reset signal when going from Hibernate to Active.<br>0 = Do a register reset when leaving the hibernate state.<br>1 = Do not do a register reset when leaving the hibernate state |

Table 59 Register Reset Control

### 14.3.6 RESET SIGNALS

The WM8350 provides an active-low reset output signal to the host processor on the open-drain /RST pin. The /RST pin is asserted low in the OFF state. The status of the /RST pin in HIBERNATE state is configurable using the RST\_HIB\_MODE bit.

In start-up, after all enabled power supplies reach 90% of their programmed output voltage, the /RST output is held low for a programmable duration set by RSTB\_TO. The /RST pin is then set high. The /RST output is set low during the shutdown sequence.

An additional GPIO output, /RST can be generated, with the same functionality as the /RST pin. A GPIO pin must be configured as /RST in order to output this signal (see Section 20).

The WM8350 can also generate a separate /MEMRST signal for other subsystems such as external memory. This allows resetting some subsystems in the HIBERNATE state, while not resetting others. The /MEMRST feature is provided via a GPIO pin (see Section 20). Note that /MEMRST is not a valid control signal during the start-up as the GPIO pins are not configured at this time. The MEM\_VALID field provides an indication of whether the contents of the external memory (under control of /MEMRST) are valid.

The /RST and /MEMRST signals can also be asserted under control of a manual reset input. A GPIO pin (see Section 20) must be configured as /MR to enable this feature. Note that the /MR input has no effect on the WM8350 circuits other than asserting /RST and /MEMRST.

| ADDRESS                         | BIT   | LABEL               | DEFAULT | DESCRIPTION  |
|---------------------------------|-------|---------------------|---------|--|
| R3 (03h)<br>System<br>Control 1 | 11:10 | RSTB_TO<br>[1:0]    | 11      | Time that the /RST pin and /MEMRST output is held low after the chip reaches the active state.<br>00 = 15ms<br>01 = 30ms<br>10 = 60ms<br>11 = 120ms  |
|                                 | 5     | MEM_VALID           | 0       | Indicates that the contents of external memory are still valid.<br>This bit is cleared on startup and whenever /MEMRST is asserted from the main state machine. The system software should set this bit once the external memory has been set up.<br>Controlled in hibernate mode by MEMRST_HIB_MODE<br>0 = External memory is not valid and needs restoring.<br>1 = External memory is valid. |
| R5 (05h)<br>System<br>Hibernate | 4     | RST_HIB_M<br>ODE    | 0       | /RST pin state in hibernate mode:<br>0 = Asserted (low)<br>1 = Not asserted (high)   |
|                                 | 2     | MEMRST_H<br>IB_MODE | 0       | /MEMRST (Alternative GPIO function) pin state in hibernate mode<br>0 = Asserted (low)<br>1 = Not asserted (high)   |

Table 60 Controlling Reset Signals



The WM8350 can be commanded to assert the /RST and /MEMRST signals by writing a logic '1' to the SYS\_RST register bit. In this case, the /RST and /MEMRST outputs are asserted low for the duration specified by RSTB\_TO.

Care must be taken if writing to this bit in 2-wire (I2C) Control Interface mode. The WM8350 will act upon the register write operation as soon as it has received the address and data fields; this may happen before the I2C Acknowledge has been clocked by the host processor. If the /RST signal causes the processor to reset before it has clocked the I2C Acknowledge, then the WM8350 will continue to assert the Acknowledge signal (ie. pull the SDA pin low) after the processor has completed its reset. On some processors, it may be necessary to toggle the SCLK pin in order to clear the Acknowledge signal and resume I2C communications.

| ADDRESS                         | BIT | LABEL   | DEFAULT | DESCRIPTION  |
|---------------------------------|-----|---------|---------|--|
| R3 (03h)<br>System<br>Control 1 | 14  | SYS_RST | 0       | Allows the processors to reboot itself<br>0 = Do nothing<br>1 = Perform a processor reset by asserting the /RST and /MEMRST (GPIO) pins for the programmed duration<br><i>Protected by security key.</i> |

**Table 61 Software Reset Command**

## 14.4 DEVELOPMENT MODE

The WM8350 can start in different modes depending on the state of the CONF1 and CONF0 pins. Development mode is selected by tying CONF1 and CONF0 to logic 0.

Development mode gives complete control over the configuration and startup behaviour of the WM8350 and allows overriding the default values of selected registers (listed in Table 64). It enables configuration of the WM8350 before startup. This is especially useful for evaluation and debugging.

In low-volume production, an external 'genie' (low-cost, small-size microcontroller) may be used to configure the WM8350 in Development mode. The 'genie' is used to write the required register values to generate the desired supplies and to configure the GPIO pins as required. These register write operations can be achieved via a secondary control interface, which is provided by redirecting the control interface to two GPIO pins as described below.

The configuration mode pins CONF1 and CONF0 should be tied to fixed logic levels. The start-up sequence that they control is initiated on every transition from the OFF to the ACTIVE state.

### 14.4.1 CONTROL INTERFACE REDIRECTION

In Development mode, the 2-wire control interface is initially redirected from the primary control interface (dedicated SDATA and SCLK pins, which require a DBVDD supply) to the secondary control interface (the GPIO10 and GPIO11 pins, which can run on an externally generated supply provided through the LINE pin). When using GPIO pins for the Control Interface, GPIO11 provides the SDATA functionality, and GPIO10 provides the SCLK functionality.

Use of the secondary interface makes it possible to configure the WM8350 before the DBVDD supply voltage becomes available (e.g. in the OFF and PRE-ACTIVE states). The control interface can be switched back to the primary interface at any time by writing to the USE\_DEV\_PINS bit. In a typical application, the primary control interface would be selected after the WM8350 is fully configured.

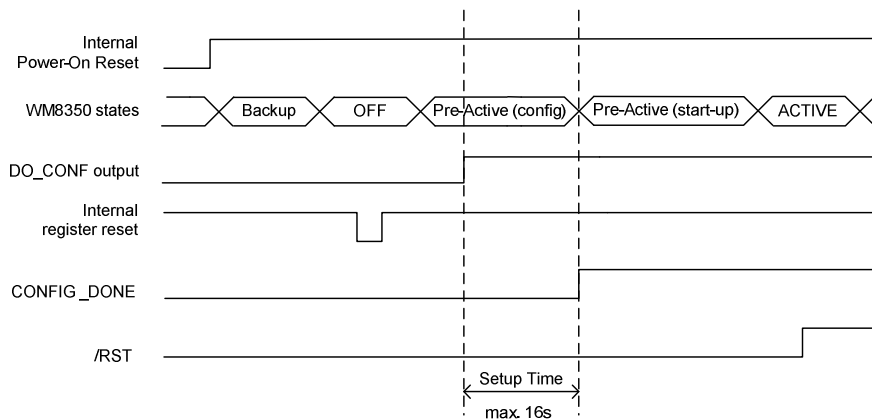
The device address for the secondary control interface is 0x34h, and cannot be changed. In development mode only, the primary interface address can be selected by writing to the DEV\_ADDR bits through the secondary interface. Note that this functionality is only available in Development mode.

| ADDRESS  | BIT   | LABEL          | DEFAULT | DESCRIPTION   |
|--|-------|----------------|---------|---|
| R6 (06h)<br>Interface<br>Control   | 15    | USE_DEV_PINS   | 1       | Selects which pins to use for the 2-wire control:<br>0 = Use 2-wire I/F pins as 2-wire interface<br>1 = Use GPIO 10 and 11 as 2-wire interface, e.g. to download settings from PIC.<br>Only applies when CONFIG pins[1:0] = 00. |
|  | 14:13 | DEV_ADDR [1:0] | 00      | Selects device address (only valid when CONF_STS = 00)<br>00 = 0x34<br>01 = 0x36<br>10 = 0x3C<br>11 = 0x3E  |
| <b>Note:</b> In custom modes (CONF[1:0]≠00), the secondary control interface is never used and the control bits described here have no effect. |       |                |         |   |

Table 62 Control Interface Switching in Development Mode

### 14.4.2 STARTING UP IN DEVELOPMENT MODE

In Development mode, the GPIO1 pin is configured as a DO\_CONF output (see Section 20), which is asserted high to indicate that the WM8350 is about to start up. This may be used to trigger the 'genie' to configure the WM8350 via the secondary control interface.



**Figure 65 Configuration Timing in Development Mode**

On completion of the register configuration, the power-up sequence is initiated by writing a logic 1 to the CONFIG\_DONE bit. If the CONFIG\_DONE bit is not set before the maximum set-up time has elapsed (see Figure 65), then the WM8350 will revert to the OFF state.

An alternative implementation is to start up the WM8350 by setting CONFIG\_DONE to '1' without first programming the converter/LDO settings. By this method, the rising edge of the /RST signal may be used to trigger the WM8350 configuration process after the device has entered the ACTIVE state. In this case, the DC-DC converters and LDOs turn on immediately when they are enabled (time slots are no longer relevant because the WM8350 is already in the ACTIVE state). To reduce in-rush current, any configuration sequence triggered by /RST should therefore include supply staggering in software (i.e. time delays between powering up individual supply domains).

Note that, whether using DO\_CONF or /RST to trigger configuration, the on-chip watchdog imposes a time-out for configuration; if the WM8350 watchdog is not serviced, it restarts the system. This can be prevented, if necessary, by disabling the watchdog.

By default, the DO\_CONF output will be set low when the WM8350 enters the OFF state and set high on every transition from OFF to ACTIVE, re-triggering the external 'genie'. Also, by default, the internal control registers will be reset when the WM8350 enters the OFF state. This behaviour can be changed using the RECONFIG\_AT\_ON register bit. If RECONFIG\_AT\_ON is set to 0, then the control registers will not be reset when going into the OFF state, and the DO\_CONF output will remain set high after the first powering up of the chip, regardless of subsequent state transitions.

De-selection of RECONFIG\_AT\_ON should be used with caution, as this can potentially lead to system failures in some applications. If RECONFIG\_AT\_ON is set to 0, and an OFF event occurs, then it is possible that control registers will not be set to the intended start-up values when the WM8350 subsequently returns to the ON state. The impact of this will depend upon the hardware and software of the particular target application, and is not necessarily a risk in every instance. Please contact Wolfson Applications support if further guidance is required on this topic.

Note that RECONFIG\_AT\_ON should never be set to 0 in Custom Modes 01, 10 or 11. Setting this bit to 0 may result in erroneous behaviour and deviation from the custom configuration settings. Under default settings, the control registers are always reset in the OFF state.

The register fields DO\_CONF and RECONFIG\_AT\_ON are defined in Table 63.

| ADDRESS                          | BIT | LABEL              | DEFAULT | DESCRIPTION  |
|----------------------------------|-----|--------------------|---------|--|
| R6 (06h)<br>Interface<br>Control | 12  | CONFIG_D<br>ONE    | 0       | Tells the system that the PIC micro has completed its programming.<br>0 = Programming still to be done<br>1 = Programming complete<br>Only applies when CONFIG pins[1:0] = 00.   |
|                                  | 11  | RECONFIG<br>_AT_ON | 1       | Selects whether to reset the registers in the OFF state and whether to reload the device configuration from the PIC when an ON event occurs.<br>0 = Do not reset registers in the OFF state. Do not load configuration data when an ON event occurs.<br>1 = Reset registers in the OFF state. Load configuration from the PIC when an ON event occurs.<br>Note that, in development mode, the device configuration from the PIC is always loaded when first powering up the chip.<br>This bit must always be set to default (1) in Custom Modes 01, 10 and 11. |

**Table 63 Start-Up Control in Development Mode**

Note: if the WM8350 enters the BACKUP state as a result of an undervoltage condition (see Section 18), then the control registers will be reset, but DO\_CONF will remain high. When the supply voltage rises and device comes out of BACKUP, the DO\_CONF output will still be high. If the DO\_CONF signal is used to trigger an external 'genie' device, then this may not work, as the DO\_CONF has remained high through the BACKUP state transition, and the WM8350 device will become locked in the PRE-ACTIVE state when an ON event occurs.

This problem may be avoided by ensuring that the 'genie' monitors the LINE voltage in order to recognise the undervoltage condition, and that it verifies the I2C Acknowledge signal on the secondary interface (GPIO10 and GPIO11) to determine whether it can execute its programming function.

### 14.4.3 CONFIGURING THE WM8350 IN DEVELOPMENT MODE

The WM8350 can be configured in Development mode by writing to control bits that determine its startup behaviour. The locations of these register bits are shown in Table 64 below. A typical configuration sequence would include writes to some or all of the registers listed. If none of the highlighted bits in any given register needs to be changed from its default, then no write to that register is recommended.

The configuration bits include:

- Duration control bits for the /RST reset signal (RSTB\_TO)
- GPIO pull-up / pull-down settings and debounce times (GPn\_PD, GPn\_PU, GPn\_DB and GP\_DBTIME)
- Alternate function and input/output selection for GPIO pins (GPn\_FN, GPn\_DIR and GPn\_CFG)
- Voltage settings for DC-DC converters and LDO regulators (DCn\_VSEL and LDO<sub>n</sub>\_VSEL)
- Time slots for automatic start of all DC-DC converters, all LDO regulators and the Current Limit Switch during startup (DCn\_ENSLOT, LDO<sub>n</sub>\_ENSLOT and LS\_ENSLOT). Note that supplies can be programmed to not start up automatically by setting the respective \_ENSLOT bits to 0000.

Typically, the final step in the sequence is a write to register R6, in order to:

- Select the WM8350 device address on the primary control interface, using the DEV\_ADDR bits.
- Allow the WM8350 to proceed to startup. This is achieved by setting the CONFIG\_DONE bit (R6 bit 12) to 1.
- Switch the control interface back to the primary interface (if desired), so that a host processor can communicate with the WM8350. This is achieved by setting USE\_DEV\_PINS (R6 bit 15) to 0.

| REGISTER   | 15      | 14           | 13               | 12                    | 11      | 10 | 9      | 8 | 7 | 6      | 5 | 4 | 3              | 2 | 1 | 0       |
|--|---------|--------------|------------------|-----------------------|---------|----|--------|---|---|--------|---|---|----------------|---|---|---------|
| Select /RST duration   |         |              |                  |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| R3 (03h)   |         |              |                  |                       | RSTB_TO |    |        |   |   |        |   |   |                |   |   |         |
| Unlock protected registers   |         |              |                  |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| R219 (DBh)   | 0013h   |              |                  |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| Alternate function and input/output selection for GPIO pins                          |         |              |                  |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| R140 (8Ch)   | GP3_FN  |              |                  | GP2_FN                |         |    | GP1_FN |   |   | GP0_FN |   |   |                |   |   |         |
| R141 (8Dh)   | GP7_FN  |              |                  | GP6_FN                |         |    | GP5_FN |   |   | GP4_FN |   |   |                |   |   |         |
| R142 (8Eh)   | GP11_FN |              |                  | GP10_FN               |         |    | GP9_FN |   |   | GP8_FN |   |   |                |   |   |         |
| R143 (8Fh)   |         |              |                  |                       |         |    |        |   |   |        |   |   |                |   |   | GP12_FN |
| R128 (80h)   |         |              |                  | GPn_DB (n = 0 to 12)  |         |    |        |   |   |        |   |   |                |   |   |         |
| R129 (81h)   |         |              |                  | GPn_PU (n = 0 to 12)  |         |    |        |   |   |        |   |   |                |   |   |         |
| R130 (82h)   |         |              |                  | GPn_PD (n = 0 to 12)  |         |    |        |   |   |        |   |   |                |   |   |         |
| R134 (86h)   |         |              |                  | GPn_DIR (n = 0 to 12) |         |    |        |   |   |        |   |   |                |   |   |         |
| R135 (87h)   |         |              |                  | GPn_CFG (n = 0 to 12) |         |    |        |   |   |        |   |   |                |   |   |         |
| Disable battery charger (only if battery type is not compatible with WM8350 charger) |         |              |                  |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| R168 (A8h)   | 0       |              |                  |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| Re-lock protected registers  |         |              |                  |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| R219 (DBh)   | FFFFh   |              |                  |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| Configure supply generation  |         |              |                  |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| R180 (B4h)   |         |              |                  |                       |         |    |        |   |   |        |   |   | DC1_VSEL[6:0]  |   |   |         |
| R181 (B5h)   |         |              | DC1_ENSLOT[3:0]  |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| R183 (B7h)   |         |              | DC2_ENSLOT[3:0]  |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| R186 (BAh)   |         |              |                  |                       |         |    |        |   |   |        |   |   | DC3_VSEL[6:0]  |   |   |         |
| R187 (BBh)   |         |              | DC3_ENSLOT 3:0]  |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| R189 (BDh)   |         |              |                  |                       |         |    |        |   |   |        |   |   | DC4_VSEL[6:0]  |   |   |         |
| R190 (BEh)   |         |              | DC4_ENSLOT[3:0]  |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| R193 (C1h)   |         |              | DC5_ENSLOT[3:0]  |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| R195 (C3h)   |         |              |                  |                       |         |    |        |   |   |        |   |   | DC6_VSEL[6:0]  |   |   |         |
| R196 (C4h)   |         |              | DC6_ENSLOT[3:0]  |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| R199 (C7h)   |         |              | LS_ENSLOT[3:0]   |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| R200 (C8h)   |         |              |                  |                       |         |    |        |   |   |        |   |   | LDO1_VSEL[4:0] |   |   |         |
| R201 (C9h)   |         |              | LDO1_ENSLOT[3:0] |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| R203 (CAh)   |         |              |                  |                       |         |    |        |   |   |        |   |   | LDO2_VSEL[4:0] |   |   |         |
| R204 (CBh)   |         |              | LDO2_ENSLOT[3:0] |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| R206 (CEh)   |         |              |                  |                       |         |    |        |   |   |        |   |   | LDO3_VSEL[4:0] |   |   |         |
| R207 (CFh)   |         |              | LDO3_ENSLOT[3:0] |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| R209 (D1h)   |         |              |                  |                       |         |    |        |   |   |        |   |   | LDO4_VSEL[4:0] |   |   |         |
| R210 (D2h)   |         |              | LDO4_ENSLOT[3:0] |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| Proceed to startup and hand over to host processor                                   |         |              |                  |                       |         |    |        |   |   |        |   |   |                |   |   |         |
| R6 (06h)   | 0       | DEV_ADD<br>R | 1                |                       |         |    |        |   |   |        |   |   |                |   |   |         |

**Table 64 Suggested Sequence of Register Writes for WM8350 Configuration in Development Mode**

Note that configuration only includes registers that are required for starting up correctly. All other register settings should be loaded after the WM8350 has started up.

Most of these control fields are described here within Section 14. See Section 11.6 for details of Register Locking. See Section 20 for details of the GPIO configuration fields. See Section 17.7 for details of the Battery Charger configuration.

When using the /RST signal to trigger configuration, writing to the \_ENSLOT and RSTB\_TO fields can be omitted (the reset and power-up sequence has already taken place, so the write would have no effect). However, additional writes to R13 or R176 should be added to enable the DC-DC converters and LDO regulators one by one.

## 14.5 CUSTOM MODES

The WM8350 provides three custom start-up modes. These are selected by setting the CONF1 and CONF0 pins = 01, 10 or 11. The custom mode start-up sequences define the following parameters:

- Polarity of the ON pin (Active low or high)
- Configuration of the USB power source
- Configuration of the Watchdog timer mode
- Configuration of the Control Interface mode
- Configuration of the 32kHz oscillator (enabled or disabled)
- Configuration of the real-time-clock (enabled or disabled)
- Configuration of LDO1
- Configuration of the voltage settings and start-up timeslots for DC-DC and LDO supplies
- Configuration of GPIO pins

In Development Mode, the RECONFIG\_AT\_ON register bit (see Section 14.4.2) may be used to control the device configuration behaviour. In Custom Modes 01, 10 or 11, the default setting (RECONFIG\_AT\_ON = 1) should always be used. Setting this bit to 0 may result in erroneous behaviour and deviation from the custom configuration settings.

The custom modes do not allow configuring the WM8350 in the OFF state. As a result, evaluation and debugging in custom modes is limited.

### 14.5.1 CONFIGURATION MODE 01

In Configuration Mode 01, the following general default settings apply:

| PARAMETER         | REGISTER SETTING                              | DESCRIPTION                                 |
|-------------------|---|---|
| ON polarity       | ON_POL = 1                                    | ON pin is Active Low                        |
| USB power source  | USB_SLV_500MA = 1                             | Selects 500mA limit in USB slave            |
| Watchdog timer    | WDOG_MODE [1:0] = 00                          | Watchdog is disabled                        |
| Control Interface | SPI_3WIRE = 0<br>SPI_4WIRE = 0<br>SPI_CFG = 0 | Control Interface is 2-wire mode            |
| 32kHz oscillator  | OSC32K_ENA = 1                                | 32kHz Oscillator is enabled                 |
| Real Time Clock   | RTC_TICK_ENA = 1<br>RTC_CLKSRC = 0            | Real Time Clock is enabled                  |
| LDO1              | LDO1_PIN_MODE = 0<br>LDO1_PIN_EN = 0          | LDO1 controlled as normal via register bits |

The default voltages and the power-up sequence for all DC-DCs and LDOs in Configuration Mode 01 are shown below in Table 65 and Figure 66.

The time delay between each time slot is approximately 1.28ms.

Note that the Limit Switch is not enabled automatically in Configuration Mode 01; as a result, the Limit Switch remains open when the WM8350 enters the ACTIVE state.

| SUPPLY | REGISTER SETTING                                     | DESCRIPTION             |
|--------|--|-------------------------|
| DCDC1  | DC1_ENSLOT [3:0] = 0100<br>DC1_VSEL [6:0] = 000_0110 | Fourth timeslot<br>1.0V |
| DCDC2  | DC2_ENSLOT [3:0] = 0000                              | Disabled                |
| DCDC3  | DC3_ENSLOT [3:0] = 0001<br>DC3_VSEL [6:0] = 010_0110 | First timeslot<br>1.8V  |
| DCDC4  | DC4_ENSLOT [3:0] = 0001<br>DC4_VSEL [6:0] = 101_0110 | First timeslot<br>3.0V  |
| DCDC5  | DC5_ENSLOT [3:0] = 0000                              | Disabled                |
| DCDC6  | DC6_ENSLOT [3:0] = 0100<br>DC6_VSEL [6:0] = 000_1010 | Fourth timeslot<br>1.1V |
| LDO1   | LDO1_ENSLOT [3:0] = 0011<br>LDO1_VSEL [4:0] = 0_0010 | Third timeslot<br>1.0V  |
| LDO2   | LDO2_ENSLOT [3:0] = 0010<br>LDO2_VSEL [4:0] = 1_1111 | Second timeslot<br>3.3V |
| LDO3   | LDO3_ENSLOT [3:0] = 0001<br>LDO3_VSEL [4:0] = 1_1100 | First timeslot<br>3.0V  |
| LDO4   | LDO4_ENSLOT [3:0] = 0010<br>LDO4_VSEL [4:0] = 0_0100 | Second timeslot<br>1.1V |

Table 65 Default Supply Voltages / Power-up Sequence for Configuration Mode 01

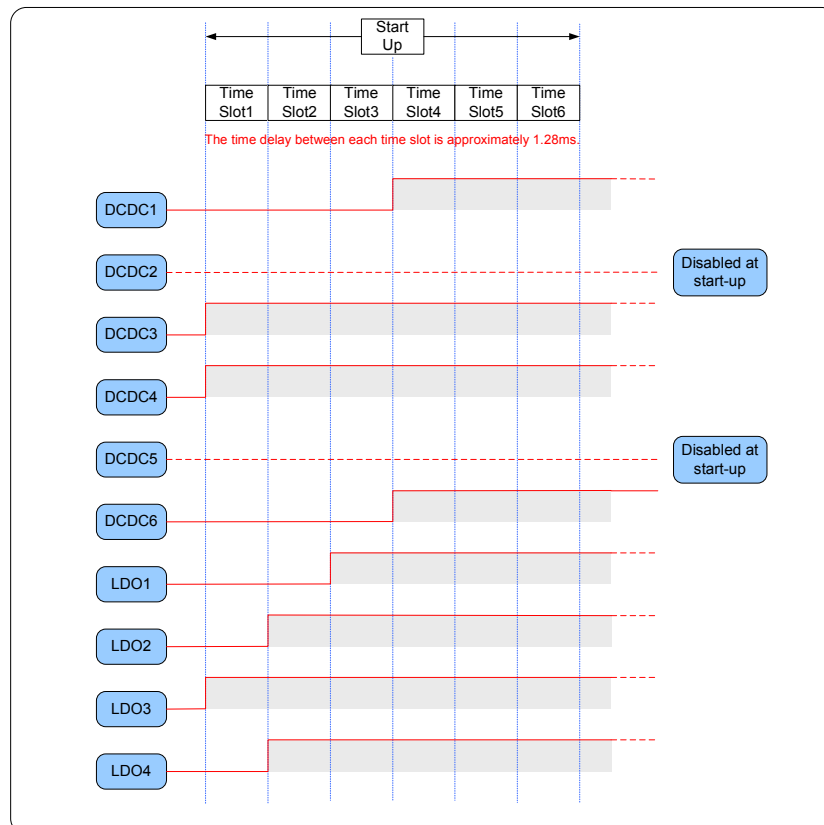


Figure 66 Power-up Sequence - Configuration Mode 01



The default GPIO settings for configuration mode 01 are shown below in Table 66.

| GPIO PIN | POWER DOMAIN | DEFAULT GPIO FUNCTION              | DEFAULT DIRECTION                                  | DEFAULT PULL-UP / PULL-DOWN           | DEFAULT DE-BOUNCE               |
|----------|--------------|------------------------------------|--|---------------------------------------|---------------------------------|
| GPIO0    | VRTC         | GP0_FN [3:0] = 0000<br>GPIO        | GP0_DIR = 1<br>GP0_CFG = 1<br>Input, Active High   | GP0_PD=0<br>GP0_PU=0<br>Normal Mode   | GP0_DB = 1<br>Debounce enabled  |
| GPIO1    | VRTC         | GP1_FN [3:0] = 0000<br>GPIO        | GP1_DIR = 1<br>GP1_CFG = 1<br>Input, Active High   | GP1_PD=0<br>GP1_PU=0<br>Normal Mode   | GP1_DB = 1<br>Debounce enabled  |
| GPIO2    | VRTC         | GP2_FN [3:0] = 0000<br>GPIO        | GP2_DIR = 1<br>GP2_CFG = 1<br>Input, Active High   | GP2_PD=0<br>GP2_PU=0<br>Normal Mode   | GP2_DB = 1<br>Debounce enabled  |
| GPIO3    | VRTC         | GP3_FN [3:0] = 0000<br>GPIO        | GP3_DIR = 1<br>GP3_CFG = 1<br>Input, Active High   | GP3_PD=0<br>GP3_PU=0<br>Normal Mode   | GP3_DB = 1<br>Debounce enabled  |
| GPIO4    | DBVDD        | GP4_FN [3:0] = 0000<br>GPIO        | GP4_DIR = 1<br>GP4_CFG = 1<br>Input, Active High   | GP4_PD=0<br>GP4_PU=0<br>Normal Mode   | GP4_DB = 1<br>Debounce enabled  |
| GPIO5    | DBVDD        | GP5_FN [3:0] = 0001<br>L_PWR1      | GP5_DIR = 1<br>GP5_CFG = 0<br>Input, Active Low    | GP5_PD=0<br>GP5_PU=0<br>Normal Mode   | GP5_DB = 1<br>Debounce enabled  |
| GPIO6    | DBVDD        | GP6_FN [3:0] = 0001<br>L_PWR2      | GP6_DIR = 1<br>GP6_CFG = 0<br>Input, Active Low    | GP6_PD=0<br>GP6_PU=0<br>Normal Mode   | GP6_DB = 1<br>Debounce enabled  |
| GPIO7    | DBVDD        | GP7_FN [3:0] = 0001<br>L_PWR3      | GP7_DIR = 1<br>GP7_CFG = 0<br>Input, Active Low    | GP7_PD=0<br>GP7_PU=0<br>Normal Mode   | GP7_DB = 1<br>Debounce enabled  |
| GPIO8    | DBVDD        | GP8_FN [3:0] = 0011<br>/BATT_FAULT | GP8_DIR = 0<br>GP8_CFG = 0<br>Output, CMOS         | GP8_PD=0<br>GP8_PU=0<br>Normal Mode   | GP8_DB = 1<br>Debounce enabled  |
| GPIO9    | DBVDD        | GP9_FN [3:0] = 0001<br>/VCC_FAULT  | GP9_DIR = 0<br>GP9_CFG = 0<br>Output, CMOS         | GP9_PD=0<br>GP9_PU=0<br>Normal Mode   | GP9_DB = 1<br>Debounce enabled  |
| GPIO10   | LINE         | GP10_FN [3:0] = 0000<br>GPIO       | GP10_DIR = 1<br>GP10_CFG = 1<br>Input, Active High | GP10_PD=0<br>GP10_PU=0<br>Normal Mode | GP10_DB = 1<br>Debounce enabled |
| GPIO11   | LINE         | GP11_FN [3:0] = 0000<br>GPIO       | GP11_DIR = 1<br>GP11_CFG = 1<br>Input, Active High | GP11_PD=0<br>GP11_PU=0<br>Normal Mode | GP11_DB = 1<br>Debounce enabled |
| GPIO12   | LINE         | GP12_FN [3:0] = 0011<br>LINE_SW    | GP12_DIR = 0<br>GP12_CFG = 0<br>Output, CMOS       | GP12_PD=0<br>GP12_PU=0<br>Normal Mode | GP12_DB = 1<br>Debounce enabled |

Table 66 Default GPIO Settings for Configuration Mode 01

### 14.5.2 CONFIGURATION MODE 10

In Configuration Mode 10, the following general default settings apply:

| PARAMETER         | REGISTER SETTING                              | DESCRIPTION   |
|-------------------|---|---|
| ON polarity       | ON_POL = 1                                    | ON pin is Active Low  |
| USB power source  | USB_SLV_500MA = 1                             | Selects 500mA limit in USB slave                                    |
| Watchdog timer    | WDOG_MODE [1:0] = 01                          | Watchdog set to Interrupt on Timeout                                |
| Control Interface | SPI_3WIRE = 0<br>SPI_4WIRE = 0<br>SPI_CFG = 0 | Control Interface is 2-wire mode                                    |
| 32kHz oscillator  | OSC32K_ENA = 1                                | 32kHz Oscillator is enabled   |
| Real Time Clock   | RTC_TICK_ENA = 1<br>RTC_CLKSRC = 0            | Real Time Clock is enabled, driven by the internal 32kHz oscillator |
| LDO1              | LDO1_PIN_MODE = 0<br>LDO1_PIN_EN = 0          | LDO1 controlled as normal via register bits                         |

The default voltages and the power-up sequence for all DC-DCs and LDOs in Configuration Mode 10 are shown below in Table 67 and Figure 67.

The time delay between each time slot is approximately 1.28ms.

Note that the Limit Switch is not enabled automatically in Configuration Mode 10; as a result, the Limit Switch remains open when the WM8350 enters the ACTIVE state.

| SUPPLY | REGISTER SETTING                                     | DESCRIPTION             |
|--------|--|-------------------------|
| DCDC1  | DC1_ENSLOT [3:0] = 0001<br>DC1_VSEL [6:0] = 001_0010 | First timeslot<br>1.3V  |
| DCDC2  | DC2_ENSLOT [3:0] = 0000                              | Disabled                |
| DCDC3  | DC3_ENSLOT [3:0] = 0000<br>DC3_VSEL [6:0] = 010_1110 | Disabled<br>2.0V        |
| DCDC4  | DC4_ENSLOT [3:0] = 0000<br>DC4_VSEL [6:0] = 000_1110 | Disabled<br>1.2V        |
| DCDC5  | DC5_ENSLOT [3:0] = 0000                              | Disabled                |
| DCDC6  | DC6_ENSLOT [3:0] = 0011<br>DC6_VSEL [6:0] = 010_0110 | Third timeslot<br>1.8V  |
| LDO1   | LDO1_ENSLOT [3:0] = 0000<br>LDO1_VSEL [4:0] = 1_1100 | Disabled<br>3.0V        |
| LDO2   | LDO2_ENSLOT [3:0] = 0010<br>LDO2_VSEL [4:0] = 1_0000 | Second timeslot<br>1.8V |
| LDO3   | LDO3_ENSLOT [3:0] = 0000<br>LDO3_VSEL [4:0] = 1_0101 | Disabled<br>2.3V        |
| LDO4   | LDO4_ENSLOT [3:0] = 0000<br>LDO4_VSEL [4:0] = 1_1010 | Disabled<br>2.8V        |

Table 67 Default Supply Voltages / Power-up Sequence for Configuration Mode 10

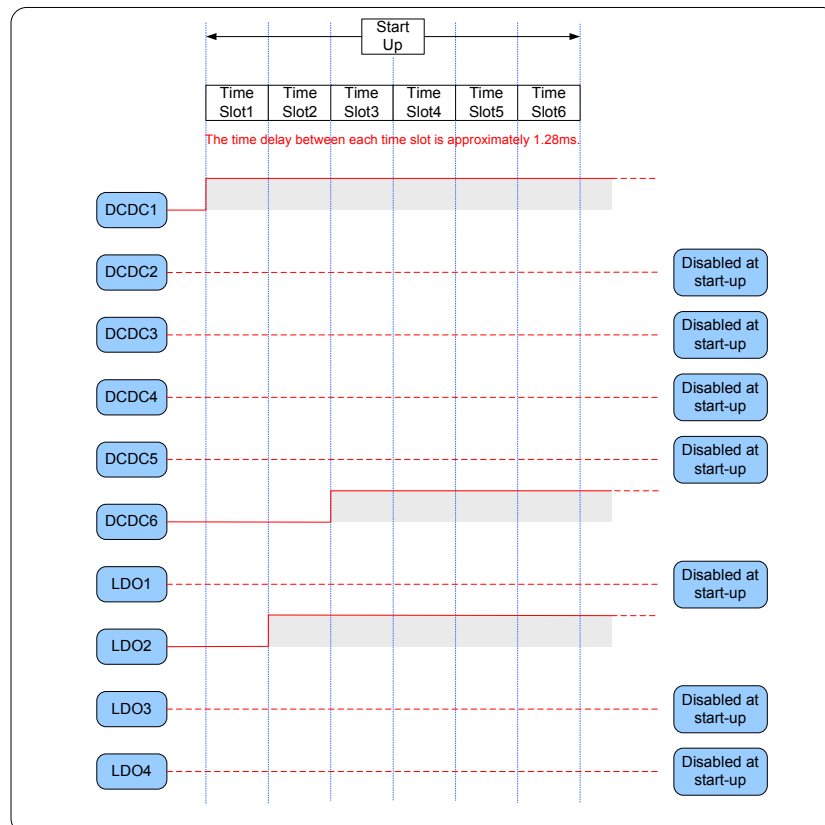


Figure 67 Power-up Sequence - Configuration Mode 10

The default GPIO settings for configuration mode 10 are shown below in Table 68.

| GPIO PIN | POWER DOMAIN | DEFAULT GPIO FUNCTION                  | DEFAULT DIRECTION                                  | DEFAULT PULL-UP / PULL-DOWN           | DEFAULT DE-BOUNCE               |
|----------|--------------|--|--|---------------------------------------|---------------------------------|
| GPIO0    | VRTC         | GP0_FN [3:0] = 0000<br>GPIO            | GP0_DIR = 0<br>GP0_CFG = 0<br>Output, CMOS         | GP0_PD=0<br>GP0_PU=0<br>Normal Mode   | GP0_DB = 1<br>Debounce enabled  |
| GPIO1    | VRTC         | GP1_FN [3:0] = 0001<br>PWR_ON          | GP1_DIR = 1<br>GP1_CFG = 1<br>Input, Active High   | GP1_PD=0<br>GP1_PU=0<br>Normal Mode   | GP1_DB = 1<br>Debounce enabled  |
| GPIO2    | VRTC         | GP2_FN [3:0] = 0011<br>32kHz           | GP2_DIR = 0<br>GP2_CFG = 1<br>Output, Open Drain   | GP2_PD=0<br>GP2_PU=0<br>Normal Mode   | GP2_DB = 1<br>Debounce enabled  |
| GPIO3    | VRTC         | GP3_FN [3:0] = 0001<br>PWR_ON          | GP3_DIR = 1<br>GP3_CFG = 0<br>Input, Active Low    | GP3_PD=0<br>GP3_PU=0<br>Normal Mode   | GP3_DB = 1<br>Debounce enabled  |
| GPIO4    | DBVDD        | GP4_FN [3:0] = 0011<br>HIBERNATE Level | GP4_DIR = 1<br>GP4_CFG = 1<br>Input, Active High   | GP4_PD=1<br>GP4_PU=0<br>Pull-down     | GP4_DB = 1<br>Debounce enabled  |
| GPIO5    | DBVDD        | GP5_FN [3:0] = 0000<br>GPIO            | GP5_DIR = 1<br>GP5_CFG = 1<br>Input, Active High   | GP5_PD=0<br>GP5_PU=0<br>Normal Mode   | GP5_DB = 1<br>Debounce enabled  |
| GPIO6    | DBVDD        | GP6_FN [3:0] = 0000<br>GPIO            | GP6_DIR = 1<br>GP6_CFG = 1<br>Input, Active High   | GP6_PD=0<br>GP6_PU=0<br>Normal Mode   | GP6_DB = 1<br>Debounce enabled  |
| GPIO7    | DBVDD        | GP7_FN [3:0] = 0000<br>GPIO            | GP7_DIR = 1<br>GP7_CFG = 1<br>Input, Active High   | GP7_PD=0<br>GP7_PU=0<br>Normal Mode   | GP7_DB = 1<br>Debounce enabled  |
| GPIO8    | DBVDD        | GP8_FN [3:0] = 0000<br>GPIO            | GP8_DIR = 1<br>GP8_CFG = 1<br>Input, Active High   | GP8_PD=1<br>GP8_PU=0<br>Pull-down     | GP8_DB = 1<br>Debounce enabled  |
| GPIO9    | DBVDD        | GP9_FN [3:0] = 0000<br>GPIO            | GP9_DIR = 0<br>GP9_CFG = 0<br>Output, CMOS         | GP9_PD=0<br>GP9_PU=0<br>Normal Mode   | GP9_DB = 1<br>Debounce enabled  |
| GPIO10   | LINE         | GP10_FN [3:0] = 0000<br>GPIO           | GP10_DIR = 0<br>GP10_CFG = 1<br>Output, Open Drain | GP10_PD=0<br>GP10_PU=0<br>Normal Mode | GP10_DB = 1<br>Debounce enabled |
| GPIO11   | LINE         | GP11_FN [3:0] = 0010<br>/WAKEUP        | GP11_DIR = 1<br>GP11_CFG = 1<br>(see note)         | GP11_PD=0<br>GP11_PU=0<br>Normal Mode | GP11_DB = 1<br>Debounce enabled |
| GPIO12   | LINE         | GP12_FN [3:0] = 0000<br>GPIO           | GP12_DIR = 0<br>GP12_CFG = 0<br>Output, CMOS       | GP12_PD=0<br>GP12_PU=0<br>Normal Mode | GP12_DB = 1<br>Debounce enabled |

**Note:** The alternate GPIO functions PWR\_ON and /WAKEUP are system wakeup events. The debounce time of these functions are determined by GP\_DBTIME[1:0] + 40ms

**Table 68 Default GPIO Settings for Configuration Mode 10**

Note that setting GP11\_CFG = 1 results in Active Low function for /WAKEUP. In most cases, setting GPn\_CFG = 1 results in Active High function, but /MR, /WAKEUP and /LDO\_ENA are exceptions to this. See Section 20.)

### 14.5.3 CONFIGURATION MODE 11

In Configuration Mode 11, the following general default settings apply:

| PARAMETER         | REGISTER SETTING                              | DESCRIPTION   |
|-------------------|---|---|
| ON polarity       | ON_POL = 1                                    | ON pin is Active Low  |
| USB power source  | USB_SLV_500MA = 1                             | Selects 500mA limit in USB slave                                    |
| Watchdog timer    | WDOG_MODE [1:0] = 00                          | Watchdog is disabled  |
| Control Interface | SPI_3WIRE = 0<br>SPI_4WIRE = 0<br>SPI_CFG = 0 | Control Interface is 2-wire mode                                    |
| 32kHz oscillator  | OSC32K_ENA = 1                                | 32kHz Oscillator is enabled   |
| Real Time Clock   | RTC_TICK_ENA = 1<br>RTC_CLKSRC = 0            | Real Time Clock is enabled, driven by the internal 32kHz oscillator |
| LDO1              | LDO1_PIN_MODE = 1<br>LDO1_PIN_EN = 0          | LDO1 enabled at all times   |

The default voltages and the power-up sequence for all DC-DCs and LDOs in configuration mode 11 are shown below in Table 69 and Figure 68.

The time delay between each time slot is approximately 1.28ms.

Note that the Limit Switch is not enabled automatically in Configuration Mode 11; as a result, the Limit Switch remains open when the WM8350 enters the ACTIVE state.

| SUPPLY | REGISTER SETTING                                     | DESCRIPTION              |
|--------|--|--------------------------|
| DCDC1  | DC1_ENSLOT [3:0] = 0010<br>DC1_VSEL [6:0] = 110_0010 | Second timeslot<br>3.3V  |
| DCDC2  | DC2_ENSLOT [3:0] = 0000                              | Disabled                 |
| DCDC3  | DC3_ENSLOT [3:0] = 0000<br>DC3_VSEL [6:0] = 000_1110 | Disabled<br>1.2V         |
| DCDC4  | DC4_ENSLOT [3:0] = 0011<br>DC4_VSEL [6:0] = 000_0110 | Third timeslot<br>1.0V   |
| DCDC5  | DC5_ENSLOT [3:0] = 0000                              | Disabled                 |
| DCDC6  | DC6_ENSLOT [3:0] = 0001<br>DC6_VSEL [6:0] = 010_0110 | First timeslot<br>1.8V   |
| LDO1   | LDO1_ENSLOT [3:0] = 0000<br>LDO1_VSEL [4:0] = 0_0010 | (See note below)<br>1.0V |
| LDO2   | LDO2_ENSLOT [3:0] = 0000<br>LDO2_VSEL [4:0] = 1_1010 | Disabled<br>2.8V         |
| LDO3   | LDO3_ENSLOT [3:0] = 0000<br>LDO3_VSEL [4:0] = 1_1111 | Disabled<br>3.3V         |
| LDO4   | LDO4_ENSLOT [3:0] = 0000<br>LDO4_VSEL [4:0] = 1_1111 | Disabled<br>3.3V         |

**Table 69 Default Supply Voltages / Power-up Sequence for Configuration Mode 11**

**Note:** In this Configuration Mode, LDO1 is enabled at all times. Therefore, the setting of LDO1\_ENSLOT has no effect.

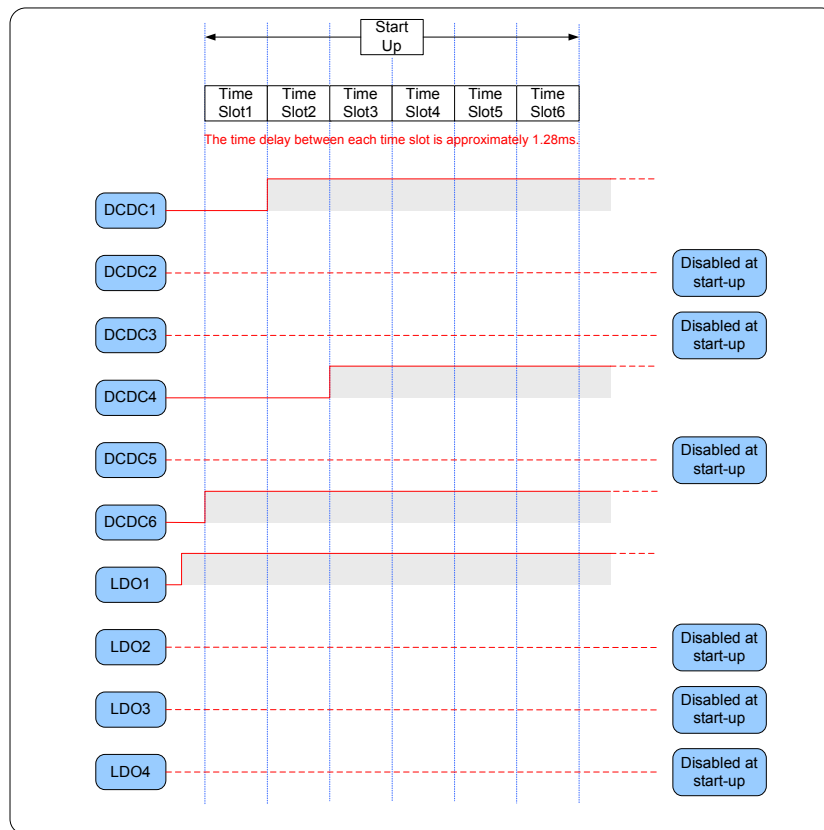


Figure 68 Power-up Sequence - Configuration Mode 11

The default GPIO settings for configuration mode 11 are shown below in Table 70.

| GPIO PIN | POWER DOMAIN | DEFAULT GPIO FUNCTION           | DEFAULT DIRECTION                                  | DEFAULT PULL-UP / PULL-DOWN           | DEFAULT DE-BOUNCE               |
|----------|--------------|---------------------------------|--|---------------------------------------|---------------------------------|
| GPIO0    | VRTC         | GP0_FN [3:0] = 0000<br>GPIO     | GP0_DIR = 1<br>GP0_CFG = 1<br>Input, Active High   | GP0_PD=0<br>GP0_PU=0<br>Normal Mode   | GP0_DB = 1<br>Debounce enabled  |
| GPIO1    | VRTC         | GP1_FN [3:0] = 0001<br>PWR_ON   | GP1_DIR = 1<br>GP1_CFG = 0<br>Input, Active Low    | GP1_PD=0<br>GP1_PU=0<br>Normal Mode   | GP1_DB = 1<br>Debounce enabled  |
| GPIO2    | VRTC         | GP2_FN [3:0] = 0011<br>32kHz    | GP2_DIR = 0<br>GP2_CFG = 1<br>Output, Open Drain   | GP2_PD=0<br>GP2_PU=0<br>Normal Mode   | GP2_DB = 1<br>Debounce enabled  |
| GPIO3    | VRTC         | GP3_FN [3:0] = 0000<br>GPIO     | GP3_DIR = 1<br>GP3_CFG = 1<br>Input, Active High   | GP3_PD=0<br>GP3_PU=0<br>Normal Mode   | GP3_DB = 1<br>Debounce enabled  |
| GPIO4    | DBVDD        | GP4_FN [3:0] = 0001<br>/MR      | GP4_DIR = 1<br>GP4_CFG = 1<br>(see note)           | GP4_PD=0<br>GP4_PU=1<br>Pull-up       | GP4_DB = 1<br>Debounce enabled  |
| GPIO5    | DBVDD        | GP5_FN [3:0] = 0000<br>GPIO     | GP5_DIR = 1<br>GP5_CFG = 1<br>Input, Active High   | GP5_PD=0<br>GP5_PU=0<br>Normal Mode   | GP5_DB = 1<br>Debounce enabled  |
| GPIO6    | DBVDD        | GP6_FN [3:0] = 0000<br>GPIO     | GP6_DIR = 1<br>GP6_CFG = 1<br>Input, Active High   | GP6_PD=0<br>GP6_PU=0<br>Normal Mode   | GP6_DB = 1<br>Debounce enabled  |
| GPIO7    | DBVDD        | GP7_FN [3:0] = 0000<br>GPIO     | GP7_DIR = 1<br>GP7_CFG = 1<br>Input, Active High   | GP7_PD=0<br>GP7_PU=0<br>Normal Mode   | GP7_DB = 1<br>Debounce enabled  |
| GPIO8    | DBVDD        | GP8_FN [3:0] = 0000<br>GPIO     | GP8_DIR = 1<br>GP8_CFG = 1<br>Input, Active High   | GP8_PD=0<br>GP8_PU=0<br>Normal Mode   | GP8_DB = 1<br>Debounce enabled  |
| GPIO9    | DBVDD        | GP9_FN [3:0] = 0000<br>GPIO     | GP9_DIR = 1<br>GP9_CFG = 1<br>Input, Active High   | GP9_PD=0<br>GP9_PU=0<br>Normal Mode   | GP9_DB = 1<br>Debounce enabled  |
| GPIO10   | LINE         | GP10_FN [3:0] = 0011<br>CH_IND  | GP10_DIR = 0<br>GP10_CFG = 1<br>Output, Open Drain | GP10_PD=0<br>GP10_PU=0<br>Normal Mode | GP10_DB = 1<br>Debounce enabled |
| GPIO11   | LINE         | GP11_FN [3:0] = 0010<br>/WAKEUP | GP11_DIR = 1<br>GP11_CFG = 1<br>(see note)         | GP11_PD=0<br>GP11_PU=0<br>Normal Mode | GP11_DB = 1<br>Debounce enabled |
| GPIO12   | LINE         | GP12_FN [3:0] = 0011<br>LINE_SW | GP12_DIR = 0<br>GP12_CFG = 0<br>Output, CMOS       | GP12_PD=0<br>GP12_PU=0<br>Normal Mode | GP12_DB = 1<br>Debounce enabled |

**Note:** The alternate GPIO functions PWR\_ON and /WAKEUP are system wakeup events. The debounce time of these functions are determined by GP\_DBTIME[1:0] + 40ms

**Table 70 Default GPIO Settings for Configuration Mode 11**

Note that setting GP4\_CFG = 1 results in Active Low function for /MR. Also, setting GP11\_CFG = 1 results in Active Low function for /WAKEUP. In most cases, setting GPn\_CFG = 1 results in Active High function, but /MR, /WAKEUP and /LDO\_ENA are exceptions to this. See Section 20.)

## 14.6 CONFIGURING THE DC-DC CONVERTERS

The configuration of the DC-DC converters is described in the following sections. Some of the control fields form part of the Custom Mode configuration settings and therefore will not require to be set in software in some applications.

### 14.6.1 DC-DC CONVERTER ENABLE

The DC-DC Converters can be enabled in software using the register fields defined in Table 71. All DC-DC converters include a soft-start feature that helps to reduce the inductor current at start up. In order to further reduce supply in-rush current, individual converters should be programmed to start in different time slots within the start-up sequence.

In the WM8350 ACTIVE state, the DC-DC Converters can be enabled in software using the DC<sub>n</sub>\_ENA bits. Setting these bits whilst in the Pre-Active state (see Figure 65) will not immediately enable the corresponding DC-DC converter; these bits will only become effective once the WM8350 has reached the ACTIVE state.

Each Converter may be programmed to switch on in a selected timeslot within the start-up sequence. The WM8350 will set the DC<sub>n</sub>\_ENA field for any DC-DC converter that is enabled during the start-up sequence. Note that setting the DC<sub>n</sub>\_ENSLOT fields in software is only relevant to the Development Mode, as these fields are assigned preset values in each of the Custom Modes.

Each Converter may be programmed to switch off in a selected timeslot within the shutdown sequence. If a Converter is not allocated to one of the 14 shutdown timeslots, it will be disabled when the WM8350 enters the OFF state.

| ADDRESS   | BIT             | LABEL                             | DEFAULT                            | DESCRIPTION  |
|---|-----------------|-----------------------------------|------------------------------------|--|
| R13 (0Dh) or<br>R176 (B0h)  | 0,1,2,3<br>,4,5 | DC <sub>n</sub> _ENA              | Dependant<br>on CONFIG<br>settings | DCDC <sub>n</sub> converter enable<br>0 = disabled<br>1 = enabled<br><br>Note: internal conditions may prevent<br>the converter from actually switching on<br>- see DCDC/LDO Status register for<br>actual converter status. |
| <b>Note:</b> These bits can be accessed through R13 or through R176. Reading from or writing to either register location has the same effect. |                 |                                   |                                    |  |
| R181 (B5h) for<br>DC-DC1<br><br>R184 (B8h) for<br>DC-DC2  | 13:10           | DC <sub>n</sub> _ENSLO<br>T [3:0] | Dependant<br>on CONFIG<br>settings | Time slot for DC-DC <sub>n</sub> start-up<br>0000 = Disabled (do not start up)<br>0001 = Start-up in time slot 1<br>... (total 14 slots available)<br>1110 = Start-up in time slot 14<br>1111 = Start up on entering ACTIVE  |
| R187 (BBh) for<br>DC-DC3<br><br>R190 (BEh) for<br>DC-DC4<br><br>R193 (C1h) for<br>DC-DC5<br><br>R196 (C4h) for<br>DC-DC6                      | 9:6             | DC <sub>n</sub> _SDSLO<br>T [3:0] | 0000                               | Time slot for DC-DC <sub>n</sub> shutdown.<br>0000 = Shut down on entering OFF<br>0001 = Shutdown in time slot 1<br>... (total 14 slots available)<br>1110 = Shutdown in time slot 14<br>1111 = Shut down on entering OFF    |
| <b>Note:</b> <i>n</i> is number between 1 and 6 that identifies the individual DC-DC converter  |                 |                                   |                                    |  |

**Table 71 Enabling and Disabling the DC-DC Converters**



### 14.6.2 CLOCKING

The DC-DC converters are controlled by an internally generated clock signal from the RC Oscillator with a constant frequency of around 2.0MHz for DC-DC 1, 3, 4 and 6, and a constant frequency of around 1.0MHz for DC-DC 2 and 5.

### 14.6.3 DC-DC BUCK (STEP-DOWN) CONVERTER CONTROL

DC-DC Converters 1, 3, 4 and 6 are buck converters which can be configured to operate in different operating modes using the register bits described in Table 72.

In Active mode, the DC-DC Converters operate to their highest level of performance. The DC-DC Converters will automatically select PWM or Pulse-Skipping operation according to the load condition. This enables the power efficiency to be maximised across a wide range of load conditions. It is possible to force the Converters to use the higher performance PWM mode; in this mode, pulse-skipping is disabled and the output voltage is regulated by switching at a constant frequency which improves the transient response at light loads.

In Standby/Hysteretic Mode, the DC-DC Converters disable some of the internal control circuitry in order to reduce power consumption. The load regulation may be degraded in this mode of operation. The efficiency data in Section 9.2.1 shows the conditions under which Standby Mode can offer better efficiency than Active Mode.

In LDO Mode, the DC-DC Converters are reconfigured as low power LDOs.

When  $DCn\_SLEEP = 0$ , the corresponding  $DCn\_ACTIVE$  register bit selects between Active and Standby/Hysteretic modes for the associated DC-DC converter.

The  $DCn\_SLEEP$  register bits control the selection of LDO Mode. Setting  $DCn\_SLEEP = 1$  selects LDO Mode. This bit takes precedence over the corresponding  $DCn\_ACTIVE$  bit.

| ADDRESS   | BIT | LABEL             | DEFAULT | DESCRIPTION   |
|---|-----|-------------------|---------|---|
| R177 (B1h)<br>DC-DC Active<br>Options   | 0   | DC1_ACTIVE        | 1       | DC-DC $n$ Active mode<br>0 = Select Standby mode<br>1 = Select Active mode      |
|   | 2   | DC3_ACTIVE        | 1       |   |
|   | 3   | DC4_ACTIVE        | 1       |   |
|   | 5   | DC6_ACTIVE        | 1       |   |
| R178 (B2h)<br>DC-DC Sleep<br>Options  | 0   | DC1_SLEEP         | 0       | DC-DC $n$ Sleep Mode<br>0 = Normal DC-DC operation<br>1 = Select LDO mode       |
|   | 2   | DC3_SLEEP         | 0       |   |
|   | 3   | DC4_SLEEP         | 0       |   |
|   | 5   | DC6_SLEEP         | 0       |   |
| <b>Note:</b> $n$ is either 1, 3, 4 or 6 and identifies the individual DC-DC converter |     |                   |         |   |
| R248 (F8h)<br>DCDC1 Test<br>Controls  | 4   | DC1_FORCE_<br>PWM | 0       | Force DC-DC1 PWM mode<br>0 = Normal DC-DC operation<br>1 = Force DC-DC PWM mode |
| R250 (FAh)<br>DCDC3 Test<br>Controls  | 4   | DC3_FORCE_<br>PWM | 0       | Force DC-DC3 PWM mode<br>0 = Normal DC-DC operation<br>1 = Force DC-DC PWM mode |
| R251 (FBh)<br>DCDC4 Test<br>Controls  | 4   | DC4_FORCE_<br>PWM | 0       | Force DC-DC4 PWM mode<br>0 = Normal DC-DC operation<br>1 = Force DC-DC PWM mode |
| R253 (FDh)<br>DCDC4 Test<br>Controls  | 4   | DC6_FORCE_<br>PWM | 0       | Force DC-DC6 PWM mode<br>0 = Normal DC-DC operation<br>1 = Force DC-DC PWM mode |

Table 72 Operating Mode Control for DC-DC Converters 1, 3, 4 and 6

DC-DC Converters 1, 3, 4 and 6 can also be controlled by the device HIBERNATE bit, or by hardware input signals L\_PWR1, L\_PWR2 and L\_PWR3. Several GPIO pins can be assigned as L\_PWR pins. Each converter can be assigned to one of these three signals, or else to the device HIBERNATE bit. The signals are active high and each converter's response to the selected signal is programmable as defined in Table 73.

Note that, when a GPIO pin is configured as a Hibernate input pin, and this input is asserted, then all DC-DC Converters will be placed in Hibernate mode.

In order to use GPIO pins as L\_PWR pins, they must be configured by setting the respective GPn\_FN, and GPn\_DIR bits to the appropriate value (see Section 20).

| ADDRESS   | BIT   | LABEL               | DEFAULT | DESCRIPTION  |
|---|-------|---------------------|---------|--|
| R182 (B6h) for DC-DC1   | 14:12 | DCn_HIB_M ODE [2:0] | 001     | DC-DCn Hibernate behaviour:<br>000 = Use current settings (no change)<br>001 = Select voltage image settings<br>010 = Force standby mode<br>011 = Force standby mode and voltage image settings<br>100 = Force LDO mode<br>101 = Force LDO mode and voltage image settings<br>110 = Reserved<br>111 = Disable output |
| R188 (BCh) for DC-DC3   |       |                     |         |  |
| R191 (BFh) for DC-DC4   |       |                     |         |  |
| R197 (C5h) for DC-DC6   |       |                     |         |  |
|   | 9:8   | DCn_HIB_T RIG [1:0] | 00      | DC-DCn Hibernate signal select<br>00 = HIBERNATE register bit<br>01 = L_PWR1<br>10 = L_PWR2<br>11 = L_PWR3<br>Note that Hibernate is also selected when a GPIO Hibernate input is asserted.  |
| <b>Note:</b> n is either 1, 3, 4 or 6 and identifies the individual DC-DC converter |       |                     |         |  |

**Table 73 Low-Power Mode Control for DC-DC Converters 1, 3, 4 and 6**

The default output voltage for DC-DC Converters 1, 3, 4 and 6 is set by writing to the  $DCn\_VSEL$  register bits. The 'image' voltage settings  $DCn\_VIMG$  are alternate values that may be invoked when the HIBERNATE software or hardware control is asserted as described above.

The DC-DC Converters 1, 3, 4 and 6 are dynamically programmable - the output voltage may be adjusted in software at any time. These Converters are buck (step-down) converters; their output voltage can therefore be lower than the input voltage, but cannot be higher.

| ADDRESS               | BIT | LABEL             | DEFAULT                      | DESCRIPTION  |
|-----------------------|-----|-------------------|------------------------------|--|
| R180 (B4h) for DC-DC1 | 6:0 | $DCn\_VSEL$ [6:0] | Dependant on CONFIG settings | DC-DC $n$ Converter output voltage settings in 25mV steps.<br>Maximum output = 3.4V.                                     |
| R186 (BAh) for DC-DC3 |     |                   |                              | 110 0110 = 3.4V  |
| R189 (BDh) for DC-DC4 |     |                   |                              | 110 0010 = 3.3V  |
| R195 (C3h) for DC-DC6 |     |                   |                              | 101 0110 = 3.0V<br>100 1110 = 2.8V<br>.....<br>010 0110 = 1.8V<br>000 1110 = 1.2V<br>000 0110 = 1.0V<br>000 0000 = 0.85V |
| R182 (B6h) for DC-DC1 | 6:0 | $DCn\_VIMG$ [6:0] | 000 0110                     | DC-DC $n$ Converter output image voltage settings in 25mv steps.<br>Maximum output = 3.4V.                               |
| R188 (BCh) for DC-DC3 |     |                   |                              | 110 0110 = 3.4V  |
| R191 (BFh) for DC-DC4 |     |                   |                              | 110 0010 = 3.3V  |
| R197 (C5h) for DC-DC6 |     |                   |                              | 101 0110 = 3.0V<br>100 1110 = 2.8V<br>.....<br>010 0110 = 1.8V<br>000 1110 = 1.2V<br>000 0110 = 1.0V<br>000 0000 = 0.85V |

**Note:**  $n$  is either 1, 3, 4 or 6 and identifies the individual DC-DC converter

**Table 74 Output Voltage Control for DC-DC Converters 1, 3, 4 and 6**

When the DC-DC Converters 1, 3, 4 and 6 are disabled, the output can be set to float or else the outputs can be actively discharged through internal resistors. This feature is controlled using the register bits described in Table 75.

| ADDRESS               | BIT | LABEL        | DEFAULT | DESCRIPTION   |
|-----------------------|-----|--------------|---------|---|
| R180 (B4h) for DC-DC1 | 10  | $DCn\_OPFLT$ | 0       | Enable discharge of DC-DC $n$ outputs when DC-DC $n$ is disabled<br>0 = Enabled - Output to be discharged<br>1 = Disabled - Output is left floating |
| R186 (BAh) for DC-DC3 |     |              |         |   |
| R189 (BDh) for DC-DC4 |     |              |         |   |
| R195 (C3h) for DC-DC6 |     |              |         |   |

**Note:**  $n$  is either 1, 3, 4 or 6 and identifies the individual DC-DC converter

**Table 75 Output Float Control for DC-DC Converters 1, 3, 4 and 6**

A summary of the Mode Control and Voltage Control for DC-DC Converter 1 is provided in Table 76. Note that “Hibernate” in Table 76 refers to a GPIO Hibernate input or to the applicable Hibernate signal selected by the DC1\_HIB\_TRIG field.

The equivalent logic applies for DC-DC 3, 4 and 6. Note that the DC-DC Converters must also be enabled as described in Table 71.

| HIBERNATE | DC1_HIB_MODE | DC1_SLEEP | DC1_ACTIVE | OPERATING MODE     | OUTPUT VOLTAGE |
|-----------|--------------|-----------|------------|--------------------|----------------|
| 0         | X            | 0         | 0          | Standby/Hysteretic | DC1_VSEL       |
| 0         | X            | 0         | 1          | Active             | DC1_VSEL       |
| 0         | X            | 1         | X          | LDO Mode           | DC1_VSEL       |
| 1         | 000          | 0         | 0          | Standby/Hysteretic | DC1_VSEL       |
|           |              | 0         | 1          | Active             | DC1_VSEL       |
|           |              | 1         | X          | LDO Mode           | DC1_VSEL       |
|           | 001          | 0         | 0          | Standby/Hysteretic | DC1_VIMG       |
|           |              | 0         | 1          | Active             | DC1_VIMG       |
|           |              | 1         | X          | LDO Mode           | DC1_VIMG       |
|           | 010          | X         | X          | Standby/Hysteretic | DC1_VSEL       |
|           | 011          | X         | X          | Standby/Hysteretic | DC1_VIMG       |
|           | 100          | X         | X          | LDO Mode           | DC1_VSEL       |
|           | 101          | X         | X          | LDO Mode           | DC1_VIMG       |
|           | 110          | X         | X          | Disabled           | N/A            |
|           | 111          | X         | X          | Disabled           | N/A            |

**Table 76 DC1 Converter Operating Mode Selection**

#### 14.6.4 DC-DC BOOST (STEP-UP) CONVERTER CONTROL

DC-DC Converters 2 and 5 are boost converters which can be configured to operate in different operating modes, using the register bits described in Table 77.

In Switch mode, the DC-DC Converter acts as a switch between VP2 and L2 or between VP5 and L5 for Converter 2 and 5 respectively. The switch is enabled (closed) by setting  $DCn\_ENA = 1$ . The switch is disabled (opened) by setting  $DCn\_ENA = 0$ . Note that the switch voltage source on VP2 or VP5 must be  $>1.2V$  to ensure reliable operation.

In Boost mode, the DC-DC Converters operate as step-up converters, employing current-mode architecture, capable of powering LED lights. The output voltage can be higher than the input voltage, but cannot be lower. Different configurations of voltage feedback are available in boost mode, to control the output voltage in different ways. The voltage feedback mode is selected by the  $DCn\_FBSRC$  register field.

When  $DCn\_FBSRC = 00$ , the converter's output voltage is set by two external resistors connected to FB2 or FB5. See Section 29 for Applications Information covering the selection of suitable components.

When  $DCn\_FBSRC = 01$ , the converter uses the ISINKA pin as feedback and adjusts its output voltage in order to achieve the required ISINKA current.

When  $DCn\_FBSRC = 10$ , the converter uses the ISINKB pin as feedback and adjusts its output voltage in order to achieve the required ISINKB current.

When  $DCn\_FBSRC = 11$ , the converter's output voltage is set by two internal resistors, resulting in a fixed 5V output, suitable for USB interfaces.

The current-controlled configurations using ISINKA or ISINKB are intended for controlling a string of serially-connected LEDs driven by one of the DC-DC boost converters. See Table 97 for a definition of the  $CSn\_ISEL$  register field which determines the required ISINKA or ISINKB current. In these modes, external resistors connected on the FB2 or FB5 pin determine the maximum output voltage. See Section 29 for Applications Information covering the selection of suitable components.

In all configurations, the input pins VP2 and VP5 must be externally wired to one of the supply rails, BATT or LINE. Using LINE has the advantage that the converters can operate when the battery is flat, defective or absent. Note that VP2 and VP5 should not be connected to the USB supply rail.

The DC<sub>n</sub>\_RMPH and DC<sub>n</sub>\_RMPL bits defined in Table 77 should be set according to the desired output voltage in order to optimise the transient response of the converter. Selecting a different value could result in sub-harmonic oscillation of the converter.

The DC<sub>n</sub>\_ILIM bits defined in Table 77 should be set according to the intended output load conditions.

| ADDRESS  | BIT | LABEL  | DEFAULT | DESCRIPTION  |
|--|-----|--|---------|--|
| R183 (B7h)<br>for DC-DC2   | 14  | DC <sub>n</sub> _MODE                          | 0       | DC-DC <sub>n</sub> Converter Mode<br>0 = boost mode<br>1 = switch mode   |
| R192 (C0h)<br>for DC-DC5   | 6   | DC <sub>n</sub> _ILIM                          | 0       | DC-DC <sub>n</sub> peak current limit select<br>0 = Higher peak current<br>1 = Lower peak current  |
|  | 4:3 | DC <sub>n</sub> _RMPH<br>DC <sub>n</sub> _RMPL | 01      | DC-DC <sub>n</sub> compensation ramp<br>{DC <sub>n</sub> _RMPH, DC <sub>n</sub> _RMPL}<br>00 = 20V < VOUT ≤ 30V<br>01 = 10V < VOUT ≤ 20V<br>10 = 5V < VOUT ≤ 10V<br>11 = VOUT ≤ 5V (will be chosen<br>automatically if DC <sub>n</sub> _FBSRC=11)  |
|  | 1:0 | DC <sub>n</sub> _FBSRC<br>[1:0]                | 00      | DC-DC <sub>n</sub> voltage feedback selection<br>00 = voltage feedback (using external<br>resistor divider on pin FB <sub>n</sub> )<br>01 = current sink ISINKA used as<br>feedback<br>10 = current sink ISINKB used as<br>feedback<br>11 = voltage feedback (using internal<br>resistor divider on pin USB) |
| <b>Note:</b> <i>n</i> is either 2 or 5 and identifies the individual DC-DC converter |     |  |         |  |

**Table 77 Operating Mode Control for DC-DC Converters 2 and 5**

DC-DC Converters 2 and 5 can also be controlled by the device HIBERNATE bit, or by hardware input signals L\_PWR1, L\_PWR2 and L\_PWR3. Several GPIO pins can be assigned as L\_PWR pins. Each converter can be assigned to one of these three signals, or else to the device HIBERNATE bit. The signals are active high and each converter's response to the selected signal is programmable as defined in Table 78.

Note that, when a GPIO pin is configured as a Hibernate input pin, and this input is asserted, then all DC-DC Converters will be placed in Hibernate mode.

In order to use GPIO pins as L\_PWR pins, they must be configured by setting the respective GP<sub>n</sub>\_FN, and GP<sub>n</sub>\_DIR bits to the appropriate value (see Section 20).

| ADDRESS  | BIT | LABEL                               | DEFAULT | DESCRIPTION   |
|--|-----|-------------------------------------|---------|---|
| R183 (B7h) for DC-DC2  | 12  | DC <sub>n</sub> _HIB_MO<br>DE       | 0       | DC-DC <sub>n</sub> Hibernate behaviour:<br>0 = Continue as in Active state<br>1 = Disable converter output  |
| R192 (C0h) for DC-DC5  | 9:8 | DC <sub>n</sub> _HIB_TRI<br>G [1:0] | 00      | DC-DC <sub>n</sub> Hibernate signal select<br>00 = HIBERNATE register bit<br>01 = L_PWR1<br>10 = L_PWR2<br>11 = L_PWR3<br>Note that Hibernate is also selected when a GPIO Hibernate input is asserted. |
| <b>Note:</b> <i>n</i> is either 2 or 5 and identifies the individual DC-DC converter |     |                                     |         |   |

Table 78 Hibernate Mode Control for DC-DC Converters 2 and 5

#### 14.6.5 INTERRUPTS AND FAULT PROTECTION

Each DC-DC Converter is monitored for voltage accuracy and fault conditions. An undervoltage condition is set if the voltage falls below 95% of the required level. The action taken in response to a fault condition can be set independently for each DC-DC Converter, as described in Table 79.

The DC<sub>n</sub>\_ERRACT fields configure the fault response to disable the respective converter or to shut down the entire system if desired. In addition, DC-DC Converter fault conditions also generate a second-level interrupt (see Section 24).

To prevent false alarms during short current surges, faults are only signalled if the fault condition persists. When a DC-DC Converter is started up, any initial fault condition is ignored until the Converter has been allowed time to settle. The time for which any fault condition is ignored is set by the PUTO register field, as described in Table 79.

| ADDRESS  | BIT   | LABEL                              | DEFAULT | DESCRIPTION  |
|--|-------|------------------------------------|---------|--|
| R181 (B5h) for DC-DC1  | 15:14 | DC <sub>n</sub> _ERRACT<br>T [1:0] | 00      | Action to take on DC-DC <sub>n</sub> fault (as well as generating an interrupt):<br>00 = ignore<br>01 = shut down converter<br>10 = shut down system<br>11 = reserved (shut down system) |
| R184 (B8h) for DC-DC2  |       |                                    |         |  |
| R187 (BBh) for DC-DC3  |       |                                    |         |  |
| R190 (BEh) for DC-DC4  |       |                                    |         |  |
| R193 (C1h) for DC-DC5  |       |                                    |         |  |
| R196 (C4h) for DC-DC6  |       |                                    |         |  |
| R177 (B1h) DCDC Active options   | 13:12 | PUTO [1:0]                         | 00      | Power up time out value for all converters<br>00 = 0.5ms<br>01 = 2ms<br>10 = 32ms<br>11 = 256ms  |
| <b>Note:</b> <i>n</i> is a number between 1 and 6 that identifies the individual DC-DC converter |       |                                    |         |  |

Table 79 Fault Responses for DC-DC Converters

The DC-DC Converters and the LDO Regulators have a first-level interrupt, UV\_INT (see Section 24). This comprises second-level interrupts from each of the DC-DC Converters and the LDO Regulators.

Each DC-DC Converter has a dedicated second-level interrupt which indicates an under-voltage condition. These can be masked by setting the applicable mask bit as defined in Table 80.

| ADDRESS   | BIT          | LABEL                                    | DESCRIPTION   |
|---|--------------|--|---|
| R28 (1Ch)<br>Under Voltage<br>Interrupt Status                                | 5            | UV_DC6_EINT                              | DCDC6 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 4            | UV_DC5_EINT                              | DCDC5 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 3            | UV_DC4_EINT                              | DCDC4 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 2            | UV_DC3_EINT                              | DCDC3 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 1            | UV_DC2_EINT                              | DCDC2 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 0            | UV_DC1_EINT                              | DCDC1 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
| R36 (24h)<br>Under Voltage<br>Interrupt Mask                                  | as in<br>R28 | "IM_" + name of respective<br>bit in R28 | Mask bits for DC-DC converter under-<br>voltage interrupts<br>Each of these bits masks the respective<br>bit in R28 when it is set to 1 (e.g.<br>UV_DC1_EINT in R28 does not trigger a<br>UV_INT interrupt when<br>IM_UV_DC1_EINT in R36 is set). |
| <b>Note:</b> there is no over-current fault condition for converters 2 and 5. |              |  |   |

**Table 80 DC-DC Converter Interrupts**

The status of the DC-DC Converters can be indicated and monitored externally via a GPIO pin configured as `/VCC_FAULT` (see Section 20). When a GPIO pin is configured as `/VCC_FAULT` output, a logic low level on this pin indicates that there is a fault condition on one of the LDO Regulators, DC-DC Converters, or the Current Limit switch.

The `/VCC_FAULT` output is configurable by the control fields in Register R215. The fields described in Table 81 determine which of the DC-DCs contribute to the `/VCC_FAULT` indication. An undervoltage or overvoltage condition on any unmasked DC-DC Converter will cause the `/VCC_FAULT` output to be set to logic low.

| ADDRESS                              | BIT | LABEL                  | DEFAULT | DESCRIPTION  |
|--------------------------------------|-----|------------------------|---------|--|
| R215 (D7h)<br><code>VCC_FAULT</code> | 5   | <code>DC6_FAULT</code> | 0       | DCDC6 fault mask for the <code>/VCC_FAULT</code><br>0 = don't mask converter fault<br>1 = mask converter fault |
|                                      | 4   | <code>DC5_FAULT</code> | 0       | DCDC5 fault mask for the <code>/VCC_FAULT</code><br>0 = don't mask converter fault<br>1 = mask converter fault |
|                                      | 3   | <code>DC4_FAULT</code> | 0       | DCDC4 fault mask for the <code>/VCC_FAULT</code><br>0 = don't mask converter fault<br>1 = mask converter fault |
|                                      | 2   | <code>DC3_FAULT</code> | 0       | DCDC3 fault mask for the <code>/VCC_FAULT</code><br>0 = don't mask converter fault<br>1 = mask converter fault |
|                                      | 1   | <code>DC2_FAULT</code> |         | DCDC2 fault mask for the <code>/VCC_FAULT</code><br>0 = don't mask converter fault<br>1 = mask converter fault |
|                                      | 0   | <code>DC1_FAULT</code> |         | DCDC1 fault mask for the <code>/VCC_FAULT</code><br>0 = don't mask converter fault<br>1 = mask converter fault |

**Table 81 DC Converter `/VCCFAULT` Mask Bits**



## 14.7 CONFIGURING THE LDO REGULATORS

The configuration of the LDO Regulators is described in the following sections. Some of the control fields form part of the Custom Mode configuration settings and therefore will not require to be set in software in some applications.

### 14.7.1 LDO REGULATOR ENABLE

The LDO Regulators can be enabled in software using the register fields defined in Table 82. To reduce supply in-rush current, individual regulators should be programmed to start in different time slots within the start-up sequence.

In the WM8350 ACTIVE state, the LDO Regulators can be enabled in software using the LDO<sub>n</sub>\_ENA bits. Setting these bits whilst in the Pre-Active state (see Figure 65) will not immediately enable the corresponding LDO Regulators; these bits will only become effective once the WM8350 has reached the ACTIVE state.

Each Regulator may be programmed to switch on in a selected timeslot within the start-up sequence. The WM8350 will set the LDO<sub>n</sub>\_ENA field for any LDO Regulator that is enabled during the start-up sequence. Note that setting the LDO<sub>n</sub>\_ENSL0T fields in software is only relevant to the Development Mode, as these fields are assigned preset values in each of the Custom Modes.

Each Regulator may be programmed to switch off in a selected timeslot within the shutdown sequence. If a Regulator is not allocated to one of the 14 shutdown timeslots, it will be disabled when the WM8350 enters the OFF state.

| ADDRESS   | BIT | LABEL    | DEFAULT | DESCRIPTION  |
|---|-----|----------|---------|--|
| R13 (0Dh) or<br>R176 (B0h)<br>DC-DC / LDO<br>requested  | 8   | LDO1_ENA | 0       | LDO1 enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. |
|   | 9   | LDO2_ENA | 0       | LDO2 enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. |
|   | 10  | LDO3_ENA | 0       | LDO3 enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. |
|   | 11  | LDO4_ENA | 0       | LDO4 enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status. |
| <b>Note:</b> These bits can be accessed through R13 or through R176. Reading from or writing to either register location has the same effect. |     |          |         |  |

| ADDRESS                | BIT   | LABEL                              | DEFAULT                               | DESCRIPTION   |
|------------------------|-------|------------------------------------|---------------------------------------|---|
| R201 (C9h)<br>for LDO1 | 13:10 | LDO <sub>n</sub> _ENSL<br>OT [3:0] | Dependant<br>on<br>CONFIG<br>settings | Time slot for LDO <sub>n</sub> start-up<br>0000 = Disabled (do not start up)<br>0001 = Start-up in time slot 1<br>... (total 14 slots available)<br>1110 = Start-up in time slot 14<br>1111 = Start up on entering ACTIVE |
| R204 (CCh)<br>for LDO2 |       |                                    |                                       |   |
| R207 (CFh)<br>for LDO3 | 9:6   | LDO <sub>n</sub> _SDSL<br>OT [3:0] | 0000                                  | Time slot for LDO <sub>n</sub> shutdown.<br>0000 = Shut down on entering OFF<br>0001 = Shutdown in time slot 1<br>.... (total 14 slots available)<br>1110 = Shutdown in time slot 14<br>1111 = Shut down on entering OFF  |
| R210 (D2h)<br>for LDO4 |       |                                    |                                       |   |

**Note:** *n* is a number between 1 and 4 that identifies the individual DC-DC converter

Table 82 Enabling and Disabling the LDO Regulators

### 14.7.2 LDO REGULATOR CONTROL

The LDO Regulators can be configured to operate in different modes using the register bits described in Table 83.

In Switch mode, the Regulators operate as current-limited switches with no voltage regulation.

In LDO Regulator mode, the Regulators generate an output voltage determined by the LDO<sub>n</sub>\_VSEL fields. The LDO Regulators are dynamically programmable - the output voltage may be adjusted in software at any time. The Regulators are critically damped to ensure there is no voltage overshoot or undershoot when adjusting the output voltage.

The default output voltage for the LDO Regulators is set by writing to the LDO<sub>n</sub>\_VSEL register bits. The 'image' voltage settings LDO<sub>n</sub>\_VIMG are alternate values that may be invoked when the HIBERNATE software or hardware control is asserted.

| ADDRESS                | BIT | LABEL                           | DEFAULT                            | DESCRIPTION  |
|------------------------|-----|---------------------------------|------------------------------------|--|
| R200 (C8h)<br>for LDO1 | 14  | LDO <sub>n</sub> _SWI           | 0                                  | LDO <sub>n</sub> Regulator mode<br>0 = LDO voltage regulator<br>1 = Current-limited switch (no voltage regulation, LDO <sub>n</sub> _VSEL has no effect)                                   |
| R203 (CBh)<br>for LDO2 |     |                                 |                                    |  |
| R206 (CEh)<br>for LDO3 | 4:0 | LDO <sub>n</sub> _VSEL<br>[4:0] | Dependant<br>on CONFIG<br>settings | LDO <sub>n</sub> Regulator output voltage (when LDO <sub>n</sub> _SWI=0)<br><br>1 1111 = 3.3V<br>... (100mV steps)<br>1 0000 = 1.8V<br>0 1111 = 1.65V<br>... (50mV steps)<br>0 0000 = 0.9V |
| R209 (D1h)<br>for LDO4 |     |                                 |                                    |  |
| R202 (CAh)<br>for LDO1 | 4:0 | LDO <sub>n</sub> _VIMG<br>[4:0] | 1 1100                             | LDO <sub>n</sub> Regulator output image voltage<br><br>1 1111 = 3.3V<br>... (100mV steps)<br>1 0000 = 1.8V<br>0 1111 = 1.65V<br>... (50mV steps)<br>0 0000 = 0.9V                          |
| R205 (CDh)<br>for LDO2 |     |                                 |                                    |  |
| R208 (D0h)<br>for LDO3 |     |                                 |                                    |  |
| R211 (D3h)<br>for LDO4 |     |                                 |                                    |  |

**Note:** *n* is a number between 1 and 4 that identifies the individual LDO regulator

Table 83 Controlling Regulator Voltage and Switch Mode

The LDO Regulators can also be controlled by the device HIBERNATE bit, or by hardware input signals L\_PWR1, L\_PWR2 and L\_PWR3. Several GPIO pins can be assigned as L\_PWR pins. Each Regulator can be assigned to one of these three signals, or else to the device HIBERNATE bit. The signals are active high and each Regulator's response to the selected signal is programmable as defined in Table 84.

Note that, when a GPIO pin is configured as a Hibernate input pin, and this input is asserted, then all LDO Regulators will be placed in Hibernate mode.

In order to use GPIO pins as L\_PWR pins, they must be configured by setting the respective GPn\_FN, and GPn\_DIR bits to the appropriate value (see Section 20).

| ADDRESS  | BIT   | LABEL                                | DEFAULT | DESCRIPTION  |
|--|-------|--------------------------------------|---------|--|
| R202 (CAh)<br>for LDO1   | 13:12 | LDO <sub>n</sub> _HIB_M<br>ODE [1:0] | 00      | LDO <sub>n</sub> Hibernate behaviour:<br>00 = Select voltage image settings<br>01 = disable output<br>10 = reserved<br>11 = reserved |
| R205 (CDh)<br>for LDO2   |       |                                      |         |  |
| R208 (D0h)<br>for LDO3   | 9:8   | LDO <sub>n</sub> _HIB_T<br>RIG [1:0] | 00      | LDO <sub>n</sub> Hibernate signal select<br>00 = Hibernate register bit<br>01 = L_PWR1<br>10 = L_PWR2<br>11 = L_PWR3                 |
| R211 (D3h)<br>for LDO4   |       |                                      |         |  |
| <b>Note:</b> <i>n</i> is a number between 1 and 4 that identifies the individual LDO regulator |       |                                      |         |  |

**Table 84 Configuring Hardware Control for LDO Regulators**

When the LDO Regulators are disabled, the output can be set to float or else the outputs can be actively discharged through internal resistors. This feature is controlled using the register bits described in Table 85.

Note that the "float" option is only supported when at least one other LDO Regulator remains enabled. If LDO Regulators 1, 2, 3 and 4 are all disabled, then the LDO Regulator outputs will be discharged, regardless of the LDO<sub>n</sub>\_OPFLT registers.

| ADDRESS  | BIT | LABEL                   | DEFAULT | DESCRIPTION   |
|--|-----|-------------------------|---------|---|
| R200 (C8h)<br>for LDO1   | 10  | LDO <sub>n</sub> _OPFLT | 0       | Enable discharge of LDO <sub>n</sub> outputs<br>when LDO <sub>n</sub> is disabled<br>0 = Enabled - Output to be discharged<br>1 = Disabled - Output is left floating<br>Note - if LDO Regulators 1, 2, 3 and 4<br>are all disabled, then the outputs will all<br>be discharged, regardless of the<br>LDO <sub>n</sub> _OPFLT bit. |
| R203 (CBh)<br>for LDO2   |     |                         |         |   |
| R206 (CEh)<br>for LDO3   |     |                         |         |   |
| R209 (D1h)<br>for LDO4   |     |                         |         |   |
| <b>Note:</b> <i>n</i> is a number between 1 and 4 that identifies the individual LDO regulator |     |                         |         |   |

**Table 85 Output Float Control for LDO Regulators**

### 14.7.3 INTERRUPTS AND FAULT PROTECTION

Each LDO Regulator is monitored for voltage accuracy and fault conditions. An undervoltage condition is set if the voltage falls below 95% of the required level. The action taken in response to a fault condition can be set independently for each LDO Regulator, as described in Table 86. The LDO<sub>n</sub>\_ERRACT fields configure the fault response to disable the respective regulator or to shut down the entire system if desired. In addition, LDO Regulator fault conditions also generate a second-level interrupt (see Section 24).

To prevent false alarms during short current surges, faults are only signalled if the fault condition persists.

| ADDRESS  | BIT   | LABEL                             | DEFAULT | DESCRIPTION  |
|--|-------|-----------------------------------|---------|--|
| R201 (C9h)<br>for LDO1   | 15:14 | LDO <sub>n</sub> _ERRACT<br>[1:0] | 00      | Action to take on LDO <sub>n</sub> fault (as well as generating an interrupt):<br>00 = ignore<br>01 = shut down regulator<br>10 = shut down system<br>11 = reserved (shut down system) |
| R204 (CCh)<br>for LDO2   |       |                                   |         |  |
| R207 (CFh)<br>for LDO3   |       |                                   |         |  |
| R210 (D2h)<br>for LDO4   |       |                                   |         |  |
| <b>Note:</b> <i>n</i> is a number between 1 and 4 that identifies the individual LDO regulator |       |                                   |         |  |

**Table 86 Fault Responses for LDO Regulators**

The DC-DC Converters and the LDO Regulators have a first-level interrupt, UV\_INT (see Section 24). This comprises second-level interrupts from each of the DC-DC Converters and the LDO Regulators.

Each LDO Regulator has a dedicated second-level interrupt which indicates an under-voltage condition. These can be masked by setting the applicable mask bit as defined in Table 87.

| ADDRESS  | BIT          | LABEL                                    | DESCRIPTION  |
|--|--------------|--|--|
| R28 (1Ch)<br>Under Voltage<br>Interrupt Status | 11           | UV_LDO4_EINT                             | LDO4 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|  | 10           | UV_LDO3_EINT                             | LDO3 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|  | 9            | UV_LDO2_EINT                             | LDO2 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|  | 8            | UV_LDO1_EINT                             | LDO1 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
| R36 (24h)<br>Under Voltage<br>Interrupt Mask   | as in<br>R28 | "IM_" + name of respective<br>bit in R28 | Mask bits for LDO regulator under-voltage<br>interrupts<br>Each of these bits masks the respective<br>bit in R28 when it is set to 1 (e.g.<br>UV_LDO1_EINT in R28 does not trigger a<br>UV_INT interrupt when<br>IM_UV_LDO1_EINT in R36 is set). |

**Table 87 LDO Regulator Interrupts**

The status of the LDO Regulators can be indicated and monitored externally via a GPIO pin configured as `/VCC_FAULT` (see Section 20). When a GPIO pin is configured as `/VCC_FAULT` output, a logic low level on this pin indicates that there is a fault condition on one of the LDO Regulators, DC-DC Converters, or the Current Limit switch.

The `/VCC_FAULT` output is configurable by the control fields in Register R215. The fields described in Table 88 determine which of the LDOs contribute to the `/VCC_FAULT` indication. An undervoltage or overvoltage condition on any unmasked LDO will cause the `/VCC_FAULT` output to be set to logic low.

| ADDRESS                              | BIT | LABEL                   | DEFAULT | DESCRIPTION   |
|--------------------------------------|-----|-------------------------|---------|---|
| R215 (D7h)<br><code>VCC_FAULT</code> | 11  | <code>LDO4_FAULT</code> | 0       | LDO4 fault mask for the <code>/VCC_FAULT</code><br>0 = don't mask converter fault<br>1 = mask converter fault |
|                                      | 10  | <code>LDO3_FAULT</code> | 0       | LDO3 fault mask for the <code>/VCC_FAULT</code><br>0 = don't mask converter fault<br>1 = mask converter fault |
|                                      | 9   | <code>LDO2_FAULT</code> | 0       | LDO2 fault mask for the <code>/VCC_FAULT</code><br>0 = don't mask converter fault<br>1 = mask converter fault |
|                                      | 8   | <code>LDO1_FAULT</code> | 0       | LDO1 fault mask for the <code>/VCC_FAULT</code><br>0 = don't mask converter fault<br>1 = mask converter fault |

**Table 88 LDO Regulator `/VCCFAULT` mask bits**

#### 14.7.4 ADDITIONAL CONTROL FOR LDO1

By default, all DC Converters and LDOs are disabled in the OFF state. Additional control is provided to enable LDO1 to be configured differently, allowing it to be enabled in the OFF state, or else to be controlled by a GPIO pin configured as `/LDO_ENA` (see Section 20.2.2). These options are selected by setting the register fields described in Table 89. In practical applications, however, these options are set by the Config Mode settings and are not set by users.

Operation of LDO1 in the OFF state is subject to the restriction that `VOUT1` must be set to at least 1.8V.

| CONDITION  | DESCRIPTION                                   |
|--|---|
| <code>LDO1_PIN_MODE = 0</code>                                 | LDO1 controlled as normal via register bits   |
| <code>LDO1_PIN_MODE = 1</code><br><code>LDO1_PIN_EN = 0</code> | LDO1 enabled at all times                     |
| <code>LDO1_PIN_MODE = 1</code><br><code>LDO1_PIN_EN = 1</code> | LDO1 controlled by <code>/LDO_ENA</code> only |

**Table 89 LDO1 Additional Control**

Note that LDO1 is always disabled in BACKUP and ZERO states.

Note that, when `LDO1_PIN_MODE = 1`, then LDO1 only operates as determined by the `LDO1_VSEL` field. The Hibernate settings are ignored under this configuration.

## 14.8 DC-DC CONVERTER OPERATION

### 14.8.1 OVERVIEW

The WM8350 provides six DC-DC switching converters. Four of these are Buck (Step-down) converters and two are Boost (Step-up) converters. The principal characteristics and typical usage for each DC-DC converter are shown below.

|                      | <b>DC-DC 1 / 6</b>                          | <b>DC-DC 2 / 5</b>                         | <b>DC-DC 3 / 4</b>                             |
|----------------------|---|--|--|
| Typical Application  | Other system components                     | Constant-current LED drivers or I/O supply | Digital supply for WM8350 and other components |
| Converter Type       | Step-down                                   | Step-up, using external NFET               | Step-down                                      |
| Input Voltage Range  | 2.7V to 5.5V                                |  |  |
| Output Voltage Range | 0.85V to 3.4V                               | 5V to 20V                                  | 0.85V to 3.4V                                  |
| Load Current Rating  | Up to 1A<br>(may be limited by application) | 170mA @ 5V<br>40mA @ 20V                   | Up to 500mA<br>(may be limited by application) |
| Switching Frequency  | 2.0MHz                                      | 1.0MHz                                     | 2.0MHz   |

**Table 90 DC-DC Converter Characteristics**

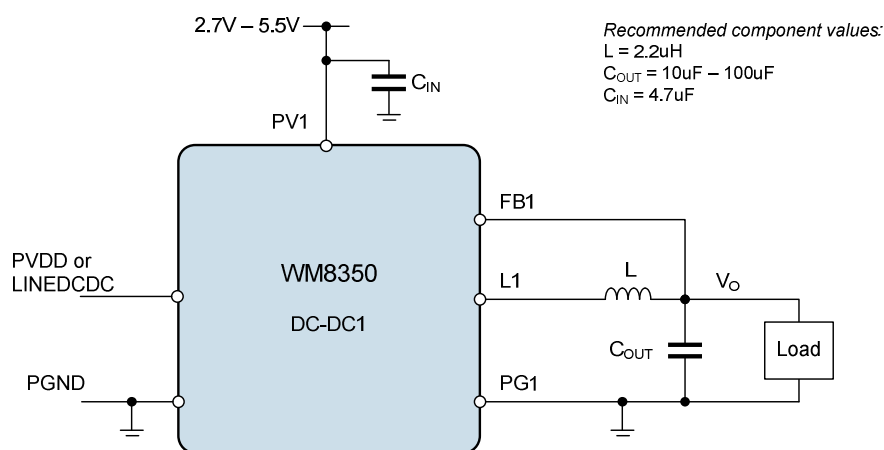
### 14.8.2 DC-DC STEP DOWN CONVERTERS

DC-DC Converters 1, 3, 4 and 6 are versatile step-down, pulse-width-modulated (PWM) DC-DC converters designed to deliver high power efficiency across full load conditions. The converters offer Active and Standby/Hysteretic operating modes in order to maximise efficiency for different loads. A low-power LDO sleep mode is also available to further reduce quiescent current at very lightly loaded conditions. The DC-DC Converters maintain output voltage regulation during the switch-over between operating modes.

The step-down regulators are designed with a fixed frequency current mode architecture. The current feedback loop is through the PMOS current path and is amplified and summed with an internal slope compensation network. The voltage feedback loop is through an internal feedback divider. The ON time is determined by comparing the summed current feedback and the output of the switcher error amplifier. The period is set by the internal RC oscillator, which provides a 2.0MHz clock.

A supply pin (PVDD) provides the core supply for DC-DC Converters 3 and 6. Another supply pin (LINEDCDC) provides the core supply for DC-DC Converters 1 and 4. The input voltage connection to DC-DC Converters 1, 3, 4 and 6 is provided on PV1, PV3, PV4 and PV6 respectively. These input voltages may be provided from the LINE voltage.

The connections to DC-DC Converter 1 are illustrated in Figure 69. The equivalent circuit applies to DC-DC Converters 3, 4 and 6 also.



*Note: Equivalent circuit applies for DC-DC 3, 4 and 6.*

**Figure 69 Step-Down DC-DC Converter Connections**

The external components at the converter output are required by the DC-DC Converter integral loop compensation circuit. Note that the recommended output capacitor  $C_{\text{out}}$  varies according to the required transient response on DC-DC1 and DC-DC6. A single recommended value is provided for  $C_{\text{out}}$  on DC-DC3 and DC-DC4.

See Section 29.2 for details of the recommended external components.

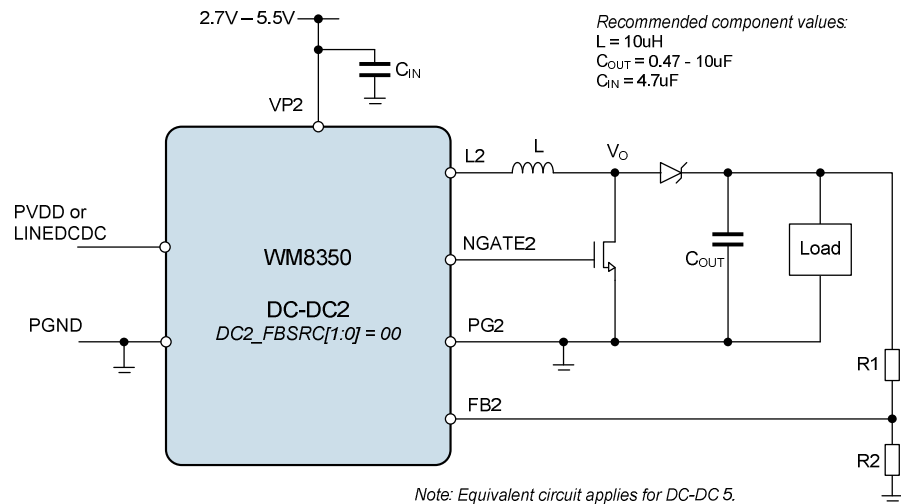
### 14.8.3 DC-DC STEP UP CONVERTERS

DC-DC Converters 2 and 5 are versatile step-up pulse-width-modulated (PWM) DC-DC converters designed to deliver high power efficiency across full load conditions. The converters can also be used as switches.

DC-DC Converters 2 and 5 are designed with a fixed frequency current mode architecture. The clock frequency is set by the internal RC oscillator, which provides a 1.0MHz clock.

The PVDD supply pin provides the core supply for DC-DC Converter 2. The LINEDCDC supply pin provides the core supply for DC-DC Converter 5.

The connections to DC-DC Converter 2 in Constant Voltage Mode are illustrated in Figure 70. The equivalent circuit applies to DC-DC Converter 5 also. See Section 29.4 for details of the connections for the Constant Current and USB operating modes of the DC-DC Step-Up Converters.



**Figure 70 Step-Up DC-DC Converter Connections**

The external components at the converter output are required by the DC-DC Converter integral loop compensation circuit. Note that the recommended output capacitor  $C_{\text{out}}$  varies according to the required output voltage.

See Section 29.4 for details of the recommended external components.



## 14.9 LDO REGULATOR OPERATION

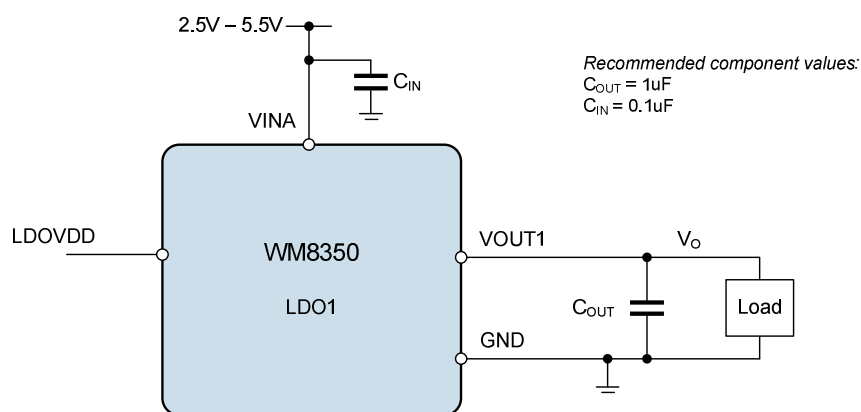
The WM8350 provides four identical LDO voltage regulators to generate accurate, low-noise supply voltages for various system components. The LDOs can also operate as current-limited switches, with no voltage regulation; this is useful for 'Hot Swap' outputs, i.e. supply rails for external devices that are plugged in when the system is already powered up - the current-limiting function prevents the in-rush current into the external device from disturbing other system power supplies.

The LDO regulators are dynamically programmable. Each regulator output is current-limited; the output voltage is automatically throttled back if the load current exceeds the limit.

A single supply pin (LDOVDD) provides the core supply for all four LDOs. The input voltage connection to LDO1 and LDO2 is provided on the VINA pin. The input voltage connection to LDO3 and LDO4 is provided on the VINB pin. These input voltages can be provided from one of the DC-DC Converters or from the LINE voltage.

Note that separate voltage regulators are provided to generate the backup supply VRTC and the microphone bias voltage MICBIAS.

The connections to LDO Regulator 1 are illustrated in Figure 71. The equivalent circuit applies to LDO2, LDO3 and LDO4.



*Note: Equivalent circuit applies for LDO2, LDO3 and LDO4.  
 Input pin VINA supplies LDO1 and LDO2; Input pin VINB supplies LDO3 and LDO4.*

**Figure 71 LDO Regulator Connections**

An input and output capacitor are recommended for each LDO Regulator, as illustrated above. See Section 29.5 for details of the recommended external components.

## 15 CURRENT LIMIT SWITCH

### 15.1 GENERAL DESCRIPTION

The WM8350 includes an on-chip Current Limit Switch to control external devices and to support hot-plugging of accessories and power supplies.

When the switch is enabled, it normally has a low resistance, allowing current to pass through (from the IP pin to the OP pin). If the current limit threshold is reached, the WM8350 can raise an interrupt, disable the switch and/or shut down the whole device.

### 15.2 CONFIGURING THE CURRENT LIMIT SWITCH

#### 15.2.1 CURRENT LIMIT SWITCH ENABLE

The Current Limit Switch can be enabled in software using the register fields defined in Table 91.

In Active mode, the Current Limit Switch can be enabled in software using the LS\_ENA bit. Setting this bit whilst in the Pre-Active state (see Figure 65) will not immediately enable the Current Limit Switch; this bit will only become effective once the WM8350 has reached the Active state.

The Current Limit Switch may be programmed to become enabled in a selected timeslot within the start-up sequence. When this happens, the WM8350 will set the LS\_ENA bit. Note that setting the LS\_ENSLOT field in software is only relevant to the Development Mode, as this field is assigned a preset value in each of the Custom Modes.

The Current Limit Switch may be programmed to switch off in a selected timeslot within the shutdown sequence. If the Limit Switch is not allocated to one of the 14 shutdown timeslots, it will be disabled when the WM8350 enters the OFF state.

The Current Limit Switch behaviour in Hibernate mode is controlled by the LS\_HIB\_MODE bit.

| ADDRESS   | BIT   | LABEL           | DEFAULT | DESCRIPTION   |
|---|-------|-----------------|---------|---|
| R13 (0Dh)   | 15    | LS_ENA          | 0       | Limit Switch enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.                      |
| R176 (B0h)<br>DC-DC / LDO requested   | 15    |                 |         |   |
| <b>Note:</b> LS_ENA can be accessed through R13 or through R176. Reading from or writing to either register location has the same effect. |       |                 |         |   |
| R199 (C7h)<br>Limit switch control  | 13:10 | LS_ENSLOT [3:0] | 0000    | Time slot for Limit Switch start-up<br>0000 = Disabled (do not start up)<br>0001 = Start-up in time slot 1<br>... (total 14 slots available)<br>1110 = Start-up in time slot 14<br>1111 = Start-up on entering ACTIVE |
|   | 9:6   | LS_SDSLOT [3:0] | 0000    | Time slot for Limit Switch shutdown.<br>0000 = Shut down on entering OFF<br>0001 = Shutdown in time slot 1<br>.... (total 14 slots available)<br>1110 = Shutdown in time slot 14<br>1111 = Shut down on entering OFF  |
|   | 4     | LS_HIB_MODE     | 0       | Limit switch hibernate mode setting<br>0 = disabled<br>1 = leave setting as in Active mode  |

Table 91 Enabling and Disabling the Current Limit Switch

### 15.2.2 CURRENT LIMIT SWITCH BULK DETECTION CONTROL

The Current Limit Switch can be connected to voltages which may be higher than the device LINE voltage. To support this capability, the switch is powered from the highest available voltage; this requires a bulk detection circuit in order to select the highest available voltage. The bulk detection circuit is always enabled whenever the Current Limit Switch is enabled.

It is possible to control whether the bulk detection circuit is enabled or not when the Current Limit Switch is disabled. This is controlled in Active mode by the LS\_PROT bit, and in Hibernate mode by the LS\_HIB\_PROT bit.

Disabling the Bulk Detection circuit will reduce power consumption. It is important to note, however, that the Bulk Detection circuit should always be enabled if voltages greater than LINE could be present on IP or OP. This applies regardless of whether the Current Switch is open or closed.

| ADDRESS                            | BIT | LABEL       | DEFAULT | DESCRIPTION   |
|------------------------------------|-----|-------------|---------|---|
| R199 (C7h)<br>Limit switch control | 1   | LS_HIB_PROT | 1       | Controls the bulk detection circuit when Limit Switch is disabled in Hibernate mode.<br>0 = bulk detection disabled<br>1 = bulk detection enabled |
|                                    | 0   | LS_PROT     | 1       | Controls the bulk detection circuit when Limit Switch is disabled in Active mode.<br>0 = bulk detection disabled<br>1 = bulk detection enabled    |

**Table 92 Current Limit Switch Bulk Detection Control**

### 15.2.3 INTERRUPTS AND FAULT PROTECTION

The response to an over-current condition is selectable. To prevent false alarms during short current surges, faults are only signalled if the fault condition persists.

| ADDRESS                            | BIT   | LABEL           | DEFAULT | DESCRIPTION   |
|------------------------------------|-------|-----------------|---------|---|
| R199 (C7h)<br>Limit switch control | 15:14 | LS_ERRACT [1:0] | 00      | Current limit detection behaviour<br>00 = ignore<br>01 = disable switch<br>10 = shut down system<br>11 = shut down system |

**Table 93 Fault Response for the Current Limit Switch**

The limit switch has its own first-level interrupt, OC\_INT (see Section 24). This contains a single second-level interrupt, OC\_LS\_EINT, indicating an over-current condition. OC\_LS\_EINT can be masked by setting the IM\_OC\_LS\_EINT bit.

| ADDRESS                                    | BIT | LABEL         | DESCRIPTION  |
|--|-----|---------------|--|
| R29 (1Dh)<br>Over Current Interrupt Status | 15  | OC_LS_EINT    | Limit Switch Over-current interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
| R37 (25h)<br>Over Current Interrupt Mask   | 15  | IM_OC_LS_EINT | Mask bit for Limit switch over-current interrupt<br>When set to 1, IM_OC_LS_EINT masks OC_LS_EINT in R29 and does not trigger an OC_INT interrupt when OC_LS_EINT is set). |

**Table 94 Current Limit Switch Interrupts**

The status of the Current Limit Switch can be indicated and monitored externally via a GPIO pin configured as `/VCC_FAULT` (see Section 20). When a GPIO pin is configured as `/VCC_FAULT` output, a logic low level on this pin indicates that there is a fault condition on one of the LDO Regulators, DC-DC Converters, or the Current Limit switch.

The `/VCC_FAULT` output is configurable by the control fields in Register R215. The `LS_FAULT` bit described in Table 95 selects whether the Limit Switch contributes to the `/VCC_FAULT` indication. When `LS_FAULT = 0`, then an overcurrent condition on the Limit Switch will cause the `/VCC_FAULT` output to be set to logic low.

| ADDRESS                              | BIT | LABEL                 | DEFAULT | DESCRIPTION   |
|--------------------------------------|-----|-----------------------|---------|---|
| R215 (D7h)<br><code>VCC_FAULT</code> | 15  | <code>LS_FAULT</code> | 0       | Limit Switch fault mask for the <code>/VCC_FAULT</code><br>0 = don't mask converter fault<br>1 = mask converter fault |

**Table 95** Limit Switch `/VCCFAULT` Mask

## 16 CURRENT SINKS (LED DRIVERS)

### 16.1 GENERAL DESCRIPTION

The WM8350 includes five pins for driving different types of LEDs.

The pins ISINKA and ISINKB provide programmable constant-current sinks designed to drive strings of serially connected LEDs, including white LEDs used in display backlights or in camera flash applications. Using ISINKA and ISINKB in conjunction with DC-DC Converters 2 or 5 provides a particularly power-efficient way to drive such LED strings. The ground connection associated with these two Current Sinks is the SINKGND pin.

ISINKC, ISINKD and ISINKE are regular open-drain outputs. They are alternate functions of the GPIO10, GPIO11 and GPIO12 pins respectively. These GPIOs are provided on the LINE power domain; the associated ground connection is the GND pin.

### 16.2 CONSTANT-CURRENT SINKS

ISINKA and ISINKB are dedicated LED driver pins equipped with programmable constant current sinks. They are designed to drive strings of serially connected white LEDs such as those used in display backlights or photo-flash applications. Powering LEDs in this way is particularly power efficient because no series resistor is required. DC-DC converters 2 or 5, operating as a current-controlled voltage source, are ideal power sources for LED strings. These converters can generate voltages higher than BATT or LINE, which can overcome the combined forward voltages of long LED strings (e.g. a string of 7 white LEDs with a forward voltage of 4V requires at least 28V).

#### 16.2.1 ENABLING THE SINK CURRENT

In Active mode, ISINKA and ISINKB can be enabled in software using the register fields defined in Table 96. If required, the Current Sink functions may also be controlled by the Hibernate bit.

Note that these control bits do not exist for ISINKC, ISINKD or ISINKE.

| ADDRESS   | BIT | LABEL            | DEFAULT | DESCRIPTION   |
|---|-----|------------------|---------|---|
| R14 (0Eh)<br>Power mgmt<br>(7)  | 0   | CS1_ENA          | 0       | Current Sink 1 enable (ISINKA pin)<br>0 = disabled<br>1 = enabled   |
| R172 (ACh)<br>Current Sink<br>Driver A  | 15  | CS1_HIB_MO<br>DE | 0       | Current Sink 1 behaviour in Hibernate<br>mode<br>0 = disable current sink in Hibernate<br>1 = leave current sink as in Active |
|   | 12  |                  |         |   |
| R14 (0Eh)<br>Power mgmt<br>(7)  | 1   | CS2_ENA          | 0       | Current Sink 2 enable (ISINKB pin)<br>0 = disabled<br>1 = enabled   |
| R174 (AEh)<br>Current Sink<br>Driver B  | 15  | CS2_HIB_MO<br>DE | 0       | Current Sink 2 behaviour in Hibernate<br>mode<br>0 = disable current sink in Hibernate<br>1 = leave current sink as in Active |
|   | 12  |                  |         |   |
| <b>Note:</b> CS1_ENA and CS2_ENA can be accessed through R14 or through R172/R174. Reading from or writing to either register location has the same effect. |     |                  |         |   |

**Table 96 Enabling ISINKA and ISINKB**

When ISINKA or ISINKB is used in conjunction with DC-DC Converter 2 or 5, the ISINK should always be switched on before the DC-DC Converter is switched on. Conversely, the DC-DC Converter should always be switched off before the ISINK is switched off. If high voltages are used, additional external components may also be needed to protect the WM8350.

### 16.2.2 PROGRAMMING THE SINK CURRENT

The sink currents for ISINKA and ISINKB can be independently programmed by writing to the CS1\_ISEL and CS2\_ISEL register bits. The current steps are logarithmic to match the logarithmic light sensitivity characteristic of the human eye. The step size is 1.5dB (i.e. the current doubles every four steps).

| ADDRESS                                | BIT | LABEL    | DEFAULT | DESCRIPTION  |
|--|-----|----------|---------|--|
| R172 (ACh)<br>Current Sink<br>Driver A | 5:0 | CS1_ISEL | 00 0000 | ISINKA current = $4.05\mu\text{A} \times 2^{\text{CS1\_ISEL}/4}$<br>where CS1_ISEL is an unsigned binary number<br>Minimum: 00 0000 = 4.05 $\mu\text{A}$ ,<br>Maximum: 11 1111 = 220mA<br>(from circuit simulation)<br>or<br>CS1_ISEL = $13.3 \times \log(\text{desired current} / 4.05\mu\text{A})$ |
| R174 (AEh)<br>Current Sink<br>Driver B | 5:0 | CS2_ISEL | 00 0000 | ISINKB current = $4.05\mu\text{A} \times 2^{\text{CS2\_ISEL}/4}$<br>where CS2_ISEL is an unsigned binary number<br>Minimum: 00 0000 = 4.05 $\mu\text{A}$ ,<br>Maximum: 11 1111 = 220mA<br>(from circuit simulation)<br>or<br>CS2_ISEL = $13.3 \times \log(\text{desired current} / 4.05\mu\text{A})$ |

**Table 97 Controlling the Sink Current for ISINKA and ISINKB**

Note that currents above 40mA are not supported continuously; these settings are intended for flash mode only.

### 16.2.3 FLASH MODE

Each current sink can either sink current continuously (LED mode) or in short bursts (flash mode). The operating mode is selected by the CS $_n$ \_FLASH\_MODE bits, as described in Table 98.

In LED mode, the current sink is controlled by setting CS $_n$ \_DRIVE. For as long as this bit is asserted, the LED is enabled continuously.

In Flash mode, the current sink may be set to automatically flash every 4 seconds by setting CS $_n$ \_FLASH\_RATE = 1, or may be triggered normally by setting CS $_n$ \_FLASH\_RATE = 0.

When normal triggering is selected in Flash mode, the trigger control can be either a GPIO Flash input (see Section 20) or a register control. Setting CS $_n$ \_TRIGSRC = 1 selects GPIO as the trigger. The flash will be edge triggered by the selected GPIO input. Setting CS $_n$ \_TRIGSRC = 0 selects the register field CS $_n$ \_DRIVE as the trigger. In this case, writing a 1 to CS $_n$ \_DRIVE will trigger a flash; this bit will be reset at the end of the flash.

In all flash modes, the duration of each flash is set by CS $_n$ \_FLASH\_DUR. The status of each current sink may be read from the CS $_n$ \_DRIVE bits.

In all modes, the current sink must also be enabled via the applicable CS $_n$ \_ENA bit (see Table 96).

Note that some photo-flash applications may require a reservoir capacitor to store sufficient charge for the flash.

| ADDRESS               | BIT  | LABEL                                 | DEFAULT | DESCRIPTION   |
|-----------------------|--|---------------------------------------|---------|---|
| R173 (ADh) for ISINKA | 15   | CS <sub>n</sub> _FLASH_MODE           | 0       | Determines the function of the current sink<br>0 = LED mode<br>1 = Flash mode   |
| R175 (AFh) for ISINKB | 14   | CS <sub>n</sub> _TRIGSRC              | 0       | Selects the trigger in Flash mode.<br>0 = Flash triggered by CS <sub>n</sub> _DRIVE bit<br>1 = Flash triggered from GPIO pin configured as FLASH<br>This bit has no effect when CS <sub>n</sub> _FLASH_MODE=0   |
|                       | 13   | CS <sub>n</sub> _DRIVE                | 0       | Enables the current sink ISINK <sub>n</sub><br><br>LED mode-<br>0 = disable LED<br>1 = enabled LED<br><br>FLASH mode-<br>Register bit used to trigger the flash, if CS <sub>1</sub> _TRIGSRC is set to 0. Flash is started when the bit goes high, it is then reset at the end of the flash duration. Duration is determined by CS <sub>1</sub> _FLASH_DUR. This bit has no effect if CS <sub>1</sub> _TRIGSRC is set to 1. |
|                       | 12   | CS <sub>n</sub> _FLASH_RATE           | 0       | Determines the Flash rate<br>0 = Normal Operation. Once per trigger (Either register bit or GPIO)<br>1 = Flash will be internally triggered every 4 second  |
|                       | 9:8  | CS <sub>n</sub> _FLASH_DURATION [1:0] | 00      | Sets duration of flash<br>00 = 32ms<br>01 = 64ms<br>10 = 96ms<br>11 = 1024ms  |
|                       | <b>Note:</b> <i>n</i> is either '1' for ISINKA or '2' for ISINKB |                                       |         |   |

Table 98 Configuring Flash Mode for ISINKA and ISINKB

Note that the CS<sub>n</sub>\_DRIVE bits are always reset when exiting the hibernate state, regardless of the REG\_RESET\_HIB\_MODE bit. If the CS<sub>n</sub>\_DRIVE is enabled in the hibernate state, then it must be re-enabled by writing to the applicable control register after exiting the hibernate state. This may result in a short interruption to the Current Sink output.

### 16.2.4 ON/OFF RAMP TIMING

The sink currents for ISINKA and ISINKB can be programmed to switch on and off gradually in LED and in Flash modes. The current ramp durations are set as described in Table 99.

| ADDRESS  | BIT | LABEL                            | DEFAULT | DESCRIPTION  |  |
|--|-----|----------------------------------|---------|--|--|
| R173 (ADh) for ISINKA<br><br>R175 (AFh) for ISINKB | 5:4 | CS <sub>n</sub> _OFF_RAM P [1:0] | 00      | Switch-off ramp duration   |  |
|  |     |                                  |         | LED Mode   | Flash Mode   |
|  |     |                                  |         | 00 = instant (no ramp)<br>01 = 0.25s<br>10 = 0.5s<br>11 = 1s     | 00 = instant (no ramp)<br>01 = 1.95ms<br>10 = 3.91ms<br>11 = 7.8ms |
|  | 1:0 | CS <sub>n</sub> _ON_RAM P [1:0]  | 00      | Switch-on ramp duration<br>Similar to CS <sub>n</sub> _OFF_RAM P |  |

**Note:** *n* is either '1' for ISINKA or '2' for ISINKB

**Table 99 Configuring On/Off Ramp Timing for ISINKA and ISINKB**

### 16.2.5 INTERRUPTS AND FAULT PROTECTION

The Current Sinks have a first-level interrupt, CS\_INT (see Section 24). This comprises two second-level interrupts which indicate if the Current Sinks are unable to sink the amount of current that has been programmed. CS1\_EINT and CS2\_EINT can be masked by setting the applicable mask bit as defined in Table 100.

| ADDRESS                              | BIT   | LABEL                                 | DESCRIPTION   |
|--------------------------------------|-------|---------------------------------------|---|
| R26 (1Ah)<br>Interrupt Status 2      | 13    | CS1_EINT                              | Flag to indicate drain voltage can no longer be regulated and output current may be out of spec.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |
|                                      | 12    | CS2_EINT                              | Flag to indicate drain voltage can no longer be regulated and output current may be out of spec.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |
| R34 (22h)<br>Interrupt Status 2 Mask | 13:12 | "IM_" + name of respective bit in R26 | Each bit in R34 enables or masks the corresponding bit in R26. The default value for these bits is 0 (unmasked).  |

**Table 100 Current Sink Interrupts**



### 16.3 OPEN-DRAIN LED OUTPUTS

The three open-drain outputs ISINKC, ISINKD and ISINKE are alternate functions of the GPIO10, GPIO11 and GPIO12 pins, respectively (see Section 20). They can drive LEDs connected to LINE, with a series resistor. Note that the GPIO pins have other alternate functions, which will not be available that pin is configured as ISINKC, ISINKD or ISINKE.

### 16.4 LED DRIVER CONNECTIONS

The recommended connections for LEDs on ISINKA and ISINKB are illustrated in Figure 72.

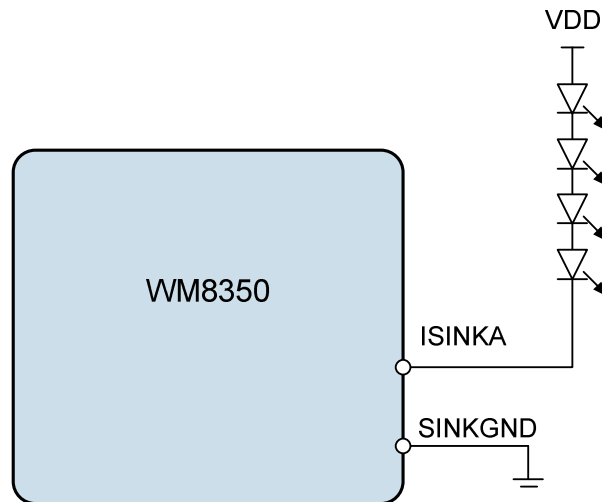


Figure 72 LED Connections to ISINKA and ISINKB

The recommended connections for LEDs on ISINKC, ISINKD and ISINKE are illustrated in Figure 73.

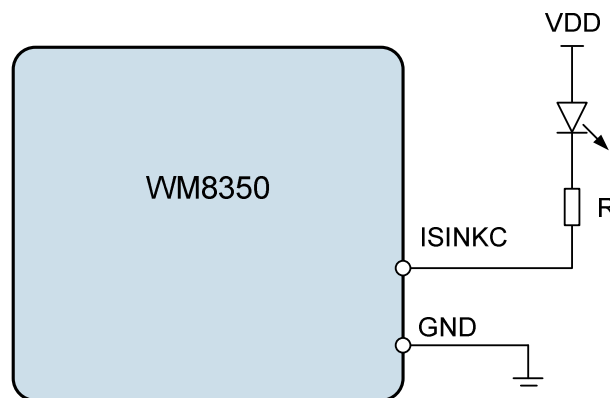


Figure 73 LED Connections to ISINKC, ISINKD and ISINKE

## 17 POWER SUPPLY CONTROL

### 17.1 GENERAL DESCRIPTION

The WM8350 can take its power supply from a Wall adaptor, a USB interface or from a single-cell lithium battery. The WM8350 autonomously chooses the most appropriate power source available, and supports hot-swapping between sources (ie. the system can remain in operation while different sources are connected and disconnected).

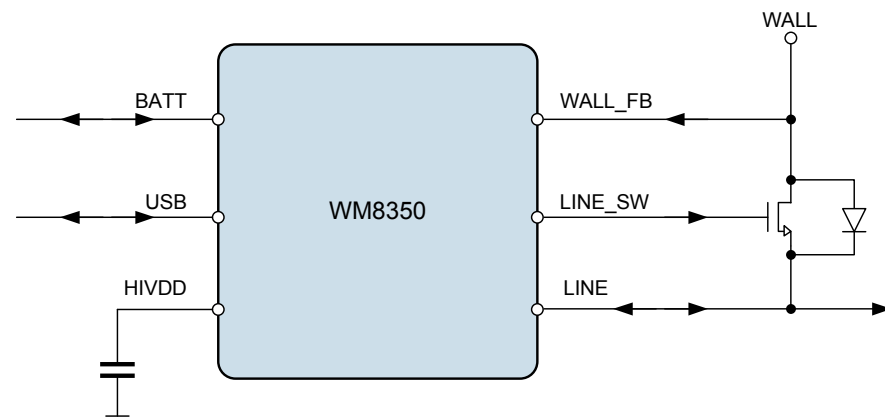
Comparators within the WM8350 identify which power supplies are available and select the power source in the following order of preference:

- Wall adaptor (LINE pins)
- USB power rail (USB pins)
- Battery (BATT pins)

Note that the Wall supply is always the first choice of supply, (providing that it is within required limits), even if the Wall supply voltage is lower than the USB voltage.

When Wall or USB is selected as the power source, this may be used to charge the Battery, using the integrated battery charger circuit. For battery charging to occur, the USB or LINE supply voltage must be no less than 4.0V.

Figure 74 illustrates the WM8350 connections associated with the WALL, USB and Battery supplies.



**Figure 74 WM8350 Power Supply Connections**

The Wall Adaptor supply connects to LINE via a FET switch as illustrated in Figure 74. The FET switch is necessary in order to provide isolation between the Wall supply and the Battery/USB supplies; this is vital in the event of the USB voltage being greater than the Wall supply voltage.

The Wall Adapter voltage is sensed directly on the WALL\_FB pin; this allows the WM8350 to determine the preferred supply, including when the FET is switched off.

The gate connection to the external FET is controlled by LINE\_SW, which is an alternate function that can be enabled on GPIO12 (see Section 20). Note that, if the USB connection is not used, then the FET may not be required and the Wall supply may be connected directly to LINE.

LINE is primarily an output from the WM8350; this output is the preferred supply, where the WM8350 has arbitrated between the Wall, Battery and USB connections. This output is suitable for supplying power to the other blocks of the WM8350, including the DC-DC Converters and LDO Regulators. LINE is also an input under some conditions, such as battery charging from Wall or providing power at the USB connection.

HIVDD is an external connection which exists for the purposes of decoupling only. It represents the highest available power supply connected to the WM8350. It should be noted that the preferred supply (on the LINE pin) is not necessarily the same voltage as HIVDD - the Wall supply will always be the preferred voltage when it is within the intended limits, even if it is not also the highest available source.

The main battery connects directly to the BATT pin. When the battery is the preferred supply source, this pin is an input. When battery charging is in operation, this pin is an output. (Note that the backup VRTC battery is connected separately - see Section 17.6.)

The USB interface connects directly to the USB pin. In USB Master Mode (USB is less than LINE), the WM8350 can supply power to external devices on this pin. In USB Slave Mode (USB is greater than LINE), the WM8350 can use this pin as an input to power the device and/or to charge a battery connected to the BATT pin. Note that, when USB is the preferred power supply, the Battery may also be used if necessary to supplement the current drawn from the USB pin (ie. to source current into LINE when required).

All loads connected to the WM8350 should normally be connected to the LINE pin. The inputs to the DC-DC Converters and LDOs should be connected to the LINE pin. It is not recommended to connect any load directly to the battery (BATT).

Note that the inputs to the LDOs may be connected to the outputs of the DC-DCs if desired.

## 17.2 BATTERY POWERED OPERATION

The WM8350 selects battery power when the Battery voltage is higher than the Wall (LINE) and USB supplies. In practical usage, this means the Battery is used when Wall (LINE) and USB are both disconnected.

The battery can also be used to supplement the USB supply when required (ie. to source current into LINE).

If the Wall (LINE) or USB supply becomes available during battery operation, then the selected power source is adjusted accordingly.

Battery pack temperature sensing is enabled by default. The battery's NTC resistor is monitored via the AUX1 pin on the WM8350, as described in Section 17.7. Note that the absence of this NTC connection will lead to a temperature failure condition being detected and battery charging will not be possible.

Safe operation of the battery charger outside the designed operating temperatures is not guaranteed when a battery NTC resistor is not used. The designed operating temperatures are noted in Section 17.7.7.

## 17.3 WALL ADAPTOR (LINE) POWERED OPERATION

The WM8350 selects Wall Adaptor power via the LINE pins whenever the Wall Adaptor supply is within the normal operating limits of 4.0V to 5.5V. The Wall Adaptor is also selected as the power source below 4.0V in the case where it is the highest available power source. The minimum LINE voltage is a programmable threshold in the range 2.9V to 3.6V (see Section 18). The maximum recommended operating voltage for LINE is 5.5V.

Note that USB power is not used when a suitable LINE supply is available, even if the USB supply is higher than the Wall (LINE) supply.

If the Wall (LINE) supply becomes unsuitable and a USB is available, then the USB supply will be selected as the preferred power source. Note that, when hot-swapping from Wall (LINE) to USB supply, a usable Battery must be present on the BATT pin.

When the Wall (LINE) supply is selected and a Battery is connected, then trickle charging is enabled by default, including when the WM8350 is in the OFF or HIBERNATE states. When the WM8350 is in the ACTIVE state, then fast charging may be selected under software control.

## 17.4 USB POWERED OPERATION

The WM8350 selects USB Slave mode by default. In USB Slave Mode, the USB pin can be used as one of the sources of power for the WM8350. In USB Master Mode (selected using the USB\_MSTR register bit) the WM8350 can provide power to an external USB device.

In USB Slave mode, the WM8350 selects USB power if the Wall (LINE) supply is outside its normal operating limits and the USB supply is the highest supply source available. For a transition from OFF to ACTIVE state to occur under USB power, the USB supply must be no less than 4.0V.

The maximum current drawn from the USB supply can be set to 100mA (USB low power mode) or 500mA (USB high power mode). The default is set according to the selected Config Mode (see Section 14).

When the WM8350 is in the ACTIVE state, USB high power mode can be selected using the register bits USB\_MSTR\_500MA (in USB Master Mode) or USB\_SLV\_500MA (in USB Slave Mode) as defined in Table 101. If a USB current higher than the applicable threshold is demanded, then internal protection circuits will limit the USB current, and the USB\_LIMIT\_EINT interrupt will be asserted.

Short term currents higher than 500mA can also be supported. This may be necessary for supporting transient demands (eg. for a hard drive starting up). When the USB\_NOLIM register field is set, the internal protection circuits are disabled, and the current limit interrupt threshold is raised to double the normal value. In 500mA mode, the current limit interrupt threshold is raised to approximately 1A. This feature must be used with caution, as the internal protection circuits are disabled when USB\_NOLIM is set. The maximum steady-state current supported is 500mA; higher currents can only be supported for short term transients.

USB power may be supplemented by battery power if available and if necessary to maintain the USB current within the applicable limit. If a suitable Wall (LINE) supply becomes available during USB operation, then the Wall (LINE) supply will be selected as the preferred power source. Note that, when hot-swapping from USB to Wall supply, a usable Battery must be present on the BATT pin.

In USB low power mode, trickle charging is enabled by default. Trickle charging is suspended if necessary to keep within the 100mA USB limit.

In USB high power mode, fast charging is possible (subject to other conditions - see Section 17.7.4). The fast charge current is controlled dynamically as necessary to keep the overall USB current within the 500mA limit.

Note that Battery Charging from the USB source is only possible in USB Slave Mode.

USB power may be suspended by writing to the USB\_SUSPEND register bit. Setting this bit to '1' disconnects the WM8350 from the USB supply, resulting in the selection of Battery as the power source. USB Suspend mode is invoked under software control, by writing to the USB\_SUSPEND bit. Suspend mode should be invoked whenever the USB connection is not used.

To comply with the USB 2.0 specification, the host processor should initially invoke USB Suspend mode after the WM8350 has successfully started up, and whenever the USB connection is not in use. If the USB connection is active and USB enumeration has been completed, the host processor may (but is not required to) switch the WM8350 into USB low-power mode or USB high-power mode. However, if wall adaptor power is available, it is recommended to remain in USB Suspend mode.

| ADDRESS                         | BIT | LABEL          | DEFAULT                      | DESCRIPTION  |
|---------------------------------|-----|----------------|------------------------------|--|
| R4 (04h)<br>System<br>Control 2 | 14  | USB_SUSPEND    | 0                            | Opens the USB switch<br>0 = USB enabled<br>1 = USB suspended<br>The register bit defaults to 0, when a reset happens or LINE < UVLO or the system fail on boot due to the upper limit of the Hysteresis Comp not being met.                        |
|                                 | 13  | USB_MSTR       | 0                            | Set the chip to be a USB master<br>0 = Slave<br>1 = Master<br>The register bit defaults to 0, when a reset happens or the USB state machine moves from MASTER mode to SLAVE mode.  |
|                                 | 11  | USB_MSTR_500MA | 0                            | Set 500mA or 100mA mode when the USB switch is in master mode<br>0 = 100mA<br>1 = 500mA  |
|                                 | 9   | USB_SLV_500MA  | Dependant on CONFIG settings | Set 500mA or 100mA mode when the USB switch is in slave mode<br>0 = 100mA<br>1 = 500mA<br>The register bit defaults to 0, when a reset happens or LINE<UVLO or the system fail on boot due to the upper limit of the Hysteresis Comp not been met. |

Table 101 Selecting USB Power Modes

The USB connection has its own first-level interrupt, USB\_INT (see Section 24). This contains a single second-level interrupt, USB\_LIMIT\_EINT, which indicates an over-current condition. USB\_LIMIT\_EINT can be masked by setting the IM\_USB\_LIMIT\_EINT bit.

USB Current monitoring is effective in USB Master and USB Slave Modes. The current limit threshold is determined by USB\_MSTR\_500MA (in USB Master Mode) or USB\_SLV\_500MA (in USB Slave Mode).

| ADDRESS                                 | BIT | LABEL             | DESCRIPTION  |
|---|-----|-------------------|--|
| R26 (1Ah)<br>Interrupt<br>Status 2      | 10  | USB_LIMIT_EINT    | USB Limit Switch interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
| R34 (22h)<br>Interrupt<br>Status 2 Mask | 10  | IM_USB_LIMIT_EINT | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br>When IM_USB_LIMIT_EINT is set to 1, then USB_LIMIT_EINT in R26 does not trigger an USB_INT interrupt when set.<br>The default value is 0 (unmasked). |

Table 102 USB Interrupt

## 17.5 EXTERNAL INTERRUPTS

The power supply control circuit has a first-level interrupt, EXT\_INT (see Section 24). This comprises three second-level interrupts which indicate if the USB, Wall or Battery supplies have been connected or disconnected. Internal feedback signals USB\_FB, WALL\_FB and BATT\_FB are used to indicate when the associated supplies are present. Note that these interrupt events occur on both the rising and falling edges of the trigger events. They can be masked by setting the applicable mask bits as defined in Table 103.

| ADDRESS   | BIT   | LABEL                                    | DESCRIPTION  |
|---|-------|--|--|
| R31 (1Fh)<br>Comparator<br>Interrupt Status         | 15    | EXT_USB_FB_EINT                          | USB_FB changed interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 14    | EXT_WALL_FB_EINT                         | WALL_FB changed interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.  |
|   | 13    | EXT_BATT_FB_EINT                         | BATT_FB changed interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.  |
| R39 (27h)<br>Comparator<br>Interrupt Status<br>Mask | 15:13 | "IM_" + name of respective bit<br>in R31 | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br>Each bit in R39 enables or masks the<br>corresponding bit in R31. The default<br>value for these bits is 0 (unmasked). |

Table 103 External Interrupts

## 17.6 BACKUP POWER

A backup power source should be provided for the WM8350 on the VRTC pin. This can be a small rechargeable battery or a high-capacitance capacitor (supercap). The purpose of this component is to power the always-on functions such as the on-chip crystal oscillator, RTC and ALARM control registers and UVLO comparator. As these circuit blocks store settings required for start-up, it is desirable that they continue to operate even when no other power source is available.

The VRTC battery (or capacitor) maintains its charge from the Wall (LINE), USB or BATT sources. The connection is illustrated in Figure 75. The series resistor limits the VRTC charge current. The 1 $\mu$ F capacitor is recommended also for stability; if this capacitor is too small or is not present, the VRTC output may oscillate and cause a system reset.

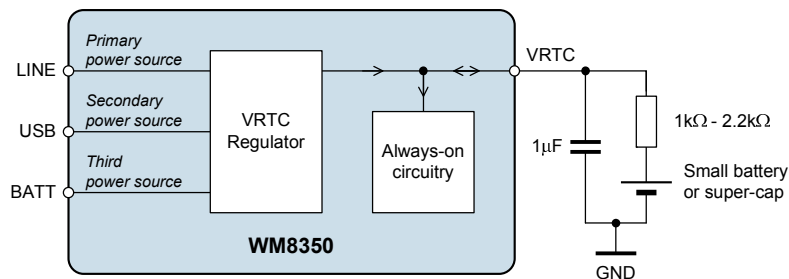


Figure 75 Backup Power

Note that, if the main battery is not present or is heavily discharged, and the WM8350 enters BACKUP mode from Wall or USB power, then leakage may occur between VRTC and LINE. This will cause the Backup Power source to be drained more quickly, and reduce the time for which the WM8350 can maintain the RTC.

The leakage occurs via the switched-VRTC connection (SWVRTC) and the AUX1 pin; a resistor is normally connected between these pins as part of the battery temperature detection circuit, as illustrated in Section 17.7.1. The leakage does not occur if the WM8350 enters BACKUP mode from Battery power, because the switched-VRTC output is not enabled in this case.

If no main battery is present in the system, then the SWVRTC pin should be left floating; this will prevent any leakage in BACKUP mode.

If the application supports the connection of a main battery, then it is important to select a battery pack where the NTC resistance is around 100k $\Omega$  at 25°C. This will limit the leakage current to a maximum of 23 $\mu$ A in BACKUP mode. Battery packs with lower NTC resistance are not recommended as the leakage current in BACKUP will be higher.

If no backup battery is present in the system, then the leakage current is of no importance, as the BACKUP state is not supported.

## 17.7 BATTERY CHARGER

### 17.7.1 GENERAL DESCRIPTION

The WM8350 incorporates a battery charger which is designed for single-cell lithium batteries. The battery charger can operate from either the Wall (LINE) or USB power sources. Trickle charging at 50mA is enabled by default. The battery charger configuration and termination can run without any intervention required by the host processor.

The battery charger voltage and currents are programmable. Trickle charging at either 50mA or 100mA is supported; fast charging from 50mA up to 750mA is possible under certain conditions. Note that charging from the USB power is subject to the 100mA or 500mA overall limit on the USB source (see Section 17.4).

Battery pack temperature sensing is enabled by default. The connection to the battery's NTC resistor is made using the SWVRTC pin and the AUX1 pin, as illustrated in Figure 76. The SWVRTC pin is a reference source controlled by the WM8350. The AUX1 pin (also an input to the AUXADC) is used as the input to the temperature sensing circuit. Note that the absence of the NTC connection will lead to a temperature failure condition being detected and battery charging will not be possible.

Typical connections for the WM8350 battery charger are illustrated in Figure 76. The resistor value between SWVRTC and AUX1 should be selected to match the NTC. A typical value is 100k $\Omega$ .

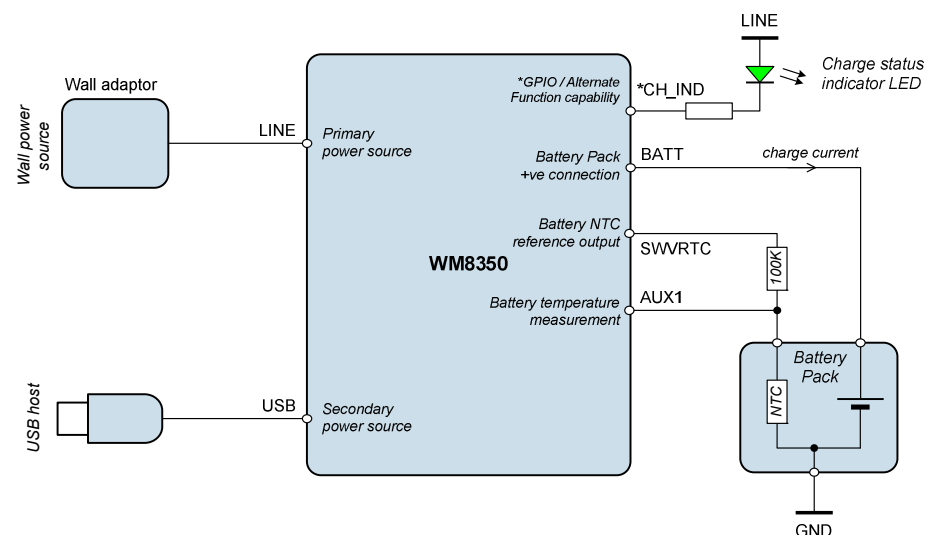


Figure 76 Typical Connections for WM8350 Battery Charger

The WM8350 monitors the battery status via the AUX1 pin and by voltage/current sensing on other pins. See Section 17.7.7 for details of the battery fault conditions and reporting.

If the application is intended to run without a battery present, then it is recommended that a 3.3 $\mu$ F capacitor be placed on the BATT pin to ensure correct charger behaviour. Also, the SWRTC pin should be left floating, to avoid leakage in BACKUP mode as described in Section 17.6. The Battery Charger interrupts should also be masked, as these will be invalid - see Section 17.7.8 for details of the Battery Charger Interrupts. It is recommended that the Battery Charger also be disabled in this case - note that the Battery Charger is enabled by default, including on entry to the OFF power state.

A typical battery charge cycle is illustrated in Figure 77. This shows both the trickle charge and fast charge processes.

The trickle charge mode is a constant current mode. Trickle charging is enabled when the battery voltage falls below a charging threshold voltage; it is disabled when the charge current falls to a programmable 'End of Charge' threshold level.

Fast charging consists of two phases:

In the constant current phase, the WM8350 drives a programmable constant current into the battery through the BATT pin. During this phase, the battery voltage rises monotonically until the battery reaches the target voltage.

When the battery reaches the target voltage, the charger enters the constant voltage phase, in which the WM8350 regulates BATT to the target voltage. To achieve this, the WM8350 adjusts the charge current adaptively. The charge current decreases monotonically over time. Fast charging is disabled when the current falls to a programmable 'End of Charge' threshold level.

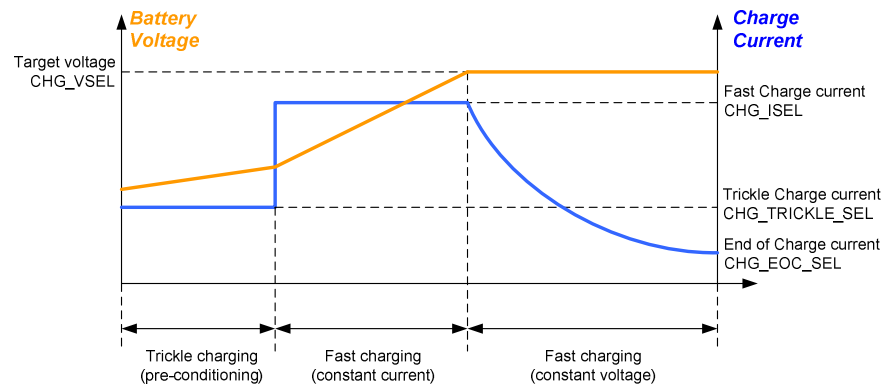


Figure 77 A Typical Charge Cycle

### 17.7.2 BATTERY CHARGER ENABLE

The battery charger is enabled by default when the WM8350 is in the ACTIVE, HIBERNATE or OFF states. Note that battery charging is only possible when the selected power source is within normal operating limits (see Section 7.5) and is more than 100mV higher than the battery voltage.

The battery charger can be disabled by setting the CHG\_ENA register bit to '0'. When the battery charger is enabled, it autonomously checks if the conditions for charging are fulfilled and controls the charging processes accordingly. The status of the battery charger can be read from the CHG\_ACTIVE register bit. (Note this bit is read-only.)

The battery charger can be paused by writing to the CHG\_PAUSE register bit. This provides a simple option to halt the battery charger and to subsequently restart it without affecting the charge timer or other settings.



The battery charger target voltage is set by the CHG\_VSEL field, as defined in Table 104.

| ADDRESS   | BIT | LABEL          | DEFAULT | DESCRIPTION  |
|---|-----|----------------|---------|--|
| R12 (0Ch)<br>Power Mgmt<br>(5)  | 9   | CHG_ENA        | 1       | CHG_ENA bit selects battery charger current control<br>0 = Set battery charger current to zero<br>1 = Enable battery charge control<br><i>Protected by security key.</i>                               |
| R168 (A8h)<br>Battery charger control 1   | 15  |                |         |  |
| R169 (A9h)<br>Battery charger control 2   | 15  | CHG_ACTIVE     | 0       | Charger Status.<br>0 = Battery Charging is inactive<br>1 = Battery Charging is active<br>(Note CHG_ENA is just a request; the WM8350 determines if the conditions are satisfied for Battery Charging). |
|   | 14  | CHG_PAUSE      | 0       | Charger pause:<br>0 = Don't pause the charger<br>1 = Pause charging  |
|   | 5:4 | CHG_VSEL [1:0] | 00      | Battery charge voltage:<br>00 = 4.05V<br>01 = 4.1V<br>10 = 4.15V<br>11 = 4.2V  |
| <b>Note:</b> CHG_ENA can be accessed through R9 or through R168. Reading from or writing to either register location has the same effect. |     |                |         |  |

**Table 104 Battery Charger Control**

### 17.7.3 TRICKLE CHARGING

Trickle charging is enabled by default when the Wall (LINE) or USB pins are selected as the power source. It is autonomously initiated, supervised and terminated by the WM8350, without requiring any intervention by the host processor.

By default, trickle charging is initiated when the battery voltage is below the battery charge voltage CHG\_VSEL by more than 100mV. Setting the CHG\_FRC bit allows trickle charging to be initiated at higher battery voltages.

The trickle charge current is set by the CHG\_TRICKLE\_SEL field, as described in Table 105.

A choke circuit is provided to enhance the trickle charge current control. This allows the charge current to be modified according to temperature conditions or according to the USB current limit restrictions.

If the WM8350 temperature is above 115°C and trickle charge temperature choking is enabled, then charging is interrupted for at least 8 seconds and until the temperature has fallen below the threshold. If trickle charge temperature choking is not enabled, then charging continues. (Note that the device shutdown temperature is set at 140°C - this threshold cannot be disabled.) Trickle charge temperature choking is controlled by the CHG\_TRICKLE\_TEMP\_CHOKE register bit.

If the USB current limit cannot support the charge current demanded by CHG\_TRICKLE\_SEL and USB current choking is enabled, then the charge current will be modified, where possible, in order to continue charging. The trickle charge current cannot be controlled dynamically - the only possible charge currents are 50mA or 100mA. Therefore, the only form of USB choking in trickle charge mode is for a demanded current of 100mA to be reduced to 50mA. Trickle charge USB current choking is controlled by the CHG\_TRICKLE\_USB\_CHOKE register bit. The time constant for the charger's attempts to increase the current after USB choking can be controlled by CHG\_RECOVERY\_T.

The register control fields for Trickle Charging are described in Table 105. See Section 17.7.5 for details of battery charger termination.

| ADDRESS                                 | BIT | LABEL                  | DEFAULT | DESCRIPTION   |
|---|-----|------------------------|---------|---|
| R168 (A8h)<br>Battery charger control 1 | 9   | CHG_TRICKLE_TEMP_CHOKE | 0       | Enable trickle charge temperature choking<br>0 = disable<br>1 = enable<br><i>Protected by security key.</i>   |
|   | 8   | CHG_TRICKLE_USB_CHOKE  | 0       | Enable USB current choking in trickle charge<br>0 = disable<br>1 = enable<br><i>Protected by security key.</i>  |
|   | 7   | CHG_RECOVER_T          | 0       | Time constant adjust for charger choke recovery (step-up):<br>0 = Step-up time constant is 180us (allows faster recovery between processor wakeups)<br>1 = Step-up time constant is >20ms (outside audio band)<br><i>Protected by security key.</i> |
| R169 (A9h)<br>Battery charger control 2 | 6   | CHG_TRICKLE_SEL        | 0       | Selects the trickle charge current.<br>0 = Set the trickle charge current to 50mA.<br>1 = Set the trickle charge current to 100mA.<br><i>Protected by security key.</i>   |
| R170 (AAh)<br>Battery charger control 3 | 7   | CHG_FRC                | 0       | Allows trickle-charging to be forced even if the battery voltage is above the default threshold<br>0 = only trickle-charge if the battery voltage is below CHG_VSEL - 100mV<br>1 = always trickle-charge<br><i>Protected by security key.</i>       |

**Table 105 Trickle Charging Control**

#### 17.7.4 FAST CHARGING

Fast charging provides a faster way to charge the battery. This is only possible under certain conditions. Fast charging must be initiated by the system controller, and can never start autonomously.

Fast charging is normally possible in the ACTIVE state when the selected power source is Wall (LINE) or when USB high power mode is selected. The battery charger determines whether the conditions for fast charging are satisfied; these conditions include a suitable selected power source voltage (see Section 17.7.2) and a suitable battery voltage (greater than 3.1V).

If the conditions for fast charging are satisfied, this is indicated by the WM8350 setting the CHG\_FAST\_RDY\_EINT register bit, as described in Table 106. Providing that the conditions for fast charging are satisfied, then fast charging is enabled by setting the CHG\_FAST bit. If the conditions are not satisfied, then CHG\_FAST will be held at 0.

The maximum fast charge current is set by the CHG\_ISEL register field, as described in Table 106. During fast charging, the current may be dynamically controlled by the WM8350 in order to achieve optimum battery charging. It is recommended that the charge current limit should not be set higher than 400mA when charging from a USB power rail.

A throttle circuit is provided to enhance the fast charge current control. This allows the charge current to be modified according to temperature conditions or according to the USB current limit restrictions.

If the WM8350 temperature is above 115°C, then charging is interrupted for at least 8 seconds and until the temperature has fallen below the threshold. Temperature control of the battery charger is always enabled during Fast Charging.

If the USB current limit is reached during Fast Charging, then the charge current must be reduced. If USB current throttling is enabled, then the charge current will be controlled dynamically in order to continue charging. If USB current throttling is not enabled, then the charging will be terminated. (Note that this may give rise to an erroneous indication of 'End of Charge' as the charging may have terminated prematurely.) If USB current throttling is enabled, then 'End of Charge' will not be indicated, even if the throttle circuit causes the charger current to fall below the End of Charge current threshold. Fast charge USB current throttling is controlled by the CHG\_FAST\_USB\_THROTTLE register bit. The time constant for the charger's attempts to increase the current after USB throttling can be controlled by CHG\_THROTTLE\_T.

The WM8350 will revert to Trickle charging if the conditions for fast charging are no longer satisfied. This includes selection of the OFF or HIBERNATE states, or selection of USB low power mode. The WM8350 will also revert to Trickle charging if it detects a low battery voltage condition (see Section 17.7.8).

The register control fields for Fast Charging are described in Table 106. See Section 17.7.5 for details of battery charger termination.

| ADDRESS                                       | BIT | LABEL                         | DEFAULT | DESCRIPTION   |
|---|-----|-------------------------------|---------|---|
| R25 (15h)<br>Interrupt Status<br>1            | 9   | CHG_FAST_R<br>DY_EINT         | 0       | Indicates that the charger is ready to go into fast charge.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
| R168 (A8h)<br>Battery charger<br>control 1    | 5   | CHG_FAST                      | 0       | Enable fast charging.<br>0 = Fast charging cannot take place.<br>1 = Enable fast charging (will not start until valid charging conditions are met).<br>Note: This register is held low and can only be written to once the fast charge ready signal has gone high.<br><i>Protected by security key.</i> |
|   | 4   | CHG_FAST_U<br>SB_THROTTL<br>E | 0       | Enable USB current throttling in fast charge:<br>0 = Don't do any current throttling when fast charging.<br>1 = Do current throttle while fast charging.<br><i>Protected by security key.</i>   |
| R169 (A9h)<br>Battery charger<br>control 2    | 3:0 | CHG_ISEL<br>[3:0]             | 0110    | Fast charge current limit setting.<br>0000 = off<br>0001 = 50mA<br>0010 = 100mA<br>... (50mA steps)<br>1111 = 750mA<br>Note: Do not set the charger to be more than 400mA when USB powered.<br><i>Protected by security key.</i>  |
| R170 (AAh)<br>Battery<br>Charger<br>Control 3 | 6:5 | CHG_THROTT<br>LE_T [1:0]      | 00      | Time between steps when the charger throttles back due to USB current limit.<br>00 = 8us<br>01 = 16us<br>10 = 32us<br>11 = 128us<br><i>Protected by security key.</i>   |

**Table 106 Fast Charging Control**

### 17.7.5 BATTERY CHARGER TIMEOUT AND TERMINATION

Fast charging and Trickle charging is terminated under any of the following conditions:

- Charge current falls below a programmable threshold
- Charger timeout
- Charger fault condition (see Section 17.7.7)

The End of Charge Current threshold can be set between 20mA and 90mA, using the CHG\_EOC\_SEL register field, as defined in Table 107. Care should be taken to ensure that the End of Charge Threshold is lower than the selected Charge Current Limit (CHG\_ISEL and/or CHG\_TRICKLE\_SEL).

When the End of Charge Current threshold is reached, the CHG\_END\_EINT interrupt field is set (see Section 17.7.8). The action taken when the End of Charge Current threshold occurs is set by CHG\_END\_ACT. The battery charging will either be terminated or will continue until timeout.

When Trickle charge choking or Fast charge throttling is enabled, it is possible that these circuits may cause the charge current to be reduced below the CHG\_EOC\_SEL threshold even though the battery is not fully charged. When choke or throttle control is enabled, the End of Charge detection described above is disabled, and charging always continues until timeout. It is recommended that Trickle charge choking and Fast charge throttling is enabled.

The WM8350 battery charger has a programmable timer. The timer is initiated when either fast charging or trickle charging commences. The initial value of the timer may be set by writing to the CHG\_TIME register field. This field can also be read back as an indicator of the charge time remaining. Note that the readback value of this field is coded differently to the write value. Due to the limited resolution provided by the 4-bit field, the readback value is approximate only, to an accuracy of around 30 minutes.

If charging is paused by setting CHG\_PAUSE (see Table 104), or is paused due to temperature or maximum current conditions, the charge timer is halted so that the time limit is extended accordingly.

If the charging mode is changed by asserting or de-asserting CHG\_FAST, then the timer is reset to its initial value.

If the charging mode reverts to Trickle charge mode as a result of a change in power source or a change in USB power mode, then the timer is not reset, but continues to count down from its earlier value. (Note that the charger will never autonomously switch from Trickle charge mode to Fast charge mode.)

When the Charger Timer completes, the CHG\_TO\_EINT interrupt field is set (see Section 17.7.8) and charging is terminated.

| ADDRESS                                 | BIT   | LABEL             | DEFAULT | DESCRIPTION   |
|---|-------|-------------------|---------|---|
| R168 (A8h)<br>Battery charger control 1 | 12:10 | CHG_EOC_SEL [1:0] | 000     | Selects what the end of charge current should be set to<br>000 = 20mA<br>001 = 30mA<br>(10mA steps)<br>...<br>111 = 90mA<br><i>Protected by security key.</i> |
|   | 6     | CHG_END_ACT       | 0       | Action to take when charging ends:<br>0 = Set charge current to 0<br>1 = Do nothing (leave charger on till timeout)<br><i>Protected by security key</i>       |

| ADDRESS                                 | BIT  | LABEL          | DEFAULT | DESCRIPTION   |
|---|------|----------------|---------|---|
| R169 (A9h)<br>Battery charger control 2 | 11:8 | CHG_TIME [3:0] | 1011    | Writing to this field sets the charge timeout duration:<br>0000 = 60min<br>0001 = 90min<br>0010 = 120min<br>0011 = 150min<br>0100 = 180min<br>0101 = 210min<br>0110 = 240min<br>0111 = 270min<br>1000 = 300min<br>1001 = 330min<br>1010 = 360min<br>1011 = 390min<br>1100 = 420min<br>1101 = 450min<br>1110 = 480min<br>1111 = 510min<br>Reading from this field indicates the charge time remaining:<br>Time remaining = CHG_TIME * 2048s<br><i>Protected by security key.</i> |

Table 107 Battery Charger Termination

### 17.7.6 BATTERY CHARGER STATUS

The status of the Battery Charger can be read from the CHG\_STS register field, as described in Table 108. This field indicates whether the charger is active in trickle or fast charge modes.

| ADDRESS                                 | BIT   | LABEL         | DEFAULT | DESCRIPTION  |
|---|-------|---------------|---------|--|
| R169 (A9h)<br>Battery charger control 2 | 13:12 | CHG_STS [1:0] | 00      | Charger status:<br>00 = Charger off, current set to 0.<br>01 = In trickle charge mode.<br>10 = In fast charge mode.<br>11 - Reserved |

Table 108 Battery Charger Status

In addition to the CHG\_STS register readback, the charger status can be indicated on an LED connected to a GPIO pin configured as CH\_IND (see Section 20). The CH\_IND function is an open-drain LED output that provides a visible indication of the charger status.

| CHARGER STATUS              | CH_IND ACTION             |
|-----------------------------|---------------------------|
| Charger current set to zero | LED off                   |
| Trickle charging            | LED blinks slowly (0.5Hz) |
| Fast charging               | LED blinks quickly (1Hz)  |

Table 109 Battery Charger Status via CH\_IND

### 17.7.7 BATTERY FAULT CONDITIONS

The WM8350 continuously monitors battery temperature, chip temperature and battery voltage. In case of a fault condition, it autonomously takes appropriate action, and alerts the host processor via the applicable interrupt flags.

#### Battery Temperature Monitoring

The WM8350 can monitor the battery temperature via the NTC (negative temperature coefficient) resistor which is incorporated into suitable battery packs. The NTC resistor must be connected to the AUX1 pin as shown in Section 17.7.1. Typical NTC resistor values vary over a range of temperature (source of information is Vishay Dale's "R-T Curve 2").

The NTC monitoring circuit is designed to detect temperature conditions outside the typical 0°C and 45°C safe battery charging conditions. The WM8350 indicates a cold battery temperature condition is indicated by setting the CHG\_BATT\_COLD\_EINT interrupt. A hot battery temperature is indicated by setting the CHG\_BATT\_HOT\_EINT interrupt. Battery charging is suspended when either of these conditions is set. (Note that trickle charging will resume once the battery temperature has returned to within normal levels.)

It is possible to disable the NTC detection circuit and associated flags. This option is protected by a security key. The associated register bits are described in Table 110.

Safety warning - The battery temperature sensor is a safety mechanism and it is strongly recommended that it be used, as directed, in all applications requiring charger functionality. Disabling this feature by any means, intentional or otherwise, could result in incorrect behaviour of the battery charger function.

| ADDRESS   | BIT | LABEL                 | DEFAULT | DESCRIPTION  |
|---|-----|-----------------------|---------|--|
| R168 (A8h)<br>Battery<br>Charger<br>Control 1   | 3   | CHG_NTC_M<br>ON       | 1       | Enable charger battery NTC detection (some batteries may not need this - turn off with caution)<br>0 = Charger ignores NO_NTC detection.<br>1 = Charger monitors NO_NTC detection.<br><i>Protected by user key, read-only in ROM configs.</i>                                      |
|   | 2   | CHG_BATT_H<br>OT_MON  | 1       | Enable charger battery temperature high detection (some batteries may not need this - turn off with caution)<br>0 = Charger ignores battery temperature too high.<br>1 = Charger monitors battery temperature too high.<br><i>Protected by user key, read-only in ROM configs.</i> |
|   | 1   | CHG_BATT_C<br>OLD_MON | 1       | Enable charger battery temperature low detection (some batteries may not need this - turn off with caution)<br>0 = Charger ignores battery temperature low.<br>1 = Charger monitors battery temperature low.<br><i>Protected by user key, read-only in ROM configs.</i>            |
| <b>Note:</b> Some batteries may not require battery temperature monitoring. Disable with caution. |     |                       |         |  |

**Table 110 Battery Temperature Monitoring**

### Chip Temperature Monitoring

The WM8350 has a built-in temperature sensor to monitor the silicon die temperature. If the chip temperature reaches the thermal warning level, the WM8350 sets the SYS\_CHIP\_GT115\_EINT (see Section 25) and Battery Charger operation may be paused (this is programmable in Trickle Charge mode). The charger operation will resume once the chip temperature has dropped below the thermal warning level.

If the chip temperature reaches the thermal shutdown level, the WM8350 sets the SYS\_CHIP\_GT140\_EINT interrupt and shuts down. (Battery charging is always terminated in this case.)

### Battery Voltage Detection / Defective Battery Detection

A low battery voltage is an indicator that the battery may be defective or removed.

In trickle charge mode, the battery voltage is checked after 30 minutes of charging, or after a quarter of the charging time CHG\_TIME (the larger of these two times applies). If the battery voltage is less than the defective battery threshold (nominal value 2.85V) at this time, then the battery charging stops and the WM8350 sets the CHG\_BATT\_FAIL\_EINT interrupt as defined in Table 111.

The battery failure condition is cleared if the battery voltage rises above the defective battery threshold. It is also cleared if any of the WM8350 power sources (including BATT) is removed and re-applied, or if the host processor invokes USB Suspend mode. When the failure condition is cleared, the charger then reverts back to its initial state, and may re-start if the conditions for charging are fulfilled (see Section 17.7.2).

If fast charging mode is selected, and the battery voltage is less than the defective battery threshold, then the WM8350 immediately reverts to trickle charging. If the fault persists, then trickle charging stops as described above.



### 17.7.8 INTERRUPTS AND FAULT PROTECTION

The battery charger can raise a first-level interrupt, CHG\_INT (see Section 24) to report status and fault conditions to the host processor. The CHG\_INT interrupt is the logical OR of all the second-level interrupts described in Table 111.

Note: If a battery is connected to the BATT pin, but the WM8350 is being powered from the Wall or USB supplies, then disconnection of the Wall or USB supply will cause the CHG\_VBATT\_LT\_3P1\_EINT and CHG\_VBATT\_LT\_2P85\_EINT interrupts to be set.

The CHG\_VBATT\_LT\_3P1\_EINT and CHG\_VBATT\_LT\_2P85\_EINT interrupts can be masked by setting the associated mask bits defined in Table 111.

Alternatively, the EXT\_USB\_FB\_EINT and/or EXT\_WALL\_FB\_EINT interrupts (see Section 17.5) can be used to validate the Battery Undervoltage interrupts - if one of the External Feedback interrupts is set at the same time as the Battery Undervoltage interrupts, then the Battery Undervoltage interrupts should be ignored.

| ADDRESS                                    | BIT                    | LABEL  | DESCRIPTION  |
|--|------------------------|--|--|
| R25 (19h)<br>Interrupt<br>Status 1         | 15                     | CHG_BATT_HOT_EINT  | Battery temp too hot.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|  | 14                     | CHG_BATT_COLD_EINT   | Battery temp too cold.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
|  | 13                     | CHG_BATT_FAIL_EINT   | Battery fail.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|  | 12                     | CHG_TO_EINT  | Charger timeout.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
|  | 11                     | CHG_END_EINT   | Charging final stage.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|  | 10                     | CHG_START_EINT   | Charging started.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|  | 9                      | CHG_FAST_RDY_EINT  | Indicates that the charger is ready to go into fast charge.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|  | 2                      | CHG_VBATT_LT_3P9_EINT  | Battery Voltage < 3.9 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
|  | 1                      | CHG_VBATT_LT_3P1_EINT  | Battery voltage < 3.1 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
| 0  | CHG_VBATT_LT_2P85_EINT | Battery voltage < 2.85 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |  |
| R33 (21h)<br>Interrupt<br>Status 1<br>mask | 15:0                   | "IM_" + name of respective bit in R25 (19h)  | Mask bits for battery charger interrupts<br>Each of these bits masks the respective bit in R25 when it is set to 1 (e.g. CHG_FAST_RDY in R25 does not trigger a CHG_INT interrupt when IM_CHG_FAST_RDY in R33 is set). |

Table 111 Battery Charger Interrupts

## 18 SYSTEM MONITORING AND UNDERVOLTAGE LOCKOUT (UVLO)

The WM8350 includes several mechanisms to prevent the system from starting up, or force it to shut down, when power sources are critically low.

The under-voltage lockout (UVLO) is a non-programmable voltage limit. When the available supplies are below this limit, the WM8350 enters the BACKUP state. The WM8350 can only proceed from BACKUP to the OFF state if LINE is above the UVLO level. Whenever the WM8350 is in ACTIVE, HIBERNATE or OFF state and LINE falls below the UVLO level, the WM8350 returns to the BACKUP state.

The UVLO limit threshold is equal to  $V_{RTC} + 50\text{mV}$ . The precise value of  $V_{RTC}$  may vary between devices, within the limits defined in the Electrical Characteristics (see Section 7.5).

The startup threshold is a programmable voltage limit. The WM8350 can only proceed from OFF to the ACTIVE state if LINE is above the startup threshold. (Note that, in the case of USB-powered operation, there are additional requirements; see Section 17.4). The startup threshold is determined by the PCCMP\_ON\_THR register field.

The shutdown threshold is determined by the PCCMP\_OFF\_THR register field. When LINE falls below this threshold, the WM8350 raises a SYS\_HYST\_COMP\_FAIL\_EINT interrupt. In addition, the WM8350 takes the action set by PCCOMP\_ERRACT. If this bit is set, then the WM8350 will shut down in response to the LINE voltage falling below the shutdown threshold.

The startup and shutdown control register fields are described in Table 112. Note that the startup threshold should always be set higher than the shutdown threshold in order to create a hysteresis, making the system more stable.

The SYS\_HYST\_COMP\_FAIL\_EINT interrupt is one of the second-level interrupts which triggers a first-level System Interrupt, SYS\_INT (see Section 24). This can be masked by setting the mask bit as described in Table 113.

| ADDRESS                                 | BIT | LABEL               | DEFAULT | DESCRIPTION  |
|---|-----|---------------------|---------|--|
| R179 (B3h)<br>Power Check<br>Comparator | 14  | PCCMP_ERRACT        | 0       | Action to take when LINE falls below PCCMP_OFF_THR level (as well as generating an interrupt)<br>0 = ignore<br>1 = shut down system          |
|   | 6:4 | PCCMP_OFF_THR [2:0] | 010     | Power check comparator system shutdown threshold value<br>000 = 2.9V<br>001 = 3.0V<br>...<br>111 = 3.6V<br><i>Protected by security key.</i> |
|   | 2:0 | PCCMP_ON_THR [2:0]  | 101     | Power check comparator system startup threshold value<br>000 = 2.9V<br>001 = 3.0V<br>...<br>111 = 3.6V<br><i>Protected by security key.</i>  |

Table 112 Battery Monitoring and UVLO Control

| ADDRESS                                    | BIT | LABEL                      | DESCRIPTION  |
|--|-----|----------------------------|--|
| R26 (1Ah)<br>Interrupt<br>Status 2         | 3   | SYS_HYST_COMP_FAIL_EINT    | Hysteresis comparator indication that LINE or BATT is less than shutdown threshold.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
| R34 (22h)<br>Interrupt<br>Status 2<br>Mask | 3   | IM_SYS_HYST_COMP_FAIL_EINT | Mask bit for Hysteresis comparator interrupt<br>When set to 1, IM_SYS_HYST_COMP_FAIL_EINT masks SYS_HYST_COMP_FAIL_EINT in R29 and does not trigger an SYS_INT interrupt when SYS_HYST_COMP_FAIL_EINT is set). |

Table 113 Battery Monitoring and UVLO Interrupts

## 19 AUXILIARY ADC

### 19.1 GENERAL DESCRIPTION

The WM8350 incorporates a low-power 12-bit Auxiliary ADC (AUXADC). This can be used to measure a number of internal or external voltages, with either VREF or VRTC as its reference. A programmable potential divider enables the AUXADC to measure voltages higher than the reference.

Note that the AUX1 pin is also the input for the battery pack temperature monitoring circuit and is therefore not freely available for other analogue inputs. The battery NTC input can still be sampled and readback via AUX1 in the same way as the other AUXADC inputs. The AUX1 pin may be used for other purposes if the NTC detection is disabled and/or the associated Battery Charger interrupts are masked. See Section 17.7 for details of the battery pack NTC functions.

The AUXADC circuit is illustrated in Figure 78.

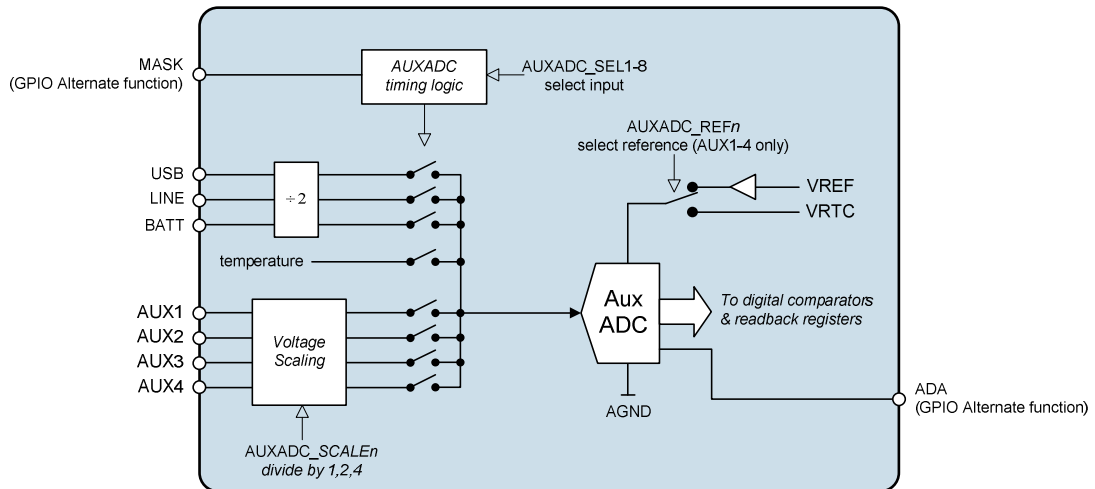


Figure 78 Auxiliary ADC

The AUXADC is enabled using the AUXADC\_ENA register bit as described in Table 114.

| ADDRESS   | BIT | LABEL      | DEFAULT | DESCRIPTION                                   |
|---|-----|------------|---------|---|
| R12 (0Ch) Power Mgmt (5)  | 7   | AUXADC_ENA | 0       | AUXADC control<br>0 = disabled<br>1 = enabled |
| R144 (90h) Digitizer Control (1)  | 15  |            |         |   |
| <b>Note:</b> AUXADC_ENA can be accessed through R12 or through R144. Reading from or writing to either register location has the same effect. |     |            |         |   |

Table 114 AUXADC Enable

## 19.2 INITIATING AUXADC MEASUREMENTS

The AUXADC can measure voltages on four external pins, AUX1, AUX2, AUX3 and AUX4. It can also measure voltages on the USB, LINE and BATT pins, and also the temperature sensor level. Each of these 8 inputs can be independently selected or deselected as an AUXADC input. Whenever the AUXADC is triggered, the AUXADC performs a measurement of each of the selected AUXADC inputs. By default, none of the AUXADC inputs is selected. Therefore, the required inputs must be enabled using the AUXADC\_SEL $n$  bits prior to initiating an AUXADC measurement.

AUXADC measurements can be scheduled in a number of different ways, as determined by the AUXADC\_CTC register bit. In Polling Mode, a set of measurements is initiated by writing a logic '1' to the AUXADC\_POLL bit. (This bit is then automatically reset once the measurements have been completed.) In Continuous Mode, the WM8350 initiates a set of measurements at a time interval that is determined by the AUXADC\_CRATE field.

Additional control can be provided using a GPIO pin configured as a 'MASK' input (see Section 20). The behaviour of the MASK input is selected using the AUXADC\_MASKMODE register field - it can be used to inhibit any measurements triggered by the Polling or Continuous modes, or else it can be used as a hardware input to initiate a set of measurements.

Note that, when AUXADC\_MASKMODE = 11, then AUXADC\_CTC, AUXADC\_POLL and AUXADC\_CRATE have no effect. The polarity of the MASK input can be adjusted to be active high or active low using the GP $n$ \_CFG bits defined in Section 20, where 'n' identifies the particular GPIO pin in use.

The control fields associated with initiating AUXADC measurements are defined in Table 115.

| ADDRESS                                | BIT         | LABEL       | DEFAULT   | DESCRIPTION   |
|--|-------------|-------------|---|---|
| R144 (90h)<br>Digitiser Control<br>(1) | 14          | AUXADC_CTC  | 0   | Continuous conversion mode:<br>0 = Polling mode<br>1 = Continuous mode  |
|  | 13          | AUXADC_POLL | 0   | Writing "1" initiates a set of measurements in polling mode (AUXADC_CTC=0). This bit is automatically reset after the measurements are completed. |
|  | 7           | AUXADC_SEL8 | 0   | AUXADC TEMP input select<br>0 = Disable TEMP measurement<br>1 = Enable TEMP measurement   |
|  | 6           | AUXADC_SEL7 | 0   | AUXADC BATT input select<br>0 = Disable BATT measurement<br>1 = Enable BATT measurement   |
|  | 5           | AUXADC_SEL6 | 0   | AUXADC LINE input select<br>0 = Disable LINE measurement<br>1 = Enable LINE measurement   |
|  | 4           | AUXADC_SEL5 | 0   | AUXADC USB input select<br>0 = Disable USB measurement<br>1 = Enable USB measurement  |
|  | 3           | AUXADC_SEL4 | 0   | AUXADC AUX4 input select<br>0 = Disable AUX4 measurement<br>1 = Enable AUX4 measurement   |
|  | 2           | AUXADC_SEL3 | 0   | AUXADC AUX3 input select<br>0 = Disable AUX3 measurement<br>1 = Enable AUX3 measurement   |
|  | 1           | AUXADC_SEL2 | 0   | AUXADC AUX2 input select<br>0 = Disable AUX2 measurement<br>1 = Enable AUX2 measurement   |
| 0                                      | AUXADC_SEL1 | 0           | AUXADC AUX1 input select<br>0 = Disable AUX1 measurement<br>1 = Enable AUX1 measurement |   |

| ADDRESS                                | BIT   | LABEL                     | DEFAULT | DESCRIPTION   |
|--|-------|---------------------------|---------|---|
| R145 (91h)<br>Digitiser Control<br>(2) | 13:12 | AUXADC_MASK<br>MODE [1:0] | 00      | AUXADC MASK input control<br>00 = MASK is ignored<br>01 = When MASK is asserted, all<br>AUXADC measurements are<br>inhibited.<br>10 = Reserved<br>11 = MASK input initiates AUXADC<br>measurements. AUXADC_POLL<br>and AUXADC_CTC have no effect.<br>MASK polarity is controlled by<br>GPn_CFG. |
|  | 10:8  | AUXADC_CRAT<br>E [2:0]    | 000     | AUXADC measurement frequency<br>in Continuous mode<br>000 = 1Hz<br>001 = 4Hz<br>010 = 8Hz<br>011 = 16Hz<br>100 = 32Hz<br>101 = 64Hz<br>110 = 128Hz<br>111 = 256Hz   |

**Table 115 Initiating AUXADC Measurements**

In Polling mode, setting AUXADC\_POLL = 1 initiates one set of measurements, after which the AUXADC waits for a new trigger.

In Continuous mode, a set of measurements will be initiated at the frequency set by AUXADC\_CRATE.

When using MASK to initiate measurements (AUXADC\_MASKMODE=11), a rising edge (if GPn\_CFG = 1) or a falling edge (if GPn\_CFG = 0) initiates one set of AUXADC measurements. The MASK signal must be asserted for long enough for the AUXADC to perform all the selected measurements.

The AUXADC\_SELn bits should not be changed until all previous measurement results stored in the AUXn readback registers have been read.

### 19.3 VOLTAGE SCALING AND REFERENCES

For inputs AUX1, AUX2, AUX3 and AUX4, the AUXADC measurements may be referenced to either VRTC or VREF (see Section 21). The selected reference can be selected independently for each input, using the control fields described in Table 116. In the case of USB, BATT, LINE and Temperature, the AUXADC measurements are referenced to VRTC.

In the case of AUXADC measurements which are referenced to VREF, a buffered copy of VREF is used as an input to the AUXADC. Setting the AUXADC\_RBMODE field allows this buffer to be enabled at all times when the AUXADC is enabled, or else to only be enabled when a VREF-referenced measurement is made.

In order to measure voltages that may be higher than VRTC or VREF, a programmable divider is provided on each of AUX1, AUX2, AUX3 and AUX4. These are controlled using the AUXADC\_SCALE $n$  bits, allowing the inputs to be divided by 1, 2 or 4. In the case of USB, BATT and LINE, a fixed 'divide by 2' applies.

| ADDRESS                                | BIT   | LABEL                   | DEFAULT | DESCRIPTION   |
|--|-------|-------------------------|---------|---|
| R152 (98h)<br>AUX1                     | 14:13 | AUXADC_SCAL<br>En [1:0] | 11      | AUX $n$ input select<br>00 = Off<br>01 = Input divided by 1<br>10 = Input divided by 2<br>11 = Input divided by 4   |
| R153 (99h)<br>AUX2                     |       |                         |         |   |
| R154 (9Ah)<br>AUX3                     | 12    | AUXADC_REF $n$          | 1       | AUX $n$ reference select<br>0 = AUX $n$ measured relative to VRTC<br>1 = AUX $n$ measured relative to VREF  |
| R155 (9Bh)<br>AUX4                     |       |                         |         |   |
| R145 (91h)<br>Digitizer Control<br>(2) | 1     | AUXADC_RBM<br>ODE       | 1       | Enable for AUXADC bandgap (VREF) buffer.<br>0 = AUXADC REFBUF is only enabled during conversions that use the VREF as a reference<br>1 = AUXADC REFBUF is always enabled when the AUXADC is enabled |

Table 116 AUXADC Reference Selection

## 19.4 AUXADC READBACK

Measured data from the AUXADC can be accessed by reading registers R152 through to R159, as defined in Table 117. This data may be read at any time, or may be read in response to the WM8350 indicating that new data is available.

The WM8350 indicates that new AUXADC data is available by setting the AUX\_DATARDY\_EINT interrupt flag as described in Section 19.7. This is one of five second-level interrupts which triggers a first-level System Interrupt, AUXADC\_INT (see Section 24). This interrupt can be masked by setting the mask bit as described in Table 120. The AUX\_DATARDY\_EINT interrupt is set high when new data is available. It is reset when the associated interrupt register R26 is read.

The WM8350 can also indicate that new AUXADC data is available via a GPIO pin configured as ADA (Aux Data Available). This flag is set high when new data is available. It is reset when the associated data has been read from the readback registers R152 through to R159. See Section 20 for details of how to configure a GPIO pin as ADA.

To avoid losing data that has not yet been read, the WM8350 can inhibit overwriting the measurement registers with new data until the previous data has been read. When the AUXADC\_WAIT bit is set, then AUXADC measurements are prevented from being overwritten until they have been read. Any Poll, Continuous or Mask-triggered AUXADC measurement will be ignored if the AUXADC\_WAIT feature prevents the measurement from being overwritten.

Always specify the address of the starting register. Single data read from last register is not supported.

Reading from registers R152 to R159 returns a 12-bit code which represents the most recent AUXADC measurement on the associated channel. This code can be equated to the actual voltage (or temperature) according to the following equations:

To calculate the voltage for external measurements on the AUX input pins use the following formula:

$$\text{AUX}_n = (\text{Output Code} / 4095) \times \text{Reference Voltage} \times \text{AUX Input Scale}$$

To calculate the voltage for internal AUXADC measurements on USB, LINE and Battery:

$$\text{USB, LINE \& BATT} = (\text{Output Code} / 4095) \times \text{VRTC} \times 2$$

To calculate the temperature (in degrees Celsius) from AUXADC measurements on TEMP:

$$\text{Temperature} = 460.32 - ((\text{Output Code} / 4095) \times \text{VRTC} \times 614.6)$$

where-

Output Code = the relevant AUXADC\_DATA field, decoded as an unsigned integer

Reference Voltage = VRTC voltage or VREF voltage, depending on AUXADC\_REF $n$

AUX Input Scale = 1, 2 or 4, depending on AUXADC\_SCALE $n$  [1:0]

In a typical application, the AUX1 input is the battery pack temperature sensing (NTC) input. The voltage at this input may be used as an indicator of the battery pack temperature.

The NTC input should be measured relative to the VRTC voltage. The hot temperature threshold (CHG\_BATT\_HOT\_EINT) corresponds to 0.33 x VRTC. This equates to approximately +45°C. The cold temperature threshold (CHG\_BATT\_COLD\_EINT) corresponds to 0.74 x VRTC. This equates to approximately 0°C.



| ADDRESS                                 | BIT  | LABEL                        | DEFAULT | DESCRIPTION  |
|---|------|------------------------------|---------|--|
| R152 (98h)<br>AUX1                      | 11:0 | AUXADC_DATA_ <i>n</i> [11:0] | 000h    | Measured AUXn data value relative to reference:<br>000 = 0V<br>FFF = measured voltage after divide matches reference   |
| R153 (99h)<br>AUX2                      |      |                              |         |  |
| R154 (9Ah)<br>AUX3                      |      |                              |         |  |
| R155 (9Bh)<br>AUX4                      |      |                              |         |  |
| R156 (9Ch)<br>USB Voltage Readback      | 11:0 | AUXADC_DATA_ USB [11:0]      | 0h      | Measured USB voltage data value.   |
| R157 (9Dh)<br>LINE Voltage Readback     | 11:0 | AUXADC_DATA_ LINE [11:0]     | 0h      | Measured LINE voltage data value   |
| R158 (9Eh)<br>BATT Voltage Readback     | 11:0 | AUXADC_DATA_ BATT [11:0]     | 0h      | Measured Battery Voltage   |
| R159 (9Fh)<br>Chip Temperature Readback | 11:0 | AUXADC_DATA_ CHIPTEMP [11:0] | 0h      | Measured Internal chip temperature   |
| R145 (91h)<br>Digitizer Control (2)     | 0    | AUXADC_WAIT                  | 0       | Whether the old data must be read before new conversions can be made<br>0 = No effect (new conversions overwrite old)<br>1 = New conversions are held back (and measurements delayed) until AUX_DATA <sub>n</sub> has been read. |

Table 117 Reading AUXADC Measurements

In a typical application, one of the following methods is likely to be used to control the AUXADC readback:

For interrupt-driven AUXADC readback, the host processor would read the AUXADC data registers in response to the AUXADC Interrupt or ADA output. In Continuous AUXADC mode, the processor should complete this action before the next measurement occurs, in order to avoid losing any AUXADC samples. In Polling mode, the interrupt (or ADA) signal provides confirmation that the commanded set of measurements has been completed.

For host-controlled AUXADC readback, the Continuous AUXADC mode would be used, and the AUXADC\_WAIT bit would be asserted. The host processor would read the AUXADC data registers periodically, causing the next AUXADC measurement to be enabled. This limits the frequency of the AUXADC measurements to the readback frequency.

## 19.5 CALIBRATION

The on-chip reference VREF provides a highly accurate reference voltage to the AUXADC. For best measurement accuracy, the WM8350 provides a way to determine the voltage offset of the AUXADC's VREF buffer and the gain error introduced by scaling the AUXADC input. Measured data can then be adjusted accordingly, eliminating these errors.

To determine the buffer's offset, the AUXADC AUX3 input is disconnected from the AUX3 pin and connected to the unbuffered VREF voltage. Note that input scaling must be used, (i.e. AUXADC\_SCALE3 = 10 or 11), in order to ensure that the AUXADC input is within the measurable range. Measuring this voltage using the buffered VREF as the reference (AUXADC\_REF3 = 1) makes it possible to calculate the combined error.

| ADDRESS                                | BIT | LABEL      | DEFAULT | DESCRIPTION   |
|--|-----|------------|---------|---|
| R145 (91h)<br>Digitizer Control<br>(2) | 2   | AUXADC_CAL | 0       | Configure AUX3 input to be the VREF supply for AUXADC calibration.<br>0 = AUX3 input connected to AUX3 pin<br>1 = AUX3 input connected to unbuffered VREF |

**Table 118 AUXADC Calibration**

## 19.6 DIGITAL COMPARATORS

The WM8350 has four digital comparators which may be used to compare AUXADC measurement data against programmable threshold values. Each comparator has an associated interrupt flag, as described in Section 19.7, which indicates that the associated data is beyond the threshold value.

The digital comparators are enabled using the DCMP $n$ \_ENA register bits as described in Table 119.

The source data for each comparator is selected using the DCMP $n$ \_SRCSEL register bits; this selects one of the eight AUXADC channels for each comparator. Note that, if required, the same AUXADC channel may be selected for more than one comparator; this would allow more than one threshold to be monitored on the same AUXADC channel.

The DCMP $n$ \_GT register bits select whether an interrupt will be indicated when the measured value is above the threshold or when the measured value is below the threshold.

The threshold DCMP $n$ \_THR is a 12-bit code for each comparator. This field follows the same voltage scaling and voltage reference as the associated AUXADC channel source.

| ADDRESS   | BIT   | LABEL                      | DEFAULT | DESCRIPTION  |
|---|-------|----------------------------|---------|--|
| R12 (0Ch)<br>Power Mgmt (5)   | 3     | DCMP4_ENA                  | 0       | Digital comparator 4 enable<br>0 = disabled<br>1 = enabled   |
| or  | 2     | DCMP3_ENA                  | 0       | Digital comparator 3 enable<br>0 = disabled<br>1 = enabled   |
| R163 (A3h)<br>Generic<br>Comparator<br>Control  | 1     | DCMP2_ENA                  | 0       | Digital comparator 2 enable<br>0 = disabled<br>1 = enabled   |
|   | 0     | DCMP1_ENA                  | 0       | Digital comparator 1 enable<br>0 = disabled<br>1 = enabled   |
| R164 (A4h)<br>Generic<br>comparator 1   | 15:13 | DCMP $n$ _SRCS<br>EL [2:0] | 000     | DCOMP $n$ source select.<br>000 = AUX1<br>001 = AUX2<br>010 = AUX3<br>011 = AUX4<br>100 = USB<br>101 = LINE<br>110 = BATT<br>111 = TEMP              |
| R165 (A5h)<br>Generic<br>Comparator 2   |       |                            |         |  |
| R166 (A6h)<br>Generic<br>Comparator 3   | 12    | DCMP $n$ _GT               | 0       | DCOMP $n$ interrupt control<br>0 = interrupt when the source is<br>less than threshold<br>1 = interrupt when the source is<br>greater than threshold |
| R167 (A7h)<br>Generic<br>Comparator 4   | 11:0  | DCMP $n$ _THR<br>[11:0]    | 000h    | DCOMP $n$ threshold<br>(12-bit unsigned binary<br>number)  |
| <p><b>Note:</b> <math>n</math> is a number between 1 and 4 that identifies the individual comparator</p> <p><b>Note:</b> The Comparator Enable bits can each be accessed through two separate control registers. Reading from or writing to either register location has the same effect.</p> |       |                            |         |  |

**Table 119 AUXADC Digital Comparator Control**

## 19.7 AUXADC INTERRUPTS

The AUXADC has five second-level interrupts which can trigger a first-level System Interrupt, AUXADC\_INT (see Section 24). These are described in Table 120. Each AUXADC interrupt in Register R26 can be masked by setting the associated mask bit in Register R34.

The AUX\_DATARDY\_EINT interrupt indicates that new AUXADC data is ready. This bit is cleared when Register R26 is read. Note that this bit is not cleared by reading the measured AUXADC data in Registers R152 to R159.

The AUXADC\_DCOMP<sub>n</sub>\_EINT interrupts indicate that the selected AUXADC channel on Comparator 'n' is beyond the programmed threshold. The DCOMP<sub>n</sub>\_GT register bits defined in Table 119 select whether an interrupt indicates the measured value is above the threshold or indicates the measured value is below the threshold.

| ADDRESS                                 | BIT | LABEL                                    | DESCRIPTION  |
|---|-----|--|--|
| R26 (1Ah)<br>Interrupt<br>Status 2      | 8   | AUXADC_DATARDY_EINT                      | Auxiliary data ready.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |
|   | 7   | AUXADC_DCOMP4_EINT                       | DCOMP4 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.     |
|   | 6   | AUXADC_DCOMP3_EINT                       | DCOMP3 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.     |
|   | 5   | AUXADC_DCOMP2_EINT                       | DCOMP2 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.     |
|   | 4   | AUXADC_DCOMP1_EINT                       | DCOMP1 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.     |
| R34 (22h)<br>Interrupt<br>Status 2 Mask | 8:4 | "IM_" + name of respective<br>bit in R26 | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.                     |

**Table 120 AUXADC Interrupts**

## 20 GENERAL PURPOSE INPUTS / OUTPUTS (GPIO)

### 20.1 GENERAL DESCRIPTION

The WM8350 has thirteen general-purpose input/output (GPIO) pins; GPIO0 - GPIO12. These can be configured as inputs or outputs, active high or active low, with optional on-chip pull-up or pull-down resistors. Alternate functions are also available for each GPIO pin.

Note that different GPIO pins are supported on different power domains. The applicable power domain is specific to a pin, not to a particular GPIO function. The power domains are as follows:

- GPIO0 to GPIO3 : VRTC
- GPIO4 to GPIO9 : DBVDD
- GPIO10 to GPIO12 : LINE

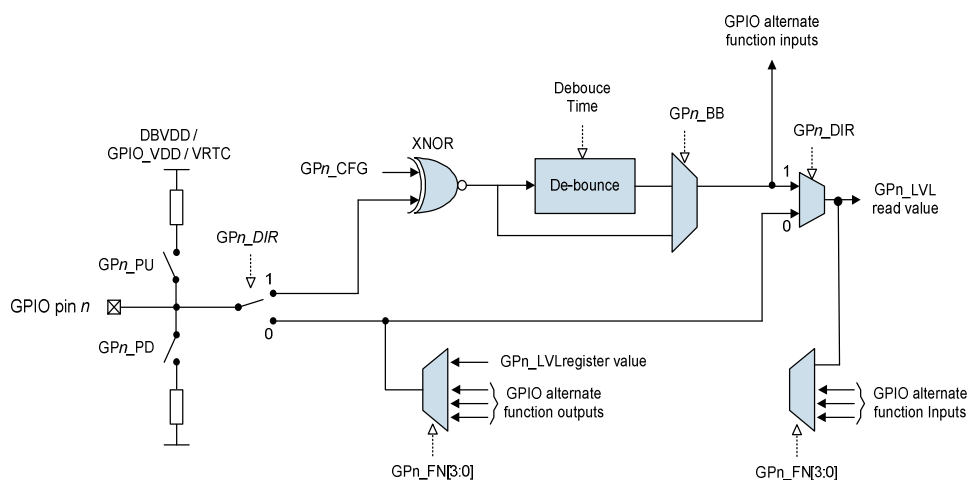


Figure 79 GPIO Equivalent Circuit

### 20.1.1 CONFIGURING GPIO PINS

To configure a pin as a GPIO, the corresponding  $GPn\_FN$  register bits must be set to 0000 (see Table 125). Each GPIO pin can be set up as an input or as an output through the corresponding  $GPn\_DIR$  register bits. Note that, when changing  $GPn\_DIR$ , it is recommended to set  $GPn\_FN = 0000$  first. See Section 20.2.2 for the recommended sequence of commands when updating the GPIO pin function.

The state of a GPIO output is determined by writing to the corresponding  $GPn\_LVL$  register bit. For GPIO inputs, reading the  $GPn\_LVL$  bit returns the logic level at the GPIO pin.

The polarity of GPIO inputs can be selected through the corresponding  $GPn\_CFG$  bit. For GPIO outputs, the  $GPn\_CFG$  bit controls the electrical characteristics of the output pin.

GPIO inputs can also generate an interrupt (see Section 20.1.3). The  $GPn\_INTMODE$  selects whether an interrupt occurs on a rising edge only, or else on both rising and falling edges. The input to this function is influenced by the polarity bit  $GPn\_CFG$  described above.

| ADDRESS  | BIT  | LABEL                 | DEFAULT                      | DESCRIPTION  |                        |                         |  |  |
|--|--|-----------------------|------------------------------|--|------------------------|-------------------------|--|--|
| R129 (81h)<br>GPIO pull-up   | 12:0                                       | $GPn\_PU$ [12:0]      | Dependant on CONFIG settings | GPIO $n$ pull-up<br>0 = Normal<br>1 = Pull-up enabled<br>Only valid when GPIO $n$ is set to input. Do not select pull-up and pull-down at the same time. (see note)  |                        |                         |  |  |
| R130 (82h)<br>GPIO pull-down   | 12:0                                       | $GPn\_PD$ [12:0]      | Dependant on CONFIG settings | GPIO $n$ pull-down<br>0 = Normal<br>1 = Pull-down enabled<br>Only valid when GPIO $n$ is set to input. Do not select pull-up and pull-down at the same time. (see note)  |                        |                         |  |  |
| R131 (83h)<br>GPIO Interrupt Mode  | 12:0                                       | $GPn\_INTMODE$ [12:0] | 0                            | GPIO $n$ Pin Mode:<br>0 = GPIO interrupt is rising edge triggered and taken after the effect of $GPn\_CFG$ register bit<br>1 = GPIO interrupt is both rising and falling edge triggered  |                        |                         |  |  |
| R134 (86h)<br>GPIO Pin Configuration   | 12:0                                       | $GPn\_DIR$ [12:0]     | Dependant on CONFIG settings | GPIO $n$ pin direction<br>0 = Output<br>1 = Input  |                        |                         |  |  |
| R135 (87h)<br>GPIO Pin Polarity / Type   | 12:0                                       | $GPn\_CFG$ [12:0]     | Dependant on CONFIG settings | Selects input polarity /output type for GPIO $n$<br><table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Input (<math>GPn\_DIR=1</math>)</th> <th>Output (<math>GPn\_DIR=0</math>)</th> </tr> </thead> <tbody> <tr> <td>0 = active low<br/>1 = active high<br/>(see note)</td> <td>0 = CMOS<br/>1 = open-drain<br/>(see note)</td> </tr> </tbody> </table>                                | Input ( $GPn\_DIR=1$ ) | Output ( $GPn\_DIR=0$ ) | 0 = active low<br>1 = active high<br>(see note)                      | 0 = CMOS<br>1 = open-drain<br>(see note)   |
| Input ( $GPn\_DIR=1$ )   | Output ( $GPn\_DIR=0$ )                    |                       |                              |  |                        |                         |  |  |
| 0 = active low<br>1 = active high<br>(see note)                                    | 0 = CMOS<br>1 = open-drain<br>(see note)   |                       |                              |  |                        |                         |  |  |
| R230 (E6h)<br>GPIO pin status  | 12:0                                       | $GPn\_LVL$ [12:0]     | N/A                          | Logic level of GPIO $n$ pin<br><table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Input (<math>GPn\_DIR=1</math>)</th> <th>Output (<math>GPn\_DIR=0</math>)</th> </tr> </thead> <tbody> <tr> <td>Read <math>GPn\_LVL</math> to check logic level. Writing '0' clears <math>GPn\_EINT</math></td> <td>Write to <math>GPn\_LVL</math> to change logic level.</td> </tr> </tbody> </table> | Input ( $GPn\_DIR=1$ ) | Output ( $GPn\_DIR=0$ ) | Read $GPn\_LVL$ to check logic level. Writing '0' clears $GPn\_EINT$ | Write to $GPn\_LVL$ to change logic level. |
| Input ( $GPn\_DIR=1$ )   | Output ( $GPn\_DIR=0$ )                    |                       |                              |  |                        |                         |  |  |
| Read $GPn\_LVL$ to check logic level. Writing '0' clears $GPn\_EINT$               | Write to $GPn\_LVL$ to change logic level. |                       |                              |  |                        |                         |  |  |
| <b>Note:</b> $n$ is a number between 0 and 12 that identifies the individual GPIO. |  |                       |                              |  |                        |                         |  |  |

**Table 121 Configuring the GPIO Pins**

**Note:** The GPIO input functions  $/MR$ ,  $/WAKEUP$  and  $/LDO\_ENA$  behave differently to other GPIO inputs. These functions are Active Low by default, when  $GPn\_CFG = 1$ . These functions may be changed to Active High by setting  $GPn\_CFG = 0$ .

**Note:** If a GPIO pin is configured as an open drain output, (ie.  $GPn\_DIR=0$ ,  $GPn\_CFG=1$ ), then the external pull-up voltage must not be greater than the supply domain for the corresponding GPIO. For example, if the GPIO supply domain is DBVDD then the external pull-up voltage must be less than or equal to DBVDD.

**Note:** Do not enable pull-up and pull-down resistors for the same GPIO pin.

**Note:** The internal pull-up and pull-down on GPIO10

, GPIO11 and GPIO12 may be too weak for many applications. If pull-up or pull-down is required on these pins, it is recommended to ensure that the pull resistance is  $<100k\Omega$ . This can be achieved using an external resistor on its own or in combination with the internal resistance.

### 20.1.2 INPUT DE-BOUNCE

GPIO inputs have an optional de-bounce function to remove glitches from the input signal. This may be useful when the GPIO is connected to a mechanical switch. The de-bounce function can be enabled for each pin individually using  $GPn\_DB$ , with a globally selectable de-bounce time set by  $GP\_DBTIME$ .

GPIO alternative functions  $PWR\_ON$ ,  $PWR\_OFF$  and  $/WAKEUP$  are special cases with regard to debouncing.  $PWR\_ON$  and  $/WAKEUP$  have a debounce time of  $GP\_DBTIME[1:0] + 40ms$  and  $PWR\_OFF$  has a debounce time of  $GP\_DBTIME[1:0] + 5ms$ .

| ADDRESS                      | BIT  | LABEL              | DEFAULT | DESCRIPTION   |
|------------------------------|------|--------------------|---------|---|
| R128 (80h)<br>GPIO de-bounce | 12:0 | $GPn\_DB$ [12:0]   | 1       | GPIO $n$ debounce<br>0 = GPIO is not debounced.<br>1 = GPIO is debounced (time from $GP\_DBTIME[1:0]$ )   |
| R133 (85h)<br>GPIO Control   | 7:6  | $GP\_DBTIME$ [1:0] | 00      | De-bounce time for all GPIO inputs<br>00 = 64 $\mu$ s<br>01 = 0.5ms<br>10 = 1ms<br>11 = 4ms<br>Note: $PWR\_ON$ , $PWR\_OFF$ and $/WAKEUP$ have additional debounce times. |

**Note:**  $n$  is a number between 0 and 12 that identifies the individual GPIO.

Table 122 Configuring GPIO De-bounce

### 20.1.3 GPIO INTERRUPTS

The GPIO logic can raise a first-level interrupt,  $GPIO\_INT$  (see Section 24). This interrupt is the logical OR of the second-level GPIO interrupts described in Table 123.

| ADDRESS                            | BIT  | LABEL                                 | DESCRIPTION  |
|------------------------------------|------|---------------------------------------|--|
| R30 (1Eh)<br>GPIO Interrupt Status | 12:0 | $GPn\_EINT$ [12:0]                    | GPIO $n$ interrupt.<br>(Trigger controlled by $GPn$ registers.)<br>Note: This bit is cleared once read.  |
| R38 (26h)<br>GPIO Interrupt Mask   | 12:0 | "IM_" + name of respective bit in R30 | Mask bits for GPIO interrupts<br>Each of these bits masks the respective bit in R30 when it is set to 1 (e.g. $GPn\_EINT$ in R30 does not trigger a $GPIO\_INT$ interrupt when $IM\_GPn\_EINT$ in R38 is set). |

**Note:**  $n$  is a number between 0 and 12 that identifies the individual GPIO.

Table 123 GPIO Interrupts

## 20.2 GPIO ALTERNATE FUNCTIONS

### 20.2.1 LIST OF ALTERNATE FUNCTIONS

The following alternate functions are available.

| ALTERNATE FUNCTION NAME | INPUT / OUTPUT | DESCRIPTION   |
|-------------------------|----------------|---|
| ADCLRCLK                | Input          | Alternate Left/Right clock for CODEC ADC digital interface. When this function is selected, the LRCLK pin supports the DAC interface only, and GPIO5 provides the ADC digital interface L/R clock. See Section 12.  |
| ADCBCLK                 | Input          | Alternate BCLK for CODEC ADC digital interface. When this function is selected, the BCLK pin supports the DAC interface only, and GPIO6 or GPIO8 provides the ADC digital interface BCLK signal. See Section 12.  |
| CHIP_RESET              | Input          | Logic input to reset the Chip. When this input is asserted, the chip performs a full reset and re-starts in accordance with the current config mode settings.<br><br>Note that CHIP_RESET_ENA in register R3 should be set to 1 when using CHIP_RESET as alternative GPIO function.   |
| CSB                     | Input          | 3-/4-wire Control Interface Chip Select pin (CSB). Note that this function is selected automatically on GPIO7 when 3-/4-wire mode is selected, ie. regardless of the GP7_FN control field. See Section 11.  |
| FLASH                   | Input          | Hardware trigger for flash function on ISINKA or ISINKB. This function is rising edge triggered. The Current Sink must be in Flash mode, and with the trigger set to GPIO. See Section 16.  |
| HIBERNATE (Level)       | Input          | Logic input to place the chip into hibernate. The behaviour of some components of the WM8350 in Hibernate mode is configurable. See Section 14.<br><br>This "level triggered" input is deemed to be asserted for as long as it is logic 1 (or logic 0 if the polarity is inverted).   |
| HIBERNATE (Edge)        | Input          | Logic input to place the chip into hibernate. The behaviour of some components of the WM8350 in Hibernate mode is configurable. See Section 14.<br><br>When the "edge triggered" input is used, Hibernate is selected when a rising edge occurs (or a falling edge if the polarity is inverted). After Hibernate has been selected by this method, a "StartUp" event (see Section 14.3.1) is required to exit from Hibernate. |
| HEARTBEAT               | Input          | Input to Watchdog function, rising edge triggered. See Section 23.  |
| /LDO_ENA                | Input          | Enable signal for LDO1. See Section 14.7.4.   |
| L_PWR1                  | Input          | Logic input used to place DC-DC Converters or LDOs into a Low Power state. See Section 14.  |
| L_PWR2                  | Input          | Logic input used to place DC-DC Converters or LDOs into a Low Power state. See Section 14.  |
| L_PWR3                  | Input          | Logic input used to place DC-DC Converters or LDOs into a Low Power state. See Section 14.  |
| MASK                    | Input          | Mask input to AUXADC. This input may be used either to block all inputs to the AUXADC, or to initiate A-D Conversions. See Section 19.  |
| /MR                     | Input          | Logic input used to drive the /RST pin and the /RST and /MEMRST (GPIO outputs) low. Note that this input has no other effect on internal circuits. See Section 14.  |
| PWR_OFF                 | Input          | Logic input signal causes a controlled shutdown of the WM8350. See Section 14.  |
| PWR_ON                  | Input          | Power on input signal from processor (input switching threshold 1.0V). See Section 14.  |



| ALTERNATE FUNCTION NAME | INPUT / OUTPUT | DESCRIPTION   |
|-------------------------|----------------|---|
| /WAKEUP                 | Input          | Logic input signal causes wakeup from OFF or HIBERNATE states. Can be used for accessory detection. See Section 14.   |
| 32kHz                   | Input          | 32kHz clock input to Real Time Clock. See Section 22.   |
| ADA                     | Output         | Aux ADC external data available signal. See Section 19.<br>0 = AUXADC external data not available<br>1 = AUXADC external data available   |
| ADCLRCLK                | Output         | Alternate Left/Right clock for CODEC ADC digital interface. When this function is selected, the LRCLK pin supports the DAC interface only, and GPIO5 provides the ADC digital interface L/R clock. See Section 12.  |
| ADCLRCLKB               | Output         | Inverted Left/Right clock for CODEC ADC digital interface. When this function is selected, the LRCLK pin supports the DAC interface only, and GPIO6 provides the inverted ADC digital interface L/R clock. See Section 12.  |
| ADCBCLK                 | Output         | Alternate BCLK for CODEC ADC digital interface. When this function is selected, the BCLK pin supports the DAC interface only, and GPIO8 provides the ADC digital interface BCLK signal. See Section 12.   |
| /BATT_FAULT             | Output         | Same as /UVLO signal – indicates no power present. Should be output as soon as possible after /UVLO.  |
| CH_IND                  | Output         | Battery Charge status indication. This output can drive an LED, which indicates battery charging status through different flash rates. See Section 17.  |
| CODEC_OPCLK             | Output         | Output clock from CODEC. Frequency is determined by OPCLK_DIV. See Section 12.  |
| DO_CONF                 | Output         | Output used for development mode programming. Signal goes high to indicate that external programming can take place (during the Pre-Active state). Same functionality as PWR_ON (GPIO output) but with additional programmable option to prevent reset in OFF mode. See Section 14. |
| FLASH_OUT               | Output         | Logic output asserted for the duration of a Flash. Triggered by either SINKA or SINKB; Triggered by GPIO or CSn_FLASH bit. See Section 16.  |
| FLL_CLK                 | Output         | Output FLL clock. See Section 12.4.   |
| ISINKC                  | Output         | Open-drain output which can be used to drive LEDs connected to LINE via a series resistor. See Section 16.  |
| ISINKD                  | Output         | Open-drain output which can be used to drive LEDs connected to LINE via a series resistor. See Section 16.  |
| ISINKE                  | Output         | Open-drain output which can be used to drive LEDs connected to LINE via a series resistor. See Section 16.  |
| LINE_SW                 | Output         | Used to drive an external PFET between 'Wall' supply and LINE input, in order to prevent reverse conduction when the Wall Adapter is disconnected. See Section 17.1.  |
| LINE_GT_BATT            | Output         | Output to enable external PFET to reduce IR losses when LINE is greater than BATT   |
| MICDET                  | Output         | Logic output indicating microphone bias current detection.<br>0 = Mic Bias Current not detected<br>1 = Mic Bias Current detected<br>Note that an Interrupt is also generated by this event. See Section 13.12.2.  |
| MICSHT                  | Output         | Logic output indicating microphone bias short circuit detection.<br>0 = Mic Bias Short Circuit not detected<br>1 = Mic Bias Short Circuit detected<br>Note that an Interrupt is also generated by this event. See Section 13.12.2.  |

| ALTERNATE FUNCTION NAME | INPUT / OUTPUT | DESCRIPTION   |
|-------------------------|----------------|---|
| /MEMRST                 | Output         | Output used to control other subsystems such as external memory. Signal goes low to reset external memory. The status of this signal in the Hibernate state is configurable, allowing external memory contents to be retained in Hibernate. See Section 14. |
| P_CLK                   | Output         | 1MHz output clock in phase with the internal DC-DC converters. This signal can be used to sync external circuits (e.g. DC-DCs).   |
| POR_B                   | Output         | Output which toggles low to high during power-on reset  |
| PWR_ON                  | Output         | Output used to indicate that device is powered on (eg. to enable external DC-DC converters). This output is disabled in the OFF state.  |
| /RST                    | Output         | Output used to indicate system resets. Signal goes low during reset, same as the /RST pin. The pulse duration is programmable. See Section 14.  |
| RTC                     | Output         | Real Time Clock output - frequency is controlled by RTC_DSW[3:0]. See Section 22.   |
| SDOUT                   | Output         | 4-wire Control Interface data output pin (SDOUT). Note that this function is selected automatically on GPIO6 when 4-wire mode is selected, ie. regardless of the GP6_FN control field. See Section 11.  |
| /VCC_FAULT              | Output         | Indicates a fault condition on selectable DC Converters, LDO Regulators and the Limit Switch. The mask bits in Register 215 determine which supplies contribute to this status flag. See Section 14.6.5, Section 14.7.3 and Section 15.2.3.                 |
| VRTC                    | Output         | Output from on-chip backup power source voltage regulator VRTC.   |
| 32kHz                   | Output         | 32kHz clock output from the Real Time Clock oscillator.   |

Table 124 List of GPIO Alternate Functions

### 20.2.2 SELECTING GPIO ALTERNATE FUNCTIONS

The function of each GPIO pin is programmable by writing to the respective GP $n$  register bits. GP $n$ \_FN = 0000 selects the GPIO function and settings other than 0000 select various alternate functions.

The GPIO function is also determined by the value of the GP $n$ \_DIR register bit. Note that, when changing GP $n$ \_DIR, it is recommended to set GP $n$ \_FN = 0000 first.

When changing the function of a GPIO pin, (updating GP $n$ \_FN or GP $n$ \_DIR), it is recommended that the following sequence of actions is taken sequentially.

- Set GP $n$ \_FN = 0000
- Update the other GPIO configuration fields GP $n$ \_DB, GP $n$ \_PU, GP $n$ \_PD, GP $n$ \_CFG, GP $n$ \_DIR
- If the new function is an input, ensure that the input trigger is in the inactive state (ie. logic 0 for a function that is active High)
- Set GP $n$ \_FN according to the new GPIO function
- Read the GPIO Interrupt Status Register R30 (1Eh) to clear any GPIO Interrupt events
- If any bit in Register R30 (1Eh) was set when read, then read the System Interrupts Register R24 (18h) to clear the IRQ pin

Note that GPIO7 is automatically enabled as CSB in 3-wire and 4-wire control modes. GPIO6 is automatically enabled as SDO<sub>UT</sub> in 4-wire control mode. These automatic selections take precedence over all other GPIO6 and GPIO7 control fields.

| ADDRESS                                 | BIT   | LABEL   | DEFAULT                               | DESCRIPTION                |
|---|-------|---------|---------------------------------------|----------------------------|
| R140 (8Ch)<br>GPIO function<br>select 1 | 3:0   | GP0_FN  | Dependant<br>on<br>CONFIG<br>settings | Selects function of GPIO0  |
|   | 7:4   | GP1_FN  |                                       | Selects function of GPIO1  |
|   | 11:8  | GP2_FN  |                                       | Selects function of GPIO2  |
|   | 15:12 | GP3_FN  |                                       | Selects function of GPIO3  |
| R141 (8Dh)<br>GPIO function<br>select 2 | 3:0   | GP4_FN  |                                       | Selects function of GPIO4  |
|   | 7:4   | GP5_FN  |                                       | Selects function of GPIO5  |
|   | 11:8  | GP6_FN  |                                       | Selects function of GPIO6  |
|   | 15:12 | GP7_FN  |                                       | Selects function of GPIO7  |
| R142 (8Eh)<br>GPIO function<br>select 3 | 3:0   | GP8_FN  |                                       | Selects function of GPIO8  |
|   | 7:4   | GP9_FN  |                                       | Selects function of GPIO9  |
|   | 11:8  | GP10_FN |                                       | Selects function of GPIO10 |
|   | 15:12 | GP11_FN |                                       | Selects function of GPIO11 |
| R143 (8Fh)                              | 3:0   | GP12_FN | Selects function of GPIO12            |                            |

**Table 125 Control Registers to Select GPIO Alternate Functions**

| ADDRESS                                   | BIT       | LABEL           | DEFAULT                            | DESCRIPTION               |                                   |                                    |
|---|-----------|-----------------|------------------------------------|---------------------------|-----------------------------------|------------------------------------|
| R140 (8Ch<br>GPIO<br>function<br>select 1 | 3:0       | GP0_FN<br>[3:0] | Dependant on<br>CONFIG<br>settings | GPIO0 function definition |                                   |                                    |
|   |           |                 |                                    |                           | Input<br>(GP <sub>n</sub> _DIR=1) | Output<br>(GP <sub>n</sub> _DIR=0) |
|   |           |                 |                                    | 0000                      | GPIO                              | GPIO                               |
|   |           |                 |                                    | 0001                      | PWR_ON                            | PWR_ON                             |
|   |           |                 |                                    | 0010                      | /LDO_ENA                          | VRTC                               |
|   |           |                 |                                    | 0011                      | L_PWR1                            | POR_B                              |
|   |           |                 |                                    | 0100                      | PWR_OFF                           | /RST                               |
|   | 0101      | CHIP_RESET      |                                    |                           |                                   |                                    |
|   | 7:4       | GP1_FN<br>[3:0] | Dependant on<br>CONFIG<br>settings | GPIO1 function definition |                                   |                                    |
|   |           |                 |                                    |                           | Input                             | Output                             |
|   |           |                 |                                    | 0000                      | GPIO                              | GPIO                               |
|   |           |                 |                                    | 0001                      | PWR_ON                            | DO_CONF                            |
|   |           |                 |                                    | 0010                      | /LDO_ENA                          | /RST                               |
|   |           |                 |                                    | 0011                      | L_PWR2                            | /MEMRST                            |
|   | 11:8      | GP2_FN<br>[3:0] | Dependant on<br>CONFIG<br>settings | GPIO2 function definition |                                   |                                    |
|   |           |                 |                                    |                           | Input                             | Output                             |
|   |           |                 |                                    | 0000                      | GPIO                              | GPIO                               |
|   |           |                 |                                    | 0001                      | PWR_ON                            | PWR_ON                             |
|   |           |                 |                                    | 0010                      | /WAKEUP                           | VRTC                               |
|   |           |                 |                                    | 0011                      | 32kHz                             | 32kHz                              |
|   | 15:1<br>2 | GP3_FN<br>[3:0] | Dependant on<br>CONFIG<br>settings | GPIO3 function definition |                                   |                                    |
|   |           |                 |                                    | Input                     | Output                            |                                    |
| 0000                                      |           |                 |                                    | GPIO                      | GPIO                              |                                    |
| 0001                                      |           |                 |                                    | PWR_ON                    | P_CLK                             |                                    |
| 0010                                      |           |                 |                                    | /LDO_ENA                  | VRTC                              |                                    |
| 0011                                      |           |                 |                                    | PWR_OFF                   | 32kHz                             |                                    |
| 0100                                      | FLASH     | /MEMRST         |                                    |                           |                                   |                                    |

**Note:** Undocumented combinations for GP<sub>n</sub>\_FN (n = 0 to 3) are reserved

**Table 126 GPIO Function Select 1**

| ADDRESS                                   | BIT       | LABEL           | DEFAULT                            | DESCRIPTION               |                      |                       |
|---|-----------|-----------------|------------------------------------|---------------------------|----------------------|-----------------------|
| R141(8Dh)<br>GPIO<br>function<br>select 2 | 3:0       | GP4_FN<br>[3:0] | Dependant on<br>CONFIG<br>settings | GPIO4 function definition |                      |                       |
|   |           |                 |                                    |                           | Input<br>(GPn_DIR=1) | Output<br>(GPn_DIR=0) |
|   |           |                 |                                    | 0000                      | GPIO                 | GPIO                  |
|   |           |                 |                                    | 0001                      | /MR                  | /MEMRST               |
|   |           |                 |                                    | 0010                      | FLASH                | ADA                   |
|   |           |                 |                                    | 0011                      | HIBERNATE<br>(Level) | FLASH_OUT             |
|   |           |                 |                                    | 0100                      | MASK                 | /VCC_FAULT            |
|   |           |                 |                                    | 0101                      | CHIP_RESET           | MICSHT                |
|   | 1010      |                 | MICDET                             |                           |                      |                       |
|   | 7:4       | GP5_FN<br>[3:0] | Dependant on<br>CONFIG<br>settings | GPIO5 function definition |                      |                       |
|   |           |                 |                                    |                           | Input                | Output                |
|   |           |                 |                                    | 0000                      | GPIO                 | GPIO                  |
|   |           |                 |                                    | 0001                      | L_PWR1               | P_CLK                 |
|   |           |                 |                                    | 0010                      | ADCLRCLK             | ADCLRCLK              |
|   |           |                 |                                    | 0011                      | HIBERNATE<br>(Edge)  | 32kHz                 |
|   |           |                 |                                    | 0100                      | PWR_OFF              | /BATT_FAULT           |
|   |           |                 |                                    | 0101                      | HIBERNATE<br>(Level) | MICSHT                |
|   |           |                 |                                    | 0110                      | -                    | ADA                   |
|   |           |                 |                                    | 0111                      | -                    | CODEC_OPCLK           |
|   | 11:8      | GP6_FN<br>[3:0] | Dependant on<br>CONFIG<br>settings | GPIO6 function definition |                      |                       |
|   |           |                 |                                    |                           | Input                | Output                |
|   |           |                 |                                    | 0000                      | GPIO                 | GPIO                  |
|   |           |                 |                                    | 0001                      | L_PWR2               | /MEMRST               |
|   |           |                 |                                    | 0010                      | FLASH                | ADA                   |
|   |           |                 |                                    | 0011                      | HIBERNATE<br>(Edge)  | RTC                   |
|   |           |                 |                                    | 0100                      | HIBERNATE<br>(Level) | MICDET                |
|   |           |                 |                                    | 0101                      | -                    | MICSHT                |
|   | 0110      | -               | ADCLRCLKB                          |                           |                      |                       |
|   | 15:1<br>2 | GP7_FN<br>[3:0] | Dependant on<br>CONFIG<br>settings | GPIO7 function definition |                      |                       |
|   |           |                 |                                    |                           | Input                | Output                |
|   |           |                 |                                    | 0000                      | GPIO                 | GPIO                  |
|   |           |                 |                                    | 0001                      | L_PWR3               | P_CLK                 |
| 0010                                      |           |                 |                                    | MASK                      | /VCCFAULT            |                       |
| 0011                                      |           |                 |                                    | HIBERNATE<br>(Level)      | /BATT_FAULT          |                       |
| 0100                                      |           |                 |                                    | -                         | MICDET               |                       |
| 0101                                      |           |                 |                                    | -                         | MICSHT               |                       |
| 0110                                      |           |                 |                                    | -                         | ADA                  |                       |
| 1100                                      |           |                 |                                    | -                         | FLL_CLK              |                       |

**Note:** Undocumented combinations for GPn\_FN (n = 4 to 7) are reserved

**Table 127 GPIO Function Select 2**

| ADDRESS  | BIT               | LABEL                              | DEFAULT                            | DESCRIPTION                |                      |                       |
|--|-------------------|------------------------------------|------------------------------------|----------------------------|----------------------|-----------------------|
| R142 (8Eh)<br>GPIO<br>function<br>select 3                                   | 3:0               | GP8_FN<br>[3:0]                    | Dependant on<br>CONFIG<br>settings | GPIO8 function definition  |                      |                       |
|  |                   |                                    |                                    |                            | Input<br>(GPn_DIR=1) | Output<br>(GPn_DIR=0) |
|  |                   |                                    |                                    | 0000                       | GPIO                 | GPIO                  |
|  |                   |                                    |                                    | 0001                       | /MR                  | /VCC_FAULT            |
|  |                   |                                    |                                    | 0010                       | ADCBCLK              | ADCBCLK               |
|  |                   |                                    |                                    | 0011                       | PWR_OFF              | /BATT_FAULT           |
|  |                   | 0100                               | HIBERNATE<br>(Edge)                | /RST                       |                      |                       |
|  | 7:4               | GP9_FN<br>[3:0]                    | Dependant on<br>CONFIG<br>settings | GPIO9 function definition  |                      |                       |
|  |                   |                                    |                                    |                            | Input                | Output                |
|  |                   |                                    |                                    | 0000                       | GPIO                 | GPIO                  |
|  |                   |                                    |                                    | 0001                       | HEARTBEAT            | /VCC_FAULT            |
|  |                   |                                    |                                    | 0010                       | MASK                 | LINE_GT_BATT          |
|  |                   |                                    |                                    | 0011                       | PWR_OFF              | /BATT_FAULT           |
|  |                   | 0100                               | HIBERNATE<br>(Level)               | /MEMRST                    |                      |                       |
|  | 11:8              | GP10_F<br>N [3:0]                  | Dependant on<br>CONFIG<br>settings | GPIO10 function definition |                      |                       |
|  |                   |                                    |                                    |                            | Input                | Output                |
|  |                   |                                    |                                    | 0000                       | GPIO                 | GPIO                  |
|  |                   |                                    |                                    | 0001                       | -                    | ISINKC                |
|  |                   |                                    |                                    | 0010                       | -                    | LINE_GT_BATT          |
|  |                   | 0011                               | PWR_OFF                            | CH_IND                     |                      |                       |
| 15:1<br>2  | GP11_F<br>N [3:0] | Dependant on<br>CONFIG<br>settings | GPIO11 function definition         |                            |                      |                       |
|  |                   |                                    |                                    | Input                      | Output               |                       |
|  |                   |                                    | 0000                               | GPIO                       | GPIO                 |                       |
|  |                   |                                    | 0001                               | -                          | ISINKD               |                       |
|  |                   |                                    | 0010                               | /WAKEUP                    | LINE_GT_BATT         |                       |
|  | 0011              | -                                  | CH_IND                             |                            |                      |                       |
| <b>Note:</b> Undocumented combinations for GPn_FN (n = 8 to 11) are reserved |                   |                                    |                                    |                            |                      |                       |

Table 128 GPIO Function Select 3

| ADDRESS   | BIT  | LABEL             | DEFAULT                            | DESCRIPTION                 |                      |                       |
|---|------|-------------------|------------------------------------|-----------------------------|----------------------|-----------------------|
| R143 (8Fh)<br>GPIO<br>function<br>select 4          | 3:0  | GP12_F<br>N [3:0] | Dependant on<br>CONFIG<br>settings | GPIO 12 function definition |                      |                       |
|   |      |                   |                                    |                             | Input<br>(GPn_DIR=1) | Output<br>(GPn_DIR=0) |
|   |      |                   |                                    | 0000                        | GPIO                 | GPIO                  |
|   |      |                   |                                    | 0001                        | CHIP_RESET           | ISINKE                |
|   |      |                   |                                    | 0010                        | -                    | LINE_GT_BATT          |
|   |      |                   |                                    | 0011                        | -                    | LINE_SW               |
|   | 0100 | -                 | 32kHz                              |                             |                      |                       |
| <b>Note:</b> Undocumented combinations are reserved |      |                   |                                    |                             |                      |                       |

Table 129 GPIO Function Select 4

## 21 VOLTAGE REFERENCES

The WM8350 generates several reference voltages used for different purposes.

The main reference voltage VREF, and additional internal references derived from it, are used in the DC-DC converters, the LDO regulators and the auxiliary ADC. VREF is highly stable, accurate, and independent of the supply voltage. It can be trimmed for improved accuracy.

The VRTC regulator (see Section 17.6) uses a separate, low-power reference at start-up.

The mid-rail reference VMID is used in the audio CODEC. It is generated from AVDD.

Each reference voltage is internally provided to those parts of the WM8350 where it is needed.

### 21.1 MAIN REFERENCE (VREF)

The main reference generates a highly accurate reference voltage VREF. It requires a decoupling capacitor on the CREF pin; a 2.2 $\mu$ F X5R capacitor is recommended, as noted in Section 29.2; and an accurate resistor on the RREF pin; a 100k $\Omega$  (1%) resistor is recommended, as noted in Section 29.2.

The WM8350 will malfunction if those components are omitted.

The accuracy of supply voltages generated by the WM8350 depends on VREF, and can be improved by trimming. This scales VREF by up to +15/-16% in 1% steps, to compensate for deviations from the nominal value.

The main reference can be overdriven with an externally generated reference voltage, if desired.

### 21.2 LOW-POWER REFERENCE

The low-power reference determines the accuracy of VRTC on start-up. Once the main bandgap has been trimmed and has settled VRTC switches across to the main bandgap for greater accuracy.

## 22 REAL-TIME CLOCK (RTC)

### 22.1 GENERAL DESCRIPTION

The WM8350 contains a Real Time Clock (RTC), which maintains the current date and time, and also has the capability to generate alarms and periodic interrupt signals. The RTC is powered by the backup supply (VRTC), in order that it can keep running when the normal power sources are unavailable.

The RTC uses the 32.768kHz clock generated by the on-chip crystal oscillator. To compensate for errors in this clock frequency, the RTC includes a frequency trim option. Alternatively the RTC can be clocked from external 32.768kHz input on a GPIO pin configured as 32kHz input. See Section 12.2 for details of the 32kHz oscillator control.

### 22.2 RTC CONTROL

#### 22.2.1 MODES OF OPERATION

The Real Time Clock is enabled when RTC\_TICK\_ENA is set to 1. (This is the default setting.) See Table 135 for the definition of this RTC\_TICK\_ENA.

The RTC can operate as a 24-hour clock or else as a 12-hour clock with a separate AM/PM flag bit. The RTC time register fields can be treated as BCD (binary-coded decimal) or as binary data formats. These options are selected as described in Table 130.

| ADDRESS                       | BIT | LABEL    | DEFAULT | DESCRIPTION   |
|-------------------------------|-----|----------|---------|---|
| R23 (17h)<br>RTC Time control | 15  | RTC_BCD  | 0       | RTC Coding (applies to all time registers)<br>0 = Binary<br>1 = BCD   |
|                               | 14  | RTC_12HR | 0       | RTC 12/24 hours mode<br>1 = 12 hours (MSB of RTC_HRS indicates AM/PM)<br>0 = 24 hours (MSB of RTC_HRS is 0) |

Table 130 RTC Modes of Operation

#### 22.2.2 RTC TIME REGISTERS

The current time and date are held in registers R16 to R19, as described in Table 131.

| ADDRESS                     | BIT  | LABEL               | DEFAULT   | DESCRIPTION   |
|-----------------------------|------|---------------------|-----------|---|
| R16 (10h)<br>RTC sec / min  | 14:8 | RTC_MINS [6:0]      | 000 0000  | RTC Minutes; 0 to 59  |
|                             | 6:0  | RTC_SECS [6:0]      | 000 0000  | RTC Seconds; 0 to 59  |
| R17 (11h)<br>RTC hour / day | 10:8 | RTC_DAY [2:0]       | 1         | RTC Day of the week; 1 to 7, 1 = Sunday                                 |
|                             | 5    | RTC_HPM             | 0         | RTC Hours AM/PM flag<br>0 = AM<br>1 = PM<br>Only valid in 12hour mode.  |
|                             | 4:0  | RTC_HRS [4:0]       | 0 0000    | Hours register with 0-23 range in 24hour mode and 1-12 in 12 hour mode. |
| R18 (12h)<br>RTC date       | 12:8 | RTC_MTH [5:0]       | 0_0001    | Month register with range 1-12.   |
|                             | 5:0  | RTC_DATE [5:0]      | 00_0001   | Date register with range 1-31.  |
| R19 (13h)<br>RTC year       | 13:8 | RTC_YHUNDREDS [6:0] | 01_0100   | Year hundreds register tied to 20(dec)                                  |
|                             | 7:0  | RTC_YUNITS [7:0]    | 0000_0000 | Year units register with range 0-99.                                    |

Table 131 RTC Time Registers



The current time can be read from the registers defined above. As the content of the time registers changes every second, a single register read, executed at an arbitrary time, does not guarantee an accurate time reading. Two possible methods are recommended for reliable reading of the time registers:

- Read after interrupt: the RTC\_SEC interrupt (see Section 22.5) indicates that the seconds counter has just been incremented, and that the RTC registers will not change again within the next 999ms. A register read executed immediately after an RTC\_SEC interrupt can therefore be taken as an accurate time reading.
- Two consecutive reads: if two consecutive reads within a short time (less than 1s apart) return the same result, this can be taken as an accurate reading. If the two results differ, the procedure should be repeated.

### 22.2.3 SETTING THE TIME

When writing to the RTC time registers, the seconds counter should first be stopped in order to prevent glitches. The following procedure should be used:

- Set the RTC\_SET bit to stop seconds counter
- Read the RTC\_STS bit. Repeat this step until RTC\_STS=1
- Set new time in Registers R16 to R19
- Clear the RTC\_SET bit to re-enable seconds counter.

The RTC\_SET and RTC\_STS bits are defined in Table 132.

| ADDRESS                       | BIT | LABEL   | DEFAULT | DESCRIPTION  |
|-------------------------------|-----|---------|---------|--|
| R23 (17h)<br>RTC Time control | 11  | RTC_SET | 0       | Stops RTC seconds counter (instruction only)<br>0 = normal operation<br>1 = stop counter |
|                               | 10  | RTC_STS | 0       | Status of RTC seconds counter<br>0 = normal operation<br>1 = counter stopped             |

**Table 132 Setting the RTC Time**

### 22.2.4 RTC ALARM REGISTERS

An RTC Alarm can be set by writing to the control fields in registers R20 to R22, which are in a similar format to the RTC Time registers.

Setting any of these fields to "All 1's" results in that field being a "don't care" field. For example, setting the RTC\_ALMDAY field to 0001 determines that the alarm is set for a Sunday, whilst setting RTC\_ALMDAY to 1111 results in the programmed alarm occurring on every day of the week.

When the RTC Alarm time/date fields match the RTC time, the alarm event is signalled by the WM8350 raising the RTC\_ALM\_EINT interrupt. See Section 22.5 for further details.

| ADDRESS                          | BIT  | LABEL                | DEFAULT  | DESCRIPTION   |
|----------------------------------|------|----------------------|----------|---|
| R20 (14h)<br>ALARM<br>sec / min  | 14:8 | RTC_ALMMINS<br>[6:0] | 000_0000 | Minutes alarm register with range 0-59. All 1's sets to 'don't care' state.<br>Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms.   |
|                                  | 6:0  | RTC_ALMSECS<br>[6:0] | 000_0000 | Seconds alarm register with range 0-59. All 1's set to 'don't care' state.<br>Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms.  |
| R21 (15h)<br>ALARM<br>hour / day | 11:8 | RTC_ALMDAY<br>[3:0]  | 0000     | Day alarm register, with range 1-7, 1 = Sunday. All 1's sets to 'don't care' state.<br>Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms.   |
|                                  | 5    | RTC_ALMHPM           | 0        | Alarm hours AM/PM flag<br>0 = AM<br>1 = PM<br>Only applicable in 12 hour mode. In 24 hour mode set to 1 if RTC_ALMHRS is set to all 1's 'don't care' or 0 otherwise.  |
|                                  | 4:0  | RTC_ALMHRS<br>[4:0]  | 0_0000   | Hours alarm register with range 0-23 in 24 hours mode and 1-12 in 12 hour. In 12 hour mode bit 5 is used as PM/not-AM flag. All 1's sets to 'don't care' state.<br>Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms. |
| R22 (16h)<br>ALARM<br>date       | 12:8 | RTC_ALMMTH<br>[4:0]  | 0_0000   | Month alarm register with range 1-12. All 1's sets to 'don't care' state.<br>Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms.   |
|                                  | 5:0  | RTC_ALMDATE<br>[5:0] | 00_0000  | Date alarm register with range 1-31. All 1's sets to 'don't care' state.<br>Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms.  |

Table 133 RTC Alarm Registers

The "don't care" option (all bits set to 1) provides extra flexibility for programming ALARM duration and recurrent alarms. For example:

- Setting only RTC\_ALMSEC to "don't care" produces an alarm lasting 1 minute.
- Setting only RTC\_ALMDATE to "don't care" produces an alarm lasting 1 second that recurs once a week, on the day determined by RTC\_ALMDAY, during the month determined by RTC\_ALMMTH.
- Setting RTC\_ALMSEC, RTC\_ALMDATE, RTC\_ALMDAY and RTC\_ALMMTH to "don't care" produces a daily alarm lasting 1 minute.

### 22.2.5 SETTING THE ALARM

Writing to the RTC Alarm registers requires a procedure similar to that used when setting RTC time, in order to prevent accidental alarms being triggered:

- Set the RTC\_ALMSET bit to disable alarms
- Read the RTC\_ALMSTS bit. Repeat this step until RTC\_ALMSTS=1
- Set new RTC Alarm in Registers R20 to R22
- Clear the RTC\_ALMSET bit to re-enable RTC Alarm

The RTC\_ALMSET and RTC\_ALMSTS bits are defined in Table 134.

| ADDRESS                          | BIT | LABEL      | DEFAULT | DESCRIPTION  |
|----------------------------------|-----|------------|---------|--|
| R23 (17h)<br>RTC Time<br>control | 9   | RTC_ALMSET | 1       | Stops alarms (instruction only)<br>0 = normal operation<br>1 = stop alarms<br>It is recommended to stop alarms when setting the RTC alarm. This avoids false alarms. |
|                                  | 8   | RTC_ALMSTS | 1       | Actual status of ALARM circuitry<br>0 = normal operation<br>1 = alarms stopped   |

Table 134 Setting the RTC Alarm

### 22.3 TRIMMING THE RTC

The RTC has a frequency trim feature to allow compensation for known and constant errors in the crystal oscillator frequency up to  $\pm 8$ Hz. Programming the frequency trim requires a procedure similar to that used when setting RTC and ALARM time:

- Clear the RTC\_TICK\_ENA bit to disable the 1 second tick generator
- Read the RTC\_TICKSTS bit. Repeat this step until RTC\_TICKSTS=1
- Set new RTC frequency trim value in Register R218
- Set the RTC\_TICK\_ENA bit to resume normal operation

The applicable register bits are defined in Table 135.

| ADDRESS   | BIT | LABEL          | DEFAULT      | DESCRIPTION  |
|---|-----|----------------|--------------|--|
| R12 (0Ch)<br>Power<br>Mgmt (5)  | 11  | RTC_TICK_ENA   | 1            | Enable RTC counting (instruction only)<br>0 = disabled<br>1 = enabled<br><i>Protected by security key.</i>   |
| R218 (DAh)<br>RTC Tick<br>Control   | 15  |                |              |  |
|   | 14  | RTC_TICKSTS    | 0            | Status of tick request. This bit can be used to ensure the RTC is using the value of RTC_TICK_ENA.<br>0 = disabled<br>1 = enabled<br><i>Protected by security key.</i>   |
|   | 9:0 | RTC_TRIM [9:0] | 00_0000_0000 | RTC frequency trim. Used to adjust the count value of the Tick Gen block to compensate for crystal inaccuracies. RTC frequency trim is a 10bit fixed point <4,6> 2's complement number. MSB Scaling = -8Hz. The register indicates the error (in Hz) with respect to the ideal 32768Hz) of the input crystal frequency. e.g.:<br><br>Actual crystal freq: 32769.00Hz:<br>Required trim 0xb0001_000000 (+1.000000)<br>Actual crystal freq: 32767.00Hz:<br>Required trim 0xb1111_000000 (-1.000000)<br>Actual crystal freq: 32775.58Hz:<br>Required trim 0xb0111_100101 (+7.578125)<br>Actual crystal freq: 32763.78Hz:<br>Required trim 0xb1011_110010 (-4.218750)<br><i>Protected by security key.</i> |
| <b>Note:</b> RTC_TICK_ENA can be accessed through R12 or through R218. Reading from or writing to either register location has the same effect. |     |                |              |  |

**Table 135 Controlling the RTC Frequency Trim**

## 22.4 RTC GPIO OUTPUT

It is possible to configure GPIO6 as an RTC output, as described in Section 20. This output is a square wave that is derived from the trimmed RTC counter. The frequency can be set to values between 1Hz and 16.384kHz, as described in Table 136.

Note that, when RTC\_TRIM is used to calibrate the crystal oscillator, the nominal 50% duty ratio of this output may deviate by up to 8 clock periods of the 32.768kHz oscillator on the occasions when the RTC Seconds Counter is increased (ie. once per second).

| ADDRESS                       | BIT | LABEL         | DEFAULT | DESCRIPTION   |
|-------------------------------|-----|---------------|---------|---|
| R23 (17h)<br>RTC Time control | 3:0 | RTC_DSW [3:0] | 0000    | Divided Square wave select.<br>0000 = disabled<br>0001 = 1Hz<br>0010 = 2Hz<br>...<br>1011 = 1024Hz<br>1100 = 2048Hz<br>1101 = 4096Hz<br>1110 = 8192Hz<br>1111 = 16384Hz<br><br>Note: due to trim settings for crystal intolerances a single square wave period during seconds rollover may be decrease its on time period or increase its off time period by up to 8 32kHz periods. |

Table 136 RTC GPIO Output

## 22.5 RTC INTERRUPTS

The RTC has its own first-level interrupt, RTC\_INT (see Section 24). This comprises three second-level interrupts which indicate periodic events or RTC Alarm conditions.

The RTC raises an RTC\_SEC\_EINT interrupt on every 1 second rollover. An additional periodic interrupt, RTC\_PER\_EINT, is configurable with a frequency determined by the RTC\_PINT field, as defined in Table 138. The RTC\_ALM\_EINT interrupt is triggered by the RTC Alarm function, as described in Section 22.2.4.

These interrupts can be individually masked by setting the applicable mask bit(s) as described in Table 137.

| ADDRESS                                 | BIT | LABEL                                    | DESCRIPTION  |
|---|-----|--|--|
| R25 (19h)<br>Interrupt Status<br>1      | 7   | RTC_PER_EINT                             | RTC periodic interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                             |
|   | 6   | RTC_SEC_EINT                             | RTC 1s rollover complete (1Hz tick).<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                |
|   | 5   | RTC_ALM_EINT                             | RTC alarm etectio.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                                  |
| R33 (21h)<br>Interrupt Status<br>1 Mask | 7:5 | "IM_" + name of respective<br>bit in R25 | Each bit in R33 enables or masks the<br>corresponding bit in R25. The default<br>value for these bits is 0 (unmasked). |

Table 137 RTC Interrupts

| ADDRESS                          | BIT | LABEL             | DEFAULT | DESCRIPTION  |
|----------------------------------|-----|-------------------|---------|--|
| R23 (17h)<br>RTC Time<br>control | 6:4 | RTC_PINT<br>[2:0] | 010     | Selects frequency of periodic interrupt output<br>pulse (32kHz period duration) as shown below.<br>When set time status is high, the periodic<br>output is disabled.<br>000 = disabled<br>001 = 1 sec<br>010 = 1 min<br>011 = 1 hour<br>100 = 1 day<br>101 = 1 month<br>11x = disabled |

Table 138 Configuring RTC Periodic Interrupts

## 23 WATCHDOG TIMER

The WM8350 includes a watchdog timer designed to detect a possible software fault condition where the host processor has locked up. The watchdog timer checks for any write operation to the watchdog control register R4 (04h) or receipt of a heartbeat signal from the host processor on GPIO9 (see Section 20). If neither event occurs within a programmable time, this is interpreted as a fault in the host processor. The watchdog timer then raises an interrupt and/or generates a system reset; the desired response to a watchdog timeout is set using the WDOG\_MODE register field.

If GPIO9 is configured as HEARTBEAT input (GP9\_FN = 0001, GP9\_DIR = 1), then the Watchdog Timer can only be reset by a rising logic level applied to the GPIO9 pin.

If GPIO9 is not configured as HEARTBEAT input, then the Watchdog Timer can only be reset by a write operation to the watchdog control register R4 (04h). If a System reset is triggered by the watchdog timeout, the WM8350 asserts the /RST pin and the /RST and /MEMRST (GPIO) reset signals, resets the internal control registers and then initiates a start-up sequence.

The watchdog timer can be halted for debug purposes using the WDOG\_DEBUG bit. The watchdog can be disabled in Hibernate mode using the WDOG\_HIB\_MODE bit. The watchdog timer duration is set using WDOG\_TO, as described in Table 139.

The Watchdog timeout interrupt event is indicated by the SYS\_WDOG\_TO\_EINT register field. This is one of the second-level interrupts which triggers a first-level System Interrupt, SYS\_INT (see Section 24). This can be masked by setting the mask bit as described in Table 140.

| ADDRESS   | BIT | LABEL              | DEFAULT                                | DESCRIPTION  |
|---|-----|--------------------|--|--|
| R3 (03h)<br>System control 1  | 7   | WDOG_DEBU<br>G     | 0                                      | Halts watchdog timer for system debugging<br>0 = normal operation<br>1 = WDOG halt   |
| R4 (04h)<br>System control 2  | 7   | WDOG_HIB_M<br>ODE  | 0                                      | Watchdog behaviour in HIBERNATE state<br>0 = WDOG disabled in Hibernate<br>1 = WDOG controlled by WDOG_MODE in Hibernate   |
|   | 5:4 | WDOG_MODE<br>[2:0] | Dependan<br>t on<br>CONFIG<br>settings | Watchdog mode<br>00 = Disabled<br>01 = SYS_WDOG_TO interrupt on time-out<br>10 = WKUP_WDOG_RST interrupt and<br>System reset on time-out<br>11 = SYS_WDOG_TO interrupt on first time-<br>out, WKUP_WDOG_RST interrupt and<br>System reset on second time-out.<br><i>Protected by security key.</i> |
|   | 2:0 | WDOG_TO<br>[2:0]   | 101                                    | Watchdog timeout (seconds)<br>The timer is reset to this value when a<br>HEARTBEAT signal edge is detected or the<br>host writes to the watchdog control register.<br>000 = 0.125s<br>... (time doubles with each step)<br>101 = 4s<br>11x = Reserved<br><i>Protected by security key.</i>         |
| R5 (05h)<br>System<br>Hibernate   | 7   | WDOG_HIB_M<br>ODE  | 0                                      | Watchdog behaviour in HIBERNATE state<br>0 = WDOG disabled in Hibernate<br>1 = WDOG controlled by WDOG_MODE in<br>Hibernate  |
| <b>Note:</b> WDOG_HIB_MODE can be accessed through R4 or through R5. Reading from or writing to either register location has the same effect. |     |                    |  |  |

**Table 139 Controlling the Watchdog Timer**

| ADDRESS                                 | BIT | LABEL               | DESCRIPTION   |
|---|-----|---------------------|---|
| R26 (1Ah)<br>Interrupt Status<br>2      | 0   | SYS_WDOG_TO_EINT    | Watchdog timeout has occurred.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
| R34 (22h)<br>Interrupt Status<br>2 Mask | 0   | IM_SYS_WDOG_TO_EINT | Mask bit for Watchdog timer interrupt<br>When set to 1, IM_SYS_WDOG_TO_EINT<br>masks SYS_WDOG_TO_EINT in R26 and<br>does not trigger an SYS_INT interrupt when<br>SYS_WDOG_TO_EINT is set). |

**Table 140 Watchdog Timer Interrupts**

Note that, if GPIO9 is configured as VCC\_FAULT output (GP9\_FN = 0001, GP9\_DIR = 0), then the Watchdog Timer will be configured to expect a HEARTBEAT reset trigger. In this configuration, the Watchdog Reset will never occur and the system may lock up if the Watchdog Mode is enabled.

The Watchdog Timer function cannot be supported if GPIO9 is configured as VCC\_FAULT output. Either the GPIO9 must be reconfigured as some other function, or the Watchdog Timer must remain disabled.

Note that Config Mode 01 selects GPIO9 = VCC\_FAULT by default.



## 24 INTERRUPT CONTROLLER

The WM8350 can send an interrupt signal to the host processor through the IRQ pin. Interrupts can alert the host to a wide range of events and fault conditions. Each of these can be individually enabled or masked. After receiving an interrupt, the host processor can read the interrupt registers in order to determine what caused the interrupt, and take appropriate action if required.

The WM8350 interrupt controller has two levels:

Second-level interrupts indicate a single event in one of the circuit blocks. This is indicated by setting a register bit. This bit is a “sticky” bit - once it is set, it remains at logic 1 until the host processor reads the register. When the processor reads the register, the interrupt bits in that register are cleared. First-level interrupts are the logical OR of several second-level interrupts (usually all the interrupts associated with one particular circuit block). The default polarity of IRQ is active low, meaning that the IRQ signal is the logical NOR of all first-level interrupts.

Individual second-level interrupt bits can be masked, which prevents them from setting the First-level interrupt. (Note that the “sticky” bit will be set as normal, even if that interrupt is masked.)

Individual first-level interrupts can also be masked, preventing them from asserting the IRQ output.

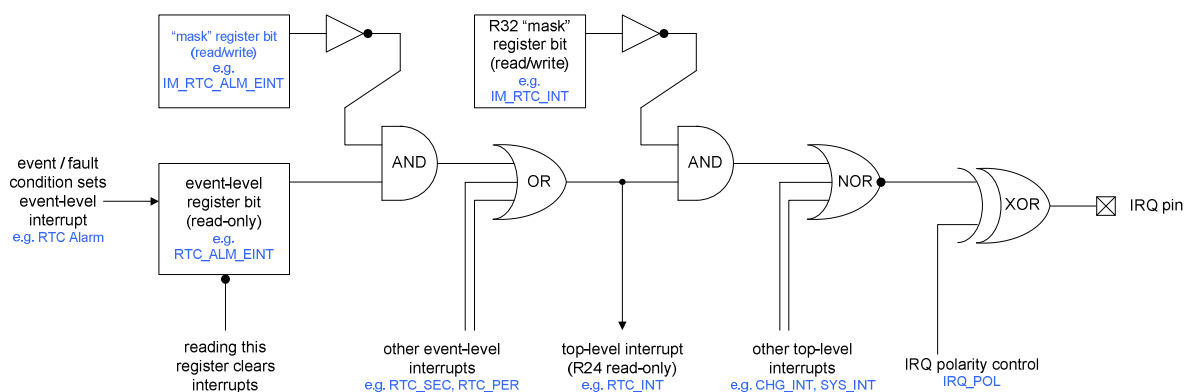


Figure 80 Interrupt Equivalent Logic

To find the cause of an interrupt signal, the host processor should first read the first-level interrupt register R24 to locate the circuit block(s) where the interrupt originated; after that, the precise cause(s) of the interrupt can be determined by reading the second-level interrupt register(s) as appropriate to the indicated first-level interrupt event.

### 24.1 CONFIGURING THE IRQ PIN

The default polarity of IRQ is active low; this can be changed to active high if desired, by writing to the IRQ\_POL bit.

When the WM8350 is in the HIBERNATE state, interrupts can be disabled or can remain active. The desired behaviour can be selected using the IRQ\_HIB\_MODE bit.

| ADDRESS                         | BIT | LABEL            | DEFAULT | DESCRIPTION  |
|---------------------------------|-----|------------------|---------|--|
| R3 (03h)<br>System<br>Control 1 | 0   | IRQ_POL          | 0       | IRQ pin polarity<br>0 = active low (/IRQ)<br>1 = active high (IRQ)                                 |
| R5 (05h)<br>System<br>Hibernate | 3   | IRQ_HIB_MOD<br>E | 0       | IRQ pin state in hibernate mode<br>0 = Normal operation<br>1 = Forced to indicate there is no IRQ. |

Table 141 Interrupts in HIBERNATE State

## 24.2 FIRST-LEVEL INTERRUPTS

Each first level interrupt has a status bit in Register R24, which can be read to determine the origin of an IRQ event.

Each of these bits may be masked by setting the corresponding field in Register R32. By default, the first-level interrupts are all masked.

| ADDRESS                               | BIT  | LABEL                                 | DESCRIPTION  |
|---------------------------------------|------|---------------------------------------|--|
| R24 (18h)<br>System<br>Interrupts     | 13   | OC_INT                                | First-level over-current interrupt.<br>Note: This bit is cleared once read.  |
|                                       | 12   | UV_INT                                | First-level under-voltage interrupt.<br>Note: This bit is cleared once read.   |
|                                       | 9    | CS_INT                                | First-level current sink interrupt.<br>Note: This bit is cleared once read.  |
|                                       | 8    | EXT_INT                               | First-level external interrupt.<br>Note: This bit is cleared once read.  |
|                                       | 7    | CODEC_INT                             | First-level codec interrupt.<br>Note: This bit is cleared once read.   |
|                                       | 6    | GP_INT                                | First-level GPIO interrupt.<br>Note: This bit is cleared once read.  |
|                                       | 5    | AUXADC_INT                            | First-level AUXADC comparator interrupt.<br>Note: This bit is cleared once read.   |
|                                       | 4    | RTC_INT                               | First-level RTC interrupt.<br>Note: This bit is cleared once read.   |
|                                       | 3    | SYS_INT                               | First-level system interrupt.<br>Note: This bit is cleared once read.  |
|                                       | 2    | CHG_INT                               | First-level charger interrupt.<br>Note: This bit is cleared once read.   |
|                                       | 1    | USB_INT                               | First-level USB interrupt.<br>Note: This bit is cleared once read.   |
|                                       | 0    | WKUP_INT                              | First-level wakeup interrupt.<br>Note: This bit is cleared once read.  |
| R32 (20h)<br>System<br>Interrupt Mask | 13:0 | "IM_" + name of respective bit in R25 | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br>Each bit in R32 enables or masks the corresponding bit in R24.<br>The default value for these bits is 1 (masked) |

**Note:** Register is R24 is read-only.

**Table 142 First Level Interrupt Status and Mask Bits**

## 24.3 SECOND-LEVEL INTERRUPTS

The following sections define the second-level interrupt status and control bits associated with each of the first-level bits defined in Table 142.

### 24.3.1 OVERCURRENT INTERRUPT

The first-level OC\_INT interrupt comprises one second-level interrupt for the limit switch. This status bit is in Register R29 and its mask bit is in Register R37, as defined in Table 143.

| ADDRESS  | BIT | LABEL         | DESCRIPTION   |
|--|-----|---------------|---|
| R29 (1Dh)<br>Over Current<br>Interrupt<br>Status | 15  | OC_LS_EINT    | Limit Switch Over-current interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
| R37 (25h)<br>Over Current<br>Interrupt Mask      | 15  | IM_OC_LS_EINT | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br>When IM_OC_LS_EINT is set to 1, then<br>OC_LS_EINT in R29 does not trigger an<br>OC_INT interrupt when set. The default<br>value is 0 (unmasked). |

Table 143 Over-Current Interrupt

### 24.3.2 UNDERVOLTAGE INTERRUPTS

The first-level UV\_INT interrupt comprises several second-level interrupts for the DC-DCs and LDOs. Each of these has a status bit in Register R28 and a mask bit in Register R36, as defined in Table 144.

| ADDRESS   | BIT | LABEL        | DESCRIPTION   |
|---|-----|--------------|---|
| R28 (1Ch)<br>Under Voltage<br>Interrupt<br>Status | 11  | UV_LDO4_EINT | LDO4 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
|   | 10  | UV_LDO3_EINT | LDO3 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
|   | 9   | UV_LDO2_EINT | LDO2 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
|   | 8   | UV_LDO1_EINT | LDO1 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
|   | 5   | UV_DC6_EINT  | DCDC6 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |
|   | 4   | UV_DC5_EINT  | DCDC5 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |
|   | 3   | UV_DC4_EINT  | DCDC4 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |
|   | 2   | UV_DC3_EINT  | DCDC3 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |
|   | 1   | UV_DC2_EINT  | DCDC2 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |

| ADDRESS                                      | BIT  | LABEL                                    | DESCRIPTION  |
|--|------|--|--|
|  | 0    | UV_DC1_EINT                              | DCDC1 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
| R36 (24h)<br>Under Voltage<br>Interrupt Mask | 11:0 | "IM_" + name of respective bit<br>in R28 | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br>Each bit in R36 enables or masks the<br>corresponding bit in R28. The default<br>value for these bits is 0 (unmasked). |

Table 144 Under-Voltage Interrupts

### 24.3.3 CURRENT SINK (LED DRIVER) INTERRUPTS

The first-level CS\_INT interrupt comprises two second-level interrupts for the Current Sink functions. Each of these has a status bit in Register R26 and a mask bit in Register R34, as defined in Table 145.

| ADDRESS                                 | BIT   | LABEL                                    | DESCRIPTION  |
|---|-------|--|--|
| R26 (1Ah)<br>Interrupt Status<br>2      | 13    | CS1_EINT                                 | Flag to indicate drain voltage can no<br>longer be regulated and output current<br>may be out of spec.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                      |
|   | 12    | CS2_EINT                                 | Flag to indicate drain voltage can no<br>longer be regulated and output current<br>may be out of spec.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                      |
| R34 (22h)<br>Interrupt Status<br>2 Mask | 13:12 | "IM_" + name of respective<br>bit in R26 | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br>Each bit in R34 enables or masks the<br>corresponding bit in R26. The default<br>value for these bits is 0 (unmasked). |

Table 145 Current Sink Interrupts

#### 24.3.4 EXTERNAL INTERRUPTS

The first-level EXT\_INT interrupt comprises three second-level interrupts for USB, Wall and Battery supply status. Each of these has a status bit in Register R31 and a mask bit in Register R39, as defined in Table 146. These flags are triggered on the rising and falling edges of the interrupt events.

| ADDRESS   | BIT   | LABEL                                    | DESCRIPTION  |
|---|-------|--|--|
| R31 (1Fh)<br>Comparator<br>Interrupt Status         | 15    | EXT_USB_FB_EINT                          | USB_FB changed interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 14    | EXT_WALL_FB_EINT                         | WALL_FB changed interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.  |
|   | 13    | EXT_BATT_FB_EINT                         | BATT_FB changed interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.  |
| R39 (27h)<br>Comparator<br>Interrupt Status<br>Mask | 15:13 | "IM_" + name of respective bit<br>in R31 | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br>Each bit in R39 enables or masks the<br>corresponding bit in R31. The default<br>value for these bits is 0 (unmasked). |

Table 146 External Interrupts

#### 24.3.5 CODEC INTERRUPTS

The first-level CODEC\_INT interrupt comprises four second-level interrupts for the CODEC. Each of these has a status bit in Register R31 and a mask bit in Register R39, as defined in Table 147. These flags are triggered on the rising and falling edges of the interrupt events.

| ADDRESS   | BIT  | LABEL                                    | DESCRIPTION  |
|---|------|--|--|
| R31 (1Fh)<br>Comparator<br>Interrupt<br>Status      | 11   | CODEC_JCK_DET_L_EINT                     | Left channel Jack detection interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.  |
|   | 10   | CODEC_JCK_DET_R_EINT                     | Right channel Jack detection interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 9    | CODEC_MICSCD_EINT                        | Mic short-circuit detect interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 8    | CODEC_MICD_EINT                          | Mic detect interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.   |
| R39 (27h)<br>Comparator<br>Interrupt<br>Status Mask | 11:8 | "IM_" + name of respective<br>bit in R31 | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br>Each bit in R39 enables or masks the<br>corresponding bit in R31. The default<br>value for these bits is 0 (unmasked). |

Table 147 CODEC Interrupts

### 24.3.6 GPIO INTERRUPTS

The first-level GP\_INT interrupt comprises several second-level interrupts for the 13 GPIO pins. Each of these has a status bit in Register R30 and a mask bit in Register R35, as defined in Table 148.

| ADDRESS                               | BIT  | LABEL                                    | DESCRIPTION  |
|---------------------------------------|------|--|--|
| R30 (1Eh)<br>GPIO Interrupt<br>Status | 12   | GP12_EINT                                | GPIO12 interrupt.<br>(Trigger controlled by GP12 registers.)<br>Note: This bit is cleared once read.   |
|                                       | 11   | GP11_EINT                                | GPIO11 interrupt.<br>(Trigger controlled by GP11 registers.)<br>Note: This bit is cleared once read.   |
|                                       | 10   | GP10_EINT                                | GPIO10 interrupt.<br>(Trigger controlled by GP10 registers.)<br>Note: This bit is cleared once read.   |
|                                       | 9    | GP9_EINT                                 | GPIO9 interrupt.<br>(Trigger controlled by GP9 registers.)<br>Note: This bit is cleared once read.   |
|                                       | 8    | GP8_EINT                                 | GPIO8 interrupt.<br>(Trigger controlled by GP8 registers.)<br>Note: This bit is cleared once read.   |
|                                       | 7    | GP7_EINT                                 | GPIO7 interrupt.<br>(Trigger controlled by GP7 registers.)<br>Note: This bit is cleared once read.   |
|                                       | 6    | GP6_EINT                                 | GPIO6 interrupt.<br>(Trigger controlled by GP6 registers.)<br>Note: This bit is cleared once read.   |
|                                       | 5    | GP5_EINT                                 | GPIO5 interrupt.<br>(Trigger controlled by GP5 registers.)<br>Note: This bit is cleared once read.   |
|                                       | 4    | GP4_EINT                                 | GPIO4 interrupt.<br>(Trigger controlled by GP4 registers.)<br>Note: This bit is cleared once read.   |
|                                       | 3    | GP3_EINT                                 | GPIO3 interrupt.<br>(Trigger controlled by GP3 registers.)<br>Note: This bit is cleared once read.   |
|                                       | 2    | GP2_EINT                                 | GPIO2 interrupt.<br>(Trigger controlled by GP2 registers.)<br>Note: This bit is cleared once read.   |
|                                       | 1    | GP1_EINT                                 | GPIO1 interrupt.<br>(Trigger controlled by GP1 registers.)<br>Note: This bit is cleared once read.   |
|                                       | 0    | GP0_EINT                                 | GPIO0 interrupt.<br>(Trigger controlled by GP0 registers.)<br>Note: This bit is cleared once read.   |
| R38 (26h)<br>GPIO Interrupt<br>Mask   | 12:0 | "IM_" + name of respective bit<br>in R30 | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br>Each bit in R38 enables or masks the<br>corresponding bit in R30. The default<br>value for these bits is 0 (unmasked). |

Table 148 GPIO Interrupts

### 24.3.7 AUXADC AND DIGITAL COMPARATOR INTERRUPTS

The first-level AUXADC\_INT interrupt comprises several second-level interrupts for the auxiliary ADC and associated digital comparators. Each of these has a status bit in Register R26 and a mask bit in Register R34, as defined in Table 149.

| ADDRESS                                 | BIT | LABEL                                 | DESCRIPTION  |
|---|-----|---------------------------------------|--|
| R26 (1Ah)<br>Interrupt<br>Status 2      | 8   | AUXADC_DATARDY_EINT                   | Auxiliary data ready.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 7   | AUXADC_DCOMP4_EINT                    | DCOMP4 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 6   | AUXADC_DCOMP3_EINT                    | DCOMP3 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 5   | AUXADC_DCOMP2_EINT                    | DCOMP2 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 4   | AUXADC_DCOMP1_EINT                    | DCOMP1 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
| R34 (22h)<br>Interrupt<br>Status 2 Mask | 8:4 | "IM_" + name of respective bit in R26 | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br>Each bit in R34 enables or masks the corresponding bit in R26. The default value for these bits is 0 (unmasked). |

Table 149 AUXADC Interrupts

### 24.3.8 RTC INTERRUPTS

The first-level RTC\_INT interrupt comprises three second-level interrupts for the Real Time Clock. Each of these has a status bit in Register R25 and a mask bit in Register R33, as defined in Table 150.

| ADDRESS                                 | BIT | LABEL                                 | DESCRIPTION  |
|---|-----|---------------------------------------|--|
| R25 (19h)<br>Interrupt Status<br>1      | 7   | RTC_PER_EINT                          | RTC periodic interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 6   | RTC_SEC_EINT                          | RTC 1s rollover complete (1Hz tick).<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
|   | 5   | RTC_ALM_EINT                          | RTC alarm etectio.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
| R33 (21h)<br>Interrupt Status<br>1 Mask | 7:5 | "IM_" + name of respective bit in R25 | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br>Each bit in R33 enables or masks the corresponding bit in R25. The default value for these bits is 0 (unmasked). |

Table 150 RTC Interrupts

### 24.3.9 SYSTEM INTERRUPTS

The first-level SYS\_INT interrupt comprises four second-level interrupts for various system events. Each of these has a status bit in Register R26 and a mask bit in Register R34, as defined in Table 151.

| ADDRESS                                 | BIT | LABEL                                    | DESCRIPTION  |
|---|-----|--|--|
| R26 (1Ah)<br>Interrupt Status<br>2      | 3   | SYS_HYST_COMP_FAIL_EI<br>NT              | Hysteresis comparator indication that LINE or BATT is less than shutdown threshold.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 2   | SYS_CHIP_GT115_EINT                      | Chip over 115°C temp limit.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 1   | SYS_CHIP_GT140_EINT                      | Chip over 140°C temp limit.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 0   | SYS_WDOG_TO_EINT                         | Watchdog timeout has occurred.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
| R34 (22h)<br>Interrupt Status<br>2 Mask | 3:0 | "IM_" + name of respective<br>bit in R26 | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br>Each bit in R34 enables or masks the<br>corresponding bit in R26. The default value<br>for these bits is 0 (unmasked). |

Table 151 System Interrupts

### 24.3.10 CHARGER INTERRUPTS

The system interrupt CHG\_INT interrupt comprises several second-level interrupts for the battery charger. Each of these has a status bit in Register R25 and a mask bit in Register R33, as defined in Table 152.

| ADDRESS                            | BIT | LABEL              | DESCRIPTION   |
|------------------------------------|-----|--------------------|---|
| R25 (19h)<br>Interrupt Status<br>1 | 15  | CHG_BATT_HOT_EINT  | Battery temp too hot.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
|                                    | 14  | CHG_BATT_COLD_EINT | Battery temp too cold.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|                                    | 13  | CHG_BATT_FAIL_EINT | Battery fail.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
|                                    | 12  | CHG_TO_EINT        | Charger timeout.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|                                    | 11  | CHG_END_EINT       | Charging final stage.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
|                                    | 10  | CHG_START_EINT     | Charging started.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
|                                    | 9   | CHG_FAST_RDY_EINT  | Indicates that the charger is ready to go<br>into fast charge.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |



| ADDRESS                                 | BIT         | LABEL                                 | DESCRIPTION  |
|---|-------------|---------------------------------------|--|
|   | 2           | CHG_VBATT_LT_3P9_EINT                 | Battery Voltage < 3.9 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
|   | 1           | CHG_VBATT_LT_3P1_EINT                 | Battery voltage < 3.1 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
|   | 0           | CHG_VBATT_LT_2P85_EINT                | Battery voltage < 2.85 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
| R33 (21h)<br>Interrupt Status<br>1 Mask | 15:9<br>2:0 | "IM_" + name of respective bit in R25 | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br>Each bit in R33 enables or masks the corresponding bit in R25. The default value for these bits is 0 (unmasked). |

Table 152 Charger Interrupts

#### 24.3.11 USB INTERRUPTS

The first-level USB\_INT interrupt comprises one second-level interrupt for the USB limit switch. This status bit is in Register R26 and its mask bit is in Register R34, as defined in Table 153.

| ADDRESS                                 | BIT | LABEL             | DESCRIPTION   |
|---|-----|-------------------|---|
| R26 (1Ah)<br>Interrupt<br>Status 2      | 10  | USB_LIMIT_EINT    | USB Limit Switch interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |
| R34 (22h)<br>Interrupt<br>Status 2 Mask | 10  | IM_USB_LIMIT_EINT | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br>When IM_USB_LIMIT_EINT is set to 1, then USB_LIMIT_EINT in R26 does not trigger an USB_INT interrupt when set. The default value is 0 (unmasked). |

Table 153 USB Interrupt

### 24.3.12 WAKE-UP INTERRUPTS

The first-level WKUP\_INT interrupt comprises several second-level interrupts. After a system reset, these indicate to the host processor why the reset occurred. Each wake-up interrupt has a status bit in Register R31 and a mask bit in Register R30, as defined in Table 154.

| ADDRESS   | BIT | LABEL                                 | DESCRIPTION  |
|---|-----|---------------------------------------|--|
| R31 (1Fh)<br>Comparator<br>Interrupt<br>Status      | 6   | WKUP_OFF_STATE_EINT                   | Indicates that the chip started from the OFF state.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 5   | WKUP_HIB_STATE_EINT                   | Indicated the chip started up from the hibernate state.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 4   | WKUP_CONV_FAULT_EINT                  | Indicates the wakeup was caused by a converter fault leading to the chip being reset.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                                 |
|   | 3   | WKUP_WDOG_RST_EINT                    | Indicates the wakeup was caused by a watchdog heartbeat being missed, and hence the chip being reset.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                 |
|   | 2   | WKUP_GP_PWR_ON_EINT                   | PWR_ON (Alternate GPIO function) pin has been pressed for longer than specified time.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                                 |
|   | 1   | WKUP_ONKEY_EINT                       | ON key has been pressed for longer than specified time.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |
|   | 0   | WKUP_GP_WAKEUP_EINT                   | WAKEUP (Alternate GPIO function) pin has been pressed for longer than specified time.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                                 |
| R39 (27h)<br>Comparator<br>Interrupt<br>Status Mask | 6:0 | "IM_" + name of respective bit in R31 | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br>Each bit in R39 enables or masks the corresponding bit in R31. The default value for these bits is 0 (unmasked). |

Table 154 Wake-up Interrupts

## 25 TEMPERATURE SENSING

### 25.1 CHIP TEMPERATURE MONITORING

The WM8350 has a built-in sensor to monitor its internal temperature, with two levels of over-temperature protection.

When the device temperature exceeds the thermal warning temperature, the WM8350 raises a SYS\_CHIP\_GT115\_EINT interrupt. If the chip temperature continues to rise, and exceeds the thermal shutdown temperature, the SYS\_CHIP\_GT140\_EINT interrupt is set and the device shuts down. After a thermal shutdown, the WM8350 can only restart after its temperature has fallen below the restart temperature.

The associated register fields are defined in Table 155.

| ADDRESS                                 | BIT | LABEL                                    | DESCRIPTION  |
|---|-----|--|--|
| R26 (1Ah)<br>Interrupt<br>Status 2      | 2   | SYS_CHIP_GT115_EINT                      | Chip over 115°C temp limit.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                         |
|   | 1   | SYS_CHIP_GT140_EINT                      | Chip over 140°C temp limit.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                         |
| R34 (22h)<br>Interrupt<br>Status 2 Mask | 2:1 | "IM_" + name of respective bit<br>in R26 | Each bit in R34 enables or masks the<br>corresponding bit in R26. The default<br>value for these bits is 0 (unmasked). |

**Table 155 Temperature Sensing Interrupts**

## 26 REGISTER MAP

### 26.1 OVERVIEW

The complete register map is shown below. The detailed description can be found in the relevant text of the device description. The WM8350 can be configured using the Control Interface. All registers not listed and all unused bits should be set to '0'.

Key to characters in brackets: K = protected by key, M = default in metal mask, R = read-only, W = write-only, O = read-only in ROM configs, D = protected by key in development mode, read-only otherwise, n = never reset, p = reset by POR only, s = reset by state machine, sd = reset by state machine except in dev mode, u = reset on UVLO, m = reset on /MEMRST

| REG      | NAME              | 15                         | 14                  | 13               | 12                    | 11                         | 10                   | 9                      | 8               | 7                  | 6                      | 5                          | 4                | 3                | 2                   | 1                   | 0                        | DEFAULT                          |  |  |
|----------|-------------------|----------------------------|---------------------|------------------|-----------------------|----------------------------|----------------------|------------------------|-----------------|--------------------|------------------------|----------------------------|------------------|------------------|---------------------|---------------------|--------------------------|----------------------------------|--|--|
| R0 (0h)  | Reset/ID          | SW_RESET/CHIP_ID[15:0] (n) |                     |                  |                       |                            |                      |                        |                 |                    |                        |                            |                  |                  |                     |                     |                          | 6143h                            |  |  |
| R1 (1h)  | ID                | CHIP_REV[3:0]              |                     |                  |                       | CONF_STS[1:0]              |                      | 0                      | 0               | CUST_ID[7:0]       |                        |                            |                  |                  |                     |                     |                          |                                  |  |  |
| R2 (2h)  | Revision          | 0                          | 0                   | 0                | 0                     | 0                          | 0                    | 0                      | 0               | MASK_REV[7:0]      |                        |                            |                  |                  |                     |                     |                          |                                  |  |  |
| R3 (3h)  | System Control 1  | CHIP_ON<br>(Ms)            | SYS_RST<br>(KMs)    | POWERCYCLE       | VCC_FAULT_OV<br>(Ms)  | RSTB_TO[1:0] (M)           |                      | BG_SLEEP<br>(M)        | 0               | WDOG_DE<br>BUG (K) | CHIP_RES<br>ET_ENA (s) | MEM_VALI<br>D (m)          | CHIP_SET_<br>UP  | ON_DEB_T<br>(K)  | 0                   | ON_POL<br>(KMs)     | IRQ_POL<br>(Ms)          | 1C02h<br>1C02h<br>1C02h<br>1C02h |  |  |
| R4 (4h)  | System Control 2  | USB_SUSP<br>END_8MA<br>(M) | USB_SUSP<br>END (M) | USB_MSTR<br>(Ms) | USB_MSTR<br>_SRC (Ms) | USB_MSTR<br>_500MA<br>(Ms) | USB_NOLI<br>M        | USB_SLV_<br>500MA (Ms) | 0               | WDOG_HIB<br>_MODE  | 0                      | WDOG_MODE[1:0] (KMs)       |                  | 0                | WDOG_TO[2:0] (K)    |                     |                          | 0004h<br>0204h<br>0214h<br>0204h |  |  |
| R5 (5h)  | System Hibernate  | HIBERNAT<br>E (Ms)         | 0                   | 0                | 0                     | 0                          | 0                    | 0                      | 0               | WDOG_HIB<br>_MODE  | HIB_START<br>UP_SEQ    | REG_RESE<br>T_HIB_MO<br>DE | RST_HIB_M<br>ODE | IRQ_HIB_M<br>ODE | MEMRST_H<br>IB_MODE | PCCOMP_<br>HIB_MODE | TEMPMON<br>_HIB_MOD<br>E | 0000h                            |  |  |
| R6 (6h)  | Interface Control | USE_DEV_<br>PINS (s)       | DEV_ADDR[1:0] (s)   |                  | CONFIG_D<br>ONE (s)   | RECONFIG<br>_AT_ON         | 0                    | AUTOINC<br>(s)         | 0               | 0                  | 0                      | 0                          | 0                | SPI_CFG<br>(KM)  | SPI_4WIRE<br>(KM)   | SPI_3WIRE<br>(KM)   | 0                        | 8A00h<br>8A00h<br>8A00h<br>8A00h |  |  |
| R8 (8h)  | Power mgmt (1)    | CODEC_ISEL[1:0]            |                     | VBUF_ENA         | 0                     | 0                          | OUTPUT_D<br>RAIN_ENA | 0                      | MIC_DET_E<br>NA | 0                  | 0                      | BIAS_ENA                   | MICB_ENA         | 0                | VMID_ENA            | VMID[1:0]           |                          | 8000h                            |  |  |
| R9 (9h)  | Power mgmt (2)    | 0                          | 0                   | 0                | 0                     | IN3R_ENA                   | IN3L_ENA             | INR_ENA                | INL_ENA         | MIXINR_EN<br>A     | MIXINL_EN<br>A         | OUT4_ENA                   | OUT3_ENA         | 0                | 0                   | MIXOUTR_<br>ENA     | MIXOUTL_<br>ENA          | 0000h                            |  |  |
| R10 (Ah) | Power mgmt (3)    | 0                          | 0                   | 0                | 0                     | 0                          | 0                    | 0                      | 0               | IN3R_TO_O<br>UT2R  | 0                      | 0                          | 0                | OUT2R_EN<br>A    | OUT2L_EN<br>A       | OUT1R_EN<br>A       | OUT1L_EN<br>A            | 0000h                            |  |  |
| R11 (Bh) | Power mgmt (4)    | 0                          | SYSCLK_E<br>NA      | ADC_HPF_<br>ENA  | 0                     | 0                          | 0                    | 0                      | TOCLK_EN<br>A   | 0                  | 0                      | DACR_ENA                   | DACL_ENA         | ADCR_ENA         | ADCL_ENA            | 0                   | 0                        | 2000h                            |  |  |

| REG       | NAME                           | 15                               | 14                                | 13                                | 12                     | 11                           | 10                           | 9                                | 8                           | 7                          | 6                           | 5                           | 4                            | 3                               | 2                                    | 1                                    | 0  | DEFAULT                          |
|-----------|--------------------------------|----------------------------------|-----------------------------------|-----------------------------------|------------------------|------------------------------|------------------------------|----------------------------------|-----------------------------|----------------------------|-----------------------------|-----------------------------|------------------------------|---------------------------------|--------------------------------------|--------------------------------------|--|----------------------------------|
| R12 (Ch)  | Power mgmt (5)                 | 0                                | 0                                 | 0                                 | CODEC_EN<br>A (s)      | RTC_TICK_<br>ENA (KMs)       | OSC32K_E<br>NA (KMs)         | CHG_ENA<br>(KMs)                 | SW_VRTC_<br>ENA (s)         | AUXADC_E<br>NA (s)         | 0                           | 0                           | 0                            | DCMP4_EN<br>A (s)               | DCMP3_EN<br>A (s)                    | DCMP2_EN<br>A (s)                    | DCMP1_EN<br>A (s)                        | 0E00h<br>0E00h<br>0E00h<br>0E00h |
| R13 (Dh)  | Power mgmt (6)                 | LS_ENA<br>(Ms)                   | 0                                 | 0                                 | 0                      | LDO4_ENA<br>(Ms)             | LDO3_ENA<br>(Ms)             | LDO2_ENA<br>(Ms)                 | LDO1_ENA<br>(Ms)            | 0                          | 0                           | DC6_ENA<br>(Ms)             | DC5_ENA<br>(Ms)              | DC4_ENA<br>(Ms)                 | DC3_ENA<br>(Ms)                      | DC2_ENA<br>(Ms)                      | DC1_ENA<br>(Ms)                          | 0000h                            |
| R14 (Eh)  | Power mgmt (7)                 | 0                                | 0                                 | 0                                 | 0                      | 0                            | 0                            | 0                                | 0                           | 0                          | 0                           | 0                           | 0                            | 0                               | 0                                    | CS2_ENA<br>(s)                       | CS1_ENA<br>(s)                           | 0000h                            |
| R16 (10h) | RTC Seconds/Minutes            | 0                                | RTC_MINS[6:0]                     |                                   |                        |                              |                              |                                  | 0                           | RTC_SECS[6:0]              |                             |                             |                              |                                 |                                      | 0000h                                |  |                                  |
| R17 (11h) | RTC Hours/Day                  | 0                                | 0                                 | 0                                 | 0                      | 0                            | RTC_DAY[2:0]                 |                                  |                             | 0                          | 0                           | RTC_HPM                     | RTC_HRS[4:0]                 |                                 |                                      |                                      | 0100h                                    |                                  |
| R18 (12h) | RTC Date/Month                 | 0                                | 0                                 | 0                                 | RTC_MTH[4:0]           |                              |                              |                                  | 0                           | 0                          | RTC_DATE[5:0]               |                             |                              |                                 |                                      |                                      | 0101h                                    |                                  |
| R19 (13h) | RTC Year                       | 0                                | 0                                 | RTC_YHUNDREDS[5:0]                |                        |                              |                              |                                  | RTC_YUNITS[7:0]             |                            |                             |                             |                              |                                 | 1400h                                |                                      |  |                                  |
| R20 (14h) | Alarm Seconds/Minutes          | 0                                | RTC_ALMMINS[6:0]                  |                                   |                        |                              |                              |                                  | 0                           | RTC_ALMSECS[6:0]           |                             |                             |                              |                                 |                                      | 0000h                                |  |                                  |
| R21 (15h) | Alarm Hours/Day                | 0                                | 0                                 | 0                                 | 0                      | RTC_ALMDAY[3:0]              |                              |                                  | 0                           | 0                          | RTC_ALMH<br>PM              | RTC_ALMHRS[4:0]             |                              |                                 |                                      | 0000h                                |  |                                  |
| R22 (16h) | Alarm Date/Month               | 0                                | 0                                 | 0                                 | RTC_ALMMTH[4:0]        |                              |                              |                                  | 0                           | 0                          | RTC_ALMDATE[5:0]            |                             |                              |                                 |                                      |                                      | 0000h                                    |                                  |
| R23 (17h) | RTC Time Control               | RTC_BCD                          | RTC_12HR                          | 0                                 | 0                      | RTC_SET                      | RTC_STS                      | RTC_ALMS<br>ET                   | RTC_ALMS<br>TS              | 0                          | RTC_PINT[2:0]               |                             |                              | RTC_DSW[3:0]                    |                                      |                                      |  | 0320h                            |
| R24 (18h) | System Interrupts              | 0                                | 0                                 | OC_INT                            | UV_INT                 | 0                            | 0                            | CS_INT                           | EXT_INT                     | CODEC_IN<br>T              | GP_INT                      | AUXADC_I<br>NT              | RTC_INT                      | SYS_INT                         | CHG_INT                              | USB_INT                              | WKUP_INT                                 | 0000h                            |
| R25 (19h) | Interrupt Status 1             | CHG_BATT_<br>HOT_EINT            | CHG_BATT_<br>COLD_EIN<br>T        | CHG_BATT_<br>FAIL_EINT            | CHG_TO_E<br>INT        | CHG_END_<br>EINT             | CHG_STAR<br>T_EINT           | CHG_FAST<br>_RDY_EINT            | 0                           | RTC_PER_<br>EINT           | RTC_SEC_<br>EINT            | RTC_ALM_<br>EINT            | 0                            | 0                               | CHG_VBAT<br>T_LT_3P9_<br>EINT        | CHG_VBAT<br>T_LT_3P1_<br>EINT        | CHG_VBAT<br>T_LT_2P85<br>_EINT           | 0000h                            |
| R26 (1Ah) | Interrupt Status 2             | 0                                | 0                                 | CS1_EINT                          | CS2_EINT               | 0                            | USB_LIMIT<br>_EINT           | 0                                | AUXADC_D<br>ATARDY_EI<br>NT | AUXADC_D<br>COMP4_EI<br>NT | AUXADC_D<br>COMP3_EI<br>NT  | AUXADC_D<br>COMP2_EI<br>NT  | AUXADC_D<br>COMP1_EI<br>NT   | SYS_HYST<br>_COMP_FA<br>IL_EINT | SYS_CHIP_<br>GT115_EIN<br>T          | SYS_CHIP_<br>GT140_EIN<br>T          | SYS_WDO<br>G_TO_EINT                     | 0000h                            |
| R28 (1Ch) | Under Voltage Interrupt status | 0                                | 0                                 | 0                                 | 0                      | UV_LDO4_<br>EINT             | UV_LDO3_<br>EINT             | UV_LDO2_<br>EINT                 | UV_LDO1_<br>EINT            | 0                          | 0                           | UV_DC6_EI<br>NT             | UV_DC5_EI<br>NT              | UV_DC4_EI<br>NT                 | UV_DC3_EI<br>NT                      | UV_DC2_EI<br>NT                      | UV_DC1_EI<br>NT                          | 0000h                            |
| R29 (1Dh) | Over Current Interrupt status  | OC_LS_EIN<br>T                   | 0                                 | 0                                 | 0                      | 0                            | 0                            | 0                                | 0                           | 0                          | 0                           | 0                           | 0                            | 0                               | 0                                    | 0                                    | 0  | 0000h                            |
| R30 (1Eh) | GPIO Interrupt Status          | 0                                | 0                                 | 0                                 | GP12_EINT              | GP11_EINT                    | GP10_EINT                    | GP9_EINT                         | GP8_EINT                    | GP7_EINT                   | GP6_EINT                    | GP5_EINT                    | GP4_EINT                     | GP3_EINT                        | GP2_EINT                             | GP1_EINT                             | GP0_EINT                                 | 0000h                            |
| R31 (1Fh) | Comparator Interrupt Status    | EXT_USB_<br>FB_EINT              | EXT_WALL_<br>_FB_EINT             | EXT_BATT_<br>_FB_EINT             | 0                      | CODEC_JC<br>K_DET_L_E<br>INT | CODEC_JC<br>K_DET_R_<br>EINT | CODEC_MI<br>CSCD_EIN<br>T        | CODEC_MI<br>CD_EINT         | 0                          | WKUP_OFF<br>_STATE_EI<br>NT | WKUP_HIB<br>_STATE_EI<br>NT | WKUP_CO<br>NV_FAULT<br>_EINT | WKUP_WD<br>OG_RST_EI<br>NT      | WKUP_GP_<br>PWR_ON_E<br>INT          | WKUP_ON<br>KEY_EINT                  | WKUP_GP_<br>WAKEUP_E<br>INT              | 0000h                            |
| R32 (20h) | System Interrupts Mask         | 0                                | 0                                 | IM_OC_INT<br>(Ms)                 | IM_UV_INT<br>(Ms)      | 0                            | 0                            | IM_CS_INT<br>(Ms)                | IM_EXT_IN<br>T (Ms)         | IM_CODEC<br>_INT (Ms)      | IM_GP_INT<br>(Ms)           | IM_AUXAD<br>C_INT (Ms)      | IM_RTC_IN<br>T (Ms)          | IM_SYS_IN<br>T (Ms)             | IM_CHG_IN<br>T (Ms)                  | IM_USB_IN<br>T (Ms)                  | IM_WKUP_I<br>NT (Ms)                     | 3FFFh                            |
| R33 (21h) | Interrupt Status 1 Mask        | IM_CHG_B<br>ATT_HOT_<br>EINT (s) | IM_CHG_B<br>ATT_COLD<br>_EINT (s) | IM_CHG_B<br>ATT_FAIL_<br>EINT (s) | IM_CHG_T<br>O_EINT (s) | IM_CHG_E<br>ND_EINT<br>(s)   | IM_CHG_S<br>TART_EINT<br>(s) | IM_CHG_F<br>AST_RDY_<br>EINT (s) | 0                           | IM_RTC_PE<br>R_EINT (s)    | IM_RTC_SE<br>C_EINT (s)     | IM_RTC_AL<br>M_EINT (s)     | 0                            | 0                               | IM_CHG_V<br>BATT_LT_3<br>P9_EINT (s) | IM_CHG_V<br>BATT_LT_3<br>P1_EINT (s) | IM_CHG_V<br>BATT_LT_2<br>P85_EINT<br>(s) | 0000h                            |

| REG       | NAME                                   | 15                            | 14                              | 13                              | 12                   | 11                                  | 10                                  | 9                                | 8                                  | 7                                 | 6                                  | 5                                  | 4                                   | 3   | 2                                     | 1                                  | 0                                  | DEFAULT         |       |
|-----------|--|-------------------------------|---------------------------------|---------------------------------|----------------------|-------------------------------------|-------------------------------------|----------------------------------|------------------------------------|-----------------------------------|------------------------------------|------------------------------------|-------------------------------------|---|---------------------------------------|------------------------------------|------------------------------------|-----------------|-------|
| R34 (22h) | Interrupt Status 2 Mask                | 0                             | 0                               | IM_CS1_EI<br>NT (s)             | IM_CS2_EI<br>NT (s)  | 0                                   | IM_USB_LI<br>MIT_EINT<br>(s)        | 0                                | IM_AUXAD<br>C_DATARD<br>Y_EINT (s) | IM_AUXAD<br>C_DCOMP4<br>_EINT (s) | IM_AUXAD<br>C_DCOMP3<br>_EINT (s)  | IM_AUXAD<br>C_DCOMP2<br>_EINT (s)  | IM_AUXAD<br>C_DCOMP1<br>_EINT (s)   | IM_SYS_HY<br>ST_COMP_<br>FAIL_EINT<br>(s) | IM_SYS_C<br>HIP_GT115<br>_EINT (s)    | IM_SYS_C<br>HIP_GT140<br>_EINT (s) | IM_SYS_W<br>DOG_TO_E<br>INT (s)    | 0000h           |       |
| R36 (24h) | Under Voltage Interrupt<br>status Mask | 0                             | 0                               | 0                               | 0                    | IM_UV_LD<br>O4_EINT (s)             | IM_UV_LD<br>O3_EINT (s)             | IM_UV_LD<br>O2_EINT (s)          | IM_UV_LD<br>O1_EINT (s)            | 0                                 | 0                                  | IM_UV_DC6<br>_EINT (s)             | IM_UV_DC5<br>_EINT (s)              | IM_UV_DC4<br>_EINT (s)                    | IM_UV_DC3<br>_EINT (s)                | IM_UV_DC2<br>_EINT (s)             | IM_UV_DC1<br>_EINT (s)             | 0000h           |       |
| R37 (25h) | Over Current Interrupt<br>status Mask  | IM_OC_LS_<br>EINT (s)         | 0                               | 0                               | 0                    | 0                                   | 0                                   | 0                                | 0                                  | 0                                 | 0                                  | 0                                  | 0                                   | 0   | 0                                     | 0                                  | 0                                  | 0000h           |       |
| R38 (26h) | GPIO Interrupt Status<br>Mask          | 0                             | 0                               | 0                               | IM_GP12_E<br>INT (s) | IM_GP11_E<br>INT (s)                | IM_GP10_E<br>INT (s)                | IM_GP9_EI<br>NT (s)              | IM_GP8_EI<br>NT (s)                | IM_GP7_EI<br>NT (s)               | IM_GP6_EI<br>NT (s)                | IM_GP5_EI<br>NT (s)                | IM_GP4_EI<br>NT (s)                 | IM_GP3_EI<br>NT (s)                       | IM_GP2_EI<br>NT (s)                   | IM_GP1_EI<br>NT (s)                | IM_GP0_EI<br>NT (s)                | 0000h           |       |
| R39 (27h) | Comparator Interrupt<br>Status Mask    | IM_EXT_US<br>B_FB_EINT<br>(s) | IM_EXT_W<br>ALL_FB_EI<br>NT (s) | IM_EXT_BA<br>TT_FB_EIN<br>T (s) | 0                    | IM_CODEC<br>_JCK_DET_<br>L_EINT (s) | IM_CODEC<br>_JCK_DET_<br>R_EINT (s) | IM_CODEC<br>_MICSCD_<br>EINT (s) | IM_CODEC<br>_MICD_EIN<br>T (s)     | 0                                 | IM_WKUP_<br>OFF_STAT<br>E_EINT (s) | IM_WKUP_<br>HIB_STATE<br>_EINT (s) | IM_WKUP_<br>CONV_FAU<br>LT_EINT (s) | IM_WKUP_<br>WDOG_RS<br>T_EINT (s)         | IM_WKUP_<br>GP_PWR_<br>ON_EINT<br>(s) | IM_WKUP_<br>ONKEY_EI<br>NT (s)     | IM_WKUP_<br>GP_WAKE<br>UP_EINT (s) | 0000h           |       |
| R40 (28h) | Clock Control 1                        | TOCLK_EN<br>A                 | TOCLK_RA<br>TE                  | 0                               | 0                    | MCLK_SEL                            | 0                                   | 0                                | MCLK_DIV                           | BCLK_DIV[3:0]                     |                                    |                                    | 0                                   | OPCLK_DIV[2:0]                            |                                       |                                    | 0040h                              |                 |       |
| R41 (29h) | Clock Control 2                        | LRC_ADC_<br>SEL               | 0                               | 0                               | 0                    | 0                                   | 0                                   | 0                                | 0                                  | 0                                 | 0                                  | 0                                  | 0                                   | 0   | 0                                     | 0                                  | MCLK_DIR                           | 0000h           |       |
| R42 (2Ah) | FLL Control 1                          | FLL_ENA                       | FLL_OSC_<br>ENA                 | 1                               | 1                    | 1                                   | FLL_OUTDIV[2:0]                     |                                  |                                    | FLL_RSP_RATE[3:0]                 |                                    |                                    | 0                                   | FLL_RATE[2:0]                             |                                       |                                    | 3A00h                              |                 |       |
| R43 (2Bh) | FLL Control 2                          | FLL_RATIO[4:0]                |                                 |                                 |                      |                                     | 0                                   | FLL_N[9:0]                       |                                    |                                   |                                    |                                    |                                     |   |                                       |                                    |                                    |                 | 7086h |
| R44 (2Ch) | FLL Control 3                          | FLL_K[15:0]                   |                                 |                                 |                      |                                     |                                     |                                  |                                    |                                   |                                    |                                    |                                     |   |                                       |                                    |                                    |                 | C226h |
| R45 (2Dh) | FLL Control 4                          | 0                             | 0                               | 0                               | 0                    | 0                                   | 0                                   | 0                                | 0                                  | FLL_REF_F<br>REQ                  | 0                                  | FLL_FRAC                           | 0                                   | 0   | 0                                     | 0                                  | FLL_CLK_SRC[1:0]                   | 0000h           |       |
| R48 (30h) | DAC Control                            | 0                             | 0                               | DAC_MON<br>O                    | AIF_LRCLK<br>RATE    | 0                                   | 0                                   | 0                                | 0                                  | 0                                 | 0                                  | DEEMP[1:0]                         |                                     | DAC_SDMC<br>LK_RATE                       | 0                                     | DACL_DATI<br>NV                    | DACR_DAT<br>INV                    | 0000h           |       |
| R50 (32h) | DAC Digital Volume L                   | DACL_ENA                      | 0                               | 0                               | 0                    | 0                                   | 0                                   | 0                                | DAC_VU                             | DACL_VOL[7:0]                     |                                    |                                    |                                     |   |                                       |                                    |                                    | 00C0h           |       |
| R51 (33h) | DAC Digital Volume R                   | DACR_ENA                      | 0                               | 0                               | 0                    | 0                                   | 0                                   | 0                                | DAC_VU                             | DACR_VOL[7:0]                     |                                    |                                    |                                     |   |                                       |                                    |                                    | 00C0h           |       |
| R53 (35h) | DAC LR Rate                            | 0                             | 0                               | 0                               | 0                    | DACLRC_E<br>NA                      | DACLRC_RATE[10:0]                   |                                  |                                    |                                   |                                    |                                    |                                     |   |                                       |                                    |                                    | 0040h           |       |
| R54 (36h) | DAC Clock Control                      | 0                             | 0                               | 0                               | 0                    | 0                                   | 0                                   | 0                                | 0                                  | 0                                 | 0                                  | 0                                  | DACCLK_P<br>OL                      | 0   | DAC_CLKDIV[2:0]                       |                                    |                                    | 0000h           |       |
| R58 (3Ah) | DAC Mute                               | 0                             | DAC_MUTE                        | 0                               | 0                    | 0                                   | 0                                   | 0                                | 0                                  | 0                                 | 0                                  | 0                                  | 0                                   | 0   | 0                                     | 0                                  | 0                                  | 4000h           |       |
| R59 (3Bh) | DAC Mute Volume                        | 0                             | DAC_MUTE<br>MODE                | DAC_MUTE<br>RATE                | DAC_SB_FI<br>LT      | 0                                   | 0                                   | 0                                | 0                                  | 0                                 | 0                                  | 0                                  | 0                                   | 0   | 0                                     | 0                                  | 0                                  | 0000h           |       |
| R60 (3Ch) | DAC Side                               | 0                             | 0                               | ADC_TO_DACL[1:0]                |                      | ADC_TO_DACR[1:0]                    |                                     | 0                                | 0                                  | 0                                 | 0                                  | 0                                  | 0                                   | 0   | 0                                     | 0                                  | 0                                  | 0000h           |       |
| R64 (40h) | ADC Control                            | ADC_HPF_<br>ENA               | 0                               | 0                               | 0                    | 0                                   | 0                                   | ADC_HPF_CUT[1:0]                 |                                    |                                   | 0                                  | 0                                  | 0                                   | 0   | 0                                     | 0                                  | ADCL_DATI<br>NV                    | ADCR_DAT<br>INV | 8000h |
| R66 (42h) | ADC Digital Volume L                   | ADCL_ENA                      | 0                               | 0                               | 0                    | 0                                   | 0                                   | 0                                | ADC_VU                             | ADCL_VOL[7:0]                     |                                    |                                    |                                     |   |                                       |                                    |                                    | 00C0h           |       |

| REG        | NAME                     | 15                    | 14             | 13       | 12                  | 11                    | 10                | 9                  | 8                  | 7                    | 6              | 5               | 4                    | 3                    | 2                   | 1                   | 0                   | DEFAULT             |       |
|------------|--------------------------|-----------------------|----------------|----------|---------------------|-----------------------|-------------------|--------------------|--------------------|----------------------|----------------|-----------------|----------------------|----------------------|---------------------|---------------------|---------------------|---------------------|-------|
| R67 (43h)  | ADC Digital Volume R     | ADCR_ENA              | 0              | 0        | 0                   | 0                     | 0                 | 0                  | ADC_VU             | ADCR_VOL[7:0]        |                |                 |                      |                      |                     |                     | 00C0h               |                     |       |
| R68 (44h)  | ADC Divider              | 0                     | 0              | 0        | 0                   | ADCL_DAC_SVOL[3:0]    |                   |                    | ADCR_DAC_SVOL[3:0] |                      |                | ADCCLK_P<br>OL  | ADC_CLKDIV[2:0]      |                      |                     | 0000h               |                     |                     |       |
| R70 (46h)  | ADC LR Rate              | 0                     | 0              | 0        | 0                   | ADCLRC_E<br>NA        | ADCLRC_RATE[10:0] |                    |                    |                      |                |                 |                      |                      |                     |                     |                     | 0040h               |       |
| R72 (48h)  | Input Control            | 0                     | 0              | 0        | 0                   | 0                     | IN2R_ENA          | IN1RN_ENA          | IN1RP_ENA          | 0                    | 0              | 0               | 0                    | 0                    | IN2L_ENA            | IN1LN_ENA           | IN1LP_ENA           | 0303h               |       |
| R73 (49h)  | IN3 Input Control        | IN3R_ENA              | IN3R_SHO<br>RT | 0        | 0                   | 0                     | 0                 | 0                  | 0                  | IN3L_ENA             | IN3L_SHOR<br>T | 0               | 0                    | 0                    | 0                   | 0                   | 0                   | 0000h               |       |
| R74 (4Ah)  | Mic Bias Control         | MICB_ENA              | MICB_SEL       | 0        | 0                   | 0                     | 0                 | 0                  | 0                  | MIC_DET_E<br>NA      | 0              | 0               | MCDTHR[2:0]          |                      | MCDSCTHR[1:0]       |                     | 0000h               |                     |       |
| R76 (4Ch)  | Output Control           | 0                     | 0              | 0        | 0                   | OUT4_VRO<br>I         | OUT3_VRO<br>I     | OUT2_VRO<br>I      | OUT1_VRO<br>I      | 0                    | 0              | 0               | OUTPUT_D<br>RAIN_ENA | 0                    | OUT2_FB             | 0                   | OUT1_FB             | 0000h               |       |
| R77 (4Dh)  | Jack Detect              | JDL_ENA               | JDR_ENA        | 0        | 0                   | 0                     | 0                 | 0                  | 0                  | 0                    | 0              | 0               | 0                    | 0                    | 0                   | 0                   | 0                   | 0000h               |       |
| R78 (4Eh)  | Anti Pop Control         | 0                     | 0              | 0        | 0                   | 0                     | 0                 | ANTI_POP[1:0]      |                    | DIS_OP_LN4[1:0]      |                | DIS_OP_LN3[1:0] |                      | DIS_OP_OUT2[1:0]     |                     | DIS_OP_OUT1[1:0]    |                     | 0000h               |       |
| R80 (50h)  | Left Input Volume        | INL_ENA               | INL_MUTE       | INL_ZC   | 0                   | 0                     | 0                 | 0                  | IN_VU              | INL_VOL[5:0]         |                |                 |                      |                      |                     | 0                   | 0                   | 0040h               |       |
| R81 (51h)  | Right Input Volume       | INR_ENA               | INR_MUTE       | INR_ZC   | 0                   | 0                     | 0                 | 0                  | IN_VU              | INR_VOL[5:0]         |                |                 |                      |                      |                     | 0                   | 0                   | 0040h               |       |
| R88 (58h)  | Left Mixer Control       | MIXOUTL_<br>ENA       | 0              | 0        | DACR_TO_<br>MIXOUTL | DACL_TO_<br>MIXOUTL   | 0                 | 0                  | 0                  | 0                    | 0              | 0               | 0                    | 0                    | IN3L_TO_M<br>IXOUTL | INR_TO_MI<br>XOUTL  | INL_TO_MI<br>XOUTL  | 0800h               |       |
| R89 (59h)  | Right Mixer Control      | MIXOUTR_<br>ENA       | 0              | 0        | DACR_TO_<br>MIXOUTR | DACL_TO_<br>MIXOUTR   | 0                 | 0                  | 0                  | 0                    | 0              | 0               | 0                    | 0                    | IN3R_TO_M<br>IXOUTR | 0                   | INR_TO_MI<br>XOUTR  | INL_TO_MI<br>XOUTR  | 1000h |
| R92 (5Ch)  | OUT3 Mixer Control       | OUT3_ENA              | 0              | 0        | 0                   | DACL_TO_<br>OUT3      | 0                 | 0                  | MIXINL_TO_<br>OUT3 | 0                    | 0              | 0               | 0                    | 0                    | OUT4_TO_<br>OUT3    | 0                   | 0                   | MIXOUTL_T<br>O_OUT3 | 0000h |
| R93 (5Dh)  | OUT4 Mixer Control       | OUT4_ENA              | 0              | 0        | DACR_TO_<br>OUT4    | DACL_TO_<br>OUT4      | OUT4_ATT<br>N     | MIXINR_TO_<br>OUT4 | 0                  | 0                    | 0              | 0               | 0                    | 0                    | OUT3_TO_<br>OUT4    | MIXOUTR_<br>TO_OUT4 | MIXOUTL_T<br>O_OUT4 | 0000h               |       |
| R96 (60h)  | Output Left Mixer Volume | 0                     | 0              | 0        | 0                   | IN3L_MIXOUTL_VOL[2:0] |                   |                    | 0                  | INR_MIXOUTL_VOL[2:0] |                |                 | 0                    | INL_MIXOUTL_VOL[2:0] |                     |                     | 0                   | 0000h               |       |
| R97 (61h)  | Output Right Mixer       | IN3R_MIXOUTR_VOL[2:0] |                |          | 0                   | 0                     | 0                 | 0                  | 0                  | INR_MIXOUTR_VOL[2:0] |                |                 | 0                    | INL_MIXOUTR_VOL[2:0] |                     |                     | 0                   | 0000h               |       |
| R98 (62h)  | Input Mixer Volume L     | 0                     | 0              | 0        | 0                   | IN3L_MIXINL_VOL[2:0]  |                   |                    | 0                  | 0                    | 0              | 0               | IN2L_MIXINL_VOL[2:0] |                      |                     | INL_MIXINL_<br>VOL  | 0000h               |                     |       |
| R99 (63h)  | Input Mixer Volume R     | IN3R_MIXINR_VOL[2:0]  |                |          | 0                   | 0                     | 0                 | 0                  | 0                  | IN2R_MIXINR_VOL[2:0] |                |                 | 0                    | 0                    | 0                   | 0                   | INR_MIXIN<br>R_VOL  | 0000h               |       |
| R100 (64h) | Input Mixer Volume       | OUT4_MIXI<br>N_DST    | 0              | 0        | 0                   | 0                     | 0                 | 0                  | 0                  | 0                    | 0              | 0               | 0                    | OUT4_MIXIN_VOL[2:0]  |                     |                     | 0                   | 0000h               |       |
| R104 (68h) | OUT1L Volume             | OUT1L_EN<br>A         | OUT1L_MU<br>TE | OUT1L_ZC | 0                   | 0                     | 0                 | 0                  | OUT1_VU            | OUT1L_VOL[5:0]       |                |                 |                      |                      |                     | 0                   | 0                   | 00E4h               |       |
| R105 (69h) | OUT1R Volume             | OUT1R_EN<br>A         | OUT1R_MU<br>TE | OUT1R_ZC | 0                   | 0                     | 0                 | 0                  | OUT1_VU            | OUT1R_VOL[5:0]       |                |                 |                      |                      |                     | 0                   | 0                   | 00E4h               |       |
| R106 (6Ah) | OUT2L Volume             | OUT2L_EN<br>A         | OUT2L_MU<br>TE | OUT2L_ZC | 0                   | 0                     | 0                 | 0                  | OUT2_VU            | OUT2L_VOL[5:0]       |                |                 |                      |                      |                     | 0                   | 0                   | 00E4h               |       |

| REG        | NAME                     | 15               | 14         | 13       | 12                | 11                | 10                | 9                | 8                | 7                   | 6                | 5                | 4                | 3                | 2                | 1                | 0                | DEFAULT                          |       |
|------------|--------------------------|------------------|------------|----------|-------------------|-------------------|-------------------|------------------|------------------|---------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|----------------------------------|-------|
| R107 (6Bh) | OUT2R Volume             | OUT2R_ENA        | OUT2R_MUTE | OUT2R_ZC | 0                 | 0                 | OUT2R_INV         | OUT2R_INV_MUTE   | OUT2_VU          | OUT2R_VOL[5:0]      |                  |                  |                  |                  |                  |                  | 0                | 0                                | 02E4h |
| R111 (6Fh) | BEEP Volume              | IN3R_TO_OUT2R    | 0          | 0        | 0                 | 0                 | 0                 | 0                | 0                | IN3R_OUT2R_VOL[2:0] |                  |                  | 0                | 0                | 0                | 0                | 0                | 0000h                            |       |
| R112 (70h) | AI Formating             | AIF_BCLK_INV     | 0          | AIF_TRI  | AIF_LRCLK_INV     | AIF_WL[1:0]       |                   | AIF_FMT[1:0]     |                  | 0                   | 0                | 0                | 0                | 0                | 0                | 0                | 0                | 0A00h                            |       |
| R113 (71h) | ADC DAC COMP             | 0                | 0          | 0        | 0                 | 0                 | 0                 | 0                | 0                | DAC_COMP            | DAC_COMP_MODE    | ADC_COMP         | ADC_COMP_MODE    | 0                | 0                | 0                | LOOPBACK         | 0000h                            |       |
| R114 (72h) | AI ADC Control           | 0                | 0          | 0        | 0                 | 0                 | 0                 | 0                | 0                | AIFADC_PD           | AIFADCL_SRC      | AIFADCR_SRC      | AIFADC_TM_CHAN   | AIFADC_TM        | 0                | 0                | 0                | 0020h                            |       |
| R115 (73h) | AI DAC Control           | 0                | BCLK_MSTR  | 0        | 0                 | 0                 | 0                 | 0                | 0                | AIFDAC_PD           | DACL_SRC         | DACR_SRC         | AIFDAC_TM_CHAN   | AIFDAC_TM        | 0                | DAC_BOOST[1:0]   |                  | 0020h                            |       |
| R128 (80h) | GPIO Debounce            | 0                | 0          | 0        | GP12_DB (s)       | GP11_DB (s)       | GP10_DB (s)       | GP9_DB (s)       | GP8_DB (s)       | GP7_DB (s)          | GP6_DB (s)       | GP5_DB (s)       | GP4_DB (s)       | GP3_DB (s)       | GP2_DB (s)       | GP1_DB (s)       | GP0_DB (s)       | 1FFFh                            |       |
| R129 (81h) | GPIO Pin pull up Control | 0                | 0          | 0        | GP12_PU (Ms)      | GP11_PU (Ms)      | GP10_PU (Ms)      | GP9_PU (Ms)      | GP8_PU (Ms)      | GP7_PU (Ms)         | GP6_PU (Ms)      | GP5_PU (Ms)      | GP4_PU (Ms)      | GP3_PU (Ms)      | GP2_PU (Ms)      | GP1_PU (Ms)      | GP0_PU (Ms)      | 0000h<br>0000h<br>0000h<br>0010h |       |
| R130 (82h) | GPIO Pull down Control   | 0                | 0          | 0        | GP12_PD (Ms)      | GP11_PD (Ms)      | GP10_PD (Ms)      | GP9_PD (Ms)      | GP8_PD (Ms)      | GP7_PD (Ms)         | GP6_PD (Ms)      | GP5_PD (Ms)      | GP4_PD (Ms)      | GP3_PD (Ms)      | GP2_PD (Ms)      | GP1_PD (Ms)      | GP0_PD (Ms)      | 0000h<br>0000h<br>0110h<br>0000h |       |
| R131 (83h) | GPIO Interrupt Mode      | 0                | 0          | 0        | GP12_INTM ODE (s) | GP11_INTM ODE (s) | GP10_INTM ODE (s) | GP9_INTM ODE (s) | GP8_INTM ODE (s) | GP7_INTM ODE (s)    | GP6_INTM ODE (s) | GP5_INTM ODE (s) | GP4_INTM ODE (s) | GP3_INTM ODE (s) | GP2_INTM ODE (s) | GP1_INTM ODE (s) | GP0_INTM ODE (s) | 0000h                            |       |
| R133 (85h) | GPIO Control             | 0                | 0          | 0        | 0                 | 0                 | 0                 | 0                | 0                | GP_DBTIME[1:0] (s)  |                  | 0                | 0                | 0                | 0                | 0                | 0                | 0000h                            |       |
| R134 (86h) | GPIO Configuration (i/o) | 0                | 0          | 0        | GP12_DIR (Ms)     | GP11_DIR (Ms)     | GP10_DIR (Ms)     | GP9_DIR (Ms)     | GP8_DIR (Ms)     | GP7_DIR (Ms)        | GP6_DIR (Ms)     | GP5_DIR (Ms)     | GP4_DIR (Ms)     | GP3_DIR (Ms)     | GP2_DIR (Ms)     | GP1_DIR (Ms)     | GP0_DIR (Ms)     | 0FFCh<br>0CFFh<br>09FAh<br>0BFBh |       |
| R135 (87h) | GPIO Pin Polarity / Type | 0                | 0          | 0        | GP12_CFG (Ms)     | GP11_CFG (Ms)     | GP10_CFG (Ms)     | GP9_CFG (Ms)     | GP8_CFG (Ms)     | GP7_CFG (Ms)        | GP6_CFG (Ms)     | GP5_CFG (Ms)     | GP4_CFG (Ms)     | GP3_CFG (Ms)     | GP2_CFG (Ms)     | GP1_CFG (Ms)     | GP0_CFG (Ms)     | 0FFCh<br>0C1Fh<br>0DF6h<br>0FFDh |       |
| R140 (8Ch) | GPIO Function Select 1   | GP3_FN[3:0] (Ms) |            |          |                   | GP2_FN[3:0] (Ms)  |                   |                  |                  | GP1_FN[3:0] (Ms)    |                  |                  |                  | GP0_FN[3:0] (Ms) |                  |                  |                  | 0013h<br>0000h<br>1310h<br>0310h |       |



| REG        | NAME                       | 15                    | 14                 | 13                       | 12                  | 11                         | 10                    | 9 | 8 | 7                | 6               | 5               | 4               | 3                 | 2                | 1                   | 0                  | DEFAULT                          |
|------------|----------------------------|-----------------------|--------------------|--------------------------|---------------------|----------------------------|-----------------------|---|---|------------------|-----------------|-----------------|-----------------|-------------------|------------------|---------------------|--------------------|----------------------------------|
| R141 (8Dh) | GPIO Function Select 2     | GP7_FN[3:0] (Ms)      |                    |                          |                     | GP6_FN[3:0] (Ms)           |                       |   |   | GP5_FN[3:0] (Ms) |                 |                 |                 | GP4_FN[3:0] (Ms)  |                  |                     |                    | 0000h<br>1110h<br>0003h<br>0001h |
| R142 (8Eh) | GPIO Function Select 3     | GP11_FN[3:0] (Ms)     |                    |                          |                     | GP10_FN[3:0] (Ms)          |                       |   |   | GP9_FN[3:0] (Ms) |                 |                 |                 | GP8_FN[3:0] (Ms)  |                  |                     |                    | 0000h<br>0013h<br>2000h<br>2300h |
| R143 (8Fh) | GPIO Function Select 4     | 0                     | 0                  | 0                        | 0                   | 0                          | 0                     | 0 | 0 | 0                | 0               | 0               | 0               | GP12_FN[3:0] (Ms) |                  |                     |                    | 0003h<br>0003h<br>0000h<br>0003h |
| R144 (90h) | Digitiser Control (1)      | AUXADC_ENA (s)        | AUXADC_CTC (s)     | AUXADC_POLL (s)          | AUXADC_HIB_MODE (s) | 0                          | 0                     | 0 | 0 | AUXADC_SEL8 (s)  | AUXADC_SEL7 (s) | AUXADC_SEL6 (s) | AUXADC_SEL5 (s) | AUXADC_SEL4 (s)   | AUXADC_SEL3 (s)  | AUXADC_SEL2 (s)     | AUXADC_SEL1 (s)    | 0000h                            |
| R145 (91h) | Digitiser Control (2)      | 0                     | 0                  | AUXADC_MASKMODE[1:0] (s) |                     | 0                          | AUXADC_CRATE[2:0] (s) |   |   | 0                | 0               | 0               | 0               | 0                 | AUXADC_CFGAL (s) | AUXADC_CFGBMODE (s) | AUXADC_CFGWAIT (s) | 0002h                            |
| R152 (98h) | AUX1 Readback              | 0                     | AUXADC_SCALE1[1:0] |                          | AUXADC_REFF1        | AUXADC_DATA1[11:0]         |                       |   |   |                  |                 |                 |                 |                   |                  |                     |                    | 7000h                            |
| R153 (99h) | AUX2 Readback              | 0                     | AUXADC_SCALE2[1:0] |                          | AUXADC_REFF2        | AUXADC_DATA2[11:0]         |                       |   |   |                  |                 |                 |                 |                   |                  |                     |                    | 7000h                            |
| R154 (9Ah) | AUX3 Readback              | 0                     | AUXADC_SCALE3[1:0] |                          | AUXADC_REFF3        | AUXADC_DATA3[11:0]         |                       |   |   |                  |                 |                 |                 |                   |                  |                     |                    | 7000h                            |
| R155 (9Bh) | AUX4 Readback              | 0                     | AUXADC_SCALE4[1:0] |                          | AUXADC_REFF4        | AUXADC_DATA4[11:0]         |                       |   |   |                  |                 |                 |                 |                   |                  |                     |                    | 7000h                            |
| R156 (9Ch) | USB Voltage Readback       | 0                     | 0                  | 0                        | 0                   | AUXADC_DATA_USB[11:0]      |                       |   |   |                  |                 |                 |                 |                   |                  |                     |                    | 0000h                            |
| R157 (9Dh) | LINE Voltage Readback      | 0                     | 0                  | 0                        | 0                   | AUXADC_DATA_LINE[11:0]     |                       |   |   |                  |                 |                 |                 |                   |                  |                     |                    | 0000h                            |
| R158 (9Eh) | BATT Voltage Readback      | 0                     | 0                  | 0                        | 0                   | AUXADC_DATA_BATT[11:0]     |                       |   |   |                  |                 |                 |                 |                   |                  |                     |                    | 0000h                            |
| R159 (9Fh) | Chip Temp Readback         | 0                     | 0                  | 0                        | 0                   | AUXADC_DATA_CHIPTEMP[11:0] |                       |   |   |                  |                 |                 |                 |                   |                  |                     |                    | 0000h                            |
| R163 (A3h) | Generic Comparator Control | 0                     | 0                  | 0                        | 0                   | 0                          | 0                     | 0 | 0 | 0                | 0               | 0               | 0               | DCMP4_ENA (s)     | DCMP3_ENA (s)    | DCMP2_ENA (s)       | DCMP1_ENA (s)      | 0000h                            |
| R164 (A4h) | Generic comparator 1       | DCMP1_SRCSEL[2:0] (s) |                    |                          | DCMP1_GT            | DCMP1_THR[11:0]            |                       |   |   |                  |                 |                 |                 |                   |                  |                     |                    | 0000h                            |
| R165 (A5h) | Generic comparator 2       | DCMP2_SRCSEL[2:0] (s) |                    |                          | DCMP2_GT            | DCMP2_THR[11:0]            |                       |   |   |                  |                 |                 |                 |                   |                  |                     |                    | 0000h                            |
| R166 (A6h) | Generic comparator 3       | DCMP3_SRCSEL[2:0] (s) |                    |                          | DCMP3_GT            | DCMP3_THR[11:0]            |                       |   |   |                  |                 |                 |                 |                   |                  |                     |                    | 0000h                            |
| R167 (A7h) | Generic comparator 4       | DCMP4_SRCSEL[2:0] (s) |                    |                          | DCMP4_GT            | DCMP4_THR[11:0]            |                       |   |   |                  |                 |                 |                 |                   |                  |                     |                    | 0000h                            |

| REG        | NAME                      | 15                   | 14                | 13                   | 12                   | 11                 | 10            | 9                            | 8                           | 7                     | 6                       | 5                     | 4                           | 3                 | 2                      | 1                     | 0                                | DEFAULT                          |       |
|------------|---------------------------|----------------------|-------------------|----------------------|----------------------|--------------------|---------------|------------------------------|-----------------------------|-----------------------|-------------------------|-----------------------|-----------------------------|-------------------|------------------------|-----------------------|----------------------------------|----------------------------------|-------|
| R168 (A8h) | Battery Charger Control 1 | CHG_ENA (KMs)        | 0                 | 0                    | CHG_EOC_SEL[2:0] (K) |                    |               | CHG_TRIC_KLE_TEMP_CHOKE (Ks) | CHG_TRIC_KLE_USB_CHOKE (Ks) | CHG_REC_OVER_T (Ks)   | CHG_END_ACT (Ks)        | CHG_FAST (KMs)        | CHG_FAST_USB_THR OTTLE (Ks) | CHG_NTC_MON (M)   | CHG_BATT_HOT_MON (M)   | CHG_BATT_COLD_MON (M) | CHG_CHIP_TEMP_MON (KM)           | A00Fh<br>A00Fh<br>A00Fh<br>A00Fh |       |
| R169 (A9h) | Battery Charger Control 2 | CHG_ACTIVE (M)       | CHG_PAUSE (s)     | CHG_STS[1:0]         |                      | CHG_TIME[3:0] (KM) |               |                              |                             | CHG_MASK_WALL_FB (Ks) | CHG_TRIC_KLE_SEL (K)    | CHG_VSEL[1:0] (K)     |                             | CHG_ISEL[3:0] (K) |                        |                       |                                  | 0B06h                            |       |
| R170 (AAh) | Battery Charger Control 3 | 0                    | 0                 | 0                    | 0                    | 0                  | 0             | 0                            | 0                           | CHG_FRC (Ks)          | CHG_THROTTLE_T[1:0] (K) |                       | 0                           | 0                 | 0                      | 0                     | 0                                | 0000h                            |       |
| R172 (ACh) | Current Sink Driver A     | CS1_ENA (s)          | 0                 | 0                    | CS1_HIB_MODE (s)     | 0                  | 0             | 0                            | 0                           | 0                     | 0                       | CS1_ISEL[5:0] (s)     |                             |                   |                        |                       | 0000h                            |                                  |       |
| R173 (ADh) | CSA Flash control         | CS1_FLASH_MODE (s)   | CS1_TRIGSRC (s)   | CS1_DRIVE (Ms)       | CS1_FLASH_RATE (s)   | 0                  | 0             | CS1_FLASH_DUR[1:0] (s)       |                             | 0                     | 0                       | CS1_OFF_RAMP[1:0] (s) |                             | 0                 | 0                      | CS1_ON_RAMP[1:0] (s)  |                                  | 0000h                            |       |
| R174 (AEh) | Current Sink Driver B     | CS2_ENA (s)          | 0                 | 0                    | CS2_HIB_MODE (s)     | 0                  | 0             | 0                            | 0                           | 0                     | 0                       | CS2_ISEL[5:0] (s)     |                             |                   |                        |                       | 0000h                            |                                  |       |
| R175 (AFh) | CSB Flash control         | CS2_FLASH_MODE (s)   | CS2_TRIGSRC (s)   | CS2_DRIVE (Ms)       | CS2_FLASH_RATE (s)   | 0                  | 0             | CS2_FLASH_DUR[1:0] (s)       |                             | 0                     | 0                       | CS2_OFF_RAMP[1:0] (s) |                             | 0                 | 0                      | CS2_ON_RAMP[1:0] (s)  |                                  | 0000h                            |       |
| R176 (B0h) | DCDC/LDO requested        | LS_ENA (Ms)          | 0                 | 0                    | 0                    | LDO4_ENA (Ms)      | LDO3_ENA (Ms) | LDO2_ENA (Ms)                | LDO1_ENA (Ms)               | 0                     | 0                       | DC6_ENA (Ms)          | DC5_ENA (Ms)                | DC4_ENA (Ms)      | DC3_ENA (Ms)           | DC2_ENA (Ms)          | DC1_ENA (Ms)                     | 0000h                            |       |
| R177 (B1h) | DCDC Active options       | DCDC_DISCLKS (s)     | 0                 | PUTO[1:0] (s)        |                      |                    | 0             | 0                            | 0                           | 0                     | 0                       | 0                     | DC6_ACTIVATE (s)            | 0                 | DC4_ACTIVATE (s)       | DC3_ACTIVATE (s)      | 0                                | DC1_ACTIVATE (s)                 | 032Dh |
| R178 (B2h) | DCDC Sleep options        | 0                    | 0                 | 0                    | 0                    | 0                  | 0             | 0                            | 0                           | 0                     | 0                       | DC6_SLEEP (s)         | 0                           | DC4_SLEEP (s)     | DC3_SLEEP (s)          | 0                     | DC1_SLEEP (s)                    | 0000h                            |       |
| R179 (B3h) | Power-check comparator    | 0                    | PCCMP_ERACT (s)   | 0                    | PCCOMP_HIB_MODE      | 0                  | 0             | 0                            | 0                           | 0                     | PCCMP_OFF_THR[2:0] (KM) |                       |                             | 0                 | PCCMP_ON_THR[2:0] (KM) |                       |                                  | 0025h<br>0025h<br>0025h<br>0025h |       |
| R180 (B4h) | DCDC1 Control             | DC1_CAP[1:0] (s)     |                   | 0                    | 0                    | DC1_DISOVP (Ms)    | DC1_OPFLT     | 0                            | 0                           | 0                     | DC1_VSEL[6:0] (Ms)      |                       |                             |                   |                        |                       | 000Eh<br>0006h<br>0012h<br>0062h |                                  |       |
| R181 (B5h) | DCDC1 Timeouts            | DC1_ERRACT[1:0] (Ms) |                   | DC1_ENSLOT[3:0] (Ms) |                      |                    |               | DC1_SDSL[3:0]                |                             |                       | 0                       | 0                     | 0                           | 0                 | 0                      | 0                     | 0                                | 0000h<br>1000h<br>0400h<br>0800h |       |
| R182 (B6h) | DCDC1 Low Power           | 0                    | DC1_HIB_MODE[2:0] |                      |                      | 0                  | 0             | DC1_HIB_TRIG[1:0] (Ms)       |                             | 0                     | DC1_VIMG[6:0]           |                       |                             |                   |                        |                       | 1006h                            |                                  |       |

| REG        | NAME            | 15                   | 14                     | 13                   | 12                | 11               | 10         | 9                      | 8 | 7 | 6                  | 5 | 4             | 3             | 2 | 1                   | 0                                | DEFAULT |
|------------|-----------------|----------------------|------------------------|----------------------|-------------------|------------------|------------|------------------------|---|---|--------------------|---|---------------|---------------|---|---------------------|----------------------------------|---------|
| R183 (B7h) | DCDC2 Control   | 0                    | DC2_MODE (s)           | 0                    | DC2_HIB_M ODE (s) | 0                | 0          | DC2_HIB_TRIG[1:0] (s)  |   | 0 | DC2_ILIM (Ms)      | 0 | DC2_RMPH (Ms) | DC2_RMPL (Ms) | 0 | DC2_FBSRC[1:0] (Ms) |                                  | 0018h   |
| R184 (B8h) | DCDC2 Timeouts  | DC2_ERRACT[1:0] (Ms) |                        | DC2_ENSLOT[3:0] (Ms) |                   |                  |            | DC2_SDSLOT[3:0]        |   |   | 0                  | 0 | 0             | 0             | 0 | 0                   | 0000h<br>0000h<br>0000h<br>0000h |         |
| R186 (BAh) | DCDC3 Control   | 0                    | 0                      | 0                    | 0                 | DC3_DISO VP (Ms) | DC3_OPFL T | 0                      | 0 | 0 | DC3_VSEL[6:0] (Ms) |   |               |               |   |                     | 0000h<br>0026h<br>002Eh<br>000Eh |         |
| R187 (BBh) | DCDC3 Timeouts  | DC3_ERRACT[1:0] (Ms) |                        | DC3_ENSLOT[3:0] (Ms) |                   |                  |            | DC3_SDSLOT[3:0]        |   |   | 0                  | 0 | 0             | 0             | 0 | 0                   | 0000h<br>0400h<br>0000h<br>0000h |         |
| R188 (BCh) | DCDC3 Low Power | 0                    | DC3_HIB_MODE[2:0] (Ms) |                      |                   | 0                | 0          | DC3_HIB_TRIG[1:0] (Ms) |   | 0 | DC3_VIMG[6:0]      |   |               |               |   |                     | 0006h                            |         |
| R189 (BDh) | DCDC4 Control   | 0                    | 0                      | 0                    | 0                 | DC4_DISO VP (Ms) | DC4_OPFL T | 0                      | 0 | 0 | DC4_VSEL[6:0] (Ms) |   |               |               |   |                     | 0000h<br>0056h<br>000Eh<br>0006h |         |
| R190 (BEh) | DCDC4 Timeouts  | DC4_ERRACT[1:0] (Ms) |                        | DC4_ENSLOT[3:0] (Ms) |                   |                  |            | DC4_SDSLOT[3:0]        |   |   | 0                  | 0 | 0             | 0             | 0 | 0                   | 0000h<br>0400h<br>0000h<br>0C00h |         |
| R191 (BFh) | DCDC4 Low Power | 0                    | DC4_HIB_MODE[2:0] (Ms) |                      |                   | 0                | 0          | DC4_HIB_TRIG[1:0] (Ms) |   | 0 | DC4_VIMG[6:0]      |   |               |               |   |                     | 0006h                            |         |
| R192 (C0h) | DCDC5 Control   | 0                    | DC5_MODE (s)           | 0                    | DC5_HIB_M ODE (s) | 0                | 0          | DC5_HIB_TRIG[1:0] (s)  |   | 0 | DC5_ILIM (Ms)      | 0 | DC5_RMPH (Ms) | DC5_RMPL (Ms) | 0 | DC5_FBSRC[1:0] (Ms) |                                  | 0008h   |
| R193 (C1h) | DCDC5 Timeouts  | DC5_ERRACT[1:0] (Ms) |                        | DC5_ENSLOT[3:0] (Ms) |                   |                  |            | DC5_SDSLOT[3:0]        |   |   | 0                  | 0 | 0             | 0             | 0 | 0                   | 0000h<br>0000h<br>0000h<br>0000h |         |
| R195 (C3h) | DCDC6 Control   | DC6_CAP[1:0]         |                        | 0                    | 0                 | DC6_DISO VP (Ms) | DC6_OPFL T | 0                      | 0 | 0 | DC6_VSEL[6:0] (Ms) |   |               |               |   |                     | 0000h<br>000Ah<br>0026h<br>0026h |         |
| R196 (C4h) | DCDC6 Timeouts  | DC6_ERRACT[1:0] (Ms) |                        | DC6_ENSLOT[3:0] (Ms) |                   |                  |            | DC6_SDSLOT[3:0]        |   |   | 0                  | 0 | 0             | 0             | 0 | 0                   | 0000h<br>1000h<br>0C00h<br>0400h |         |

| REG        | NAME                 | 15                    | 14                     | 13                      | 12 | 11 | 10                     | 9                       | 8 | 7             | 6           | 5 | 4                   | 3           | 2       | 1     | 0                                | DEFAULT                          |
|------------|----------------------|-----------------------|------------------------|-------------------------|----|----|------------------------|-------------------------|---|---------------|-------------|---|---------------------|-------------|---------|-------|----------------------------------|----------------------------------|
| R197 (C5h) | DCDC6 Low Power      | 0                     | DC6_HIB_MODE[2:0] (Ms) |                         | 0  | 0  | DC6_HIB_TRIG[1:0] (Ms) |                         | 0 | DC6_VIMG[6:0] |             |   |                     |             |         | 0006h |                                  |                                  |
| R199 (C7h) | Limit Switch Control | LS_ERRACT[1:0] (Ms)   |                        | LS_ENSLOT[3:0] (Ms)     |    |    | LS_SDSLOT[3:0]         |                         |   | 0             | LS_HIB_MODE | 0 | 0                   | LS_HIB_PROT | LS_PROT |       |                                  | 0003h                            |
| R200 (C8h) | LDO1 Control         | 0                     | LDO1_SWI (Ms)          | 0                       | 0  | 0  | LDO1_OPFLT             | 0                       | 0 | 0             | 0           | 0 | LDO1_VSEL[4:0] (Ms) |             |         |       | 001Ch<br>0002h<br>001Ch<br>0002h |                                  |
| R201 (C9h) | LDO1 Timeouts        | LDO1_ERRACT[1:0] (Ms) |                        | LDO1_ENSLOT[3:0] (Ms)   |    |    | LDO1_SDSLOT[3:0]       |                         |   | 0             | 0           | 0 | 0                   | 0           | 0       |       |                                  | 0000h<br>0C00h<br>0000h<br>0000h |
| R202 (CAh) | LDO1 Low Power       | 0                     | 0                      | LDO1_HIB_MODE[1:0] (Ms) |    | 0  | 0                      | LDO1_HIB_TRIG[1:0] (Ms) |   | 0             | 0           | 0 | LDO1_VIMG[4:0]      |             |         |       | 001Ch                            |                                  |
| R203 (CBh) | LDO2 Control         | 0                     | LDO2_SWI (Ms)          | 0                       | 0  | 0  | LDO2_OPFLT             | 0                       | 0 | 0             | 0           | 0 | LDO2_VSEL[4:0] (Ms) |             |         |       | 001Bh<br>001Fh<br>0010h<br>001Ah |                                  |
| R204 (CCh) | LDO2 Timeouts        | LDO2_ERRACT[1:0] (Ms) |                        | LDO2_ENSLOT[3:0] (Ms)   |    |    | LDO2_SDSLOT[3:0]       |                         |   | 0             | 0           | 0 | 0                   | 0           | 0       |       |                                  | 0000h<br>0800h<br>0800h<br>0000h |
| R205 (CDh) | LDO2 Low Power       | 0                     | 0                      | LDO2_HIB_MODE[1:0] (Ms) |    | 0  | 0                      | LDO2_HIB_TRIG[1:0] (Ms) |   | 0             | 0           | 0 | LDO2_VIMG[4:0]      |             |         |       | 001Ch                            |                                  |
| R206 (CEh) | LDO3 Control         | 0                     | LDO3_SWI (Ms)          | 0                       | 0  | 0  | LDO3_OPFLT             | 0                       | 0 | 0             | 0           | 0 | LDO3_VSEL[4:0] (Ms) |             |         |       | 001Bh<br>001Ch<br>0015h<br>001Fh |                                  |
| R207 (CFh) | LDO3 Timeouts        | LDO3_ERRACT[1:0] (Ms) |                        | LDO3_ENSLOT[3:0] (Ms)   |    |    | LDO3_SDSLOT[3:0]       |                         |   | 0             | 0           | 0 | 0                   | 0           | 0       |       |                                  | 0000h<br>0400h<br>0000h<br>0000h |
| R208 (D0h) | LDO3 Low Power       | 0                     | 0                      | LDO3_HIB_MODE[1:0] (Ms) |    | 0  | 0                      | LDO3_HIB_TRIG[1:0] (Ms) |   | 0             | 0           | 0 | LDO3_VIMG[4:0]      |             |         |       | 001Ch                            |                                  |
| R209 (D1h) | LDO4 Control         | 0                     | LDO4_SWI (Ms)          | 0                       | 0  | 0  | LDO4_OPFLT             | 0                       | 0 | 0             | 0           | 0 | LDO4_VSEL[4:0] (Ms) |             |         |       | 001Bh<br>0004h<br>001Ah<br>001Fh |                                  |

| REG        | NAME                      | 15                    | 14                  | 13                      | 12                | 11                     | 10                     | 9                       | 8                 | 7                 | 6                 | 5                 | 4                  | 3                  | 2                     | 1                     | 0                      | DEFAULT                          |
|------------|---------------------------|-----------------------|---------------------|-------------------------|-------------------|------------------------|------------------------|-------------------------|-------------------|-------------------|-------------------|-------------------|--------------------|--------------------|-----------------------|-----------------------|------------------------|----------------------------------|
| R210 (D2h) | LDO4 Timeouts             | LDO4_ERRACT[1:0] (Ms) |                     | LDO4_ENSLOT[3:0] (Ms)   |                   |                        |                        | LDO4_SDSLOT[3:0]        |                   |                   |                   | 0                 | 0                  | 0                  | 0                     | 0                     | 0                      | 0000h<br>0800h<br>0000h<br>0000h |
| R211 (D3h) | LDO4 Low Power            | 0                     | 0                   | LDO4_HIB_MODE[1:0] (Ms) |                   | 0                      | 0                      | LDO4_HIB_TRIG[1:0] (Ms) |                   | 0                 | 0                 | 0                 | LDO4_VIMG[4:0]     |                    |                       |                       |                        | 001Ch                            |
| R215 (D7h) | VCC_FAULT Masks           | LS_FAULT (s)          | 0                   | 0                       | 0                 | LDO4_FAU LT (s)        | LDO3_FAU LT (s)        | LDO2_FAU LT (s)         | LDO1_FAU LT (s)   | 0                 | 0                 | DC6_FAULT (s)     | DC5_FAULT (s)      | DC4_FAULT (s)      | DC3_FAULT (s)         | DC2_FAULT (s)         | DC1_FAULT (s)          | 0000h                            |
| R216 (D8h) | Main Bandgap Control      | MBG_LOAD_FUSES        | 0                   | 0                       | 0                 | 0                      | 0                      | 0                       | 0                 | 0                 | 0                 | 0                 | 0                  | 0                  | 0                     | 0                     | 0                      | 001Fh                            |
| R217 (D9h) | OSC Control               | OSC_LOAD_FUSES (K)    | 0                   | 0                       | 0                 | 0                      | 0                      | 0                       | 0                 | 0                 | 0                 | 0                 | 0                  | 0                  | 0                     | 0                     | 0                      | 0000h                            |
| R218 (DAh) | RTC Tick Control          | RTC_TICK_ENA (KMs)    | RTC_TICKS (K)       | RTC_CLKS (KMs)          | OSC32K_ENA (KMs)  | 0                      | 0                      | RTC_TRIM[9:0] (K)       |                   |                   |                   |                   |                    |                    |                       |                       |                        | 9000h<br>9000h<br>9000h<br>9000h |
| R219 (DBh) | Security1                 | SECURITY[15:0] (s)    |                     |                         |                   |                        |                        |                         |                   |                   |                   |                   |                    |                    |                       |                       |                        | 0000h                            |
| R224 (E0h) | Signal overrides          | 0                     | 0                   | 0                       | 0                 | WALL_FB_GT_BATT_OVRDE  | USB_FB_GT_BATT_OVRDE   | FLL_OK_OVRDE            | DEB_TICK_OVRDE    | UVLO_B_OVRDE      | RTC_ALARM_OVRDE   | 0                 | 0                  | LINE_GT_BATT_OVRDE | LINE_GT_RTC_OVRDE     | USB_GT_LI_OVRDE       | BATT_GT_USB_OVRDE      | 0000h                            |
| R225 (E1h) | DCDC/LDO status           | LS_STS (s)            | 0                   | 0                       | 0                 | LDO4_STS (s)           | LDO3_STS (s)           | LDO2_STS (s)            | LDO1_STS (s)      | 0                 | 0                 | DC6_STS (s)       | DC5_STS (s)        | DC4_STS (s)        | DC3_STS (s)           | DC2_STS (s)           | DC1_STS (s)            | 0000h                            |
| R226 (E2h) | Charger Overrides/status  | CHG_BATT_HOT_OVRDE    | CHG_BATT_COLD_OVRDE | 0                       | 0                 | CHG_END_OVRDE          | 0                      | 0                       | 0                 | 0                 | 0                 | 0                 | 0                  | 0                  | CHG_BATT_LT_3P9_OVRDE | CHG_BATT_LT_3P1_OVRDE | CHG_BATT_LT_2P85_OVRDE | 0000h                            |
| R227 (E3h) | misc overrides            | 0                     | 0                   | CS2_NOT_REG_OVRDE       | CS1_NOT_REG_OVRDE | 0                      | USB_LIMIT_OVRDE        | 0                       | 0                 | AUX_DCO_MP4_OVRDE | AUX_DCO_MP3_OVRDE | AUX_DCO_MP2_OVRDE | AUX_DCO_MP1_OVRDE  | HYST_UVL_O_OVRDE   | CHIP_GT115_OVRDE      | CHIP_GT140_OVRDE      | 0                      | 0000h                            |
| R228 (E4h) | Supply overrides/status 1 | 0                     | 0                   | 0                       | 0                 | 0                      | 0                      | 0                       | 0                 | 0                 | 0                 | OVRV_DC6_OVRDE    | 0                  | OVRV_DC4_OVRDE     | OVRV_DC3_OVRDE        | 0                     | OVRV_DC1_OVRDE         | 0000h                            |
| R229 (E5h) | Supply overrides/status 2 | OVCN_LS_OVRDE         | 0                   | 0                       | 0                 | UNDV_LDO4_OVRDE        | UNDV_LDO3_OVRDE        | UNDV_LDO2_OVRDE         | UNDV_LDO1_OVRDE   | 0                 | 0                 | UNDV_DC6_OVRDE    | UNDV_DC5_OVRDE     | UNDV_DC4_OVRDE     | UNDV_DC3_OVRDE        | UNDV_DC2_OVRDE        | UNDV_DC1_OVRDE         | 0000h                            |
| R230 (E6h) | GPIO Pin Status           | 1 (n)                 | 1 (n)               | 1 (n)                   | GP12_LVL          | GP11_LVL               | GP10_LVL               | GP9_LVL                 | GP8_LVL           | GP7_LVL           | GP6_LVL           | GP5_LVL           | GP4_LVL            | GP3_LVL            | GP2_LVL               | GP1_LVL               | GP0_LVL                | E000h                            |
| R231 (E7h) | comparator overrides      | USB_FB_OVRDE          | WALL_FB_OVRDE       | BATT_FB_OVRDE           | 0                 | CODEC_JC_K_DET_L_OVRDE | CODEC_JC_K_DET_R_OVRDE | CODEC_MI_CSCD_OVRDE     | CODEC_MI_CD_OVRDE | 0                 | 0                 | 0                 | 0                  | 0                  | 0                     | 0                     | 0                      | 0000h                            |
| R233 (E9h) | State Machine status      | 0                     | 0                   | 0                       | 0                 | 0                      | USB_SM[2:0]            |                         |                   | 0                 | CHG_SM[2:0]       |                   |                    | MAIN_SM[3:0]       |                       |                       | 0000h                  |                                  |
| R248 (F8h) | DCDC1 Test Controls       | 0                     | 0                   | 0                       | 0                 | 0                      | 0                      | 0                       | 0                 | 0                 | 0                 | 0                 | DC1_FORC_E_PWM (s) | 0                  | 0                     | 0                     | 0                      | 1000h                            |

| REG        | NAME                | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4                     | 3 | 2 | 1 | 0 | DEFAULT |
|------------|---------------------|----|----|----|----|----|----|---|---|---|---|---|-----------------------|---|---|---|---|---------|
| R250 (FAh) | DCDC3 Test Controls | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | DC3_FORC<br>E_PWM (s) | 0 | 0 | 0 | 0 | 1000h   |
| R251 (FBh) | DCDC4 Test Controls | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | DC4_FORC<br>E_PWM (s) | 0 | 0 | 0 | 0 | 1000h   |
| R253 (FDh) | DCDC6 Test Controls | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | DC6_FORC<br>E_PWM (s) | 0 | 0 | 0 | 0 | 1000h   |

## 27 REGISTER BITS BY ADDRESS

| REGISTER ADDRESS     | BIT  | LABEL                  | DEFAULT             | DESCRIPTION   | REFER TO |
|----------------------|------|------------------------|---------------------|---|----------|
| R0 (00h)<br>Reset/ID | 15:0 | SW_RESET/CHIP_ID[15:0] | 0110_0001_0100_0011 | Reading this register returns 6143h.<br><i>Never reset.</i> |          |

**Register 00h** Reset/ID

| REGISTER ADDRESS | BIT   | LABEL         | DEFAULT | DESCRIPTION  | REFER TO |
|------------------|-------|---------------|---------|--|----------|
| R1 (01h) ID      | 15:12 | CHIP_REV[3:0] |         | The functional silicon revision - this tracks changes in functionality which are separate from ROM mask settings |          |
|                  | 11:10 | CONF_STS[1:0] |         | The state of the configuration pins. This selects what register defaults should be.                              |          |
|                  | 7:0   | CUST_ID[7:0]  |         | The Chip Revision Number   |          |

**Register 01h** ID

| REGISTER ADDRESS     | BIT | LABEL         | DEFAULT | DESCRIPTION     | REFER TO |
|----------------------|-----|---------------|---------|-----------------|----------|
| R2 (02h)<br>Revision | 7:0 | MASK_REV[7:0] |         | The ROM Mask ID |          |

**Register 02h** Revision

| REGISTER ADDRESS                | BIT | LABEL        | DEFAULT | DESCRIPTION   | REFER TO |
|---------------------------------|-----|--------------|---------|---|----------|
| R3 (03h)<br>System<br>Control 1 | 15  | CHIP_ON      | 0       | Indicates whether the system is on or off. Writing 0 to this bit powers down the whole chip. Registers which are affected by state machine reset will get reset.<br><br>Once the system is turned OFF it can be restarted by any of the valid ON event.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                 | 14  | SYS_RST      | 0       | Allows the processors to reboot itself<br>0 = Do nothing<br>1 = Perform a processor reset by asserting the /RST and /MEMRST (GPIO) pins for the programmed duration<br><i>Protected by security key. Reset by state machine. Default held in metal mask.</i>  |          |
|                                 | 13  | POWERCYCLE   | 0       | Action to take on a fault (if response is set to shutdown system):<br>0 = Shut down<br>1 = Shutdown everything then go through startup sequence. i.e. Reboot the system.  |          |
|                                 | 12  | VCC_FAULT_OV | 1       | Include over voltage in the /VCC_FAULT pin (Alternative GPIO function)<br>0 = Do not include over voltage in the /VCC_FAULT signal<br>1 = Include the over voltage in the /VCC_FAULT signal<br><i>Reset by state machine. Default held in metal mask.</i>   |          |

| REGISTER ADDRESS | BIT   | LABEL          | DEFAULT | DESCRIPTION  | REFER TO |
|------------------|-------|----------------|---------|--|----------|
|                  | 11:10 | RSTB_TO[1:0]   | 11      | Time that the /RST pin and /MEMRST output is held low after the chip reaches the active state.<br>00 = 15ms<br>01 = 30ms<br>10 = 60ms<br>11 = 120ms<br><i>Default held in metal mask.</i>  |          |
|                  | 9     | BG_SLEEP       | 0       | Bandgap sleep mode<br>0 = never in sleep mode<br>1 = sleep mode is controlled by Main SM<br><i>Default held in metal mask.</i>   |          |
|                  | 7     | WDOG_DEBUG     | 0       | Halts watchdog timer for system debugging<br>0 = normal operation<br>1 = WDOG halt<br><i>Protected by security key.</i>  |          |
|                  | 6     | CHIP_RESET_ENA | 0       | [No description available]<br><i>Reset by state machine.</i>   |          |
|                  | 5     | MEM_VALID      | 0       | Indicates that the contents of external memory are still valid.<br>This bit is cleared on startup and whenever /MEMRST is asserted from the main state machine. The system software should set this bit once the external memory has been set up.<br>Controlled in hibernate mode by MEMRST_HIB_MODE<br>0 = External memory is not valid and needs restoring.<br>1 = External memory is valid.<br><i>Reset when /MEMRST is asserted.</i> |          |
|                  | 4     | CHIP_SET_UP    | 0       | A spare register bit that can be used by the system to say if the chip has been configured. It is reset by POR.  |          |
|                  | 3     | ON_DEB_T       | 0       | ON pin Shutdown function debounce time<br>0 = 10s<br>1 = 5s<br><i>Protected by security key.</i>   |          |
|                  | 1     | ON_POL         | 1       | ON pin polarity:<br>0 = Active high (ON)<br>1 = Active low (/ON)<br><i>Protected by security key. Reset by state machine. Default held in metal mask.</i>  |          |
|                  | 0     | IRQ_POL        | 0       | IRQ pin polarity:<br>0 = Active low (/IRQ)<br>1 = Active high (IRQ)<br><i>Reset by state machine. Default held in metal mask.</i>  |          |

Register 03h System Control 1



| REGISTER ADDRESS                | BIT | LABEL           | DEFAULT          | DESCRIPTION   | REFER TO |
|---------------------------------|-----|-----------------|------------------|---|----------|
| R4 (04h)<br>System<br>Control 2 | 15  | USB_SUSPEND_8MA | 0                | USB suspend mode with 8mA option<br>0 = USB is not suspended.<br>1 = USB is suspend with 8mA option enabled<br>The register bit defaults to 0, when a reset happens or LINE<UVLO or the system fail on boot due to the upper limit of the Hysteresis Comp not been met.<br><i>Default held in metal mask.</i>     |          |
|                                 | 14  | USB_SUSPEND     | 0                | Opens the USB switch<br>0 = USB enabled<br>1 = USB suspended<br>The register bit defaults to 0, when a reset happens or LINE < UVLO or the system fail on boot due to the upper limit of the Hysteresis Comp not being met.<br><i>Default held in metal mask.</i>   |          |
|                                 | 13  | USB_MSTR        | 0                | Set the chip to be a USB master<br>0 = Slave<br>1 = Master<br>The register bit defaults to 0, when a reset happens or the USB state machine moves from MASTER mode to SLAVE mode.<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                                 | 12  | USB_MSTR_SRC    | 0                | Master mode source selector<br>0 = Master mode source is DCDC2/5<br>1 = Master mode source is LINE<br><i>Reset by state machine. Default held in metal mask.</i>  |          |
|                                 | 11  | USB_MSTR_500MA  | 0                | Set 500mA or 100mA mode when the USB switch is in master mode<br>0 = 100mA<br>1 = 500mA<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                                 | 10  | USB_NOLIM       | 0                | USB current limiting<br>0 = Limit the USB current as per the settings.<br>1 = Don't limit USB current   |          |
|                                 | 9   | USB_SLV_500MA   | 0<br>1<br>1<br>1 | Set 500mA or 100mA mode when the USB switch is in slave mode<br>0 = 100mA<br>1 = 500mA<br>The register bit defaults to 0, when a reset happens or LINE<UVLO or the system fail on boot due to the upper limit of the Hysteresis Comp not being met.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                 | 7   | WDOG_HIB_MODE   | 0                | Watchdog state in hibernate state<br>0 = WDOG disabled in Hibernate<br>1 = WDOG controlled by WDOG_MODE in Hibernate  |          |

| REGISTER ADDRESS | BIT | LABEL          | DEFAULT              | DESCRIPTION  | REFER TO |
|------------------|-----|----------------|----------------------|--|----------|
|                  | 5:4 | WDOG_MODE[1:0] | 00<br>00<br>01<br>00 | 00 = Disabled<br>01 = SYS_WDOG_TO interrupt on time-out<br>10 = WKUP_WDOG_RST interrupt and System reset on time-out<br>11 = SYS_WDOG_TO interrupt on first time-out, WKUP_WDOG_RST interrupt and System reset on second time-out<br><i>Protected by security key. Reset by state machine. Default held in metal mask.</i> |          |
|                  | 2:0 | WDOG_TO[2:0]   | 100                  | Watchdog timeout (seconds)<br>The timer is reset to this value when a HEARTBEAT signal edge is detected or the host writes to the watchdog control register.<br>000 = 0.125s<br>... (time doubles with each step)<br>101 = 4s<br>11x = Reserved<br><i>Protected by security key.</i>                                       |          |

Register 04h System Control 2

| REGISTER ADDRESS                | BIT | LABEL              | DEFAULT | DESCRIPTION  | REFER TO |
|---------------------------------|-----|--------------------|---------|--|----------|
| R5 (05h)<br>System<br>Hibernate | 15  | HIBERNATE          | 0       | Determines what state the chip should operate in.<br>0 = Active state<br>1 = Hibernate state<br>The register bit defaults to 0, when a reset happens<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                 | 7   | WDOG_HIB_MODE      | 0       | Watchdog behaviour in HIBERNATE state<br>0 = WDOG disabled in Hibernate<br>1 = WDOG controlled by WDOG_MODE in Hibernate   |          |
|                                 | 6   | HIB_STARTUP_SEQ    | 0       | Direction to take when going from Hibernate state to the Active state.<br>0 = Hibernate to Active without going through startup state<br>1 = Hibernate to Active goes through startup sequence                     |          |
|                                 | 5   | REG_RESET_HIB_MODE | 0       | Action of the internal register reset signal when going from Hibernate to Active.<br>0 = Do a register reset when leaving the hibernate state.<br>1 = Do not do a register reset when leaving the hibernate state  |          |
|                                 | 4   | RST_HIB_MODE       | 0       | /RST pin state in hibernate mode:<br>0 = Asserted (low)<br>1 = Not asserted (high)   |          |
|                                 | 3   | IRQ_HIB_MODE       | 0       | IRQ pin state in hibernate mode<br>0 = Normal operation<br>1 = Forced to indicate there is no IRQ  |          |
|                                 | 2   | MEMRST_HIB_MODE    | 0       | /MEMRST (Alternative GPIO function) pin state in hibernate mode<br>0 = Asserted (low)<br>1 = Not asserted (high)   |          |

| REGISTER ADDRESS | BIT | LABEL            | DEFAULT | DESCRIPTION  | REFER TO |
|------------------|-----|------------------|---------|--|----------|
|                  | 1   | PCCOMP_HIB_MODE  | 0       | Function of the Hysteresis Comp in hibernate.<br>0 = Hysteresis Comp is not used in hibernate<br>1 = Hysteresis Comp is on in hibernate            |          |
|                  | 0   | TEMPMON_HIB_MODE | 0       | Function of the temp monitoring in hibernate.<br>0 = Temp monitoring is off in hibernate state<br>1 = Temp monitoring is on in the hibernate state |          |

**Register 05h** System Hibernate

| REGISTER ADDRESS              | BIT   | LABEL          | DEFAULT          | DESCRIPTION  | REFER TO |
|-------------------------------|-------|----------------|------------------|--|----------|
| R6 (06h)<br>Interface Control | 15    | USE_DEV_PINS   | 1                | Selects which pins to use for the 2-wire control:<br>0 = Use 2-wire I/F pins as 2-wire interface<br>1 = Use GPIO 10 and 11 as 2-wire interface, e.g. to download settings from PIC.<br>Only applies when CONFIG pins[1:0] = 00.<br><i>Reset by state machine.</i>  |          |
|                               | 14:13 | DEV_ADDR[1:0]  | 00               | Selects device address (only valid when CONF_STS = 00)<br>00 = 0x34<br>01 = 0x36<br>10 = 0x3C<br>11 = 0x3E<br><i>Reset by state machine.</i>   |          |
|                               | 12    | CONFIG_DONE    | 0                | Tells the system that the PIC micro has completed its programming.<br>0 = Programming still to be done<br>1 = Programming complete<br>Only applies when CONFIG pins[1:0] = 00.<br><i>Reset by state machine.</i>   |          |
|                               | 11    | RECONFIG_AT_ON | 1                | Selects whether to reset the registers in the OFF state and whether to reload the device configuration from the PIC when an ON event occurs.<br>0 = Do not reset registers in the OFF state. Do not load configuration data when an ON event occurs.<br>1 = Reset registers in the OFF state. Load configuration from the PIC when an ON event occurs.<br>Note that, in development mode, the device configuration from the PIC is always loaded when first powering up the chip.<br>This bit must always be set to default (1) in Custom Modes 01, 10 and 11. |          |
|                               | 9     | AUTOINC        | 1                | Enables address auto-increment<br>0 = disabled<br>1 = enabled<br><i>Reset by state machine.</i>  |          |
|                               | 3     | SPI_CFG        | 0<br>0<br>0<br>0 | Controls the SDOUT (GPIO6) pin operation in 4 wire mode<br>0 = SDOUT output is CMOS<br>1 = SDOUT output is open drain<br>Note: SPI_4WIRE must be set for this to take effect.<br><i>Protected by security key. Default held in metal</i>   |          |

| REGISTER ADDRESS | BIT | LABEL     | DEFAULT          | DESCRIPTION  | REFER TO |
|------------------|-----|-----------|------------------|--|----------|
|                  |     |           |                  | <i>mask.</i>   |          |
|                  | 2   | SPI_4WIRE | 0<br>0<br>0<br>0 | Selects 3-wire or 4-wire SPI mode<br>0 = 3-wire mode using bi-directional SDATA pin<br>1 = 4 wire mode using SDOOUT (GPIO6)<br>Note: SPI_3WIRE must be set for this to take effect.<br><i>Protected by security key. Default held in metal mask.</i> |          |
|                  | 1   | SPI_3WIRE | 0<br>0<br>0<br>0 | Selects 2- or 3-/4-wire mode.<br>0 = 2-wire mode<br>1 = 3/4 wire mode<br><i>Protected by security key. Default held in metal mask.</i>   |          |

Register 06h Interface Control

| REGISTER ADDRESS              | BIT   | LABEL            | DEFAULT | DESCRIPTION  | REFER TO |
|-------------------------------|-------|------------------|---------|--|----------|
| R8 (08h)<br>Power mgmt<br>(1) | 15:14 | CODEC_ISEL[1:0]  | 10      | CODEC Analogue current level select<br>00 = x 1.5<br>01 = x 1.0<br>10 = x 0.75<br>11 = x 0.5   |          |
|                               | 13    | VBUF_ENA         | 0       | Forces ON the tie-off amplifiers<br>0 = disabled<br>1 = enabled  |          |
|                               | 10    | OUTPUT_DRAIN_ENA | 0       | Enables a drain on the outputs allowing the amplifiers to shutdown more quickly.<br>0 = Shutdown as normal<br>1 = Sink current from an external capacitor, allowing faster shutdown. |          |
|                               | 8     | MIC_DET_ENA      | 0       | Enable MIC detect:<br>0 = disabled<br>1 = enabled  |          |
|                               | 5     | BIAS_ENA         | 0       | Enables bias to analogue audio CODEC circuitry<br>0 = disabled<br>1 = enabled  |          |
|                               | 4     | MICB_ENA         | 0       | Microphone bias enable<br>0 = OFF (high impedance output)<br>1 = ON  |          |
|                               | 2     | VMID_ENA         | 0       | Enables VMID resistor string<br>0 = disabled<br>1 = enabled  |          |
|                               | 1:0   | VMID[1:0]        | 00      | Resistor selection for VMID potential divider<br>00 = off<br>01 = Vmid comes from 300kΩ R-string<br>10 = Vmid comes from 50kΩ R-string<br>11 = Vmid comes from 5kΩ R-string          |          |

Register 08h Power mgmt (1)

| REGISTER ADDRESS              | BIT | LABEL       | DEFAULT | DESCRIPTION  | REFER TO |
|-------------------------------|-----|-------------|---------|--|----------|
| R9 (09h)<br>Power mgmt<br>(2) | 11  | IN3R_ENA    | 0       | IN3R Amplifier enable<br>0 = disabled<br>1 = enabled     |          |
|                               | 10  | IN3L_ENA    | 0       | IN3L Amplifier enable<br>0 = disabled<br>1 = enabled     |          |
|                               | 9   | INR_ENA     | 0       | Right input PGA enable<br>0 = disabled<br>1 = enabled    |          |
|                               | 8   | INL_ENA     | 0       | Left input PGA enable<br>0 = disabled<br>1 = enabled     |          |
|                               | 7   | MIXINR_ENA  | 0       | Right input mixer enable<br>0 = disabled<br>1 = enabled  |          |
|                               | 6   | MIXINL_ENA  | 0       | Left input mixer enable<br>0 = disabled<br>1 = enabled   |          |
|                               | 5   | OUT4_ENA    | 0       | OUT4 enable<br>0 = disabled<br>1 = enabled               |          |
|                               | 4   | OUT3_ENA    | 0       | OUT3 enable<br>0 = disabled<br>1 = enabled               |          |
|                               | 1   | MIXOUTR_ENA | 0       | Right Output Mixer Enable<br>0 = disabled<br>1 = enabled |          |
|                               | 0   | MIXOUTL_ENA | 0       | Left Output Mixer Enable<br>0 = disabled<br>1 = enabled  |          |

Register 09h Power mgmt (2)

| REGISTER ADDRESS               | BIT | LABEL         | DEFAULT | DESCRIPTION                                 | REFER TO |
|--------------------------------|-----|---------------|---------|---|----------|
| R10 (0Ah)<br>Power mgmt<br>(3) | 7   | IN3R_TO_OUT2R | 0       | BEEP mixer enable                           |          |
|                                | 3   | OUT2R_ENA     | 0       | OUT2R enable<br>0 = disabled<br>1 = enabled |          |
|                                | 2   | OUT2L_ENA     | 0       | OUT2L enable<br>0 = disabled<br>1 = enabled |          |
|                                | 1   | OUT1R_ENA     | 0       | OUT1R enable<br>0 = disabled<br>1 = enabled |          |
|                                | 0   | OUT1L_ENA     | 0       | OUT1L enable<br>0 = disabled<br>1 = enabled |          |

Register 0Ah Power mgmt (3)

| REGISTER ADDRESS               | BIT | LABEL       | DEFAULT | DESCRIPTION  | REFER TO |
|--------------------------------|-----|-------------|---------|--|----------|
| R11 (0Bh)<br>Power mgmt<br>(4) | 14  | SYSCLK_ENA  | 0       | CODEC SYSCLK enable<br>0 = disabled<br>1 = enabled   |          |
|                                | 13  | ADC_HPF_ENA | 1       | High Pass Filter enable<br>0 = disabled<br>1 = enabled   |          |
|                                | 8   | TOCLK_ENA   | 0       | Slow clock enable. Used the zero cross timeout.<br>0 = disabled<br>1 = enabled   |          |
|                                | 5   | DACR_ENA    | 0       | Right DAC enable<br>0 = disabled<br>1 = enabled  |          |
|                                | 4   | ADCL_ENA    | 0       | Left DAC enable<br>0 = disabled<br>1 = enabled   |          |
|                                | 3   | ADCR_ENA    | 0       | Right ADC enable<br>0 = disabled<br>1 = enabled<br>When ADCR and ADCL are used together as a stereo pair, then both ADCs must be enabled together using a single register write to Register R11 (0Bh). |          |
|                                | 2   | ADCL_ENA    | 0       | Left ADC enable<br>0 = disabled<br>1 = enabled<br>When ADCR and ADCL are used together as a stereo pair, then both ADCs must be enabled together using a single register write to Register R11 (0Bh).  |          |

Register 0Bh Power mgmt (4)

| REGISTER ADDRESS               | BIT | LABEL        | DEFAULT          | DESCRIPTION   | REFER TO |
|--------------------------------|-----|--------------|------------------|---|----------|
| R12 (0Ch)<br>Power mgmt<br>(5) | 12  | CODEC_ENA    | 0                | Master codec enable bit. Until this bit is set, all codec registers are held in reset.<br>0 = All codec registers held in reset<br>1 = Codec registers operate normally.<br><i>Reset by state machine.</i>                                      |          |
|                                | 11  | RTC_TICK_ENA | 1<br>1<br>1<br>1 | Real Time Clock control.<br>0 = RTC is disabled<br>1 = RTC is enabled.<br><i>Protected by security key. Reset by state machine. Default held in metal mask.</i>   |          |
|                                | 10  | OSC32K_ENA   | 1<br>1<br>1<br>1 | 32kHz crystal oscillator control<br>0 = 32kHz OSC is disabled<br>1 = 32kHz OSC is enabled<br><i>Protected by security key. Reset by state machine. Default held in metal mask.</i>  |          |
|                                | 9   | CHG_ENA      | 1                | Charger control<br>CHG_ENA bit selects battery charger current control<br>0 = Set battery charger current to zero<br>1 = Enable battery charge control<br><i>Protected by security key. Reset by state machine. Default held in metal mask.</i> |          |

| REGISTER ADDRESS | BIT | LABEL       | DEFAULT | DESCRIPTION   | REFER TO |
|------------------|-----|-------------|---------|---|----------|
|                  | 8   | SW_VRTC_ENA | 0       | SW_VRTC control<br>0 = VRTC is not driven out on SWVRTC pin<br>1 = VRTC is driven out on SWVRTC pin<br><i>Reset by state machine.</i> |          |
|                  | 7   | AUXADC_ENA  | 0       | AUXADC control<br>0 = disabled<br>1 = enabled<br><i>Reset by state machine.</i>   |          |
|                  | 3   | DCMP4_ENA   | 0       | Digital comparator 4 enable<br>0 = disabled<br>1 = enabled<br><i>Reset by state machine.</i>  |          |
|                  | 2   | DCMP3_ENA   | 0       | Digital comparator 3 enable<br>0 = disabled<br>1 = enabled<br><i>Reset by state machine.</i>  |          |
|                  | 1   | DCMP2_ENA   | 0       | Digital comparator 2 enable<br>0 = disabled<br>1 = enabled<br><i>Reset by state machine.</i>  |          |
|                  | 0   | DCMP1_ENA   | 0       | Digital comparator 1 enable<br>0 = disabled<br>1 = enabled<br><i>Reset by state machine.</i>  |          |

**Register 0Ch** Power mgmt (5)

| REGISTER ADDRESS               | BIT | LABEL    | DEFAULT | DESCRIPTION  | REFER TO |
|--------------------------------|-----|----------|---------|--|----------|
| R13 (0Dh)<br>Power mgmt<br>(6) | 15  | LS_ENA   | 0       | Limit Switch enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                | 11  | LDO4_ENA | 0       | LDO4 enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i>         |          |
|                                | 10  | LDO3_ENA | 0       | LDO3 enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i>         |          |

| REGISTER ADDRESS | BIT | LABEL    | DEFAULT | DESCRIPTION   | REFER TO |
|------------------|-----|----------|---------|---|----------|
|                  | 9   | LDO2_ENA | 0       | LDO2 enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i>            |          |
|                  | 8   | LDO1_ENA | 0       | LDO1 enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i>            |          |
|                  | 5   | DC6_ENA  | 0       | DCDC6 converter enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 4   | DC5_ENA  | 0       | DCDC5 converter enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 3   | DC4_ENA  | 0       | DCDC4 converter enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 2   | DC3_ENA  | 0       | DCDC3 converter enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 1   | DC2_ENA  | 0       | DCDC2 converter enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 0   | DC1_ENA  | 0       | DCDC1 converter enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i> |          |

Register 0Dh Power mgmt (6)



| REGISTER ADDRESS               | BIT | LABEL   | DEFAULT | DESCRIPTION   | REFER TO |
|--------------------------------|-----|---------|---------|---|----------|
| R14 (0Eh)<br>Power mgmt<br>(7) | 1   | CS2_ENA | 0       | Current Sink 2 enable (ISINKB pin)<br>0 = disabled<br>1 = enabled<br><i>Reset by state machine.</i> |          |
|                                | 0   | CS1_ENA | 0       | Current Sink 1 enable (ISINKA pin)<br>0 = disabled<br>1 = enabled<br><i>Reset by state machine.</i> |          |

Register 0Eh Power mgmt (7)

| REGISTER ADDRESS                 | BIT  | LABEL         | DEFAULT  | DESCRIPTION          | REFER TO |
|----------------------------------|------|---------------|----------|----------------------|----------|
| R16 (10h) RTC<br>Seconds/Minutes | 14:8 | RTC_MINS[6:0] | 000_0000 | RTC Minutes; 0 to 59 |          |
|                                  | 6:0  | RTC_SECS[6:0] | 000_0000 | RTC Seconds; 0 to 59 |          |

Register 10h RTC Seconds/Minutes

| REGISTER ADDRESS           | BIT  | LABEL        | DEFAULT | DESCRIPTION  | REFER TO |
|----------------------------|------|--------------|---------|--|----------|
| R17 (11h) RTC<br>Hours/Day | 10:8 | RTC_DAY[2:0] | 001     | RTC Day of the week register with range 1-7. 1 is Sunday   |          |
|                            | 5    | RTC_HPM      | 0       | RTC hours AM/PM flag<br>0 = AM<br>1 = PM<br>Only valid in 12 hour mode.  |          |
|                            | 4:0  | RTC_HRS[4:0] | 0_0000  | RTC Hours register with 0-23 range in 24 hour mode and 1-12 in 12 hour mode. (Bit 5 is used to indicate PM/not-AM flag in 12 hour mode.) |          |

Register 11h RTC Hours/Day

| REGISTER ADDRESS            | BIT  | LABEL         | DEFAULT | DESCRIPTION                         | REFER TO |
|-----------------------------|------|---------------|---------|-------------------------------------|----------|
| R18 (12h) RTC<br>Date/Month | 12:8 | RTC_MTH[4:0]  | 0_0001  | RTC Month register with range 1-12. |          |
|                             | 5:0  | RTC_DATE[5:0] | 00_0001 | RTC Date register with range 1-31   |          |

Register 12h RTC Date/Month

| REGISTER ADDRESS      | BIT  | LABEL              | DEFAULT   | DESCRIPTION                                | REFER TO |
|-----------------------|------|--------------------|-----------|--|----------|
| R19 (13h) RTC<br>Year | 13:8 | RTC_YHUNDREDS[5:0] | 01_0100   | RTC Year hundreds register tied to 20(dec) |          |
|                       | 7:0  | RTC_YUNITS[7:0]    | 0000_0000 | RTC Year units register with range 0-99.   |          |

Register 13h RTC Year

| REGISTER ADDRESS                | BIT  | LABEL            | DEFAULT  | DESCRIPTION   | REFER TO |
|---------------------------------|------|------------------|----------|---|----------|
| R20 (14h) Alarm Seconds/Minutes | 14:8 | RTC_ALMMINS[6:0] | 000_0000 | Minutes alarm register with range 0-59. All 1's sets to 'don't care' state.<br>Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms. |          |
|                                 | 6:0  | RTC_ALMSECS[6:0] | 000_0000 | Seconds alarm register with range 0-59. All 1's set to 'don't care' state.<br>Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms.  |          |

Register 14h Alarm Seconds/Minutes

| REGISTER ADDRESS          | BIT  | LABEL           | DEFAULT | DESCRIPTION   | REFER TO |
|---------------------------|------|-----------------|---------|---|----------|
| R21 (15h) Alarm Hours/Day | 11:8 | RTC_ALMDAY[3:0] | 0000    | Day alarm register, with range 1-7, 1 = Sunday. All 1's sets to 'don't care' state.<br>Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms.   |          |
|                           | 5    | RTC_ALMHPM      | 0       | Alarm hours AM/PM flag<br>0 = AM<br>1 = PM<br>Only applicable in 12 hour mode. In 24 hour mode set to 1 if RTC_ALMHRS is set to all 1's 'don't care' or 0 otherwise.  |          |
|                           | 4:0  | RTC_ALMHRS[4:0] | 0_0000  | Hours alarm register with range 0-23 in 24 hours mode and 1-12 in 12 hour. In 12 hour mode bit 5 is used as PM/not-AM flag. All 1's sets to 'don't care' state.<br>Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms. |          |

Register 15h Alarm Hours/Day

| REGISTER ADDRESS           | BIT  | LABEL            | DEFAULT | DESCRIPTION   | REFER TO |
|----------------------------|------|------------------|---------|---|----------|
| R22 (16h) Alarm Date/Month | 12:8 | RTC_ALMMTH[4:0]  | 0_0000  | Month alarm register with range 1-12. All 1's sets to 'don't care' state.<br>Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms. |          |
|                            | 5:0  | RTC_ALMDATE[5:0] | 00_0000 | Date alarm register with range 1-31. All 1's sets to 'don't care' state.<br>Note, during programming it is best to disable the Alarm Enable request bit to avoid false alarms.  |          |

Register 16h Alarm Date/Month

| REGISTER ADDRESS              | BIT | LABEL         | DEFAULT | DESCRIPTION   | REFER TO |
|-------------------------------|-----|---------------|---------|---|----------|
| R23 (17h)<br>RTC Time Control | 15  | RTC_BCD       | 0       | RTC Coding (applies to all time registers)<br>0 = Binary<br>1 = BCD   |          |
|                               | 14  | RTC_12HR      | 0       | RTC 12/24 hours mode<br>1 = 12 hours (MSB of RTC_HRS indicates AM/PM)<br>0 = 24 hours (MSB of RTC_HRS is 0)   |          |
|                               | 11  | RTC_SET       | 0       | Stops RTC seconds counter (instruction only)<br>0 = normal operation<br>1 = stop counter  |          |
|                               | 10  | RTC_STS       | 0       | Status of RTC seconds counter<br>0 = normal operation<br>1 = counter stopped  |          |
|                               | 9   | RTC_ALMSET    | 1       | Stops alarms (instruction only)<br>0 = normal operation<br>1 = stop alarms<br>It is recommended to stop alarms when setting the RTC alarm. This avoids false alarms.  |          |
|                               | 8   | RTC_ALMSTS    | 1       | Actual status of ALARM circuitry<br>0 = normal operation<br>1 = alarms stopped  |          |
|                               | 6:4 | RTC_PINT[2:0] | 010     | Selects frequency of periodic interrupt output pulse (32kHz period duration) as shown below. When set time status is high, the periodic output is disabled.<br>000 = disabled<br>001 = 1 sec<br>010 = 1 min<br>011 = 1 hour<br>100 = 1 day<br>101 = 1 month<br>11x = disabled   |          |
|                               | 3:0 | RTC_DSW[3:0]  | 0000    | Divided Square wave select.<br>0000 = disabled<br>0001 = 1Hz<br>0010 = 2Hz<br>...<br>1011 = 1024Hz<br>1100 = 2048Hz<br>1101 = 4096Hz<br>1110 = 8192Hz<br>1111 = 16384Hz<br>Note: due to trim settings for crystal intolerances a single square wave period during seconds rollover may be decrease its on time period or increase its off time period by up to 8 32kHz periods. |          |

Register 17h RTC Time Control

| REGISTER ADDRESS               | BIT | LABEL      | DEFAULT | DESCRIPTION  | REFER TO |
|--------------------------------|-----|------------|---------|--|----------|
| R24 (18h)<br>System Interrupts | 13  | OC_INT     | 0       | First-level over-current interrupt.<br>Note: This bit is cleared once read.      |          |
|                                | 12  | UV_INT     | 0       | First-level under-voltage interrupt.<br>Note: This bit is cleared once read.     |          |
|                                | 9   | CS_INT     | 0       | First-level current sink interrupt.<br>Note: This bit is cleared once read.      |          |
|                                | 8   | EXT_INT    | 0       | First-level external interrupt.<br>Note: This bit is cleared once read.          |          |
|                                | 7   | CODEC_INT  | 0       | First-level codec interrupt.<br>Note: This bit is cleared once read.             |          |
|                                | 6   | GP_INT     | 0       | First-level GPIO interrupt.<br>Note: This bit is cleared once read.              |          |
|                                | 5   | AUXADC_INT | 0       | First-level AUXADC comparator interrupt.<br>Note: This bit is cleared once read. |          |
|                                | 4   | RTC_INT    | 0       | First-level RTC interrupt.<br>Note: This bit is cleared once read.               |          |
|                                | 3   | SYS_INT    | 0       | First-level system interrupt.<br>Note: This bit is cleared once read.            |          |
|                                | 2   | CHG_INT    | 0       | First-level charger interrupt.<br>Note: This bit is cleared once read.           |          |
|                                | 1   | USB_INT    | 0       | First-level USB interrupt.<br>Note: This bit is cleared once read.               |          |
|                                | 0   | WKUP_INT   | 0       | First-level wakeup interrupt.<br>Note: This bit is cleared once read.            |          |

Register 18h System Interrupts

| REGISTER ADDRESS                | BIT | LABEL              | DEFAULT | DESCRIPTION  | REFER TO |
|---------------------------------|-----|--------------------|---------|--|----------|
| R25 (19h)<br>Interrupt Status 1 | 15  | CHG_BATT_HOT_EINT  | 0       | Battery temp too hot.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                                       |          |
|                                 | 14  | CHG_BATT_COLD_EINT | 0       | Battery temp too cold.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                                      |          |
|                                 | 13  | CHG_BATT_FAIL_EINT | 0       | Battery fail.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |          |
|                                 | 12  | CHG_TO_EINT        | 0       | Charger timeout.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |          |
|                                 | 11  | CHG_END_EINT       | 0       | Charging final stage.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                                       |          |
|                                 | 10  | CHG_START_EINT     | 0       | Charging started.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |          |
|                                 | 9   | CHG_FAST_RDY_EINT  | 0       | Indicates that the charger is ready to go into fast charge.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |          |

| REGISTER ADDRESS | BIT | LABEL                  | DEFAULT | DESCRIPTION   | REFER TO |
|------------------|-----|------------------------|---------|---|----------|
|                  | 7   | RTC_PER_EINT           | 0       | RTC periodic interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.              |          |
|                  | 6   | RTC_SEC_EINT           | 0       | RTC 1s rollover complete (1Hz tick).<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |          |
|                  | 5   | RTC_ALM_EINT           | 0       | RTC alarm etectio.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                   |          |
|                  | 2   | CHG_VBATT_LT_3P9_EINT  | 0       | Battery Voltage < 3.9 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.     |          |
|                  | 1   | CHG_VBATT_LT_3P1_EINT  | 0       | Battery voltage < 3.1 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.     |          |
|                  | 0   | CHG_VBATT_LT_2P85_EINT | 0       | Battery voltage < 2.85 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.    |          |

Register 19h Interrupt Status 1

| REGISTER ADDRESS                   | BIT | LABEL               | DEFAULT | DESCRIPTION   | REFER TO |
|------------------------------------|-----|---------------------|---------|---|----------|
| R26 (1Ah)<br>Interrupt<br>Status 2 | 13  | CS1_EINT            | 0       | Flag to indicate drain voltage can no longer be regulated and output current may be out of spec.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |          |
|                                    | 12  | CS2_EINT            | 0       | Flag to indicate drain voltage can no longer be regulated and output current may be out of spec.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |          |
|                                    | 10  | USB_LIMIT_EINT      | 0       | USB limit switch interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |          |
|                                    | 8   | AUXADC_DATARDY_EINT | 0       | Auxiliary data ready.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |          |
|                                    | 7   | AUXADC_DCOMP4_EINT  | 0       | DCOMP4 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |          |
|                                    | 6   | AUXADC_DCOMP3_EINT  | 0       | DCOMP3 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |          |
|                                    | 5   | AUXADC_DCOMP2_EINT  | 0       | DCOMP2 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |          |
|                                    | 4   | AUXADC_DCOMP1_EINT  | 0       | DCOMP1 interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |          |

| REGISTER ADDRESS | BIT | LABEL                   | DEFAULT | DESCRIPTION  | REFER TO |
|------------------|-----|-------------------------|---------|--|----------|
|                  | 3   | SYS_HYST_COMP_FAIL_EINT | 0       | Hysteresis comparator indication that LINE or BATT is less than shutdown threshold.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |          |
|                  | 2   | SYS_CHIP_GT115_EINT     | 0       | Chip over 115°C temp limit.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |          |
|                  | 1   | SYS_CHIP_GT140_EINT     | 0       | Chip over 140°C temp limit.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |          |
|                  | 0   | SYS_WDOG_TO_EINT        | 0       | Watchdog timeout has occurred.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |          |

Register 1Ah Interrupt Status 2

| REGISTER ADDRESS                            | BIT | LABEL        | DEFAULT | DESCRIPTION   | REFER TO |
|---|-----|--------------|---------|---|----------|
| R28 (1Ch)<br>Under Voltage Interrupt status | 11  | UV_LDO4_EINT | 0       | LDO4 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |          |
|   | 10  | UV_LDO3_EINT | 0       | LDO3 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |          |
|   | 9   | UV_LDO2_EINT | 0       | LDO2 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |          |
|   | 8   | UV_LDO1_EINT | 0       | LDO1 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.  |          |
|   | 5   | UV_DC6_EINT  | 0       | DCDC6 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |          |
|   | 4   | UV_DC5_EINT  | 0       | DCDC5 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |          |
|   | 3   | UV_DC4_EINT  | 0       | DCDC4 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |          |
|   | 2   | UV_DC3_EINT  | 0       | DCDC3 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |          |
|   | 1   | UV_DC2_EINT  | 0       | DCDC2 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |          |
|   | 0   | UV_DC1_EINT  | 0       | DCDC1 Under-voltage interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |          |

Register 1Ch Under Voltage Interrupt status

| REGISTER ADDRESS                                 | BIT | LABEL      | DEFAULT | DESCRIPTION   | REFER TO |
|--|-----|------------|---------|---|----------|
| R29 (1Dh)<br>Over Current<br>Interrupt<br>status | 15  | OC_LS_EINT | 0       | Overcurrent interrupt.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |          |

**Register 1Dh** Over Current Interrupt status

| REGISTER ADDRESS                         | BIT | LABEL     | DEFAULT | DESCRIPTION  | REFER TO |
|--|-----|-----------|---------|--|----------|
| R30 (1Eh)<br>GPIO<br>Interrupt<br>Status | 12  | GP12_EINT | 0       | GPIO12 interrupt.<br>(Trigger controlled by GP12 registers.)<br>Note: This bit is cleared once read. |          |
|  | 11  | GP11_EINT | 0       | GPIO11 interrupt.<br>(Trigger controlled by GP11 registers.)<br>Note: This bit is cleared once read. |          |
|  | 10  | GP10_EINT | 0       | GPIO10 interrupt.<br>(Trigger controlled by GP10 registers.)<br>Note: This bit is cleared once read. |          |
|  | 9   | GP9_EINT  | 0       | GPIO9 interrupt.<br>(Trigger controlled by GP9 registers.)<br>Note: This bit is cleared once read.   |          |
|  | 8   | GP8_EINT  | 0       | GPIO8 interrupt.<br>(Trigger controlled by GP8 registers.)<br>Note: This bit is cleared once read.   |          |
|  | 7   | GP7_EINT  | 0       | GPIO7 interrupt.<br>(Trigger controlled by GP7 registers.)<br>Note: This bit is cleared once read.   |          |
|  | 6   | GP6_EINT  | 0       | GPIO6 interrupt.<br>(Trigger controlled by GP6 registers.)<br>Note: This bit is cleared once read.   |          |
|  | 5   | GP5_EINT  | 0       | GPIO5 interrupt.<br>(Trigger controlled by GP5 registers.)<br>Note: This bit is cleared once read.   |          |
|  | 4   | GP4_EINT  | 0       | GPIO4 interrupt.<br>(Trigger controlled by GP4 registers.)<br>Note: This bit is cleared once read.   |          |
|  | 3   | GP3_EINT  | 0       | GPIO3 interrupt.<br>(Trigger controlled by GP3 registers.)<br>Note: This bit is cleared once read.   |          |
|  | 2   | GP2_EINT  | 0       | GPIO2 interrupt.<br>(Trigger controlled by GP2 registers.)<br>Note: This bit is cleared once read.   |          |
|  | 1   | GP1_EINT  | 0       | GPIO1 interrupt.<br>(Trigger controlled by GP1 registers.)<br>Note: This bit is cleared once read.   |          |
|  | 0   | GP0_EINT  | 0       | GPIO0 interrupt.<br>(Trigger controlled by GP0 registers.)<br>Note: This bit is cleared once read.   |          |

**Register 1Eh** GPIO Interrupt Status

| REGISTER ADDRESS                               | BIT                 | LABEL                | DEFAULT  | DESCRIPTION  | REFER TO |
|--|---------------------|----------------------|--|--|----------|
| R31 (1Fh)<br>Comparator<br>Interrupt<br>Status | 15                  | EXT_USB_FB_EINT      | 0  | USB_FB changed interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.   |          |
|  | 14                  | EXT_WALL_FB_EINT     | 0  | WALL_FB changed interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.  |          |
|  | 13                  | EXT_BATT_FB_EINT     | 0  | BATT_FB changed interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.  |          |
|  | 11                  | CODEC_JCK_DET_L_EINT | 0  | Left channel Jack detection interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.  |          |
|  | 10                  | CODEC_JCK_DET_R_EINT | 0  | Right channel Jack detection interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.   |          |
|  | 9                   | CODEC_MICSCD_EINT    | 0  | Mic short-circuit detect interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.   |          |
|  | 8                   | CODEC_MICD_EINT      | 0  | Mic detect interrupt.<br>(Rising and Falling Edge triggered)<br>Note: This bit is cleared once read.   |          |
|  | 6                   | WKUP_OFF_STATE_EINT  | 0  | Indicates that the chip started from the OFF state.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |          |
|  | 5                   | WKUP_HIB_STATE_EINT  | 0  | Indicated the chip started up from the hibernate state.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |          |
|  | 4                   | WKUP_CONV_FAULT_EINT | 0  | Indicates the wakeup was caused by a converter fault leading to the chip being reset.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                 |          |
|  | 3                   | WKUP_WDOG_RST_EINT   | 0  | Indicates the wakeup was caused by a watchdog heartbeat being missed, and hence the chip being reset.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |          |
|  | 2                   | WKUP_GP_PWR_ON_EINT  | 0  | PWR_ON (Alternate GPIO function) pin has been pressed for longer than specified time.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.                 |          |
|  | 1                   | WKUP_ONKEY_EINT      | 0  | ON key has been pressed for longer than specified time.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read.   |          |
| 0  | WKUP_GP_WAKEUP_EINT | 0                    | WAKEUP (Alternate GPIO function) pin has been pressed for longer than specified time.<br>(Rising Edge triggered)<br>Note: This bit is cleared once read. |  |          |

Register 1Fh Comparator Interrupt Status



| REGISTER ADDRESS                          | BIT | LABEL         | DEFAULT | DESCRIPTION  | REFER TO |
|---|-----|---------------|---------|--|----------|
| R32 (20h)<br>System<br>Interrupts<br>Mask | 13  | IM_OC_INT     | 1       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|   | 12  | IM_UV_INT     | 1       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|   | 9   | IM_CS_INT     | 1       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|   | 8   | IM_EXT_INT    | 1       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|   | 7   | IM_CODEEC_INT | 1       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|   | 6   | IM_GP_INT     | 1       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|   | 5   | IM_AUXADC_INT | 1       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|   | 4   | IM_RTC_INT    | 1       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|   | 3   | IM_SYS_INT    | 1       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|   | 2   | IM_CHG_INT    | 1       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|   | 1   | IM_USB_INT    | 1       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|   | 0   | IM_WKUP_INT   | 1       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine. Default held in metal mask.</i> |          |

Register 20h System Interrupts Mask

| REGISTER ADDRESS                     | BIT | LABEL                     | DEFAULT | DESCRIPTION  | REFER TO |
|--------------------------------------|-----|---------------------------|---------|--|----------|
| R33 (21h)<br>Interrupt Status 1 Mask | 15  | IM_CHG_BATT_HOT_EINT      | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 14  | IM_CHG_BATT_COLD_EINT     | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 13  | IM_CHG_BATT_FAIL_EINT     | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 12  | IM_CHG_TO_EINT            | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 11  | IM_CHG_END_EINT           | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 10  | IM_CHG_START_EINT         | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 9   | IM_CHG_FAST_RDY_EINT      | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 7   | IM_RTC_PER_EINT           | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 6   | IM_RTC_SEC_EINT           | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 5   | IM_RTC_ALM_EINT           | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 2   | IM_CHG_VBATT_LT_3P9_EINT  | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 1   | IM_CHG_VBATT_LT_3P1_EINT  | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 0   | IM_CHG_VBATT_LT_2P85_EINT | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |

Register 21h Interrupt Status 1 Mask

| REGISTER ADDRESS                     | BIT | LABEL                      | DEFAULT | DESCRIPTION  | REFER TO |
|--------------------------------------|-----|----------------------------|---------|--|----------|
| R34 (22h)<br>Interrupt Status 2 Mask | 13  | IM_CS1_EINT                | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 12  | IM_CS2_EINT                | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 10  | IM_USB_LIMIT_EINT          | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 8   | IM_AUXADC_DATARDY_EINT     | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 7   | IM_AUXADC_DCOMP4_EINT      | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 6   | IM_AUXADC_DCOMP3_EINT      | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 5   | IM_AUXADC_DCOMP2_EINT      | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 4   | IM_AUXADC_DCOMP1_EINT      | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 3   | IM_SYS_HYST_COMP_FAIL_EINT | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 2   | IM_SYS_CHIP_GT115_EINT     | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 1   | IM_SYS_CHIP_GT140_EINT     | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|                                      | 0   | IM_SYS_WDOG_TO_EINT        | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |

Register 22h Interrupt Status 2 Mask

| REGISTER ADDRESS                                 | BIT | LABEL           | DEFAULT | DESCRIPTION  | REFER TO |
|--|-----|-----------------|---------|--|----------|
| R36 (24h)<br>Under Voltage Interrupt status Mask | 11  | IM_UV_LDO4_EINT | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|  | 10  | IM_UV_LDO3_EINT | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|  | 9   | IM_UV_LDO2_EINT | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|  | 8   | IM_UV_LDO1_EINT | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|  | 5   | IM_UV_DC6_EINT  | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|  | 4   | IM_UV_DC5_EINT  | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|  | 3   | IM_UV_DC4_EINT  | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|  | 2   | IM_UV_DC3_EINT  | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|  | 1   | IM_UV_DC2_EINT  | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|  | 0   | IM_UV_DC1_EINT  | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |

Register 24h Under Voltage Interrupt status Mask

| REGISTER ADDRESS                                | BIT | LABEL         | DEFAULT | DESCRIPTION  | REFER TO |
|---|-----|---------------|---------|--|----------|
| R37 (25h)<br>Over Current Interrupt status Mask | 15  | IM_OC_LS_EINT | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |

Register 25h Over Current Interrupt status Mask

| REGISTER ADDRESS                              | BIT | LABEL        | DEFAULT | DESCRIPTION  | REFER TO |
|---|-----|--------------|---------|--|----------|
| R38 (26h)<br>GPIO<br>Interrupt<br>Status Mask | 12  | IM_GP12_EINT | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 11  | IM_GP11_EINT | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 10  | IM_GP10_EINT | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 9   | IM_GP9_EINT  | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 8   | IM_GP8_EINT  | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 7   | IM_GP7_EINT  | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 6   | IM_GP6_EINT  | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 5   | IM_GP5_EINT  | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 4   | IM_GP4_EINT  | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 3   | IM_GP3_EINT  | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 2   | IM_GP2_EINT  | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 1   | IM_GP1_EINT  | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 0   | IM_GP0_EINT  | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |

Register 26h GPIO Interrupt Status Mask

| REGISTER ADDRESS                                    | BIT                | LABEL                   | DEFAULT  | DESCRIPTION  | REFER TO |
|---|--------------------|-------------------------|--|--|----------|
| R39 (27h)<br>Comparator<br>Interrupt<br>Status Mask | 15                 | IM_EXT_USB_FB_EINT      | 0  | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 14                 | IM_EXT_WALL_FB_EINT     | 0  | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 13                 | IM_EXT_BATT_FB_EINT     | 0  | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 11                 | IM_CODEC_JCK_DET_L_EINT | 0  | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 10                 | IM_CODEC_JCK_DET_R_EINT | 0  | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 9                  | IM_CODEC_MICSCD_EINT    | 0  | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 8                  | IM_CODEC_MICD_EINT      | 0  | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 6                  | IM_WKUP_OFF_STATE_EINT  | 0  | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 5                  | IM_WKUP_HIB_STATE_EINT  | 0  | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 4                  | IM_WKUP_CONV_FAULT_EINT | 0  | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 3                  | IM_WKUP_WDOG_RST_EINT   | 0  | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
|   | 2                  | IM_WKUP_GP_PWR_ON_EINT  | 0  | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |
| 1   | IM_WKUP_ONKEY_EINT | 0                       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt. |  |          |

| REGISTER ADDRESS | BIT | LABEL                  | DEFAULT | DESCRIPTION  | REFER TO |
|------------------|-----|------------------------|---------|--|----------|
|                  |     |                        |         | <i>Reset by state machine.</i>   |          |
|                  | 0   | IM_WKUP_GP_WAKEUP_EINT | 0       | Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.<br><i>Reset by state machine.</i> |          |

Register 27h Comparator Interrupt Status Mask

| REGISTER ADDRESS                | BIT | LABEL          | DEFAULT | DESCRIPTION  | REFER TO |
|---------------------------------|-----|----------------|---------|--|----------|
| R40 (28h)<br>Clock<br>Control 1 | 15  | TOCLK_ENA      | 0       | Slow clock enable. Used for both the jack insert detect debounce circuit and the zero cross timeout.<br>0 = slow clock disabled<br>1 = slow clock enabled  |          |
|                                 | 14  | TOCLK_RATE     | 0       | Slow Clock Selection (Used for volume update timeouts and for jack detect debounce)<br>0 = SYSCLK / 2 <sup>21</sup> (Slower Response)<br>1 = SYSCLK / 2 <sup>19</sup> (Faster Response)  |          |
|                                 | 11  | MCLK_SEL       | 0       | Selects source for SYSCLK to CODEC<br>0 = MCLK pin<br>1 = FLL  |          |
|                                 | 8   | MCLK_DIV       | 0       | Selects MCLK division in slave (MCLK input) mode:<br>0 = divide MCLK by 1<br>1 = divide MCLK by 2  |          |
|                                 | 7:4 | BCLK_DIV[3:0]  | 0100    | Sets BCLK rate for Master mode<br>0000 = SYSCLK<br>0001 = SYSCLK / 1.5<br>0010 = SYSCLK / 2<br>0011 = SYSCLK / 3<br>0100 = SYSCLK / 4<br>0101 = SYSCLK / 5.5<br>0110 = SYSCLK / 6<br>0111 = SYSCLK / 8<br>1000 = SYSCLK / 11<br>1001 = SYSCLK / 12<br>1010 = SYSCLK / 16<br>1011 = SYSCLK / 22<br>1100 = SYSCLK / 24<br>1101 = SYSCLK / 32<br>1110 = SYSCLK / 32<br>1111 = SYSCLK / 32 |          |
|                                 | 2:0 | OPCLK_DIV[2:0] | 000     | OPCLK Frequency (GPIO function)<br>000 = SYSCLK<br>001 = SYSCLK / 2<br>010 = SYSCLK / 3<br>011 = SYSCLK / 4<br>100 = SYSCLK / 5.5<br>101 = SYSCLK / 6<br>110 = Reserved<br>111 = Reserved  |          |

Register 28h Clock Control 1

| REGISTER ADDRESS             | BIT | LABEL       | DEFAULT | DESCRIPTION   | REFER TO |
|------------------------------|-----|-------------|---------|---|----------|
| R41 (29h)<br>Clock Control 2 | 15  | LRC_ADC_SEL | 0       | Selects either ADCLRCLK or DACLRCLK to drive LRCLK pin in Master mode<br>0 = DACLRCLK<br>1 = ADCLRCLK |          |
|                              | 0   | MCLK_DIR    | 0       | Whether MCLK is an input or an output.<br>0 = MCLK is an input<br>1 = MCLK is an output               |          |

Register 29h Clock Control 2

| REGISTER ADDRESS           | BIT  | LABEL            | DEFAULT | DESCRIPTION  | REFER TO |
|----------------------------|------|------------------|---------|--|----------|
| R42 (2Ah)<br>FLL Control 1 | 15   | FLL_ENA          | 0       | Digital Enable for FLL<br>0 = disabled<br>1 = enabled<br>Note that FLL_OSC_ENA must be enabled before enabling FLL_ENA.  |          |
|                            | 14   | FLL_OSC_ENA      | 0       | Analogue Enable for FLL<br>0 = FLL disabled<br>1 = FLL enabled<br>Note that FLL_OSC_ENA must be enabled before enabling FLL_ENA.   |          |
|                            | 10:8 | FLL_OUTDIV [2:0] | 010     | F <sub>OUT</sub> clock divider<br>000 = F <sub>VCO</sub> / 2<br>001 = F <sub>VCO</sub> / 4<br>010 = F <sub>VCO</sub> / 8<br>011 = F <sub>VCO</sub> / 16<br>100 = F <sub>VCO</sub> / 32<br>101 = Reserved<br>110 = Reserved<br>111 = Reserved   |          |
|                            | 7:4  | FLL_RSP_RATE     | 0000    | FLL Loop Gain<br>0000 = x 1 (Recommended value)<br>0001 = x 2<br>0010 = x 4<br>0011 = x 8<br>0100 = x 16<br>0101 = x 32<br>0110 = x 64<br>0111 = x 128<br>1000 = x 256<br>Recommended that these are not changed from default.   |          |
|                            | 2:0  | FLL_RATE [2:0]   | 000     | Frequency of the FLL control block<br>000 = F <sub>VCO</sub> / 1 (Recommended value)<br>001 = F <sub>VCO</sub> / 2<br>010 = F <sub>VCO</sub> / 4<br>011 = F <sub>VCO</sub> / 8<br>100 = F <sub>VCO</sub> / 16<br>101 = F <sub>VCO</sub> / 32<br>Recommended that these are not changed from default. |          |

Register 2Ah FLL Control 1



| REGISTER ADDRESS           | BIT   | LABEL           | DEFAULT     | DESCRIPTION  | REFER TO |
|----------------------------|-------|-----------------|-------------|--|----------|
| R43 (2Bh)<br>FLL Control 2 | 15:11 | FLL_RATIO [4:0] | 14<br>(0Eh) | CLK_VCO is divided by this integer, valid from 1 .. 31.<br>1 recommended for high freq reference<br>8 recommended for low freq reference |          |
|                            | 9:0   | FLL_N [9:0]     | 086h        | FLL integer multiplier N for CLK_REF   |          |

Register 2Bh FLL Control 2

| REGISTER ADDRESS           | BIT  | LABEL        | DEFAULT | DESCRIPTION  | REFER TO |
|----------------------------|------|--------------|---------|--|----------|
| R44 (2Ch)<br>FLL Control 3 | 15:0 | FLL_K [15:0] | C226h   | FLL fractional multiplier K for CLK_REF. This is only used if FLL_FRAC is set. |          |

Register 2Ch FLL Control 3

| REGISTER ADDRESS             | BIT | LABEL             | DEFAULT | DESCRIPTION  | REFER TO |
|------------------------------|-----|-------------------|---------|--|----------|
| R45 (2Dh)<br>Clock Control 1 | 7   | FLL_REF_FREQ      | 0       | Low frequency reference locking<br>0 = High frequency reference locking (recommended for reference clock > 48kHz)<br>1 = Lock frequency reference locking (recommended for reference clock <= 48kHz) |          |
|                              | 5   | FLL_FRAC          | 0       | Fractional enable<br>0 = Integer Mode<br>1 = Fractional Mode<br><br>1 recommended in all cases   |          |
|                              | 1:0 | FLL_CLK_SRC [1:0] | 00      | Select FLL input clock Source<br>00 = MCLK<br>01 = DACLRCLK<br>10 = ADCLRCLK<br>11 = CLK_32K_REF   |          |

Register 2Dh FLL Control 4

| REGISTER ADDRESS         | BIT | LABEL           | DEFAULT | DESCRIPTION   | REFER TO |
|--------------------------|-----|-----------------|---------|---|----------|
| R48 (30h)<br>DAC Control | 13  | DAC_MONO        | 0       | Adds left and right channel and halves the resulting output to create a mono output   |          |
|                          | 12  | AIF_LRCLKRATE   | 0       | Mode Select<br>1 = USB mode (272 * Fs)<br>0 = Normal mode (256 * Fs)  |          |
|                          | 5:4 | DEEMP[1:0]      | 00      | DAC De-emphasis filter control<br>00 = No de-emphasis<br>01 = 32kHz sample rate<br>10 = 44.1kHz sample rate<br>11 = 48kHz sample rate   |          |
|                          | 3   | DAC_SDMCLK_RATE | 0       | DAC_SDMCLK_RATE allows the DAC SDM to be run at a speed higher than 64*fs. This is used for low sample rate modes to allow the SDM to run fast enough to shape the noise so that none of it appears in the audio band. On the previous version, at 8k sample rate you could hear some high frequency noise when playing back through a decent system. |          |
|                          | 1   | DACL_DATINV     | 0       | DAC data left channel polarity<br>0 = Normal<br>1 = Inverted  |          |
|                          | 0   | DACR_DATINV     | 0       | DAC data right channel polarity<br>0 = Normal<br>1 = Inverted   |          |

Register 30h DAC Control

| REGISTER ADDRESS                  | BIT | LABEL         | DEFAULT   | DESCRIPTION   | REFER TO |
|-----------------------------------|-----|---------------|-----------|---|----------|
| R50 (32h)<br>DAC Digital Volume L | 15  | DACL_ENA      | 0         | Left DAC enable<br>0 = disabled<br>1 = enabled  |          |
|                                   | 8   | DAC_VU        | 0         | DAC left and DAC right volume do not update until a 1 is written to either DAC_VU register bit.   |          |
|                                   | 7:0 | DACL_VOL[7:0] | 1100_0000 | Left DAC digital volume control:<br>0000_0000 = Digital mute<br>0000_0001 = -71.625dB<br>0000_0010 = -71.25dB<br>... (0.375dB steps)<br>1100_0000 = 0dB |          |

Register 32h DAC Digital Volume L

| REGISTER ADDRESS                     | BIT | LABEL         | DEFAULT   | DESCRIPTION   | REFER TO |
|--------------------------------------|-----|---------------|-----------|---|----------|
| R51 (33h)<br>DAC Digital<br>Volume R | 15  | DACR_ENA      | 0         | Right DAC enable<br>0 = disabled<br>1 = enabled   |          |
|                                      | 8   | DAC_VU        | 0         | DAC left and DAC right volume do not update until a 1 is written to either DAC_VU register bit.   |          |
|                                      | 7:0 | DACR_VOL[7:0] | 1100_0000 | Right DAC digital volume control:<br>0000_0000 = Digital mute<br>0000_0001 = -71.625dB<br>0000_0010 = -71.25dB<br>... (0.375dB steps)<br>1100_000 = 0dB |          |

Register 33h DAC Digital Volume R

| REGISTER ADDRESS            | BIT  | LABEL             | DEFAULT       | DESCRIPTION   | REFER TO |
|-----------------------------|------|-------------------|---------------|---|----------|
| R53 (35h)<br>DAC LR<br>Rate | 11   | DACLRC_ENA        | 0             | Enables DAC LRC generation in Master mode<br>0 = disabled<br>1 = enabled  |          |
|                             | 10:0 | DACLRC_RATE[10:0] | 000_0100_0000 | Determines the number of bit clocks per LRC phase (when enabled)<br>000000000000 = invalid<br>...<br>000000001111 = invalid<br>000000010000 = 8 BCPS<br>...<br>111111111111 = 2047 BCPS |          |

Register 35h DAC LR Rate

| REGISTER ADDRESS                  | BIT | LABEL           | DEFAULT | DESCRIPTION   | REFER TO |
|-----------------------------------|-----|-----------------|---------|---|----------|
| R54 (36h)<br>DAC Clock<br>Control | 4   | DACCLK_POL      | 0       | DAC Clock Polarity<br>0 = Normal<br>1 = Inverted  |          |
|                                   | 2:0 | DAC_CLKDIV[2:0] | 000     | DAC Sample rate divider<br>000 = SYSCLK / 1.0<br>001 = SYSCLK / 1.5<br>010 = SYSCLK / 2<br>011 = SYSCLK / 3<br>100 = SYSCLK / 4<br>101 = SYSCLK / 5.5<br>110 = SYSCLK / 6<br>111 = Reserved |          |

Register 36h DAC Clock Control

| REGISTER ADDRESS      | BIT | LABEL    | DEFAULT | DESCRIPTION                             | REFER TO |
|-----------------------|-----|----------|---------|---|----------|
| R58 (3Ah)<br>DAC Mute | 14  | DAC_MUTE | 1       | DAC Mute<br>0 = disabled<br>1 = enabled |          |

Register 3Ah DAC Mute

| REGISTER ADDRESS                | BIT | LABEL        | DEFAULT | DESCRIPTION   | REFER TO |
|---------------------------------|-----|--------------|---------|---|----------|
| R59 (3Bh)<br>DAC Mute<br>Volume | 14  | DAC_MUTEMODE | 0       | DAC Soft Mute Mode<br>0 = Disabling soft-mute (DAC_MUTE=0) will cause the volume to change immediately to the DACL_VOL / DACR_VOL settings<br>1 = Disabling soft-mute (DAC_MUTE=0) will cause the volume to ramp up gradually to the DACL_VOL / DACR_VOL settings |          |
|                                 | 13  | DAC_MUTERATE | 0       | DAC Soft Mute Ramp Rate<br>0 = Fast ramp (24kHz at fs=48k, providing maximum delay of 10.7ms)<br>1 = Slow ramp (1.5kHz at fs=48k, providing maximum delay of 171ms)   |          |
|                                 | 12  | DAC_SB_FILT  | 0       | Selects DAC filter characteristics<br>0 = Normal mode<br>1 = Sloping stopband mode  |          |

Register 3Bh DAC Mute Volume

| REGISTER ADDRESS      | BIT   | LABEL            | DEFAULT | DESCRIPTION   | REFER TO |
|-----------------------|-------|------------------|---------|---|----------|
| R60 (3Ch)<br>DAC Side | 13:12 | ADC_TO_DACL[1:0] | 00      | DAC Left Side-tone Control<br>11 = Unused<br>10 = Mix ADCR into DACL<br>01 = Mix ADCL into DACL<br>00 = No Side-tone mix into DACL  |          |
|                       | 11:10 | ADC_TO_DACR[1:0] | 00      | DAC Right Side-tone Control<br>11 = Unused<br>10 = Mix ADCR into DACR<br>01 = Mix ADCL into DACR<br>00 = No Side-tone mix into DACR |          |

Register 3Ch DAC Side

| REGISTER ADDRESS         | BIT | LABEL            | DEFAULT | DESCRIPTION  | REFER TO |
|--------------------------|-----|------------------|---------|--|----------|
| R64 (40h)<br>ADC Control | 15  | ADC_HPF_ENA      | 1       | High Pass Filter enable<br>0 = disabled<br>1 = enabled   |          |
|                          | 9:8 | ADC_HPF_CUT[1:0] | 00      | Select cut-off frequency for high-pass filter<br>00 = $2^{-11}$ (first order) = 3.7Hz @44.1kHz<br>01 = $2^{-5}$ (2nd order) = ~250Hz @8kHz<br>10 = $2^{-4}$ (2nd order) = ~250Hz @16kHz<br>11 = $2^{-3}$ (2nd order) = ~250Hz @32kHz |          |
|                          | 1   | ADCL_DATINV      | 0       | ADC Left channel polarity:<br>0 = Normal<br>1 = Inverted   |          |
|                          | 0   | ADCR_DATINV      | 0       | ADC Right Channel Polarity<br>0 = Normal<br>1 = Inverted   |          |

Register 40h ADC Control

| REGISTER ADDRESS                  | BIT | LABEL         | DEFAULT   | DESCRIPTION  | REFER TO |
|-----------------------------------|-----|---------------|-----------|--|----------|
| R66 (42h)<br>ADC Digital Volume L | 15  | ADCL_ENA      | 0         | Left ADC enable<br>0 = disabled<br>1 = enabled   |          |
|                                   | 8   | ADC_VU        | 0         | ADC left and ADC right volume do not update until a 1 is written to either ADC_VU register bit.  |          |
|                                   | 7:0 | ADCL_VOL[7:0] | 1100_0000 | Left ADC Digital Volume Control<br>0000 0000 = Digital Mute<br>0000 0001 = -71.625dB<br>0000 0010 = -71.25dB<br>... 0.375dB steps up to<br>1110 1111 = +17.625dB |          |

Register 42h ADC Digital Volume L

| REGISTER ADDRESS                  | BIT | LABEL         | DEFAULT   | DESCRIPTION   | REFER TO |
|-----------------------------------|-----|---------------|-----------|---|----------|
| R67 (43h)<br>ADC Digital Volume R | 15  | ADCR_ENA      | 0         | Right ADC enable<br>0 = disabled<br>1 = enabled   |          |
|                                   | 8   | ADC_VU        | 0         | ADC left and ADC right volume do not update until a 1 is written to either ADC_VU register bit.   |          |
|                                   | 7:0 | ADCR_VOL[7:0] | 1100_0000 | Right ADC Digital Volume Control<br>0000 0000 = Digital Mute<br>0000 0001 = -71.625dB<br>0000 0010 = -71.25dB<br>... 0.375dB steps up to<br>1110 1111 = +17.625dB |          |

Register 43h ADC Digital Volume R

| REGISTER ADDRESS         | BIT  | LABEL              | DEFAULT | DESCRIPTION   | REFER TO |
|--------------------------|------|--------------------|---------|---|----------|
| R68 (44h)<br>ADC Divider | 11:8 | ADCL_DAC_SVOL[3:0] | 0000    | Controls left digital side tone volume from -36dB to 0dB in 3dB steps.  |          |
|                          | 7:4  | ADCR_DAC_SVOL[3:0] | 0000    | Controls right digital side tone volume from -36dB to 0dB in 3dB steps.   |          |
|                          | 3    | ADCCLK_POL         | 0       | ADC Clock Polarity<br>0 = Normal<br>1 = Inverted  |          |
|                          | 2:0  | ADC_CLKDIV[2:0]    | 000     | ADC Sample rate divider<br>000 = SYSCLK / 1.0<br>001 = SYSCLK / 1.5<br>010 = SYSCLK / 2<br>011 = SYSCLK / 3<br>100 = SYSCLK / 4<br>101 = SYSCLK / 5.5<br>110 = SYSCLK / 6<br>111 = Reserved |          |

Register 44h ADC Divider

| REGISTER ADDRESS         | BIT  | LABEL             | DEFAULT       | DESCRIPTION   | REFER TO |
|--------------------------|------|-------------------|---------------|---|----------|
| R70 (46h)<br>ADC LR Rate | 11   | ADCLRC_ENA        | 0             | Enables the LRC generation for the ADC<br>0 = disabled<br>1 = enabled   |          |
|                          | 10:0 | ADCLRC_RATE[10:0] | 000_0100_0000 | Determines the number of bit clocks per LRC phase (when enabled)<br>000000000000 = invalid<br>...<br>000000001111 = invalid<br>000000010000 = 8 BCPS<br>...<br>111111111111 = 2047 BCPS |          |

Register 46h ADC LR Rate

| REGISTER ADDRESS           | BIT | LABEL     | DEFAULT | DESCRIPTION  | REFER TO |
|----------------------------|-----|-----------|---------|--|----------|
| R72 (48h)<br>Input Control | 10  | IN2R_ENA  | 0       | Connect IN2R pin to right channel input PGA<br>0 = IN2R not connected to input PGA amplifier<br>1 = IN2R connected to input PGA amplifier  |          |
|                            | 9   | IN1RN_ENA | 1       | Connect IN1RN pin to right channel input PGA negative terminal.<br>0 = IN1RN not connected to input PGA<br>1 = IN1RN connected to right channel input PGA amplifier negative terminal.                                     |          |
|                            | 8   | IN1RP_ENA | 1       | Connect IN1RP pin to right channel input PGA amplifier positive terminal.<br>0 = IN1RP not connected to input PGA<br>1 = right channel input PGA amplifier positive terminal connected to IN1RP (constant input impedance) |          |
|                            | 2   | IN2L_ENA  | 0       | Connect IN2L pin to left channel input PGA amplifier<br>0 = IN2L not connected to input PGA amplifier<br>1 = IN2L connected to input PGA amplifier   |          |

| REGISTER ADDRESS | BIT | LABEL     | DEFAULT | DESCRIPTION   | REFER TO |
|------------------|-----|-----------|---------|---|----------|
|                  | 1   | IN1LN_ENA | 1       | Connect IN1LN pin to left channel input PGA negative terminal.<br>0 = IN1LN not connected to input PGA<br>1 = IN1LN connected to input PGA amplifier negative terminal.                                     |          |
|                  | 0   | IN1LP_ENA | 1       | Connect IN1LP pin to left channel input PGA amplifier positive terminal.<br>0 = IN1LP not connected to input PGA<br>1 = input PGA amplifier positive terminal connected to IN1LP (constant input impedance) |          |

Register 48h Input Control

| REGISTER ADDRESS               | BIT | LABEL      | DEFAULT | DESCRIPTION  | REFER TO |
|--------------------------------|-----|------------|---------|--|----------|
| R73 (49h)<br>IN3 Input Control | 15  | IN3R_ENA   | 0       | IN3R Amplifier enable<br>0 = disabled<br>1 = enabled   |          |
|                                | 14  | IN3R_SHORT | 0       | Short circuit internal input resistor for IN3R amplifier.<br>0 = Internal resistor in circuit.<br>1 = Internal resistor shorted. |          |
|                                | 7   | IN3L_ENA   | 0       | IN3L Amplifier enable<br>0 = disabled<br>1 = enabled   |          |
|                                | 6   | IN3L_SHORT | 0       | Short circuit internal input resistor for IN3L amplifier.<br>0 = Internal resistor in circuit.<br>1 = Internal resistor shorted. |          |

Register 49h IN3 Input Control

| REGISTER ADDRESS              | BIT | LABEL         | DEFAULT | DESCRIPTION   | REFER TO |
|-------------------------------|-----|---------------|---------|---|----------|
| R74 (4Ah)<br>Mic Bias Control | 15  | MICB_ENA      | 0       | Microphone bias enable<br>0 = OFF (high impedance output)<br>1 = ON   |          |
|                               | 14  | MICB_SEL      | 0       | Microphone bias voltage control:<br>0 = 0.9 * AVDD<br>1 = 0.75 * AVDD   |          |
|                               | 7   | MIC_DET_ENA   | 0       | Enable MIC detect:<br>0 = Disabled<br>1 = Enabled   |          |
|                               | 4:2 | MCDTHR[2:0]   | 000     | Threshold for bias current detection<br>000 = 160µA<br>001 = 330µA<br>010 = 500µA<br>011 = 680µA<br>100 = 850µA<br>101 = 1000µA<br>110 = 1200µA<br>111 = 1400µA<br>These threshold currents scale proportionally with AVDD. The values given are for AVDD=3.3V. |          |
|                               | 1:0 | MCDSCTHR[1:0] | 00      | Threshold for microphone short-circuit detection  |          |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION  | REFER TO |
|------------------|-----|-------|---------|--|----------|
|                  |     |       |         | 00 = 400 $\mu$ A<br>01 = 900 $\mu$ A<br>10 = 1350 $\mu$ A<br>11 = 1800 $\mu$ A<br>These threshold currents scale proportionally with AVDD. The values given are for AVDD=3.3V. |          |

Register 4Ah Mic Bias Control

| REGISTER ADDRESS            | BIT | LABEL            | DEFAULT | DESCRIPTION  | REFER TO |
|-----------------------------|-----|------------------|---------|--|----------|
| R76 (4Ch)<br>Output Control | 11  | OUT4_VROI        | 0       | VREF (AVDD/2) to OUT4 resistance<br>0 = approx 500 ohms<br>1 = approx 30 kOhms   |          |
|                             | 10  | OUT3_VROI        | 0       | VREF (AVDD/2) to OUT3 resistance<br>0 = approx 500 ohms<br>1 = approx 30 kOhms   |          |
|                             | 9   | OUT2_VROI        | 0       | VREF (AVDD/2) to OUT2L and OUT2R resistance<br>0 = approx 500 ohms<br>1 = approx 30 kOhms  |          |
|                             | 8   | OUT1_VROI        | 0       | VREF (AVDD/2) to OUT1L and OUT1R resistance<br>0 = approx 500 ohms<br>1 = approx 30 kOhms  |          |
|                             | 4   | OUTPUT_DRAIN_ENA | 0       | Enables a drain on the outputs allowing the amplifiers to shutdown more quickly.<br>0 = Shutdown as normal<br>1 = Sink current from an external capacitor, allowing faster shutdown. |          |
|                             | 2   | OUT2_FB          | 0       | Enable Headphone common mode ground feedback for OUT2<br>0 = disabled (HPCOM unused)<br>1 = enabled (common mode feedback through HPCOM)   |          |
|                             | 0   | OUT1_FB          | 0       | Enable Headphone common mode ground feedback for OUT1<br>0 = disabled (HPCOM unused)<br>1 = enabled (common mode feedback through HPCOM)   |          |

Register 4Ch Output Control

| REGISTER ADDRESS         | BIT | LABEL   | DEFAULT | DESCRIPTION  | REFER TO |
|--------------------------|-----|---------|---------|--|----------|
| R77 (4Dh)<br>Jack Detect | 15  | JDL_ENA | 0       | Jack Detect Enable for inputs connected to IN2L<br>0 = disabled<br>1 = enabled |          |
|                          | 14  | JDR_ENA | 0       | Jack Detect Enable for input connected to IN2R<br>0 = disabled<br>1 = enabled  |          |

Register 4Dh Jack Detect



| REGISTER ADDRESS              | BIT | LABEL            | DEFAULT | DESCRIPTION   | REFER TO |
|-------------------------------|-----|------------------|---------|---|----------|
| R78 (4Eh)<br>Anti Pop Control | 9:8 | ANTI_POP[1:0]    | 00      | Reduces pop when VMID is enabled by setting the speed of the S-ramp for VMID.<br>00 = no S-ramp (will pop)<br>01 = Fastest S-curve<br>10 = Medium S-curve<br>11 = Slowest S-curve |          |
|                               | 7:6 | DIS_OP_LN4[1:0]  | 00      | Sets the Discharge rate for OUT4<br>00 = discharge path OFF<br>01 = fastest discharge<br>10 = medium discharge<br>11 = slowest discharge  |          |
|                               | 5:4 | DIS_OP_LN3[1:0]  | 00      | Sets the Discharge rate for OUT3<br>00 = discharge path OFF<br>01 = fastest discharge<br>10 = medium discharge<br>11 = slowest discharge  |          |
|                               | 3:2 | DIS_OP_OUT2[1:0] | 00      | Sets the discharge rate for OUT2L and OUT2R<br>00 = discharge path OFF<br>01 = fastest discharge<br>10 = medium discharge<br>11 = slowest discharge                               |          |
|                               | 1:0 | DIS_OP_OUT1[1:0] | 00      | Sets the discharge rate for OUT1L and OUT1R<br>00 = discharge path OFF<br>01 = fastest discharge<br>10 = medium discharge<br>11 = slowest discharge                               |          |

Register 4Eh Anti Pop Control

| REGISTER ADDRESS               | BIT | LABEL        | DEFAULT | DESCRIPTION  | REFER TO |
|--------------------------------|-----|--------------|---------|--|----------|
| R80 (50h)<br>Left Input Volume | 15  | INL_ENA      | 0       | Left input PGA enable<br>0 = disabled<br>1 = enabled   |          |
|                                | 14  | INL_MUTE     | 0       | Mute control for left channel input PGA:<br>0 = Input PGA not muted, normal operation<br>1 = Input PGA muted (and disconnected from the following input record mixer). |          |
|                                | 13  | INL_ZC       | 0       | Left channel input PGA zero cross enable:<br>0 = Update gain when gain register changes<br>1 = Update gain on 1st zero cross after gain register write.                |          |
|                                | 8   | IN_VU        | 0       | Input left PGA and input right PGA volume do not update until a 1 is written to either IN_VU register bit.   |          |
|                                | 7:2 | INL_VOL[5:0] | 01_0000 | Left channel input PGA volume<br>000000 = -12dB<br>000001 = -11.25dB<br>.<br>010000 = 0dB<br>.<br>111111 = 35.25dB   |          |

Register 50h Left Input Volume

| REGISTER ADDRESS                | BIT | LABEL        | DEFAULT | DESCRIPTION   | REFER TO |
|---------------------------------|-----|--------------|---------|---|----------|
| R81 (51h)<br>Right Input Volume | 15  | INR_ENA      | 0       | Right input PGA enable<br>0 = disabled<br>1 = enabled   |          |
|                                 | 14  | INR_MUTE     | 0       | Mute control for right channel input PGA:<br>0 = Input PGA not muted, normal operation<br>1 = Input PGA muted (and disconnected from the following input record mixer). |          |
|                                 | 13  | INR_ZC       | 0       | Right channel input PGA zero cross enable:<br>0 = Update gain when gain register changes<br>1 = Update gain on 1st zero cross after gain register write.                |          |
|                                 | 8   | IN_VU        | 0       | Input left PGA and input right PGA volume do not update until a 1 is written to either IN_VU register bit.  |          |
|                                 | 7:2 | INR_VOL[5:0] | 01_0000 | Right channel input PGA volume<br>000000 = -12dB<br>000001 = -11.25dB<br>.<br>010000 = 0dB<br>.<br>111111 = 35.25dB   |          |

Register 51h Right Input Volume

| REGISTER ADDRESS                | BIT | LABEL           | DEFAULT | DESCRIPTION   | REFER TO |
|---------------------------------|-----|-----------------|---------|---|----------|
| R88 (58h)<br>Left Mixer Control | 15  | MIXOUTL_ENA     | 0       | Left output mixer enable.<br>0 = disabled<br>1 = enabled                        |          |
|                                 | 12  | DACR_TO_MIXOUTL | 0       | Right DAC output to left output mixer<br>0 = not selected<br>1 = selected       |          |
|                                 | 11  | DACL_TO_MIXOUTL | 1       | Left DAC output to left output mixer<br>0 = not selected<br>1 = selected        |          |
|                                 | 2   | IN3L_TO_MIXOUTL | 0       | IN3L amplifier output to left output mixer:<br>0 = not selected<br>1 = selected |          |
|                                 | 1   | INR_TO_MIXOUTL  | 0       | Right input PGA output to left output mixer<br>0 = not selected<br>1 = selected |          |
|                                 | 0   | INL_TO_MIXOUTL  | 0       | Left input PGA output to left output mixer<br>0 = not selected<br>1 = selected  |          |

Register 58h Left Mixer Control

| REGISTER ADDRESS                 | BIT | LABEL           | DEFAULT | DESCRIPTION  | REFER TO |
|----------------------------------|-----|-----------------|---------|--|----------|
| R89 (59h)<br>Right Mixer Control | 15  | MIXOUTR_ENA     | 0       | Right output mixer enable.<br>0 = disabled<br>1 = enabled                        |          |
|                                  | 12  | DACR_TO_MIXOUTR | 1       | Right DAC output to right output mixer<br>0 = not selected<br>1 = selected       |          |
|                                  | 11  | DACL_TO_MIXOUTR | 0       | Left DAC output to right output mixer<br>0 = not selected<br>1 = selected        |          |
|                                  | 3   | IN3R_TO_MIXOUTR | 0       | IN3R amplifier output to right output mixer:<br>0 = not selected<br>1 = selected |          |
|                                  | 1   | INR_TO_MIXOUTR  | 0       | Right input PGA output to right output mixer<br>0 = not selected<br>1 = selected |          |
|                                  | 0   | INL_TO_MIXOUTR  | 0       | Left input PGA output to right output mixer<br>0 = not selected<br>1 = selected  |          |

Register 59h Right Mixer Control

| REGISTER ADDRESS                | BIT | LABEL           | DEFAULT | DESCRIPTION  | REFER TO |
|---------------------------------|-----|-----------------|---------|--|----------|
| R92 (5Ch)<br>OUT3 Mixer Control | 15  | OUT3_ENA        | 0       | OUT3 enable<br>0 = disabled<br>1 = enabled               |          |
|                                 | 11  | DACL_TO_OUT3    | 0       | Left DAC output to OUT3<br>0 = disabled<br>1 = enabled   |          |
|                                 | 8   | MIXINL_TO_OUT3  | 0       | Left input mixer to OUT3<br>0 = disabled<br>1 = enabled  |          |
|                                 | 3   | OUT4_TO_OUT3    | 0       | OUT4 mixer to OUT3<br>0 = disabled<br>1 = enabled        |          |
|                                 | 0   | MIXOUTL_TO_OUT3 | 0       | Left output mixer to OUT3<br>0 = disabled<br>1 = enabled |          |

Register 5Ch OUT3 Mixer Control

| REGISTER ADDRESS                | BIT | LABEL           | DEFAULT | DESCRIPTION  | REFER TO |
|---------------------------------|-----|-----------------|---------|--|----------|
| R93 (5Dh)<br>OUT4 Mixer Control | 15  | OUT4_ENA        | 0       | Enable OUT4 mixer<br>0 = disabled<br>1 = enabled                                     |          |
|                                 | 12  | DACR_TO_OUT4    | 0       | Right DAC output to OUT4<br>0 = disabled<br>1 = enabled                              |          |
|                                 | 11  | DACL_TO_OUT4    | 0       | Left DAC output to OUT4<br>0 = Disabled<br>1 = Enabled                               |          |
|                                 | 10  | OUT4_ATTEN      | 0       | Reduce OUT4 output by 6dB<br>0 = Output at normal level<br>1 = Output reduced by 6dB |          |
|                                 | 9   | MIXINR_TO_OUT4  | 0       | Right input mixer to OUT4<br>0 = disabled<br>1 = enabled                             |          |
|                                 | 2   | OUT3_TO_OUT4    | 0       | OUT3 mixer to OUT4<br>This function is not supported                                 |          |
|                                 | 1   | MIXOUTR_TO_OUT4 | 0       | Right output mixer to OUT4<br>0 = disabled<br>1 = enabled                            |          |
|                                 | 0   | MIXOUTL_TO_OUT4 | 0       | Left output mixer to OUT4<br>0 = disabled<br>1 = enabled                             |          |

Register 5Dh OUT4 Mixer Control

| REGISTER ADDRESS                      | BIT  | LABEL                 | DEFAULT | DESCRIPTION   | REFER TO |
|---------------------------------------|------|-----------------------|---------|---|----------|
| R96 (60h)<br>Output Left Mixer Volume | 11:9 | IN3L_MIXOUTL_VOL[2:0] | 000     | IN3L amplifier volume control to left output mixer<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer   |          |
|                                       | 7:5  | INR_MIXOUTL_VOL[2:0]  | 000     | Right input PGA volume control to left output mixer.<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer |          |
|                                       | 3:1  | INL_MIXOUTL_VOL[2:0]  | 000     | Left input PGA volume control to left output mixer.<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer  |          |

Register 60h Output Left Mixer Volume

| REGISTER ADDRESS                       | BIT   | LABEL                 | DEFAULT | DESCRIPTION  | REFER TO |
|--|-------|-----------------------|---------|--|----------|
| R97 (61h)<br>Output Right Mixer Volume | 15:13 | IN3R_MIXOUTR_VOL[2:0] | 000     | IN3R amplifier volume control to right output mixer.<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer  |          |
|  | 7:5   | INR_MIXOUTR_VOL[2:0]  | 000     | Right input PGA volume control to right output mixer.<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer |          |
|  | 3:1   | INL_MIXOUTR_VOL[2:0]  | 000     | Left input PGA volume control to right output mixer.<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer  |          |

Register 61h Output Right Mixer Volume

| REGISTER ADDRESS                  | BIT  | LABEL                | DEFAULT | DESCRIPTION  | REFER TO |
|-----------------------------------|------|----------------------|---------|--|----------|
| R98 (62h)<br>Input Mixer Volume L | 11:9 | IN3L_MIXINL_VOL[2:0] | 000     | IN3L amplifier volume control to right input mixer.<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer |          |
|                                   | 3:1  | IN2L_MIXINL_VOL[2:0] | 000     | IN2L amplifier volume control to right input mixer.<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer |          |
|                                   | 0    | INL_MIXINL_VOL       | 0       | Boost enable for left channel input PGA:<br>0 = PGA output has +0dB gain through input record mixer.<br>1 = PGA output has +20dB gain through input record mixer.                                    |          |

Register 62h Input Mixer Volume L

| REGISTER ADDRESS                     | BIT   | LABEL                | DEFAULT | DESCRIPTION  | REFER TO |
|--------------------------------------|-------|----------------------|---------|--|----------|
| R99 (63h)<br>Input Mixer<br>Volume R | 15:13 | IN3R_MIXINR_VOL[2:0] | 000     | IN3R amplifier volume control to right input mixer.<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer |          |
|                                      | 7:5   | IN2R_MIXINR_VOL[2:0] | 000     | IN2R amplifier volume control to right input mixer.<br>000 = Path disabled (disconnected)<br>001 = -12dB gain through mixer<br>010 = -9dB gain through mixer<br>...<br>111 = +6dB gain through mixer |          |
|                                      | 0     | INR_MIXINR_VOL       | 0       | Boost enable for right channel input PGA:<br>0 = PGA output has +0dB gain through input record mixer.<br>1 = PGA output has +20dB gain through input record mixer.                                   |          |

Register 63h Input Mixer Volume R

| REGISTER ADDRESS                    | BIT | LABEL               | DEFAULT | DESCRIPTION   | REFER TO |
|-------------------------------------|-----|---------------------|---------|---|----------|
| R100 (64h)<br>Input Mixer<br>Volume | 15  | OUT4_MIXIN_DST      | 0       | Select routing of OUT4 to input mixers.<br>0 = OUT4 to left input mixer.<br>1 = OUT4 to right input mixer.  |          |
|                                     | 3:1 | OUT4_MIXIN_VOL[2:0] | 000     | Controls the gain of OUT4 to left and right input mixers:<br>000 = Path disabled (left and right mute)<br>001 = -12dB gain through boost stages<br>010 = -9dB gain through boost stages<br>....<br>111 = +6dB gain through boost stages |          |

Register 64h Input Mixer Volume

| REGISTER ADDRESS              | BIT | LABEL          | DEFAULT | DESCRIPTION   | REFER TO |
|-------------------------------|-----|----------------|---------|---|----------|
| R104 (68h)<br>OUT1L<br>Volume | 15  | OUT1L_ENA      | 0       | OUT1L enable<br>0 = disabled<br>1 = enabled   |          |
|                               | 14  | OUT1L_MUTE     | 0       | OUT1L mute:<br>0 = normal operation<br>1 = mute   |          |
|                               | 13  | OUT1L_ZC       | 0       | OUT1L volume zero cross enable<br>0 = Change gain immediately<br>1 = Change gain on zero cross only |          |
|                               | 8   | OUT1_VU        | 0       | OUT1L and OUT1R volumes do not update until a 1 is written to either OUT1_VU.                       |          |
|                               | 7:2 | OUT1L_VOL[5:0] | 11_1001 | OUT1L volume:<br>000000 = -57dB<br>...<br>111001 = 0dB<br>...<br>111111 = +6dB                      |          |

Register 68h OUT1L Volume

| REGISTER ADDRESS              | BIT | LABEL          | DEFAULT | DESCRIPTION   | REFER TO |
|-------------------------------|-----|----------------|---------|---|----------|
| R105 (69h)<br>OUT1R<br>Volume | 15  | OUT1R_ENA      | 0       | OUT1R enable<br>0 = disabled<br>1 = enabled   |          |
|                               | 14  | OUT1R_MUTE     | 0       | OUT1R mute:<br>0 = normal operation<br>1 = mute   |          |
|                               | 13  | OUT1R_ZC       | 0       | OUT1R volume zero cross enable<br>0 = Change gain immediately<br>1 = Change gain on zero cross only |          |
|                               | 8   | OUT1_VU        | 0       | OUT1L and OUT1R volumes do not update until a 1 is written to either OUT1_VU register bits.         |          |
|                               | 7:2 | OUT1R_VOL[5:0] | 11_1001 | OUT1R volume:<br>000000 = -57dB<br>...<br>111001 = 0dB<br>...<br>111111 = +6dB                      |          |

Register 69h OUT1R Volume

| REGISTER ADDRESS              | BIT | LABEL          | DEFAULT | DESCRIPTION   | REFER TO |
|-------------------------------|-----|----------------|---------|---|----------|
| R106 (6Ah)<br>OUT2L<br>Volume | 15  | OUT2L_ENA      | 0       | OUT2L enable<br>0 = disabled<br>1 = enabled   |          |
|                               | 14  | OUT2L_MUTE     | 0       | OUT2L mute:<br>0 = normal operation<br>1 = mute   |          |
|                               | 13  | OUT2L_ZC       | 0       | OUT2L volume zero cross enable<br>0 = Change gain immediately<br>1 = Change gain on zero cross only |          |
|                               | 8   | OUT2_VU        | 0       | OUT2L and OUT2R volumes do not update until a 1 is written to either OUT2_VU register bits.         |          |
|                               | 7:2 | OUT2L_VOL[5:0] | 11_1001 | OUT2L volume:<br>000000 = -57dB<br>...<br>111001 = 0dB<br>...<br>111111 = +6dB                      |          |

Register 6Ah OUT2L Volume

| REGISTER ADDRESS              | BIT | LABEL          | DEFAULT | DESCRIPTION  | REFER TO |
|-------------------------------|-----|----------------|---------|--|----------|
| R107 (6Bh)<br>OUT2R<br>Volume | 15  | OUT2R_ENA      | 0       | OUT2R enable<br>0 = disabled<br>1 = enabled  |          |
|                               | 14  | OUT2R_MUTE     | 0       | OUT2R mute:<br>0 = normal operation<br>1 = mute  |          |
|                               | 13  | OUT2R_ZC       | 0       | OUT2R volume zero cross enable<br>0 = Change gain immediately<br>1 = Change gain on zero cross only  |          |
|                               | 10  | OUT2R_INV      | 0       | Enable OUT2R inverting amplifier<br>0 = disabled<br>1 = enabled<br><br>This register must be set to 0 when using the non-inverting MIXOUT2R to OUT2R path.<br>This register must be set to 1 when using the inverting MIXOUT2R to OUT2R path.  |          |
|                               | 9   | OUT2R_INV_MUTE | 1       | Mute output of PGA to inverting amplifier.<br>0 = PGA output goes to inverting amplifier<br>1 = PGA output goes to output driver<br><br>This register must be set to 0 when using the inverting MIXOUT2R to OUT2R path.<br>This register must be set to 1 when using the non-inverting MIXOUT2R to OUT2R path. |          |
|                               | 8   | OUT2_VU        | 0       | OUT2L and OUT2R volumes do not update until a 1 is written to either OUT2_VU register bits.  |          |
|                               | 7:2 | OUT2R_VOL[5:0] | 11_1001 | OUT2R volume:<br>000000 = -57dB<br>...<br>111001 = 0dB<br>...<br>111111 = +6dB   |          |

Register 6Bh OUT2R Volume



| REGISTER ADDRESS             | BIT | LABEL               | DEFAULT | DESCRIPTION  | REFER TO |
|------------------------------|-----|---------------------|---------|--|----------|
| R111 (6Fh)<br>BEEP<br>Volume | 15  | IN3R_TO_OUT2R       | 0       | Beep mixer enable<br>0 = disabled<br>1 = enabled                     |          |
|                              | 7:5 | IN3R_OUT2R_VOL[2:0] | 000     | Beep mixer volume:<br>000 = -15dB<br>... in +3dB steps<br>111 = +6dB |          |

Register 6Fh BEEP Volume

| REGISTER ADDRESS            | BIT   | LABEL         | DEFAULT | DESCRIPTION  | REFER TO |
|-----------------------------|-------|---------------|---------|--|----------|
| R112 (70h)<br>AI Formatting | 15    | AIF_BCLK_INV  | 0       | 0 = normal<br>1 = inverted   |          |
|                             | 13    | AIF_TRI       | 0       | Sets Output enables for LRCLK and BCLK and ADCDAT to inactive state<br>0 = normal<br>1 = forces pins to Hi-Z   |          |
|                             | 12    | AIF_LRCLK_INV | 0       | LRCLK clock polarity<br>0 = normal<br>1 = inverted<br><br>DSP Mode – mode A/B select<br>0 = MSB is available on 2nd BCLK rising edge after LRCLK rising edge (mode A)<br>1 = MSB is available on 1st BCLK rising edge after LRCLK rising edge (mode B) |          |
|                             | 11:10 | AIF_WL[1:0]   | 10      | Data word length<br>11 = 32 bits<br>10 = 24 bits<br>01 = 20 bits<br>00 = 16 bits<br>Note: When using the Right-Justified data format (FMT=00), the maximum word length is 24 bits.   |          |
|                             | 9:8   | AIF_FMT[1:0]  | 10      | 00 = Right-justified<br>01 = Left justified<br>10 = I2S<br>11 = DSP / PCM mode   |          |

Register 70h AI Formatting

| REGISTER ADDRESS              | BIT | LABEL        | DEFAULT | DESCRIPTION  | REFER TO |
|-------------------------------|-----|--------------|---------|--|----------|
| R113 (71h)<br>ADC DAC<br>COMP | 7   | DAC_COMP     | 0       | DAC Companding enable<br>0 = disabled<br>1 = enabled   |          |
|                               | 6   | DAC_COMPMODE | 0       | DAC Companding mode select:<br>0 = $\mu$ -law<br>1 = A-law<br>(Note: Setting DAC_COMPMODE=1 selects 8-bit mode when DAC_COMP=0 and ADC_COMP=0) |          |
|                               | 5   | ADC_COMP     | 0       | ADC Companding enable<br>0 = disabled<br>1 = enabled   |          |
|                               | 4   | ADC_COMPMODE | 0       | ADC Companding mode select:<br>0 = $\mu$ -law<br>1 = A-law<br>(Note: Setting ADC_COMPMODE=1 selects 8-bit mode when DAC_COMP=0 and ADC_COMP=0) |          |
|                               | 0   | LOOPBACK     | 0       | Digital Loopback Function<br>0 = No loopback.<br>1 = Loopback enabled, ADC data output is fed directly into DAC data input.                    |          |

Register 71h ADC DAC COMP

| REGISTER ADDRESS                | BIT | LABEL           | DEFAULT | DESCRIPTION   | REFER TO |
|---------------------------------|-----|-----------------|---------|---|----------|
| R114 (72h)<br>AI ADC<br>Control | 7   | AIFADC_PD       | 0       | Enables a pull down on ADC data pin<br>0 = disabled<br>1 = enabled                                  |          |
|                                 | 6   | AIFADCL_SRC     | 0       | Selects Left channel ADC output.<br>0 = ADC Left channel<br>1 = ADC Right channel                   |          |
|                                 | 5   | AIFADCR_SRC     | 1       | Selects Right channel ADC output.<br>0 = ADC Left channel<br>1 = ADC Right channel                  |          |
|                                 | 4   | AIFADC_TDM_CHAN | 0       | ADCDAT TDM Channel Select<br>0 = ADCDAT outputs data on slot 0<br>1 = ADCDAT outputs data on slot 1 |          |
|                                 | 3   | AIFADC_TDM      | 0       | ADC TDM Enable<br>0 = Normal ADCDAT operation<br>1 = TDM enabled on ADCDAT                          |          |

Register 72h AI ADC Control

| REGISTER ADDRESS             | BIT | LABEL           | DEFAULT | DESCRIPTION   | REFER TO |
|------------------------------|-----|-----------------|---------|---|----------|
| R115 (73h)<br>AI DAC Control | 14  | BCLK_MSTR       | 0       | Enables the Audio Interface BCLK generation and enables the BCLK pin for Master mode<br>0 = BCLK Slave mode<br>1 = BCLK Master mode |          |
|                              | 7   | AIFDAC_PD       | 0       | Enables a pull down on DAC data pin<br>0 = disabled<br>1 = enabled  |          |
|                              | 6   | DACL_SRC        | 0       | Selects Left channel DAC input.<br>0 = DAC Left channel<br>1 = DAC Right channel  |          |
|                              | 5   | DACR_SRC        | 1       | Selects Right channel DAC input.<br>0 = DAC Left channel<br>1 = DAC Right channel   |          |
|                              | 4   | AIFDAC_TDM_CHAN | 0       | DACDAT TDM Channel Select<br>0 = DACDAT outputs data on slot 0<br>1 = DACDAT outputs data on slot 1                                 |          |
|                              | 3   | AIFDAC_TDM      | 0       | DAC TDM Enable<br>0 = Normal DACDAT operation<br>1 = TDM enabled on DACDAT  |          |
|                              | 1:0 | DAC_BOOST[1:0]  | 00      | Provides a limited set of gains to be applied to the signal<br>00 = 0dB<br>01 = +6dB<br>10 = +12dB<br>11 = Reserved (+18dB)         |          |

Register 73h AI DAC Control

| REGISTER ADDRESS            | BIT | LABEL   | DEFAULT | DESCRIPTION   | REFER TO |
|-----------------------------|-----|---------|---------|---|----------|
| R128 (80h)<br>GPIO Debounce | 12  | GP12_DB | 1       | GPIO12 debounce<br>0 = GPIO is not debounced.<br>1 = GPIO is debounced (time from GP_DBTIME[1:0])<br><i>Reset by state machine.</i> |          |
|                             | 11  | GP11_DB | 1       | GPIO11 debounce<br>0 = GPIO is not debounced.<br>1 = GPIO is debounced (time from GP_DBTIME[1:0])<br><i>Reset by state machine.</i> |          |
|                             | 10  | GP10_DB | 1       | GPIO10 debounce<br>0 = GPIO is not debounced.<br>1 = GPIO is debounced (time from GP_DBTIME[1:0])<br><i>Reset by state machine.</i> |          |
|                             | 9   | GP9_DB  | 1       | GPIO9 debounce<br>0 = GPIO is not debounced.<br>1 = GPIO is debounced (time from GP_DBTIME[1:0])<br><i>Reset by state machine.</i>  |          |
|                             | 8   | GP8_DB  | 1       | GPIO8 debounce<br>0 = GPIO is not debounced.<br>1 = GPIO is debounced (time from GP_DBTIME[1:0])<br><i>Reset by state machine.</i>  |          |
|                             | 7   | GP7_DB  | 1       | GPIO7 debounce<br>0 = GPIO is not debounced.<br>1 = GPIO is debounced (time from GP_DBTIME[1:0])<br><i>Reset by state machine.</i>  |          |

| REGISTER ADDRESS | BIT | LABEL  | DEFAULT | DESCRIPTION  | REFER TO |
|------------------|-----|--------|---------|--|----------|
|                  | 6   | GP6_DB | 1       | GPIO6 debounce<br>0 = GPIO is not debounced.<br>1 = GPIO is debounced (time from GP_DBTIME[1:0])<br><i>Reset by state machine.</i> |          |
|                  | 5   | GP5_DB | 1       | GPIO5 debounce<br>0 = GPIO is not debounced.<br>1 = GPIO is debounced (time from GP_DBTIME[1:0])<br><i>Reset by state machine.</i> |          |
|                  | 4   | GP4_DB | 1       | GPIO4 debounce<br>0 = GPIO is not debounced.<br>1 = GPIO is debounced (time from GP_DBTIME[1:0])<br><i>Reset by state machine.</i> |          |
|                  | 3   | GP3_DB | 1       | GPIO3 debounce<br>0 = GPIO is not debounced.<br>1 = GPIO is debounced (time from GP_DBTIME[1:0])<br><i>Reset by state machine.</i> |          |
|                  | 2   | GP2_DB | 1       | GPIO2 debounce<br>0 = GPIO is not debounced.<br>1 = GPIO is debounced (time from GP_DBTIME[1:0])<br><i>Reset by state machine.</i> |          |
|                  | 1   | GP1_DB | 1       | GPIO1 debounce<br>0 = GPIO is not debounced.<br>1 = GPIO is debounced (time from GP_DBTIME[1:0])<br><i>Reset by state machine.</i> |          |
|                  | 0   | GP0_DB | 1       | GPIO0 debounce<br>0 = GPIO is not debounced.<br>1 = GPIO is debounced (time from GP_DBTIME[1:0])<br><i>Reset by state machine.</i> |          |

Register 80h GPIO Debounce

| REGISTER ADDRESS                             | BIT | LABEL   | DEFAULT | DESCRIPTION  | REFER TO |
|--|-----|---------|---------|--|----------|
| R129 (81h)<br>GPIO Pin<br>pull up<br>Control | 12  | GP12_PU | 0       | GPIO12 pull-up<br>0 = Normal<br>1 = Pull-up enabled<br>(Only valid when GPIO12 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|  |     |         | 0       |  |          |
|  |     |         | 0       |  |          |
|  |     |         | 0       |  |          |
|  | 11  | GP11_PU | 0       | GPIO11 pull-up<br>0 = Normal<br>1 = Pull-up enabled<br>(Only valid when GPIO11 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|  |     |         | 0       |  |          |
|  |     |         | 0       |  |          |
|  |     |         | 0       |  |          |
|  | 10  | GP10_PU | 0       | GPIO10 pull-up<br>0 = Normal<br>1 = Pull-up enabled<br>(Only valid when GPIO10 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|  |     |         | 0       |  |          |
|  |     |         | 0       |  |          |
|  |     |         | 0       |  |          |
|  | 9   | GP9_PU  | 0       | GPIO9 pull-up<br>0 = Normal<br>1 = Pull-up enabled<br>(Only valid when GPIO9 is set to input. Do not select  |          |
|  |     |         | 0       |  |          |
|  |     |         | 0       |  |          |
|  |     |         | 0       |  |          |

| REGISTER ADDRESS | BIT | LABEL  | DEFAULT          | DESCRIPTION  | REFER TO |
|------------------|-----|--------|------------------|--|----------|
|                  |     |        | 0                | pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                  | 8   | GP8_PU | 0<br>0<br>0<br>0 | GPIO8 pull-up<br>0 = Normal<br>1 = Pull-up enabled<br>(Only valid when GPIO8 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 7   | GP7_PU | 0<br>0<br>0<br>0 | GPIO7 pull-up<br>0 = Normal<br>1 = Pull-up enabled<br>(Only valid when GPIO7 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 6   | GP6_PU | 0<br>0<br>0<br>0 | GPIO6 pull-up<br>0 = Normal<br>1 = Pull-up enabled<br>(Only valid when GPIO6 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 5   | GP5_PU | 0<br>0<br>0<br>0 | GPIO5 pull-up<br>0 = Normal<br>1 = Pull-up enabled<br>(Only valid when GPIO5 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 4   | GP4_PU | 0<br>0<br>0<br>1 | GPIO4 pull-up<br>0 = Normal<br>1 = Pull-up enabled<br>(Only valid when GPIO4 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 3   | GP3_PU | 0<br>0<br>0<br>0 | GPIO3 pull-up<br>0 = Normal<br>1 = Pull-up enabled<br>(Only valid when GPIO3 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 2   | GP2_PU | 0<br>0<br>0<br>0 | GPIO2 pull-up<br>0 = Normal<br>1 = Pull-up enabled<br>(Only valid when GPIO2 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 1   | GP1_PU | 0<br>0<br>0<br>0 | GPIO1 pull-up<br>0 = Normal<br>1 = Pull-up enabled<br>(Only valid when GPIO1 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 0   | GP0_PU | 0<br>0<br>0<br>0 | GPIO0 pull-up<br>0 = Normal<br>1 = Pull-up enabled<br>(Only valid when GPIO0 is set to input. Do not select pull-up and pull-down at the same time.)   |          |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION  | REFER TO |
|------------------|-----|-------|---------|--|----------|
|                  |     |       |         | <i>Reset by state machine. Default held in metal mask.</i> |          |

**Register 81h** GPIO Pin pull up Control

| REGISTER ADDRESS                        | BIT | LABEL   | DEFAULT          | DESCRIPTION  | REFER TO |
|---|-----|---------|------------------|--|----------|
| R130 (82h)<br>GPIO Pull<br>down Control | 12  | GP12_PD | 0<br>0<br>0<br>0 | GPIO12 pull-down<br>0 = Normal<br>1 = Pull-down enabled<br>(Only valid when GPIO12 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|   | 11  | GP11_PD | 0<br>0<br>0<br>0 | GPIO11 pull-down<br>0 = Normal<br>1 = Pull-down enabled<br>(Only valid when GPIO11 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|   | 10  | GP10_PD | 0<br>0<br>0<br>0 | GPIO10 pull-down<br>0 = Normal<br>1 = Pull-down enabled<br>(Only valid when GPIO10 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|   | 9   | GP9_PD  | 0<br>0<br>0<br>0 | GPIO9 pull-down<br>0 = Normal<br>1 = Pull-down enabled<br>(Only valid when GPIO9 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|   | 8   | GP8_PD  | 0<br>0<br>1<br>0 | GPIO8 pull-down<br>0 = Normal<br>1 = Pull-down enabled<br>(Only valid when GPIO8 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|   | 7   | GP7_PD  | 0<br>0<br>0<br>0 | GPIO7 pull-down<br>0 = Normal<br>1 = Pull-down enabled<br>(Only valid when GPIO7 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|   | 6   | GP6_PD  | 0<br>0<br>0<br>0 | GPIO6 pull-down<br>0 = Normal<br>1 = Pull-down enabled<br>(Only valid when GPIO6 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|   | 5   | GP5_PD  | 0<br>0<br>0<br>0 | GPIO5 pull-down<br>0 = Normal<br>1 = Pull-down enabled<br>(Only valid when GPIO5 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i>   |          |

| REGISTER ADDRESS | BIT | LABEL  | DEFAULT          | DESCRIPTION  | REFER TO |
|------------------|-----|--------|------------------|--|----------|
|                  | 4   | GP4_PD | 0<br>0<br>1<br>0 | GPIO4 pull-down<br>0 = Normal<br>1 = Pull-down enabled<br>(Only valid when GPIO4 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 3   | GP3_PD | 0<br>0<br>0<br>0 | GPIO3 pull-down<br>0 = Normal<br>1 = Pull-down enabled<br>(Only valid when GPIO3 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 2   | GP2_PD | 0<br>0<br>0<br>0 | GPIO2 pull-down<br>0 = Normal<br>1 = Pull-down enabled<br>(Only valid when GPIO2 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 1   | GP1_PD | 0<br>0<br>0<br>0 | GPIO1 pull-down<br>0 = Normal<br>1 = Pull-down enabled<br>(Only valid when GPIO1 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 0   | GP0_PD | 0<br>0<br>0<br>0 | GPIO0 pull-down<br>0 = Normal<br>1 = Pull-down enabled<br>(Only valid when GPIO0 is set to input. Do not select pull-up and pull-down at the same time.)<br><i>Reset by state machine. Default held in metal mask.</i> |          |

Register 82h GPIO Pull down Control

| REGISTER ADDRESS                        | BIT | LABEL        | DEFAULT | DESCRIPTION  | REFER TO |
|---|-----|--------------|---------|--|----------|
| R131 (83h)<br>GPIO<br>Interrupt<br>Mode | 12  | GP12_INTMODE | 0       | GPIO12 Pin Mode<br>0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP12_CFG register bit.<br>1 = GPIO interrupt is both rising and falling edge triggered.<br><i>Reset by state machine.</i> |          |
|   | 11  | GP11_INTMODE | 0       | GPIO11 Pin Mode<br>0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP11_CFG register bit.<br>1 = GPIO interrupt is both rising and falling edge triggered.<br><i>Reset by state machine.</i> |          |
|   | 10  | GP10_INTMODE | 0       | GPIO10 Pin Mode<br>0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP10_CFG register bit.<br>1 = GPIO interrupt is both rising and falling edge triggered.<br><i>Reset by state machine.</i> |          |

| REGISTER ADDRESS | BIT | LABEL       | DEFAULT | DESCRIPTION  | REFER TO |
|------------------|-----|-------------|---------|--|----------|
|                  | 9   | GP9_INTMODE | 0       | GPIO9 Pin Mode<br>0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP9_CFG register bit.<br>1 = GPIO interrupt is both rising and falling edge triggered.<br><i>Reset by state machine.</i> |          |
|                  | 8   | GP8_INTMODE | 0       | GPIO8 Pin Mode<br>0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP8_CFG register bit.<br>1 = GPIO interrupt is both rising and falling edge triggered.<br><i>Reset by state machine.</i> |          |
|                  | 7   | GP7_INTMODE | 0       | GPIO7 Pin Mode<br>0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP7_CFG register bit.<br>1 = GPIO interrupt is both rising and falling edge triggered.<br><i>Reset by state machine.</i> |          |
|                  | 6   | GP6_INTMODE | 0       | GPIO6 Pin Mode<br>0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP6_CFG register bit.<br>1 = GPIO interrupt is both rising and falling edge triggered.<br><i>Reset by state machine.</i> |          |
|                  | 5   | GP5_INTMODE | 0       | GPIO5 Pin Mode<br>0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP5_CFG register bit.<br>1 = GPIO interrupt is both rising and falling edge triggered.<br><i>Reset by state machine.</i> |          |
|                  | 4   | GP4_INTMODE | 0       | GPIO4 Pin Mode<br>0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP4_CFG register bit.<br>1 = GPIO interrupt is both rising and falling edge triggered.<br><i>Reset by state machine.</i> |          |
|                  | 3   | GP3_INTMODE | 0       | GPIO3 Pin Mode<br>0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP3_CFG register bit.<br>1 = GPIO interrupt is both rising and falling edge triggered.<br><i>Reset by state machine.</i> |          |
|                  | 2   | GP2_INTMODE | 0       | GPIO2 Pin Mode<br>0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP2_CFG register bit.<br>1 = GPIO interrupt is both rising and falling edge triggered.<br><i>Reset by state machine.</i> |          |
|                  | 1   | GP1_INTMODE | 0       | GPIO1 Pin Mode<br>0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP1_CFG register bit.<br>1 = GPIO interrupt is both rising and falling edge triggered.<br><i>Reset by state machine.</i> |          |



| REGISTER ADDRESS | BIT | LABEL       | DEFAULT | DESCRIPTION  | REFER TO |
|------------------|-----|-------------|---------|--|----------|
|                  | 0   | GP0_INTMODE | 0       | GPIO0 Pin Mode<br>0 = GPIO interrupt is rising edge triggered, and is taken after the effect of the GP0_CFG register bit.<br>1 = GPIO interrupt is both rising and falling edge triggered.<br><i>Reset by state machine.</i> |          |

Register 83h GPIO Interrupt Mode

| REGISTER ADDRESS           | BIT | LABEL          | DEFAULT | DESCRIPTION   | REFER TO |
|----------------------------|-----|----------------|---------|---|----------|
| R133 (85h)<br>GPIO Control | 7:6 | GP_DBTIME[1:0] | 00      | Debounce time for all GPIO inputs<br>00 = 64us<br>01 = 0.5ms<br>10 = 1ms<br>11 = 4ms<br>Note: PWR_ON, PWR_OFF and /WAKEUP have additional debounce times.<br><i>Reset by state machine.</i> |          |

Register 85h GPIO Control

| REGISTER ADDRESS                       | BIT      | LABEL    | DEFAULT   | DESCRIPTION   | REFER TO |
|--|----------|----------|---|---|----------|
| R134 (86h)<br>GPIO Configuration (i/o) | 12       | GP12_DIR | 0   | GPIO12 pin direction<br>0 = Output<br>1 = Input<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|  |          |          | 0   |   |          |
|  |          |          | 0   |   |          |
|  |          |          | 0   |   |          |
|  | 11       | GP11_DIR | 1   | GPIO11 pin direction<br>0 = Output<br>1 = Input<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|  |          |          | 1   |   |          |
|  |          |          | 1   |   |          |
| 10                                     | GP10_DIR | 1        | GPIO10 pin direction<br>0 = Output<br>1 = Input<br><i>Reset by state machine. Default held in metal mask.</i> |   |          |
|  |          | 0        |   |   |          |
| 9                                      | GP9_DIR  | 1        | GPIO9 pin direction<br>0 = Output<br>1 = Input<br><i>Reset by state machine. Default held in metal mask.</i>  |   |          |
|  |          | 0        |   |   |          |
| 8                                      | GP8_DIR  | 1        | GPIO8 pin direction<br>0 = Output<br>1 = Input<br><i>Reset by state machine. Default held in metal mask.</i>  |   |          |
|  |          | 0        |   |   |          |
| 7                                      | GP7_DIR  | 1        | GPIO7 pin direction<br>0 = Output<br>1 = Input<br><i>Reset by state machine. Default held in metal mask.</i>  |   |          |
|  |          | 1        |   |   |          |
| 6                                      | GP6_DIR  | 1        | GPIO6 pin direction<br>0 = Output<br>1 = Input<br><i>Reset by state machine. Default held in metal mask.</i>  |   |          |
|  |          | 1        |   |   |          |

| REGISTER ADDRESS | BIT | LABEL   | DEFAULT          | DESCRIPTION  | REFER TO |
|------------------|-----|---------|------------------|--|----------|
|                  | 5   | GP5_DIR | 1<br>1<br>1<br>1 | GPIO5 pin direction<br>0 = Output<br>1 = Input<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 4   | GP4_DIR | 1<br>1<br>1<br>1 | GPIO4 pin direction<br>0 = Output<br>1 = Input<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 3   | GP3_DIR | 1<br>1<br>1<br>1 | GPIO3 pin direction<br>0 = Output<br>1 = Input<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 2   | GP2_DIR | 1<br>1<br>0<br>0 | GPIO2 pin direction<br>0 = Output<br>1 = Input<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 1   | GP1_DIR | 0<br>1<br>1<br>1 | GPIO1 pin direction<br>0 = Output<br>1 = Input<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 0   | GP0_DIR | 0<br>1<br>0<br>1 | GPIO0 pin direction<br>0 = Output<br>1 = Input<br><i>Reset by state machine. Default held in metal mask.</i> |          |

Register 86h GPIO Configuration (i/o)

| REGISTER ADDRESS                             | BIT | LABEL    | DEFAULT          | DESCRIPTION   | REFER TO |
|--|-----|----------|------------------|---|----------|
| R135 (87h)<br>GPIO Pin<br>Polarity /<br>Type | 12  | GP12_CFG | 0<br>0<br>0<br>0 | GPIO12 pin polarity/type:<br>Input:<br>0 = Active low<br>1 = Active high<br>Output:<br>0 = CMOS<br>1 = Open drain<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|  | 11  | GP11_CFG | 1<br>1<br>1<br>1 | GPIO11 pin polarity/type:<br>Input:<br>0 = Active low<br>1 = Active high<br>Output:<br>0 = CMOS<br>1 = Open drain<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|  | 10  | GP10_CFG | 1<br>1<br>1<br>1 | GPIO10 pin polarity/type:<br>Input:<br>0 = Active low<br>1 = Active high<br>Output:<br>0 = CMOS<br>1 = Open drain<br><i>Reset by state machine. Default held in metal mask.</i> |          |

| REGISTER ADDRESS | BIT | LABEL   | DEFAULT          | DESCRIPTION  | REFER TO |
|------------------|-----|---------|------------------|--|----------|
|                  | 9   | GP9_CFG | 1<br>0<br>0<br>1 | GPIO9 pin polarity/type:<br>Input:<br>0 = Active low<br>1 = Active high<br>Output:<br>0 = CMOS<br>1 = Open drain<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 8   | GP8_CFG | 1<br>0<br>1<br>1 | GPIO8 pin polarity/type:<br>Input:<br>0 = Active low<br>1 = Active high<br>Output:<br>0 = CMOS<br>1 = Open drain<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 7   | GP7_CFG | 1<br>0<br>1<br>1 | GPIO7 pin polarity/type:<br>Input:<br>0 = Active low<br>1 = Active high<br>Output:<br>0 = CMOS<br>1 = Open drain<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 6   | GP6_CFG | 1<br>0<br>1<br>1 | GPIO6 pin polarity/type:<br>Input:<br>0 = Active low<br>1 = Active high<br>Output:<br>0 = CMOS<br>1 = Open drain<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 5   | GP5_CFG | 1<br>0<br>1<br>1 | GPIO5 pin polarity/type:<br>Input:<br>0 = Active low<br>1 = Active high<br>Output:<br>0 = CMOS<br>1 = Open drain<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 4   | GP4_CFG | 1<br>1<br>1<br>1 | GPIO4 pin polarity/type:<br>Input:<br>0 = Active low<br>1 = Active high<br>Output:<br>0 = CMOS<br>1 = Open drain<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 3   | GP3_CFG | 1<br>1<br>0<br>1 | GPIO3 pin polarity/type:<br>Input:<br>0 = Active low<br>1 = Active high<br>Output:<br>0 = CMOS   |          |

| REGISTER ADDRESS | BIT | LABEL   | DEFAULT          | DESCRIPTION  | REFER TO |
|------------------|-----|---------|------------------|--|----------|
|                  |     |         |                  | 1 = Open drain<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                  | 2   | GP2_CFG | 1<br>1<br>1<br>1 | GPIO2 pin polarity/type:<br>Input:<br>0 = Active low<br>1 = Active high<br>Output:<br>0 = CMOS<br>1 = Open drain<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 1   | GP1_CFG | 0<br>1<br>1<br>0 | GPIO1 pin polarity/type:<br>Input:<br>0 = Active low<br>1 = Active high<br>Output:<br>0 = CMOS<br>1 = Open drain<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 0   | GP0_CFG | 0<br>1<br>0<br>1 | GPIO0 pin polarity/type:<br>Input:<br>0 = Active low<br>1 = Active high<br>Output:<br>0 = CMOS<br>1 = Open drain<br><i>Reset by state machine. Default held in metal mask.</i> |          |

Register 87h GPIO Pin Polarity / Type

| REGISTER ADDRESS                           | BIT   | LABEL       | DEFAULT                      | DESCRIPTION  | REFER TO |
|--|-------|-------------|------------------------------|--|----------|
| R140 (8Ch)<br>GPIO<br>Function<br>Select 1 | 15:12 | GP3_FN[3:0] | 0000<br>0000<br>0001<br>0000 | GPIO3 alternate function:<br>Input:<br>0000 = GPIO<br>0001 = PWR_ON<br>0010 = LDO_ENA<br>0011 = PWR_OFF<br>0100 = FLASH<br>Output:<br>0000 = GPIO<br>0001 = P_CLK<br>0010 = VRTC<br>0011 = 32kHz<br>0100 = /MEMRST<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|  | 11:8  | GP2_FN[3:0] | 0000<br>0000<br>0011<br>0011 | GPIO2 alternate function:<br>Input:<br>0000 = GPIO<br>0001 = PWR_ON<br>0010 = /WAKEUP<br>0011 = 32KHZ<br>0100 = L_PWR3<br>Output:<br>0000 = GPIO   |          |

| REGISTER ADDRESS | BIT | LABEL       | DEFAULT                      | DESCRIPTION   | REFER TO |
|------------------|-----|-------------|------------------------------|---|----------|
|                  |     |             |                              | 0001 = PWR_ON<br>0010 = VRTC<br>0011 = 32KHZ<br>0100 = /RST<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                  | 7:4 | GP1_FN[3:0] | 0001<br>0000<br>0001<br>0001 | GPIO1 alternate function:<br>Input:<br>0000 = GPIO<br>0001 = PWR_ON<br>0010 = /LDO_ENA<br>0011 = L_PWR2<br>0100 = /WAKEUP<br>Output:<br>0000 = GPIO<br>0001 = DO_CONF<br>0010 = /RST<br>0011 = /MEMRST<br>0100 = 32KHz<br><i>Reset by state machine. Default held in metal mask.</i>                  |          |
|                  | 3:0 | GP0_FN[3:0] | 0011<br>0000<br>0000<br>0000 | GPIO0 alternate function:<br>Input-<br>0000 = GPIO<br>0001 = PWR_ON<br>0010 = /LDO_ENA<br>0011 = L_PWR1<br>0100 = PWR_OFF<br>0101 = CHIP_RESET<br>Output:<br>0000 = GPIO<br>0001 = PWR_ON<br>0010 = VRTC<br>0011 = POR_B<br>0100 = /RST<br><i>Reset by state machine. Default held in metal mask.</i> |          |

Register 8Ch GPIO Function Select 1

| REGISTER ADDRESS                           | BIT   | LABEL       | DEFAULT                      | DESCRIPTION  | REFER TO |
|--|-------|-------------|------------------------------|--|----------|
| R141 (8Dh)<br>GPIO<br>Function<br>Select 2 | 15:12 | GP7_FN[3:0] | 0000<br>0001<br>0000<br>0000 | GPIO7 alternate function:<br>Input:<br>0000 = GPIO<br>0001 = L_PWR3<br>0010 = MASK<br>0011 = Hibernate (level)<br>Output:<br>0000 = GPIO<br>0001 = P_CLK (1MHz)<br>0010 = /VCC_FAULT<br>0011 = /BATT_FAULT<br>0100 = MICDET<br>0101 = MICSHT<br>0110 = ADA<br>1100 = FLL_CLK |          |

| REGISTER ADDRESS | BIT  | LABEL       | DEFAULT                      | DESCRIPTION  | REFER TO |
|------------------|------|-------------|------------------------------|--|----------|
|                  |      |             |                              | <i>Reset by state machine. Default held in metal mask.</i>   |          |
|                  | 11:8 | GP6_FN[3:0] | 0000<br>0001<br>0000<br>0000 | GPIO6 alternate function:<br>Input:<br>0000 = GPIO<br>0001 = L_PWR2<br>0010 = FLASH<br>0011 = Hibernate (Edge)<br>0100 = Hibernate (Level)<br>Output:<br>0000 = GPIO<br>0001 = /MEMRST<br>0010 = ADA<br>0011 = RTC<br>0100 = MICDET<br>0101 = MICSHT<br>0110 = ADCLRCLKB<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                  | 7:4  | GP5_FN[3:0] | 0000<br>0001<br>0000<br>0000 | GPIO5 alternate function:<br>Input:<br>0000 = GPIO<br>0001 = L_PWR1<br>0010 = ADCLRCLK<br>0011 = Hibernate (Edge)<br>0100 = PWR_OFF<br>0101 = Hibernate (Level)<br>Output:<br>0000 = GPIO<br>0001 = P_CLK<br>0010 = ADCLRCLK<br>0011 = 32kHz<br>0100 = /BATT_FAULT<br>0101 = MICSHT<br>0110 = ADA<br>0111 = CODEC_OPCLK<br>1010 = MICDET<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 3:0  | GP4_FN[3:0] | 0000<br>0000<br>0011<br>0001 | GPIO4 alternate function:<br>Input:<br>0000 = GPIO<br>0001 = /MR<br>0010 = FLASH<br>0011 = Hibernate (level)<br>0100 = MASK<br>0101 = CHIP_RESET<br>Output:<br>0000 = GPIO<br>0001 = /MEMRST<br>0010 = ADA<br>0011 = FLASH_OUT<br>0100 = /VCC_FAULT<br>0101 = MICSHT<br>1010 = MICDET<br><i>Reset by state machine. Default held in metal mask.</i>  |          |

Register 8Dh GPIO Function Select 2

| REGISTER ADDRESS                           | BIT   | LABEL        | DEFAULT                      | DESCRIPTION   | REFER TO |
|--|-------|--------------|------------------------------|---|----------|
| R142 (8Eh)<br>GPIO<br>Function<br>Select 3 | 15:12 | GP11_FN[3:0] | 0000<br>0000<br>0010<br>0010 | GPIO11 alternate function:<br>Input:<br>0000 = GPIO<br>0010 = /WAKEUP<br>Output:<br>0000 = GPIO<br>0001 = ISINKD<br>0010 = LINE_GT_BATT<br>0011 = CH_IND<br><i>Reset by state machine. Default held in metal mask.</i>  |          |
|  | 11:8  | GP10_FN[3:0] | 0000<br>0000<br>0000<br>0011 | GPIO10 alternate function:<br>Input:<br>0000 = GPIO<br>0011 = PWR_OFF<br>Output:<br>0000 = GPIO<br>0001 = ISINKC<br>0010 = LINE_GT_BATT<br>0011 = CH_IND<br><i>Reset by state machine. Default held in metal mask.</i>  |          |
|  | 7:4   | GP9_FN[3:0]  | 0000<br>0001<br>0000<br>0000 | GPIO9 alternate function:<br>Input:<br>0000 = GPIO<br>0001 = HEARTBEAT<br>0010 = MASK<br>0011 = PWR_OFF<br>0100 = HIBERNATE (Level)<br>Output:<br>0000 = GPIO<br>0001 = /VCC_FAULT<br>0010 = LINE_GT_BATT<br>0011 = /BATT_FAULT<br>0100 = /MEMRST<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|  | 3:0   | GP8_FN[3:0]  | 0000<br>0011<br>0000<br>0000 | GPIO8 alternate function:<br>Input:<br>0000 = GPIO<br>0001 = /MR<br>0010 = ADCBCLK<br>0011 = PWR_OFF<br>0100 = HIBERNATE (edge)<br>Output:<br>0000 = GPIO<br>0001 = /VCC_FAULT<br>0010 = ADCBCLK<br>0011 = /BATT_FAULT<br>0100 = /RST<br><i>Reset by state machine. Default held in metal mask.</i>             |          |

Register 8Eh GPIO Function Select 3

| REGISTER ADDRESS                           | BIT | LABEL        | DEFAULT                      | DESCRIPTION  | REFER TO |
|--|-----|--------------|------------------------------|--|----------|
| R143 (8Fh)<br>GPIO<br>Function<br>Select 4 | 3:0 | GP12_FN[3:0] | 0011<br>0011<br>0000<br>0011 | GPIO12 alternate function:<br>Input:<br>0000 = GPIO<br>0001 = CHIP_RESET<br>Output:<br>0000 = GPIO<br>0001 = ISINKE<br>0010 = LINE_GT_BATT<br>0011 = LINE_SW<br>0100 = 32kHz<br><i>Reset by state machine. Default held in metal mask.</i> |          |

Register 8Fh GPIO Function Select 4

| REGISTER ADDRESS                       | BIT | LABEL           | DEFAULT | DESCRIPTION   | REFER TO |
|--|-----|-----------------|---------|---|----------|
| R144 (90h)<br>Digitiser<br>Control (1) | 15  | AUXADC_ENA      | 0       | AUXADC control<br>0 = disabled<br>1 = enabled<br><i>Reset by state machine.</i>   |          |
|  | 14  | AUXADC_CTC      | 0       | Continuous conversion mode:<br>0 = Polling mode<br>1 = Continuous mode<br><i>Reset by state machine.</i>  |          |
|  | 13  | AUXADC_POLL     | 0       | Writing "1" initiates a set of measurements in polling mode (AUXADC_CTC=0). This bit is automatically reset after the measurements are completed.<br><i>Reset by state machine.</i> |          |
|  | 12  | AUXADC_HIB_MODE | 0       | AUXADC state in hibernate mode:<br>0 = Leave AUXADC as in Active<br>1 = Disable AUXADC.<br><i>Reset by state machine.</i>   |          |
|  | 7   | AUXADC_SEL8     | 0       | AUXADC TEMP input select<br>0 = Disable TEMP measurement<br>1 = Enable TEMP measurement<br><i>Reset by state machine.</i>   |          |
|  | 6   | AUXADC_SEL7     | 0       | AUXADC BATT input select<br>0 = Disable BATT measurement<br>1 = Enable BATT measurement<br><i>Reset by state machine.</i>   |          |
|  | 5   | AUXADC_SEL6     | 0       | AUXADC LINE input select<br>0 = Disable LINE measurement<br>1 = Enable LINE measurement<br><i>Reset by state machine.</i>   |          |
|  | 4   | AUXADC_SEL5     | 0       | AUXADC USB input select<br>0 = Disable USB measurement<br>1 = Enable USB measurement<br><i>Reset by state machine.</i>  |          |
|  | 3   | AUXADC_SEL4     | 0       | AUXADC AUX4 input select<br>0 = Disable AUX4 measurement<br>1 = Enable AUX4 measurement<br><i>Reset by state machine.</i>   |          |



| REGISTER ADDRESS | BIT | LABEL       | DEFAULT | DESCRIPTION   | REFER TO |
|------------------|-----|-------------|---------|---|----------|
|                  | 2   | AUXADC_SEL3 | 0       | AUXADC AUX3 input select<br>0 = Disable AUX3 measurement<br>1 = Enable AUX3 measurement<br><i>Reset by state machine.</i> |          |
|                  | 1   | AUXADC_SEL2 | 0       | AUXADC AUX2 input select<br>0 = Disable AUX2 measurement<br>1 = Enable AUX2 measurement<br><i>Reset by state machine.</i> |          |
|                  | 0   | AUXADC_SEL1 | 0       | AUXADC AUX1 input select<br>0 = Disable AUX1 measurement<br>1 = Enable AUX1 measurement<br><i>Reset by state machine.</i> |          |

Register 90h Digitiser Control (1)

| REGISTER ADDRESS                       | BIT   | LABEL                | DEFAULT | DESCRIPTION   | REFER TO |
|--|-------|----------------------|---------|---|----------|
| R145 (91h)<br>Digitiser<br>Control (2) | 13:12 | AUXADC_MASKMODE[1:0] | 00      | AUXADC MASK input control<br>00 = MASK is ignored<br>01 = When MASK is asserted, all AUXADC measurements are inhibited.<br>10 = Reserved<br>11 = MASK input initiates AUXADC measurements. AUXADC_POLL and AUXADC_CTC have no effect. MASK polarity is controlled by GPN_CFG.<br><i>Reset by state machine.</i> |          |
|  | 10:8  | AUXADC_CRATE[2:0]    | 000     | AUXADC measurement frequency in Continuous mode<br>000 = 1Hz<br>001 = 4Hz<br>010 = 8Hz<br>011 = 16Hz<br>100 = 32Hz<br>101 = 64Hz<br>110 = 128Hz<br>111 = 256Hz<br><i>Reset by state machine.</i>  |          |
|  | 2     | AUXADC_CAL           | 0       | Configure AUX3 input to be the VREF supply for AUXADC calibration.<br>0 = AUX3 input connected to AUX3 pin<br>1 = AUX3 input connected to unbuffered VREF<br><i>Reset by state machine.</i>   |          |
|  | 1     | AUXADC_RBMODE        | 1       | Enable for AUXADC bandgap (VREF) buffer.<br>0 = AUXADC REFBUF is only enabled during conversions that use the VREF as a reference<br>1 = AUXADC REFBUF is always enabled when the AUXADC is enabled<br><i>Reset by state machine.</i>   |          |
|  | 0     | AUXADC_WAIT          | 0       | Whether the old data must be read before new conversions can be made<br>0 = No effect (new conversions overwrite old)<br>1 = New conversions are held back (and   |          |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION  | REFER TO |
|------------------|-----|-------|---------|--|----------|
|                  |     |       |         | measurements delayed) until AUX_DATAn has been read.<br><i>Reset by state machine.</i> |          |

Register 91h Digitiser Control (2)

| REGISTER ADDRESS               | BIT   | LABEL              | DEFAULT        | DESCRIPTION  | REFER TO |
|--------------------------------|-------|--------------------|----------------|--|----------|
| R152 (98h)<br>AUX1<br>Readback | 14:13 | AUXADC_SCALE1[1:0] | 11             | AUX1 input select:<br>00 = Off<br>01 = Input divided by 1<br>10 = Input divided by 2<br>11 = Input divided by 4      |          |
|                                | 12    | AUXADC_REF1        | 1              | AUX1 reference select<br>0 = AUX1 measured relative to VRTC<br>1 = AUX1 measured relative to VREF                    |          |
|                                | 11:0  | AUXADC_DATA1[11:0] | 0000_0000_0000 | Measured AUX1 data value relative to reference:<br>000 = 0V<br>FFF = measured voltage after divide matches reference |          |

Register 98h AUX1 Readback

| REGISTER ADDRESS               | BIT   | LABEL              | DEFAULT        | DESCRIPTION  | REFER TO |
|--------------------------------|-------|--------------------|----------------|--|----------|
| R153 (99h)<br>AUX2<br>Readback | 14:13 | AUXADC_SCALE2[1:0] | 11             | AUX2 input select:<br>00 = Off<br>01 = Input divided by 1<br>10 = Input divided by 2<br>11 = Input divided by 4      |          |
|                                | 12    | AUXADC_REF2        | 1              | AUX2 reference select<br>0 = AUX2 measured relative to VRTC<br>1 = AUX2 measured relative to VREF                    |          |
|                                | 11:0  | AUXADC_DATA2[11:0] | 0000_0000_0000 | Measured AUX2 data value relative to reference:<br>000 = 0V<br>FFF = measured voltage after divide matches reference |          |

Register 99h AUX2 Readback

| REGISTER ADDRESS               | BIT   | LABEL              | DEFAULT        | DESCRIPTION  | REFER TO |
|--------------------------------|-------|--------------------|----------------|--|----------|
| R154 (9Ah)<br>AUX3<br>Readback | 14:13 | AUXADC_SCALE3[1:0] | 11             | AUX3 input select:<br>00 = Off<br>01 = Input divided by 1<br>10 = Input divided by 2<br>11 = Input divided by 4      |          |
|                                | 12    | AUXADC_REF3        | 1              | AUX3 reference select<br>0 = AUX3 measured relative to VRTC<br>1 = AUX3 measured relative to VREF                    |          |
|                                | 11:0  | AUXADC_DATA3[11:0] | 0000_0000_0000 | Measured AUX3 data value relative to reference:<br>000 = 0V<br>FFF = measured voltage after divide matches reference |          |

Register 9Ah AUX3 Readback

| REGISTER ADDRESS               | BIT   | LABEL              | DEFAULT        | DESCRIPTION  | REFER TO |
|--------------------------------|-------|--------------------|----------------|--|----------|
| R155 (9Bh)<br>AUX4<br>Readback | 14:13 | AUXADC_SCALE4[1:0] | 11             | AUX4 input select:<br>00 = Off<br>01 = Input divided by 1<br>10 = Input divided by 2<br>11 = Input divided by 4      |          |
|                                | 12    | AUXADC_REF4        | 1              | AUX4 reference select<br>0 = AUX4 measured relative to VRTC<br>1 = AUX4 measured relative to VREF                    |          |
|                                | 11:0  | AUXADC_DATA4[11:0] | 0000_0000_0000 | Measured AUX4 data value relative to reference:<br>000 = 0V<br>FFF = measured voltage after divide matches reference |          |

Register 9Bh AUX4 Readback

| REGISTER ADDRESS                         | BIT  | LABEL                 | DEFAULT        | DESCRIPTION                      | REFER TO |
|--|------|-----------------------|----------------|----------------------------------|----------|
| R156 (9Ch)<br>USB<br>Voltage<br>Readback | 11:0 | AUXADC_DATA_USB[11:0] | 0000_0000_0000 | Measured USB voltage data value. |          |

Register 9Ch USB Voltage Readback

| REGISTER ADDRESS                          | BIT  | LABEL                  | DEFAULT        | DESCRIPTION                       | REFER TO |
|---|------|------------------------|----------------|-----------------------------------|----------|
| R157 (9Dh)<br>LINE<br>Voltage<br>Readback | 11:0 | AUXADC_DATA_LINE[11:0] | 0000_0000_0000 | Measured LINE voltage data value. |          |

Register 9Dh LINE Voltage Readback

| REGISTER ADDRESS                          | BIT  | LABEL                  | DEFAULT        | DESCRIPTION               | REFER TO |
|---|------|------------------------|----------------|---------------------------|----------|
| R158 (9Eh)<br>BATT<br>Voltage<br>Readback | 11:0 | AUXADC_DATA_BATT[11:0] | 0000_0000_0000 | Measured Battery voltage. |          |

**Register 9Eh** BATT Voltage Readback

| REGISTER ADDRESS                    | BIT  | LABEL                      | DEFAULT        | DESCRIPTION                        | REFER TO |
|-------------------------------------|------|----------------------------|----------------|------------------------------------|----------|
| R159 (9Fh)<br>Chip Temp<br>Readback | 11:0 | AUXADC_DATA_CHIPTEMP[11:0] | 0000_0000_0000 | Measured internal chip temperature |          |

**Register 9Fh** Chip Temp Readback

| REGISTER ADDRESS                               | BIT | LABEL     | DEFAULT | DESCRIPTION  | REFER TO |
|--|-----|-----------|---------|--|----------|
| R163 (A3h)<br>Generic<br>Comparator<br>Control | 3   | DCMP4_ENA | 0       | Digital comparator 4 enable<br>0 = disabled<br>1 = enabled<br><i>Reset by state machine.</i> |          |
|  | 2   | DCMP3_ENA | 0       | Digital comparator 3 enable<br>0 = disabled<br>1 = enabled<br><i>Reset by state machine.</i> |          |
|  | 1   | DCMP2_ENA | 0       | Digital comparator 2 enable<br>0 = disabled<br>1 = enabled<br><i>Reset by state machine.</i> |          |
|  | 0   | DCMP1_ENA | 0       | Digital comparator 1 enable<br>0 = disabled<br>1 = enabled<br><i>Reset by state machine.</i> |          |

**Register A3h** Generic Comparator Control

| REGISTER ADDRESS                         | BIT   | LABEL             | DEFAULT        | DESCRIPTION  | REFER TO |
|--|-------|-------------------|----------------|--|----------|
| R164 (A4h)<br>Generic<br>comparator<br>1 | 15:13 | DCMP1_SRCSEL[2:0] | 000            | DCOMP1 source select.<br>000 = AUX1<br>001 = AUX2<br>010 = AUX3<br>011 = AUX4<br>100 = USB<br>101 = LINE<br>110 = BATT<br>111 = TEMP<br><i>Reset by state machine.</i> |          |
|  | 12    | DCMP1_GT          | 0              | DCOMP1 interrupt control<br>0 = interrupt when the source is less than threshold<br>1 = interrupt when the source is greater than threshold                            |          |
|  | 11:0  | DCMP1_THR[11:0]   | 0000_0000_0000 | DCOMP1 threshold<br>(12-bit unsigned binary number)  |          |

**Register A4h** Generic comparator 1

| REGISTER ADDRESS                   | BIT   | LABEL             | DEFAULT        | DESCRIPTION  | REFER TO |
|------------------------------------|-------|-------------------|----------------|--|----------|
| R165 (A5h)<br>Generic comparator 2 | 15:13 | DCMP2_SRCSEL[2:0] | 000            | DCOMP2 source select.<br>000 = AUX1<br>001 = AUX2<br>010 = AUX3<br>011 = AUX4<br>100 = USB<br>101 = LINE<br>110 = BATT<br>111 = TEMP<br><i>Reset by state machine.</i> |          |
|                                    | 12    | DCMP2_GT          | 0              | DCOMP2 interrupt control<br>0 = interrupt when the source is less than threshold<br>1 = interrupt when the source is greater than threshold                            |          |
|                                    | 11:0  | DCMP2_THR[11:0]   | 0000_0000_0000 | DCOMP2 threshold<br>(12-bit unsigned binary number)  |          |

**Register A5h** Generic comparator 2

| REGISTER ADDRESS                   | BIT   | LABEL             | DEFAULT        | DESCRIPTION  | REFER TO |
|------------------------------------|-------|-------------------|----------------|--|----------|
| R166 (A6h)<br>Generic comparator 3 | 15:13 | DCMP3_SRCSEL[2:0] | 000            | DCOMP3 source select.<br>000 = AUX1<br>001 = AUX2<br>010 = AUX3<br>011 = AUX4<br>100 = USB<br>101 = LINE<br>110 = BATT<br>111 = TEMP<br><i>Reset by state machine.</i> |          |
|                                    | 12    | DCMP3_GT          | 0              | DCOMP3 interrupt control<br>0 = interrupt when the source is less than threshold<br>1 = interrupt when the source is greater than threshold                            |          |
|                                    | 11:0  | DCMP3_THR[11:0]   | 0000_0000_0000 | DCOMP3 threshold<br>(12-bit unsigned binary number)  |          |

**Register A6h** Generic comparator 3

| REGISTER ADDRESS                   | BIT   | LABEL             | DEFAULT        | DESCRIPTION  | REFER TO |
|------------------------------------|-------|-------------------|----------------|--|----------|
| R167 (A7h)<br>Generic comparator 4 | 15:13 | DCMP4_SRCSEL[2:0] | 000            | DCOMP4 source select.<br>000 = AUX1<br>001 = AUX2<br>010 = AUX3<br>011 = AUX4<br>100 = USB<br>101 = LINE<br>110 = BATT<br>111 = TEMP<br><i>Reset by state machine.</i> |          |
|                                    | 12    | DCMP4_GT          | 0              | DCOMP4 interrupt control<br>0 = interrupt when the source is less than threshold<br>1 = interrupt when the source is greater than threshold                            |          |
|                                    | 11:0  | DCMP4_THR[11:0]   | 0000_0000_0000 | DCOMP4 threshold<br>(12-bit unsigned binary number)  |          |

Register A7h Generic comparator 4

| REGISTER ADDRESS                        | BIT   | LABEL                  | DEFAULT | DESCRIPTION  | REFER TO |
|---|-------|------------------------|---------|--|----------|
| R168 (A8h)<br>Battery Charger Control 1 | 15    | CHG_ENA                | 1       | CHG_ENA bit selects battery charger current control<br>0 = Set battery charger current to zero<br>1 = Enable battery charge control<br><i>Protected by security key. Reset by state machine. Default held in metal mask.</i> |          |
|   | 12:10 | CHG_EOC_SEL[2:0]       | 000     | Selects what the end of charge current should be set to<br>000 = 20mA<br>001 = 30mA<br>(10mA steps)<br>...<br>111 = 90mA<br><i>Protected by security key.</i>  |          |
|   | 9     | CHG_TRICKLE_TEMP_CHOKE | 0       | Enable trickle charge temperature choking<br>0 = disable<br>1 = enable<br><i>Protected by security key. Reset by state machine.</i>  |          |
|   | 8     | CHG_TRICKLE_USB_CHOKE  | 0       | Enable USB current choking in trickle charge<br>0 = disable<br>1 = enable<br><i>Protected by security key. Reset by state machine.</i>   |          |
|   | 7     | CHG_RECOVER_T          | 0       | Time constant adjust for charger choke recovery (step-up):<br>0 = Step-up time constant is 180us (allows faster recovery between processor wakeups)<br>1 = Step-up time constant is >20ms (outside audio band)               |          |

| REGISTER ADDRESS | BIT | LABEL                 | DEFAULT          | DESCRIPTION   | REFER TO |
|------------------|-----|-----------------------|------------------|---|----------|
|                  |     |                       |                  | <i>Protected by security key. Reset by state machine.</i>   |          |
|                  | 6   | CHG_END_ACT           | 0                | Action to take when charging ends:<br>0 = Set charge current to 0<br>1 = Do nothing (leave charger on till timeout)<br><i>Protected by security key. Reset by state machine.</i>  |          |
|                  | 5   | CHG_FAST              | 0                | Enable fast charging.<br>0 = Fast charging cannot take place.<br>1 = Enable fast charging (will not start until valid charging conditions are met).<br>Note: This register is held low and can only be written to once the fast charge ready signal has gone high.<br><i>Protected by security key. Reset by state machine. Default held in metal mask.</i> |          |
|                  | 4   | CHG_FAST_USB_THROTTLE | 0                | Enable USB current throttling in fast charge:<br>0 = 'on't do any current throttling when fast charging.<br>1 = Do current throttle while fast charging.<br><i>Protected by security key. Reset by state machine.</i>   |          |
|                  | 3   | CHG_NTC_MON           | 1<br>1<br>1<br>1 | Enable charger battery NTC detection (some batteries may not need this - turn off with caution)<br>0 = Charger ignores NO_NTC detection.<br>1 = Charger monitors NO_NTC detection.<br><i>Default held in metal mask.</i>  |          |
|                  | 2   | CHG_BATT_HOT_MON      | 1<br>1<br>1<br>1 | Enable charger battery temperature high detection (some batteries may not need this - turn off with caution)<br>0 = Charger ignores battery temperature too high.<br>1 = Charger monitors battery temperature too high.<br><i>Default held in metal mask.</i>   |          |
|                  | 1   | CHG_BATT_COLD_MON     | 1<br>1<br>1<br>1 | Enable charger battery temperature low detection (some batteries may not need this - turn off with caution)<br>0 = Charger ignores battery temperature low.<br>1 = Charger monitors battery temperature low.<br><i>Default held in metal mask.</i>  |          |
|                  | 0   | CHG_CHIP_TEMP_MON     | 1                | Enable charger chip temperature detection (some batteries may not need this - turn off with caution)<br>0 = Charger ignores chip temperature<br>1 = Charger monitors chip temperature<br><i>Protected by security key. Default held in metal mask.</i>  |          |

Register A8h Battery Charger Control 1

| REGISTER ADDRESS                              | BIT   | LABEL            | DEFAULT | DESCRIPTION   | REFER TO |
|---|-------|------------------|---------|---|----------|
| R169 (A9h)<br>Battery<br>Charger<br>Control 2 | 15    | CHG_ACTIVE       | 0       | Charger Status.<br>0 = Battery Charging is inactive<br>1 = Battery Charging is active<br>(Note CHG_ENA is just a request; the WM8350 determines if the conditions are satisfied for Battery Charging).<br><i>Default held in metal mask.</i>  |          |
|   | 14    | CHG_PAUSE        | 0       | 0 = 'on't pause the charger<br>1 = Pause charging<br><i>Reset by state machine.</i>   |          |
|   | 13:12 | CHG_STS[1:0]     | 00      | 00 = Charger off, current set to 0.<br>01 = In trickle charge mode.<br>10 = In fast charge mode.<br>11 = Reserved   |          |
|   | 11:8  | CHG_TIME[3:0]    | 1011    | Writing to his field set the charge timeout duration:<br>0000 = 60min<br>0001 = 90min<br>0010 = 120min<br>0011 = 150min<br>0100 = 180min<br>0101 = 210min<br>0110 = 240min<br>0111 = 270min<br>1000 = 300min<br>1001 = 330min<br>1010 = 360min<br>1011 = 390min<br>1100 = 420min<br>1101 = 450min<br>1110 = 480min<br>1111 = 510min<br>Reading from this field indicates the charge time remaining:<br>Time remaining = CHG_TIME * 2048s<br><i>Protected by security key. Default held in metal mask.</i> |          |
|   | 7     | CHG_MASK_WALL_FB | 0       | Selects whether to ignore the WALL_FB signal when charging from LINE.<br>0 = Does not mask the WALL_FB signal<br>1 = Mask the WALL_FB signal.<br>Note: Care needs to be taken when using this bit.<br><i>Protected by security key. Reset by state machine.</i>   |          |
|   | 6     | CHG_TRICKLE_SEL  | 0       | Selects the trickle charge current.<br>0 = Set the trickle charge current to 50mA.<br>1 = Set the trickle charge current to 100mA.<br><i>Protected by security key.</i>   |          |
|   | 5:4   | CHG_VSEL[1:0]    | 00      | Battery charge voltage:<br>00 = 4.05V<br>01 = 4.1V<br>10 = 4.15V<br>11 = 4.2V<br><i>Protected by security key.</i>  |          |
|   | 3:0   | CHG_ISEL[3:0]    | 0110    | Fast charge current limit setting.  |          |



| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION  | REFER TO |
|------------------|-----|-------|---------|--|----------|
|                  |     |       |         | 0000 = off<br>0001 = 50mA<br>0010 = 100mA<br>... (50mA steps)<br>1111 = 750mA<br>Note: Do not set the charger to be more than 400mA when USB powered.<br><i>Protected by security key.</i> |          |

Register A9h Battery Charger Control 2

| REGISTER ADDRESS                              | BIT | LABEL               | DEFAULT | DESCRIPTION   | REFER TO |
|---|-----|---------------------|---------|---|----------|
| R170 (AAh)<br>Battery<br>Charger<br>Control 3 | 7   | CHG_FRC             | 0       | Allows trickle-charging to be forced even if the battery voltage is above the default threshold<br>0 = only trickle-charge if the battery voltage is below CHG_VSEL-100mV<br>1 = always trickle-charge<br><i>Protected by security key. Reset by state machine.</i> |          |
|   | 6:5 | CHG_THROTTLE_T[1:0] | 00      | Time between steps when the charger throttles back due to USB current limit.<br>00 = 8us<br>01 = 16us<br>10 = 32us<br>11 = 128us<br><i>Protected by security key.</i>   |          |

Register AAh Battery Charger Control 3

| REGISTER ADDRESS                       | BIT | LABEL         | DEFAULT | DESCRIPTION   | REFER TO |
|--|-----|---------------|---------|---|----------|
| R172 (ACh)<br>Current Sink<br>Driver A | 15  | CS1_ENA       | 0       | Current Sink 1 enable (ISINKA pin)<br>0 = disabled<br>1 = enabled<br><i>Reset by state machine.</i>   |          |
|  | 12  | CS1_HIB_MODE  | 0       | Current Sink 1 behaviour in Hibernate mode<br>0 = disable current sink in Hibernate<br>1 = leave current sink as in Active<br><i>Reset by state machine.</i>  |          |
|  | 5:0 | CS1_ISEL[5:0] | 00_0000 | ISINKA current<br>00_0000 = 4.05uA<br>00_0001 = 4.85uA<br>00_0010 = 5.64uA<br>00_0011 = 6.83uA<br>00_0100 = 8.02uA<br>00_0101 = 9.6uA<br>00_0110 = 11.2uA<br>00_0111 = 13.5uA<br>00_1000 = 16.1uA<br>00_1001 = 19.3uA<br>00_1010 = 22.4uA<br>00_1011 = 27.2uA<br>00_1100 = 32uA |          |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION                    | REFER TO |
|------------------|-----|-------|---------|--------------------------------|----------|
|                  |     |       |         | 00_1101 = 38.3uA               |          |
|                  |     |       |         | 00_1110 = 44.7uA               |          |
|                  |     |       |         | 00_1111 = 54.1uA               |          |
|                  |     |       |         | 01_0000 = 64.1uA               |          |
|                  |     |       |         | 01_0001 = 76.8uA               |          |
|                  |     |       |         | 01_0010 = 89.5uA               |          |
|                  |     |       |         | 01_0011 = 109uA                |          |
|                  |     |       |         | 01_0100 = 128uA                |          |
|                  |     |       |         | 01_0101 = 153uA                |          |
|                  |     |       |         | 01_0110 = 178uA                |          |
|                  |     |       |         | 01_0111 = 216uA                |          |
|                  |     |       |         | 01_1000 = 256uA                |          |
|                  |     |       |         | 01_1001 = 307uA                |          |
|                  |     |       |         | 01_1010 = 358uA                |          |
|                  |     |       |         | 01_1011 = 434uA                |          |
|                  |     |       |         | 01_1100 = 510uA                |          |
|                  |     |       |         | 01_1101 = 612uA                |          |
|                  |     |       |         | 01_1110 = 713uA                |          |
|                  |     |       |         | 01_1111 = 865uA                |          |
|                  |     |       |         | 10_0000 = 1.02mA               |          |
|                  |     |       |         | 10_0001 = 1.22mA               |          |
|                  |     |       |         | 10_0010 = 1.42mA               |          |
|                  |     |       |         | 10_0011 = 1.73mA               |          |
|                  |     |       |         | 10_0100 = 2.03mA               |          |
|                  |     |       |         | 10_0101 = 2.43mA               |          |
|                  |     |       |         | 10_0110 = 2.83mA               |          |
|                  |     |       |         | 10_0111 = 3.43mA               |          |
|                  |     |       |         | 10_1000 = 4.08mA               |          |
|                  |     |       |         | 10_1001 = 4.89mA               |          |
|                  |     |       |         | 10_1010 = 5.7mA                |          |
|                  |     |       |         | 10_1011 = 6.91mA               |          |
|                  |     |       |         | 10_1100 = 8.13mA               |          |
|                  |     |       |         | 10_1101 = 9.74mA               |          |
|                  |     |       |         | 10_1110 = 11.3mA               |          |
|                  |     |       |         | 10_1111 = 13.7mA               |          |
|                  |     |       |         | 11_0000 = 16.3mA               |          |
|                  |     |       |         | 11_0001 = 19.6mA               |          |
|                  |     |       |         | 11_0010 = 22.8mA               |          |
|                  |     |       |         | 11_0011 = 27.6mA               |          |
|                  |     |       |         | 11_0100 = 32.5mA               |          |
|                  |     |       |         | 11_0101 = 39mA                 |          |
|                  |     |       |         | 11_0110 = 45.4mA               |          |
|                  |     |       |         | 11_0111 = 54.9mA               |          |
|                  |     |       |         | 11_1000 = 65.3mA               |          |
|                  |     |       |         | 11_1001 = 78.2mA               |          |
|                  |     |       |         | 11_1010 = 91.2mA               |          |
|                  |     |       |         | 11_1011 = 111mA                |          |
|                  |     |       |         | 11_1100 = 130mA                |          |
|                  |     |       |         | 11_1101 = 156mA                |          |
|                  |     |       |         | 11_1110 = 181mA                |          |
|                  |     |       |         | 11_1111 = 220mA                |          |
|                  |     |       |         | <i>Reset by state machine.</i> |          |

Register ACh Current Sink Driver A

| REGISTER ADDRESS                | BIT              | LABEL              | DEFAULT                 | DESCRIPTION  | REFER TO |
|---------------------------------|------------------|--------------------|-------------------------|--|----------|
| R173 (ADh)<br>CSA Flash control | 15               | CS1_FLASH_MODE     | 0                       | Determines the function of the current sink<br>0 = LED mode<br>1 = Flash mode<br><i>Reset by state machine.</i>  |          |
|                                 | 14               | CS1_TRIGSRC        | 0                       | Selects the trigger for the flash<br>0 = Flash is triggered by CS1_DRIVE bit<br>1 = Flash is triggered from GPIO pin configured as FLASH<br>This bit has no effect when CS1_FLASH_MODE=0<br><i>Reset by state machine.</i>   |          |
|                                 | 13               | CS1_DRIVE          | 0                       | Enables the current sink ISINKA<br><br>LED mode-<br>0 = disable LED<br>1 = enabled LED<br><br>FLASH mode-<br>Register bit used to trigger the flash, if CS1_TRIGSRC is set to 0. Flash is started when the bit goes high, it is then reset at the end of the flash duration. Duration is determined by CS1_FLASH_DUR. This bit has no effect if CS1_TRIGSRC is set to 1.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                 | 12               | CS1_FLASH_RATE     | 0                       | Determines the Flash rate<br>0 = Normal Operation. Once per trigger (Either register bit or GPIO)<br>1 = Flash will be internally triggered every 4 seconds<br><i>Reset by state machine.</i>  |          |
|                                 | 9:8              | CS1_FLASH_DUR[1:0] | 00                      | Sets duration of flash<br>00 = 32ms<br>01 = 64ms<br>10 = 96ms<br>11 = 1024ms<br><i>Reset by state machine.</i>   |          |
|                                 | 5:4              | CS1_OFF_RAMP[1:0]  | 00                      | Switch-off ramp duration<br><br>LED mode-<br>00 = instant (no ramp)<br>01 = 0.25s<br>10 = 0.5s<br>11 = 1s<br><br>Flash mode-<br>00 = instant (no ramp)<br>01 = 1.95ms<br>10 = 3.91ms<br>11 = 7.8ms<br><i>Reset by state machine.</i>   |          |
| 1:0                             | CS1_ON_RAMP[1:0] | 00                 | Switch-on ramp duration |  |          |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION  | REFER TO |
|------------------|-----|-------|---------|--|----------|
|                  |     |       |         | LED mode-<br>00 = instant (no ramp)<br>01 = 0.25s<br>10 = 0.5s<br>11 = 1s<br><br>Flash mode-<br>00 = instant (no ramp)<br>01 = 1.95ms<br>10 = 3.91ms<br>11 = 7.8ms<br><i>Reset by state machine.</i> |          |

Register ADh CSA Flash control

| REGISTER ADDRESS                       | BIT | LABEL         | DEFAULT | DESCRIPTION  | REFER TO |
|--|-----|---------------|---------|--|----------|
| R174 (AEh)<br>Current Sink<br>Driver B | 15  | CS2_ENA       | 0       | Current Sink 2 enable (ISINKB pin)<br>0 = disabled<br>1 = enabled<br><i>Reset by state machine.</i>  |          |
|  | 12  | CS2_HIB_MODE  | 0       | Current Sink 2 behaviour in Hibernate mode<br>0 = disable current sink in Hibernate<br>1 = leave current sink as in Active<br><i>Reset by state machine.</i>   |          |
|  | 5:0 | CS2_ISEL[5:0] | 00_0000 | ISINK2 current<br>00_0000 = 4.05uA<br>00_0001 = 4.85uA<br>00_0010 = 5.64uA<br>00_0011 = 6.83uA<br>00_0100 = 8.02uA<br>00_0101 = 9.6uA<br>00_0110 = 11.2uA<br>00_0111 = 13.5uA<br>00_1000 = 16.1uA<br>00_1001 = 19.3uA<br>00_1010 = 22.4uA<br>00_1011 = 27.2uA<br>00_1100 = 32uA<br>00_1101 = 38.3uA<br>00_1110 = 44.7uA<br>00_1111 = 54.1uA<br>01_0000 = 64.1uA<br>01_0001 = 76.8uA<br>01_0010 = 89.5uA<br>01_0011 = 109uA<br>01_0100 = 128uA<br>01_0101 = 153uA<br>01_0110 = 178uA<br>01_0111 = 216uA<br>01_1000 = 256uA<br>01_1001 = 307uA<br>01_1010 = 358uA<br>01_1011 = 434uA |          |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION  | REFER TO |
|------------------|-----|-------|---------|--|----------|
|                  |     |       |         | 01_1100 = 510uA<br>01_1101 = 612uA<br>01_1110 = 713uA<br>01_1111 = 865uA<br>10_0000 = 1.02mA<br>10_0001 = 1.22mA<br>10_0010 = 1.42mA<br>10_0011 = 1.73mA<br>10_0100 = 2.03mA<br>10_0101 = 2.43mA<br>10_0110 = 2.83mA<br>10_0111 = 3.43mA<br>10_1000 = 4.08mA<br>10_1001 = 4.89mA<br>10_1010 = 5.7mA<br>10_1011 = 6.91mA<br>10_1100 = 8.13mA<br>10_1101 = 9.74mA<br>10_1110 = 11.3mA<br>10_1111 = 13.7mA<br>11_0000 = 16.3mA<br>11_0001 = 19.6mA<br>11_0010 = 22.8mA<br>11_0011 = 27.6mA<br>11_0100 = 32.5mA<br>11_0101 = 39mA<br>11_0110 = 45.4mA<br>11_0111 = 54.9mA<br>11_1000 = 65.3mA<br>11_1001 = 78.2mA<br>11_1010 = 91.2mA<br>11_1011 = 111mA<br>11_1100 = 130mA<br>11_1101 = 156mA<br>11_1110 = 181mA<br>11_1111 = 220mA<br><i>Reset by state machine.</i> |          |

Register AEh Current Sink Driver B

| REGISTER ADDRESS                | BIT | LABEL          | DEFAULT | DESCRIPTION   | REFER TO |
|---------------------------------|-----|----------------|---------|---|----------|
| R175 (AFh)<br>CSB Flash control | 15  | CS2_FLASH_MODE | 0       | Determines the function of the current sink<br>0 = LED mode<br>1 = Flash mode<br><i>Reset by state machine.</i>   |          |
|                                 | 14  | CS2_TRIGSRC    | 0       | Selects the trigger in Flash mode.<br>0 = Flash triggered by CS2_DRIVE bit<br>1 = Flash triggered from GPIO pin configured as FLASH<br>This bit has no effect when CS2_FLASH_MODE=0<br><i>Reset by state machine.</i> |          |

| REGISTER ADDRESS | BIT | LABEL              | DEFAULT | DESCRIPTION   | REFER TO |
|------------------|-----|--------------------|---------|---|----------|
|                  | 13  | CS2_DRIVE          | 0       | <p>Enables the current sink ISINKB</p> <p>LED mode-<br/>0 = disable LED<br/>1 = enabled LED</p> <p>FLASH mode-<br/>Register bit used to trigger the flash, if CS2_TRIGSRC is set to 0. Flash is started when the bit goes high, it is then reset at the end of the flash duration. Duration is determined by CS2_FLASH_DUR. This bit has no effect if CS2_TRIGSRC is set to 1.<br/><i>Reset by state machine. Default held in metal mask.</i></p> |          |
|                  | 12  | CS2_FLASH_RATE     | 0       | <p>Determines the Flash rate<br/>0 = Normal Operation. Once per trigger (Either register bit or GPIO)<br/>1 = Flash will be internally triggered every 4 seconds<br/><i>Reset by state machine.</i></p>   |          |
|                  | 9:8 | CS2_FLASH_DUR[1:0] | 00      | <p>Sets duration of flash<br/>00 = 32ms<br/>01 = 64ms<br/>10 = 96ms<br/>11 = 1024ms<br/><i>Reset by state machine.</i></p>  |          |
|                  | 5:4 | CS2_OFF_RAMP[1:0]  | 00      | <p>Switch-off ramp duration</p> <p>LED mode-<br/>00 = instant (no ramp)<br/>01 = 0.25s<br/>10 = 0.5s<br/>11 = 1s</p> <p>Flash mode-<br/>00 = instant (no ramp)<br/>01 = 1.95ms<br/>10 = 3.91ms<br/>11 = 7.8ms<br/><i>Reset by state machine.</i></p>  |          |
|                  | 1:0 | CS2_ON_RAMP[1:0]   | 00      | <p>Switch-on ramp duration</p> <p>LED mode-<br/>00 = instant (no ramp)<br/>01 = 0.25s<br/>10 = 0.5s<br/>11 = 1s</p> <p>Flash mode-<br/>00 = instant (no ramp)<br/>01 = 1.95ms<br/>10 = 3.91ms<br/>11 = 7.8ms<br/><i>Reset by state machine.</i></p>   |          |

Register AFh CSB Flash control

| REGISTER ADDRESS                    | BIT | LABEL    | DEFAULT | DESCRIPTION   | REFER TO |
|-------------------------------------|-----|----------|---------|---|----------|
| R176 (B0h)<br>DCDC/LDO<br>requested | 15  | LS_ENA   | 0       | Limit Switch enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i>    |          |
|                                     | 11  | LDO4_ENA | 0       | LDO4 enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i>            |          |
|                                     | 10  | LDO3_ENA | 0       | LDO3 enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i>            |          |
|                                     | 9   | LDO2_ENA | 0       | LDO2 enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i>            |          |
|                                     | 8   | LDO1_ENA | 0       | LDO1 enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i>            |          |
|                                     | 5   | DC6_ENA  | 0       | DCDC6 converter enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                     | 4   | DC5_ENA  | 0       | DCDC5 converter enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                     | 3   | DC4_ENA  | 0       | DCDC4 converter enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.   |          |

| REGISTER ADDRESS | BIT | LABEL   | DEFAULT | DESCRIPTION   | REFER TO |
|------------------|-----|---------|---------|---|----------|
|                  |     |         |         | <i>Reset by state machine. Default held in metal mask.</i>  |          |
|                  | 2   | DC3_ENA | 0       | DCDC3 converter enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 1   | DC2_ENA | 0       | DCDC2 converter enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                  | 0   | DC1_ENA | 0       | DCDC1 converter enable<br>0 = disabled<br>1 = enabled<br>Note: internal conditions may prevent the converter from actually switching on - see DCDC/LDO Status register for actual converter status.<br><i>Reset by state machine. Default held in metal mask.</i> |          |

Register B0h DCDC/LDO requested

| REGISTER ADDRESS                        | BIT   | LABEL        | DEFAULT | DESCRIPTION   | REFER TO |
|---|-------|--------------|---------|---|----------|
| R177 (B1h)<br>DCDC<br>Active<br>options | 15    | DCDC_DISCLKS | 0       | DCDC clock enable<br>0 = DCDC Clocks enabled<br>1 = DCDC1, 3, 4 and 6 clocks disabled.<br>Note: This feature is useful in reducing the current consumption if all 4 DCDCs are in LDO mode. The requirement is to put them in LDO mode and then at least 100us is required before clocks are disabled. Again while coming out of LDO mode first enable the clocks and then at least 100us wait and then come out of LDO mode. This can only be used if the processor is alive to set and unset this bit.<br><i>Reset by state machine.</i> |          |
|   | 13:12 | PUTO[1:0]    | 00      | Power up time out value for all converters<br>00 = 0.5ms<br>01 = 2ms<br>10 = 32ms<br>11 = 256ms<br><i>Reset by state machine.</i>   |          |
|   | 5     | DC6_ACTIVE   | 1       | DC-DC 6 Active mode<br>0 = Select Standby mode<br>1 = Select Active mode<br><i>Reset by state machine.</i>  |          |
|   | 3     | DC4_ACTIVE   | 1       | DC-DC 4 Active mode<br>0 = Select Standby mode<br>1 = Select Active mode<br><i>Reset by state machine.</i>  |          |
|   | 2     | DC3_ACTIVE   | 1       | DC-DC 3 Active mode<br>0 = Select Standby mode<br>1 = Select Active mode  |          |



| REGISTER ADDRESS | BIT | LABEL      | DEFAULT | DESCRIPTION  | REFER TO |
|------------------|-----|------------|---------|--|----------|
|                  |     |            |         | <i>Reset by state machine.</i>   |          |
|                  | 0   | DC1_ACTIVE | 1       | DC-DC 1 Active mode<br>0 = Select Standby mode<br>1 = Select Active mode<br><i>Reset by state machine.</i> |          |

**Register B1h** DCDC Active options

| REGISTER ADDRESS                 | BIT | LABEL     | DEFAULT | DESCRIPTION   | REFER TO |
|----------------------------------|-----|-----------|---------|---|----------|
| R178 (B2h)<br>DCDC Sleep options | 5   | DC6_SLEEP | 0       | DC-DC 6 Sleep mode<br>0 = Normal DC-DC operation<br>1 = Select LDO mode<br><i>Reset by state machine.</i> |          |
|                                  | 3   | DC4_SLEEP | 0       | DC-DC 4 Sleep mode<br>0 = Normal DC-DC operation<br>1 = Select LDO mode<br><i>Reset by state machine.</i> |          |
|                                  | 2   | DC3_SLEEP | 0       | DC-DC 3 Sleep mode<br>0 = Normal DC-DC operation<br>1 = Select LDO mode<br><i>Reset by state machine.</i> |          |
|                                  | 0   | DC1_SLEEP | 0       | DC-DC 1 Sleep mode<br>0 = Normal DC-DC operation<br>1 = Select LDO mode<br><i>Reset by state machine.</i> |          |

**Register B2h** DCDC Sleep options

| REGISTER ADDRESS                     | BIT | LABEL              | DEFAULT | DESCRIPTION  | REFER TO |
|--------------------------------------|-----|--------------------|---------|--|----------|
| R179 (B3h)<br>Power-check comparator | 14  | PCCMP_ERRACT       | 0       | Action when supply falls below PCCMP_OFF_THR level<br>0 = Generate critical supply interrupt only<br>1 = Generate interrupt and trigger hard shut down<br><i>Reset by state machine.</i>       |          |
|                                      | 12  | PCCOMP_HIB_MODE    | 0       | Function of Hyst Comp in the hibernate state<br>0 = Hyst Comp is not used in hibernate state<br>1 = Hyst comp is on in the hibernate state   |          |
|                                      | 6:4 | PCCMP_OFF_THR[2:0] | 010     | Power check comparator "critical batter" ("system turn "ff") threshold value<br>000 = 2.9V<br>001 = 3.0V<br>...<br>111 = 3.6V<br><i>Protected by security key. Default held in metal mask.</i> |          |
|                                      | 2:0 | PCCMP_ON_THR[2:0]  | 101     | Power check comparator ("system turn"on") threshold value<br>000 = 2.9V<br>001 = 3.0V<br>...<br>111 = 3.6V   |          |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION   | REFER TO |
|------------------|-----|-------|---------|---|----------|
|                  |     |       |         | <i>Protected by security key. Default held in metal mask.</i> |          |

Register B3h Power-check comparator

| REGISTER ADDRESS               | BIT   | LABEL         | DEFAULT                                      | DESCRIPTION   | REFER TO |
|--------------------------------|-------|---------------|--|---|----------|
| R180 (B4h)<br>DCDC1<br>Control | 15:14 | DC1_CAP[1:0]  | 00   | DC-DC1 Output Capacitor<br>00 = 10uF, 30uF, 45uF<br>01 = 60uF, 85uF<br>10 = Not used<br>11 = 100uF<br><i>Reset by state machine.</i>  |          |
|                                | 11    | DC1_DISOVP    | 0  | Over voltage Protection<br>0 = enabled<br>1 = disabled<br><i>Reset by state machine. Default held in metal mask.</i>  |          |
|                                | 10    | DC1_OPFLT     | 0  | Enable discharge of DC-DC1 outputs when DC-DC1 is disabled<br>0 = Enabled - Output to be discharged<br>1 = Disabled - Output is left floating   |          |
|                                | 6:0   | DC1_VSEL[6:0] | 000_1110<br>000_0110<br>001_0010<br>110_0010 | DC-DC1 Converter output voltage settings in 25mV steps.<br>Maximum output = 3.4V.<br><br>110 0110 = 3.4V<br>110 0010 = 3.3V<br>101 0110 = 3.0V<br>100 1110 = 2.8V<br>.....<br>010 0110 = 1.8V<br>000 1110 = 1.2V<br>000 0110 = 1.0V<br>000 0000 = 0.85V<br><i>Reset by state machine. Default held in metal mask.</i> |          |

Register B4h DCDC1 Control

| REGISTER ADDRESS                | BIT   | LABEL           | DEFAULT                      | DESCRIPTION   | REFER TO |
|---------------------------------|-------|-----------------|------------------------------|---|----------|
| R181 (B5h)<br>DCDC1<br>Timeouts | 15:14 | DC1_ERRACT[1:0] | 00                           | Action to take on DC-DC1 fault (as well as generating an interrupt):<br>00 = ignore<br>01 = shut down converter<br>10 = shut down system<br>11 = reserved (shut down system)<br><i>Reset by state machine. Default held in metal mask.</i>                                    |          |
|                                 | 13:10 | DC1_ENSLOT[3:0] | 0000<br>0100<br>0001<br>0010 | Time slot for DC-DC1 start-up<br>0000 = Disabled (do not start up)<br>0001 = Start-up in time slot 1<br>... (total 14 slots available)<br>1110 = Start-up in time slot 14<br>1111 = Start-up on entering ACTIVE<br><i>Reset by state machine. Default held in metal mask.</i> |          |

| REGISTER ADDRESS | BIT | LABEL           | DEFAULT | DESCRIPTION  | REFER TO |
|------------------|-----|-----------------|---------|--|----------|
|                  |     |                 |         | <i>mask.</i>   |          |
|                  | 9:6 | DC1_SDSLOT[3:0] | 0000    | Time slot for DC-DC1 shutdown.<br>0000 = Shut down on entering OFF<br>0001 = Shutdown in time slot 1<br>.... (total 14 slots available)<br>1110 = Shutdown in time slot 14<br>1111 = Shut down on entering OFF |          |

Register B5h DCDC1 Timeouts

| REGISTER ADDRESS              | BIT   | LABEL             | DEFAULT  | DESCRIPTION   | REFER TO |
|-------------------------------|-------|-------------------|----------|---|----------|
| R182 (B6h)<br>DCDC1 Low Power | 14:12 | DC1_HIB_MODE[2:0] | 001      | DC-DC1 Hibernate behaviour:<br>000 = Use current settings (no change)<br>001 = Select voltage image settings<br>010 = Force standby mode<br>011 = Force standby mode and voltage image settings.<br>100 = Force LDO mode<br>101 = Force LDO mode and voltage image settings.<br>110 = Reserved.<br>111 = Disable output |          |
|                               | 9:8   | DC1_HIB_TRIG[1:0] | 00       | DC-DC1 Hibernate signal select<br>00 = HIBERNATE register bit<br>01 = L_PWR1<br>10 = L_PWR2<br>11 = L_PWR3<br>Note that Hibernate is also selected when a GPIO Hibernate input is asserted.<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                               | 6:0   | DC1_VIMG[6:0]     | 000_0110 | DC-DC1 Converter output image voltage settings in 25mv steps.<br>Maximum output = 3.4V.<br><br>110 0110 = 3.4V<br>110 0010 = 3.3V<br>101 0110 = 3.0V<br>100 1110 = 2.8V<br>.....<br>010 0110 = 1.8V<br>000 1110 = 1.2V<br>000 0110 = 1.0V<br>000 0000 = 0.85V   |          |

Register B6h DCDC1 Low Power

| REGISTER ADDRESS               | BIT | LABEL             | DEFAULT | DESCRIPTION   | REFER TO |
|--------------------------------|-----|-------------------|---------|---|----------|
| R183 (B7h)<br>DCDC2<br>Control | 14  | DC2_MODE          | 0       | DC-DC2 Converter Mode<br>0 = Boost mode<br>1 = Switch mode<br><i>Reset by state machine.</i>  |          |
|                                | 12  | DC2_HIB_MODE      | 0       | DC-DC2 Hibernate behaviour:<br>0 = Continue as in Active state<br>1 = Disable converter output<br><i>Reset by state machine.</i>  |          |
|                                | 9:8 | DC2_HIB_TRIG[1:0] | 00      | DC-DC2 Hibernate signal select<br>00 = HIBERNATE register bit<br>01 = L_PWR1<br>10 = L_PWR2<br>11 = L_PWR3<br>Note that Hibernate is also selected when a GPIO Hibernate input is asserted.<br><i>Reset by state machine.</i>   |          |
|                                | 6   | DC2_ILIM          | 0       | DC-DC2 peak current limit select<br>0 = Higher peak current<br>1 = Lower peak current<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                                | 4   | DC2_RMPH          | 1       | DC-DC2 compensation ramp<br>{DC2_RMPH, DC2_RMPL}<br>00 = 20V < VOUT ≤ 30V<br>01 = 10V < VOUT ≤ 20V<br>10 = 5V < VOUT ≤ 10V<br>11 = VOUT ≤ 5V (will be chosen automatically if DC2_FBSRC=11)<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                                | 3   | DC2_RMPL          | 1       | DC-DC2 compensation ramp<br>{DC2_RMPH, DC2_RMPL}<br>00 = 20V < VOUT ≤ 30V<br>01 = 10V < VOUT ≤ 20V<br>10 = 5V < VOUT ≤ 10V<br>11 = VOUT ≤ 5V (will be chosen automatically if DC2_FBSRC=11)<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                                | 1:0 | DC2_FBSRC[1:0]    | 00      | DC-DC2 voltage feedback selection<br>00 = voltage feedback (using external resistor divider on pin FB2)<br>01 = current sink ISINKA used as feedback<br>10 = current sink ISINKB used as feedback<br>11 = voltage feedback (using internal resistor divider on pin USB)<br><i>Reset by state machine. Default held in metal mask.</i> |          |

Register B7h DCDC2 Control

| REGISTER ADDRESS                | BIT   | LABEL           | DEFAULT                      | DESCRIPTION   | REFER TO |
|---------------------------------|-------|-----------------|------------------------------|---|----------|
| R184 (B8h)<br>DCDC2<br>Timeouts | 15:14 | DC2_ERRACT[1:0] | 00                           | Action to take on DC-DC2 fault (as well as generating an interrupt):<br>00 = ignore<br>01 = shut down converter<br>10 = shut down system<br>11 = reserved (shut down system)<br><i>Reset by state machine. Default held in metal mask.</i>                                    |          |
|                                 | 13:10 | DC2_ENSLOT[3:0] | 0000<br>0000<br>0000<br>0000 | Time slot for DC-DC2 start-up<br>0000 = Disabled (do not start up)<br>0001 = Start-up in time slot 1<br>... (total 14 slots available)<br>1110 = Start-up in time slot 14<br>1111 = Start-up on entering ACTIVE<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                 | 9:6   | DC2_SDSLOT[3:0] | 0000                         | Time slot for DC-DC2 shutdown.<br>0000 = Shut down on entering OFF<br>0001 = Shutdown in time slot 1<br>.... (total 14 slots available)<br>1110 = Shutdown in time slot 14<br>1111 = Shut down on entering OFF  |          |

Register B8h DCDC2 Timeouts

| REGISTER ADDRESS               | BIT | LABEL         | DEFAULT                                      | DESCRIPTION   | REFER TO |
|--------------------------------|-----|---------------|--|---|----------|
| R186 (BAh)<br>DCDC3<br>Control | 11  | DC3_DISOVP    | 0  | Over voltage Protection<br>0 = enabled<br>1 = disabled<br><i>Reset by state machine. Default held in metal mask.</i>  |          |
|                                | 10  | DC3_OPFLT     | 0  | Enable discharge of DC-DC3 outputs when DC-DC3 is disabled<br>0 = Enabled - Output to be discharged<br>1 = Disabled - Output is left floating   |          |
|                                | 6:0 | DC3_VSEL[6:0] | 000_0000<br>010_0110<br>010_1110<br>000_1110 | DC-DC3 Converter output voltage settings in 25mV steps.<br>Maximum output = 3.4V.<br><br>110 0110 = 3.4V<br>110 0010 = 3.3V<br>101 0110 = 3.0V<br>100 1110 = 2.8V<br>.....<br>010 0110 = 1.8V<br>000 1110 = 1.2V<br>000 0110 = 1.0V<br>000 0000 = 0.85V<br><i>Reset by state machine. Default held in metal mask.</i> |          |

Register BAh DCDC3 Control

| REGISTER ADDRESS                | BIT   | LABEL           | DEFAULT                      | DESCRIPTION   | REFER TO |
|---------------------------------|-------|-----------------|------------------------------|---|----------|
| R187 (BBh)<br>DCDC3<br>Timeouts | 15:14 | DC3_ERRACT[1:0] | 00                           | Action to take on DC-DC3 fault (as well as generating an interrupt):<br>00 = ignore<br>01 = shut down converter<br>10 = shut down system<br>11 = reserved (shut down system)<br><i>Reset by state machine. Default held in metal mask.</i>                                    |          |
|                                 | 13:10 | DC3_ENSLOT[3:0] | 0000<br>0001<br>0000<br>0000 | Time slot for DC-DC3 start-up<br>0000 = Disabled (do not start up)<br>0001 = Start-up in time slot 1<br>... (total 14 slots available)<br>1110 = Start-up in time slot 14<br>1111 = Start-up on entering ACTIVE<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                 | 9:6   | DC3_SDSLOT[3:0] | 0000                         | Time slot for DC-DC3 shutdown.<br>0000 = Shut down on entering OFF<br>0001 = Shutdown in time slot 1<br>.... (total 14 slots available)<br>1110 = Shutdown in time slot 14<br>1111 = Shut down on entering OFF  |          |

Register BBh DCDC3 Timeouts

| REGISTER ADDRESS                 | BIT   | LABEL             | DEFAULT  | DESCRIPTION   | REFER TO |
|----------------------------------|-------|-------------------|----------|---|----------|
| R188 (BCh)<br>DCDC3 Low<br>Power | 14:12 | DC3_HIB_MODE[2:0] | 000      | DC-DC3 Hibernate behaviour:<br>000 = Use current settings (no change)<br>001 = Select voltage image settings<br>010 = Force standby mode<br>011 = Force standby mode and voltage image settings.<br>100 = Force LDO mode<br>101 = Force LDO mode and voltage image settings.<br>110 = Reserved.<br>111 = Disable output<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                  | 9:8   | DC3_HIB_TRIG[1:0] | 00       | DC-DC3 Hibernate signal select<br>00 = HIBERNATE register bit<br>01 = L_PWR1<br>10 = L_PWR2<br>11 = L_PWR3<br>Note that Hibernate is also selected when a GPIO Hibernate input is asserted.<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                                  | 6:0   | DC3_VIMG[6:0]     | 000_0110 | DC-DC3 Converter output image voltage settings in 25mv steps.<br>Maximum output = 3.4V.<br><br>110 0110 = 3.4V<br>110 0010 = 3.3V<br>101 0110 = 3.0V  |          |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION   | REFER TO |
|------------------|-----|-------|---------|---|----------|
|                  |     |       |         | 100 1110 = 2.8V<br>.....<br>010 0110 = 1.8V<br>000 1110 = 1.2V<br>000 0110 = 1.0V<br>000 0000 = 0.85V |          |

Register BCh DCDC3 Low Power

| REGISTER ADDRESS               | BIT | LABEL         | DEFAULT                                      | DESCRIPTION   | REFER TO |
|--------------------------------|-----|---------------|--|---|----------|
| R189 (BDh)<br>DCDC4<br>Control | 11  | DC4_DISOVP    | 0  | Over voltage Protection<br>0 = enabled<br>1 = disabled<br><i>Reset by state machine. Default held in metal mask.</i>  |          |
|                                | 10  | DC4_OPFLT     | 0  | Enable discharge of DC-DC4 outputs when DC-DC4 is disabled<br>0 = Enabled - Output to be discharged<br>1 = Disabled - Output is left floating   |          |
|                                | 6:0 | DC4_VSEL[6:0] | 000_0000<br>101_0110<br>000_1110<br>000_0110 | DC-DC4 Converter output voltage settings in 25mV steps.<br>Maximum output = 3.4V.<br><br>110 0110 = 3.4V<br>110 0010 = 3.3V<br>101 0110 = 3.0V<br>100 1110 = 2.8V<br>.....<br>010 0110 = 1.8V<br>000 1110 = 1.2V<br>000 0110 = 1.0V<br>000 0000 = 0.85V<br><i>Reset by state machine. Default held in metal mask.</i> |          |

Register BDh DCDC4 Control

| REGISTER ADDRESS                | BIT   | LABEL           | DEFAULT                      | DESCRIPTION   | REFER TO |
|---------------------------------|-------|-----------------|------------------------------|---|----------|
| R190 (BEh)<br>DCDC4<br>Timeouts | 15:14 | DC4_ERRACT[1:0] | 00                           | Action to take on DC-DC4 fault (as well as generating an interrupt):<br>00 = ignore<br>01 = shut down converter<br>10 = shut down system<br>11 = reserved (shut down system)<br><i>Reset by state machine. Default held in metal mask.</i>                                    |          |
|                                 | 13:10 | DC4_ENSLOT[3:0] | 0000<br>0001<br>0000<br>0011 | Time slot for DC-DC4 start-up<br>0000 = Disabled (do not start up)<br>0001 = Start-up in time slot 1<br>... (total 14 slots available)<br>1110 = Start-up in time slot 14<br>1111 = Start-up on entering ACTIVE<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                 | 9:6   | DC4_SDSLOT[3:0] | 0000                         | Time slot for DC-DC4 shutdown.<br>0000 = Shut down on entering OFF<br>0001 = Shutdown in time slot 1<br>.... (total 14 slots available)<br>1110 = Shutdown in time slot 14<br>1111 = Shut down on entering OFF  |          |

Register BEh DCDC4 Timeouts

| REGISTER ADDRESS                 | BIT   | LABEL             | DEFAULT  | DESCRIPTION   | REFER TO |
|----------------------------------|-------|-------------------|----------|---|----------|
| R191 (BFh)<br>DCDC4 Low<br>Power | 14:12 | DC4_HIB_MODE[2:0] | 000      | DC-DC4 Hibernate behaviour:<br>000 = Use current settings (no change)<br>001 = Select voltage image settings<br>010 = Force standby mode<br>011 = Force standby mode and voltage image settings.<br>100 = Force LDO mode<br>101 = Force LDO mode and voltage image settings.<br>110 = Reserved.<br>111 = Disable output<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                  | 9:8   | DC4_HIB_TRIG[1:0] | 00       | DC-DC4 Hibernate signal select<br>00 = HIBERNATE register bit<br>01 = L_PWR1<br>10 = L_PWR2<br>11 = L_PWR3<br>Note that Hibernate is also selected when a GPIO Hibernate input is asserted.<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                                  | 6:0   | DC4_VIMG[6:0]     | 000_0110 | DC-DC4 Converter output image voltage settings in 25mv steps.<br>Maximum output = 3.4V.<br><br>110 0110 = 3.4V<br>110 0010 = 3.3V   |          |



| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION  | REFER TO |
|------------------|-----|-------|---------|--|----------|
|                  |     |       |         | 101 0110 = 3.0V<br>100 1110 = 2.8V<br>.....<br>010 0110 = 1.8V<br>000 1110 = 1.2V<br>000 0110 = 1.0V<br>000 0000 = 0.85V |          |

Register BFh DCDC4 Low Power

| REGISTER ADDRESS               | BIT | LABEL             | DEFAULT | DESCRIPTION   | REFER TO |
|--------------------------------|-----|-------------------|---------|---|----------|
| R192 (C0h)<br>DCDC5<br>Control | 14  | DC5_MODE          | 0       | DC-DC5 Converter Mode<br>0 = Boost mode<br>1 = Switch mode<br><i>Reset by state machine.</i>  |          |
|                                | 12  | DC5_HIB_MODE      | 0       | DC-DC5 Hibernate behaviour:<br>0 = Continue as in Active state<br>1 = Disable converter output<br><i>Reset by state machine.</i>  |          |
|                                | 9:8 | DC5_HIB_TRIG[1:0] | 00      | DC-DC5 Hibernate signal select<br>00 = HIBERNATE register bit<br>01 = L_PWR1<br>10 = L_PWR2<br>11 = L_PWR3<br>Note that Hibernate is also selected when a GPIO Hibernate input is asserted.<br><i>Reset by state machine.</i>                             |          |
|                                | 6   | DC5_ILIM          | 0       | DC-DC5 peak current limit select<br>0 = Higher peak current<br>1 = Lower peak current<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                                | 4   | DC5_RMPH          | 0       | DC-DC5 compensation ramp<br>{DC5_RMPH, DC5_RMPL}<br>00 = 20V < VOUT ≤ 30V<br>01 = 10V < VOUT ≤ 20V<br>10 = 5V < VOUT ≤ 10V<br>11 = VOUT ≤ 5V (will be chosen automatically if DC5_FBSRC=11)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                | 3   | DC5_RMPL          | 1       | DC-DC5 compensation ramp<br>{DC5_RMPH, DC5_RMPL}<br>00 = 20V < VOUT ≤ 30V<br>01 = 10V < VOUT ≤ 20V<br>10 = 5V < VOUT ≤ 10V<br>11 = VOUT ≤ 5V (will be chosen automatically if DC5_FBSRC=11)<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                | 1:0 | DC5_FBSRC[1:0]    | 00      | DC-DC5 voltage feedback selection<br>00 = voltage feedback (using external resistor divider on pin FB5)<br>01 = current sink ISINKA used as feedback  |          |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION   | REFER TO |
|------------------|-----|-------|---------|---|----------|
|                  |     |       |         | 10 = current sink ISINKB used as feedback<br>11 = voltage feedback (using internal resistor divider on pin USB)<br><i>Reset by state machine. Default held in metal mask.</i> |          |

Register C0h DCDC5 Control

| REGISTER ADDRESS                | BIT   | LABEL           | DEFAULT                      | DESCRIPTION   | REFER TO |
|---------------------------------|-------|-----------------|------------------------------|---|----------|
| R193 (C1h)<br>DCDC5<br>Timeouts | 15:14 | DC5_ERRACT[1:0] | 00                           | Action to take on DC-DC5 fault (as well as generating an interrupt):<br>00 = ignore<br>01 = shut down converter<br>10 = shut down system<br>11 = reserved (shut down system)<br><i>Reset by state machine. Default held in metal mask.</i>                                    |          |
|                                 | 13:10 | DC5_ENSLOT[3:0] | 0000<br>0000<br>0000<br>0000 | Time slot for DC-DC5 start-up<br>0000 = Disabled (do not start up)<br>0001 = Start-up in time slot 1<br>... (total 14 slots available)<br>1110 = Start-up in time slot 14<br>1111 = Start-up on entering ACTIVE<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                 | 9:6   | DC5_SDSLOT[3:0] | 0000                         | Time slot for DC-DC5 shutdown.<br>0000 = Shut down on entering OFF<br>0001 = Shutdown in time slot 1<br>.... (total 14 slots available)<br>1110 = Shutdown in time slot 14<br>1111 = Shut down on entering OFF  |          |

Register C1h DCDC5 Timeouts

| REGISTER ADDRESS               | BIT   | LABEL         | DEFAULT                                      | DESCRIPTION   | REFER TO |
|--------------------------------|-------|---------------|--|---|----------|
| R195 (C3h)<br>DCDC6<br>Control | 15:14 | DC6_CAP[1:0]  | 00   | DC-DC6 Output Capacitor<br>00 = 10uF, 30uF, 45uF<br>01 = 60uF, 85uF<br>10 = Not used<br>11 = 100uF  |          |
|                                | 11    | DC6_DISOVP    | 0  | Over voltage Protection<br>0 = enabled<br>1 = disabled<br><i>Reset by state machine. Default held in metal mask.</i>  |          |
|                                | 10    | DC6_OPFLT     | 0  | Enable discharge of DC-DC6 outputs when DC-DC6 is disabled<br>0 = Enabled - Output to be discharged<br>1 = Disabled - Output is left floating   |          |
|                                | 6:0   | DC6_VSEL[6:0] | 000_0000<br>000_1010<br>010_0110<br>010_0110 | DC-DC6 Converter output voltage settings in 25mV steps.<br>Maximum output = 3.4V.<br><br>110 0110 = 3.4V<br>110 0010 = 3.3V<br>101 0110 = 3.0V<br>100 1110 = 2.8V<br>.....<br>010 0110 = 1.8V<br>000 1110 = 1.2V<br>000 0110 = 1.0V<br>000 0000 = 0.85V<br><i>Reset by state machine. Default held in metal mask.</i> |          |

Register C3h DCDC6 Control

| REGISTER ADDRESS                | BIT   | LABEL           | DEFAULT                      | DESCRIPTION   | REFER TO |
|---------------------------------|-------|-----------------|------------------------------|---|----------|
| R196 (C4h)<br>DCDC6<br>Timeouts | 15:14 | DC6_ERRACT[1:0] | 00                           | Action to take on DC-DC6 fault (as well as generating an interrupt):<br>00 = ignore<br>01 = shut down converter<br>10 = shut down system<br>11 = reserved (shut down system)<br><i>Reset by state machine. Default held in metal mask.</i>                                    |          |
|                                 | 13:10 | DC6_ENSLOT[3:0] | 0000<br>0100<br>0011<br>0001 | Time slot for DC-DC6 start-up<br>0000 = Disabled (do not start up)<br>0001 = Start-up in time slot 1<br>... (total 14 slots available)<br>1110 = Start-up in time slot 14<br>1111 = Start-up on entering ACTIVE<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                 | 9:6   | DC6_SDSLOT[3:0] | 0000                         | Time slot for DC-DC6 shutdown.<br>0000 = Shut down on entering OFF<br>0001 = Shutdown in time slot 1<br>.... (total 14 slots available)<br>1110 = Shutdown in time slot 14  |          |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION                      | REFER TO |
|------------------|-----|-------|---------|----------------------------------|----------|
|                  |     |       |         | 1111 = Shut down on entering OFF |          |

**Register C4h** DCDC6 Timeouts

| REGISTER ADDRESS              | BIT   | LABEL             | DEFAULT  | DESCRIPTION   | REFER TO |
|-------------------------------|-------|-------------------|----------|---|----------|
| R197 (C5h)<br>DCDC6 Low Power | 14:12 | DC6_HIB_MODE[2:0] | 000      | DC-DC6 Hibernate behaviour:<br>000 = Use current settings (no change)<br>001 = Select voltage image settings<br>010 = Force standby mode<br>011 = Force standby mode and voltage image settings.<br>100 = Force LDO mode<br>101 = Force LDO mode and voltage image settings.<br>110 = Reserved.<br>111 = Disable output<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                               | 9:8   | DC6_HIB_TRIG[1:0] | 00       | DC-DC6 Hibernate signal select<br>00 = HIBERNATE register bit<br>01 = L_PWR1<br>10 = L_PWR2<br>11 = L_PWR3<br>Note that Hibernate is also selected when a GPIO Hibernate input is asserted.<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                               | 6:0   | DC6_VIMG[6:0]     | 000_0110 | DC-DC6 Converter output image voltage settings in 25mv steps.<br>Maximum output = 3.4V.<br><br>110 0110 = 3.4V<br>110 0010 = 3.3V<br>101 0110 = 3.0V<br>100 1110 = 2.8V<br>.....<br>010 0110 = 1.8V<br>000 1110 = 1.2V<br>000 0110 = 1.0V<br>000 0000 = 0.85V   |          |

**Register C5h** DCDC6 Low Power

| REGISTER ADDRESS                   | BIT   | LABEL          | DEFAULT | DESCRIPTION   | REFER TO |
|------------------------------------|-------|----------------|---------|---|----------|
| R199 (C7h)<br>Limit Switch Control | 15:14 | LS_ERRACT[1:0] | 00      | Current limit detection behaviour<br>00 = ignore<br>01 = disable switch<br>10 = shut down system<br>11 = shut down system<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                                    | 13:10 | LS_ENSLOT[3:0] | 0000    | Time slot for Limit Switch start-up<br>0000 = Disabled (do not start up)<br>0001 = Start-up in time slot 1<br>... (total 14 slots available)<br>1110 = Start-up in time slot 14<br>1111 = Start-up on entering ACTIVE<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                    | 9:6   | LS_SDSLOT[3:0] | 0000    | Time slot for Limit Switch shutdown.<br>0000 = Shut down on entering OFF<br>0001 = Shutdown in time slot 1<br>.... (total 14 slots available)<br>1110 = Shutdown in time slot 14<br>1111 = Shut down on entering OFF  |          |
|                                    | 4     | LS_HIB_MODE    | 0       | Limit switch hibernate mode setting<br>0 = disabled<br>1 = leave setting as in Active mode  |          |
|                                    | 1     | LS_HIB_PROT    | 1       | Controls the bulk detection circuit when Limit Switch is disabled in Hibernate mode.<br>0 = bulk detection disabled<br>1 = bulk detection enabled   |          |
|                                    | 0     | LS_PROT        | 1       | Controls the bulk detection circuit when Limit Switch is disabled in Active mode.<br>0 = bulk detection disabled<br>1 = bulk detection enabled  |          |

Register C7h Limit Switch Control

| REGISTER ADDRESS           | BIT | LABEL          | DEFAULT                              | DESCRIPTION   | REFER TO |
|----------------------------|-----|----------------|--------------------------------------|---|----------|
| R200 (C8h)<br>LDO1 Control | 14  | LDO1_SWI       | 0                                    | LDO1 Regulator mode<br>0 = LDO voltage regulator<br>1 = Current-limited switch (no voltage regulation, LDO1_VSEL has no effect)<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                            | 10  | LDO1_OPFLT     | 0                                    | Enable discharge of LDO1 outputs when LDO1 is disabled<br>0 = Enabled - Output to be discharged<br>1 = Disabled - Output is left floating<br>Note - if LDO Regulators 1, 2, 3 and 4 are all disabled, then the outputs will all be discharged, regardless of the LDO <sub>n</sub> _OPFLT bit. |          |
|                            | 4:0 | LDO1_VSEL[4:0] | 1_1100<br>0_0010<br>1_1100<br>0_0010 | LDO1 Regulator output voltage (when LDO1_SWI=0)<br>1 1111 = 3.3V<br>... (100mV steps)<br>1 0000 = 1.8V<br>0 1111 = 1.65V<br>... (50mV steps)  |          |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION   | REFER TO |
|------------------|-----|-------|---------|---|----------|
|                  |     |       |         | 0 0000 = 0.9V<br><i>Reset by state machine. Default held in metal mask.</i> |          |

**Register C8h** LDO1 Control

| REGISTER ADDRESS               | BIT   | LABEL            | DEFAULT                      | DESCRIPTION   | REFER TO |
|--------------------------------|-------|------------------|------------------------------|---|----------|
| R201 (C9h)<br>LDO1<br>Timeouts | 15:14 | LDO1_ERRACT[1:0] | 00                           | Action to take on LDO1 fault (as well as generating an interrupt):<br>00 = ignore<br>01 = shut down regulator<br>10 = shut down system<br>11 = reserved (shut down system)<br><i>Reset by state machine. Default held in metal mask.</i>                                    |          |
|                                | 13:10 | LDO1_ENSLOT[3:0] | 0000<br>0011<br>0000<br>0000 | Time slot for LDO1 start-up<br>0000 = Disabled (do not start up)<br>0001 = Start-up in time slot 1<br>... (total 14 slots available)<br>1110 = Start-up in time slot 14<br>1111 = Start up on entering ACTIVE<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                | 9:6   | LDO1_SDSLOT[3:0] | 0000                         | Time slot for LDO1 shutdown.<br>0000 = Shut down on entering OFF<br>0001 = Shutdown in time slot 1<br>.... (total 14 slots available)<br>1110 = Shutdown in time slot 14<br>1111 = Shut down on entering OFF  |          |

**Register C9h** LDO1 Timeouts

| REGISTER ADDRESS                | BIT   | LABEL              | DEFAULT | DESCRIPTION  | REFER TO |
|---------------------------------|-------|--------------------|---------|--|----------|
| R202 (CAh)<br>LDO1 Low<br>Power | 13:12 | LDO1_HIB_MODE[1:0] | 00      | LDO1 Hibernate behaviour:<br>00 = Select voltage image settings<br>01 = disable output<br>10 = reserved<br>11 = reserved<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                 | 9:8   | LDO1_HIB_TRIG[1:0] | 00      | LDO1 Hibernate signal select<br>00 = Hibernate register bit<br>01 = L_PWR1<br>10 = L_PWR2<br>11 = L_PWR3<br><i>Reset by state machine. Default held in metal mask.</i>                 |          |
|                                 | 4:0   | LDO1_VIMG[4:0]     | 1_1100  | LDO1 Regulator output image voltage<br><br>1 1111 = 3.3V<br>... (100mV steps)<br>1 0000 = 1.8V<br>0 1111 = 1.65V<br>... (50mV steps)   |          |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION   | REFER TO |
|------------------|-----|-------|---------|---------------|----------|
|                  |     |       |         | 0 0000 = 0.9V |          |

**Register CAh** LDO1 Low Power

| REGISTER ADDRESS              | BIT | LABEL          | DEFAULT                              | DESCRIPTION   | REFER TO |
|-------------------------------|-----|----------------|--------------------------------------|---|----------|
| R203 (CBh)<br>LDO2<br>Control | 14  | LDO2_SWI       | 0                                    | LDO2 Regulator mode<br>0 = LDO voltage regulator<br>1 = Current-limited switch (no voltage regulation, LDO2_VSEL has no effect)<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                               | 10  | LDO2_OPFLT     | 0                                    | Enable discharge of LDO2 outputs when LDO2 is disabled<br>0 = Enabled - Output to be discharged<br>1 = Disabled - Output is left floating<br>Note - if LDO Regulators 1, 2, 3 and 4 are all disabled, then the outputs will all be discharged, regardless of the LDO <sub>n</sub> _OPFLT bit. |          |
|                               | 4:0 | LDO2_VSEL[4:0] | 1_1011<br>1_1111<br>1_0000<br>1_1010 | LDO2 Regulator output voltage (when LDO2_SWI=0)<br><br>1 1111 = 3.3V<br>... (100mV steps)<br>1 0000 = 1.8V<br>0 1111 = 1.65V<br>... (50mV steps)<br>0 0000 = 0.9V<br><i>Reset by state machine. Default held in metal mask.</i>   |          |

**Register CBh** LDO2 Control

| REGISTER ADDRESS               | BIT   | LABEL            | DEFAULT                      | DESCRIPTION   | REFER TO |
|--------------------------------|-------|------------------|------------------------------|---|----------|
| R204 (CCh)<br>LDO2<br>Timeouts | 15:14 | LDO2_ERRACT[1:0] | 00                           | Action to take on LDO2 fault (as well as generating an interrupt):<br>00 = ignore<br>01 = shut down regulator<br>10 = shut down system<br>11 = reserved (shut down system)<br><i>Reset by state machine. Default held in metal mask.</i>                                    |          |
|                                | 13:10 | LDO2_ENSLOT[3:0] | 0000<br>0010<br>0010<br>0000 | Time slot for LDO2 start-up<br>0000 = Disabled (do not start up)<br>0001 = Start-up in time slot 1<br>... (total 14 slots available)<br>1110 = Start-up in time slot 14<br>1111 = Start up on entering ACTIVE<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                | 9:6   | LDO2_SDSLOT[3:0] | 0000                         | Time slot for LDO2 shutdown.<br>0000 = Shut down on entering OFF<br>0001 = Shutdown in time slot 1<br>.... (total 14 slots available)<br>1110 = Shutdown in time slot 14<br>1111 = Shut down on entering OFF  |          |

**Register CCh** LDO2 Timeouts

| REGISTER ADDRESS             | BIT   | LABEL              | DEFAULT | DESCRIPTION  | REFER TO |
|------------------------------|-------|--------------------|---------|--|----------|
| R205 (CDh)<br>LDO2 Low Power | 13:12 | LDO2_HIB_MODE[1:0] | 00      | LDO2 Hibernate behaviour:<br>00 = Select voltage image settings<br>01 = disable output<br>10 = reserved<br>11 = reserved<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                              | 9:8   | LDO2_HIB_TRIG[1:0] | 00      | LDO2 Hibernate signal select<br>00 = Hibernate register bit<br>01 = L_PWR1<br>10 = L_PWR2<br>11 = L_PWR3<br><i>Reset by state machine. Default held in metal mask.</i>                 |          |
|                              | 4:0   | LDO2_VIMG[4:0]     | 1_1100  | LDO2 Regulator output image voltage<br><br>1 1111 = 3.3V<br>... (100mV steps)<br>1 0000 = 1.8V<br>0 1111 = 1.65V<br>... (50mV steps)<br>0 0000 = 0.9V                                  |          |

Register CDh LDO2 Low Power

| REGISTER ADDRESS           | BIT | LABEL          | DEFAULT                              | DESCRIPTION   | REFER TO |
|----------------------------|-----|----------------|--------------------------------------|---|----------|
| R206 (CEh)<br>LDO3 Control | 14  | LDO3_SWI       | 0                                    | LDO3 Regulator mode<br>0 = LDO voltage regulator<br>1 = Current-limited switch (no voltage regulation, LDO3_VSEL has no effect)<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                            | 10  | LDO3_OPFLT     | 0                                    | Enable discharge of LDO3 outputs when LDO3 is disabled<br>0 = Enabled - Output to be discharged<br>1 = Disabled - Output is left floating<br>Note - if LDO Regulators 1, 2, 3 and 4 are all disabled, then the outputs will all be discharged, regardless of the LDO <sub>n</sub> _OPFLT bit. |          |
|                            | 4:0 | LDO3_VSEL[4:0] | 1_1011<br>1_1100<br>1_0101<br>1_1111 | LDO3 Regulator output voltage (when LDO3_SWI=0)<br><br>1 1111 = 3.3V<br>... (100mV steps)<br>1 0000 = 1.8V<br>0 1111 = 1.65V<br>... (50mV steps)<br>0 0000 = 0.9V<br><i>Reset by state machine. Default held in metal mask.</i>   |          |

Register CEh LDO3 Control



| REGISTER ADDRESS               | BIT   | LABEL            | DEFAULT                      | DESCRIPTION   | REFER TO |
|--------------------------------|-------|------------------|------------------------------|---|----------|
| R207 (CFh)<br>LDO3<br>Timeouts | 15:14 | LDO3_ERRACT[1:0] | 00                           | Action to take on LDO3 fault (as well as generating an interrupt):<br>00 = ignore<br>01 = shut down regulator<br>10 = shut down system<br>11 = reserved (shut down system)<br><i>Reset by state machine. Default held in metal mask.</i>                                    |          |
|                                | 13:10 | LDO3_ENSLOT[3:0] | 0000<br>0001<br>0000<br>0000 | Time slot for LDO3 start-up<br>0000 = Disabled (do not start up)<br>0001 = Start-up in time slot 1<br>... (total 14 slots available)<br>1110 = Start-up in time slot 14<br>1111 = Start up on entering ACTIVE<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                | 9:6   | LDO3_SDSLOT[3:0] | 0000                         | Time slot for LDO3 shutdown.<br>0000 = Shut down on entering OFF<br>0001 = Shutdown in time slot 1<br>.... (total 14 slots available)<br>1110 = Shutdown in time slot 14<br>1111 = Shut down on entering OFF  |          |

Register CFh LDO3 Timeouts

| REGISTER ADDRESS                | BIT   | LABEL              | DEFAULT | DESCRIPTION  | REFER TO |
|---------------------------------|-------|--------------------|---------|--|----------|
| R208 (D0h)<br>LDO3 Low<br>Power | 13:12 | LDO3_HIB_MODE[1:0] | 00      | LDO3 Hibernate behaviour:<br>00 = Select voltage image settings<br>01 = disable output<br>10 = reserved<br>11 = reserved<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                 | 9:8   | LDO3_HIB_TRIG[1:0] | 00      | LDO3 Hibernate signal select<br>00 = Hibernate register bit<br>01 = L_PWR1<br>10 = L_PWR2<br>11 = L_PWR3<br><i>Reset by state machine. Default held in metal mask.</i>                 |          |
|                                 | 4:0   | LDO3_VIMG[4:0]     | 1_1100  | LDO3 Regulator output image voltage<br><br>1 1111 = 3.3V<br>... (100mV steps)<br>1 0000 = 1.8V<br>0 1111 = 1.65V<br>... (50mV steps)<br>0 0000 = 0.9V                                  |          |

Register D0h LDO3 Low Power

| REGISTER ADDRESS              | BIT | LABEL          | DEFAULT                              | DESCRIPTION   | REFER TO |
|-------------------------------|-----|----------------|--------------------------------------|---|----------|
| R209 (D1h)<br>LDO4<br>Control | 14  | LDO4_SWI       | 0                                    | LDO4 Regulator mode<br>0 = LDO voltage regulator<br>1 = Current-limited switch (no voltage regulation, LDO4_VSEL has no effect)<br><i>Reset by state machine. Default held in metal mask.</i>   |          |
|                               | 10  | LDO4_OPFLT     | 0                                    | Enable discharge of LDO4 outputs when LDO4 is disabled<br>0 = Enabled - Output to be discharged<br>1 = Disabled - Output is left floating<br>Note - if LDO Regulators 1, 2, 3 and 4 are all disabled, then the outputs will all be discharged, regardless of the LDO <sub>n</sub> _OPFLT bit. |          |
|                               | 4:0 | LDO4_VSEL[4:0] | 1_1011<br>0_0100<br>1_1010<br>1_1111 | LDO4 Regulator output voltage (when LDO4_SWI=0)<br><br>1 1111 = 3.3V<br>... (100mV steps)<br>1 0000 = 1.8V<br>0 1111 = 1.65V<br>... (50mV steps)<br>0 0000 = 0.9V<br><i>Reset by state machine. Default held in metal mask.</i>   |          |

Register D1h LDO4 Control

| REGISTER ADDRESS               | BIT   | LABEL            | DEFAULT                      | DESCRIPTION   | REFER TO |
|--------------------------------|-------|------------------|------------------------------|---|----------|
| R210 (D2h)<br>LDO4<br>Timeouts | 15:14 | LDO4_ERRACT[1:0] | 00                           | Action to take on LDO4 fault (as well as generating an interrupt):<br>00 = ignore<br>01 = shut down regulator<br>10 = shut down system<br>11 = reserved (shut down system)<br><i>Reset by state machine. Default held in metal mask.</i>                                    |          |
|                                | 13:10 | LDO4_ENSLOT[3:0] | 0000<br>0010<br>0000<br>0000 | Time slot for LDO4 start-up<br>0000 = Disabled (do not start up)<br>0001 = Start-up in time slot 1<br>... (total 14 slots available)<br>1110 = Start-up in time slot 14<br>1111 = Start up on entering ACTIVE<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                                | 9:6   | LDO4_SDSLOT[3:0] | 0000                         | Time slot for LDO4 shutdown.<br>0000 = Shut down on entering OFF<br>0001 = Shutdown in time slot 1<br>.... (total 14 slots available)<br>1110 = Shutdown in time slot 14<br>1111 = Shut down on entering OFF  |          |

Register D2h LDO4 Timeouts

| REGISTER ADDRESS             | BIT   | LABEL              | DEFAULT | DESCRIPTION  | REFER TO |
|------------------------------|-------|--------------------|---------|--|----------|
| R211 (D3h)<br>LDO4 Low Power | 13:12 | LDO4_HIB_MODE[1:0] | 00      | LDO4 Hibernate behaviour:<br>00 = Select voltage image settings<br>01 = disable output<br>10 = reserved<br>11 = reserved<br><i>Reset by state machine. Default held in metal mask.</i> |          |
|                              | 9:8   | LDO4_HIB_TRIG[1:0] | 00      | LDO4 Hibernate signal select<br>00 = Hibernate register bit<br>01 = L_PWR1<br>10 = L_PWR2<br>11 = L_PWR3<br><i>Reset by state machine. Default held in metal mask.</i>                 |          |
|                              | 4:0   | LDO4_VIMG[4:0]     | 1_1100  | LDO4 Regulator output image voltage<br><br>1 1111 = 3.3V<br>... (100mV steps)<br>1 0000 = 1.8V<br>0 1111 = 1.65V<br>... (50mV steps)<br>0 0000 = 0.9V                                  |          |

Register D3h LDO4 Low Power

| REGISTER ADDRESS              | BIT | LABEL      | DEFAULT | DESCRIPTION  | REFER TO |
|-------------------------------|-----|------------|---------|--|----------|
| R215 (D7h)<br>VCC_FAULT Masks | 15  | LS_FAULT   | 0       | Limit Switch fault mask for the /VCC_FAULT<br>0 = 'on't mask converter fault<br>1 = mask converter fault<br><i>Reset by state machine.</i> |          |
|                               | 11  | LDO4_FAULT | 0       | LDO4 fault mask for the /VCC_FAULT<br>0 = 'on't mask converter fault<br>1 = mask converter fault<br><i>Reset by state machine.</i>         |          |
|                               | 10  | LDO3_FAULT | 0       | LDO3 fault mask for the /VCC_FAULT<br>0 = 'on't mask converter fault<br>1 = mask converter fault<br><i>Reset by state machine.</i>         |          |
|                               | 9   | LDO2_FAULT | 0       | LDO2 fault mask for the /VCC_FAULT<br>0 = 'on't mask converter fault<br>1 = mask converter fault<br><i>Reset by state machine.</i>         |          |
|                               | 8   | LDO1_FAULT | 0       | LDO1 fault mask for the /VCC_FAULT<br>0 = 'on't mask converter fault<br>1 = mask converter fault<br><i>Reset by state machine.</i>         |          |
|                               | 5   | DC6_FAULT  | 0       | DCDC6 fault mask for the /VCC_FAULT<br>0 = 'on't mask converter fault<br>1 = mask converter fault<br><i>Reset by state machine.</i>        |          |
|                               | 4   | DC5_FAULT  | 0       | DCDC5 fault mask for the /VCC_FAULT<br>0 = 'on't mask converter fault  |          |

| REGISTER ADDRESS | BIT | LABEL     | DEFAULT | DESCRIPTION   | REFER TO |
|------------------|-----|-----------|---------|---|----------|
|                  |     |           |         | 1 = mask converter fault<br><i>Reset by state machine.</i>  |          |
|                  | 3   | DC4_FAULT | 0       | DCDC4 fault mask for the /VCC_FAULT<br>0 = 'on't mask converter fault<br>1 = mask converter fault<br><i>Reset by state machine.</i> |          |
|                  | 2   | DC3_FAULT | 0       | DCDC3 fault mask for the /VCC_FAULT<br>0 = 'on't mask converter fault<br>1 = mask converter fault<br><i>Reset by state machine.</i> |          |
|                  | 1   | DC2_FAULT | 0       | DCDC2 fault mask for the /VCC_FAULT<br>0 = 'on't mask converter fault<br>1 = mask converter fault<br><i>Reset by state machine.</i> |          |
|                  | 0   | DC1_FAULT | 0       | DCDC1 fault mask for the /VCC_FAULT<br>0 = 'on't mask converter fault<br>1 = mask converter fault<br><i>Reset by state machine.</i> |          |

Register D7h VCC\_FAULT Masks

| REGISTER ADDRESS                         | BIT | LABEL          | DEFAULT | DESCRIPTION   | REFER TO |
|--|-----|----------------|---------|---|----------|
| R216 (D8h)<br>Main<br>Bandgap<br>Control | 15  | MBG_LOAD_FUSES | 0       | Enables the current to the bandgap trim fuses.<br>This must be set to 1 when writing the fuses. To<br>read the trim value held in the fuse, this bit must<br>be set and then reset. |          |

Register D8h Main Bandgap Control

| REGISTER ADDRESS          | BIT | LABEL          | DEFAULT | DESCRIPTION   | REFER TO |
|---------------------------|-----|----------------|---------|---|----------|
| R217 (D9h)<br>OSC Control | 15  | OSC_LOAD_FUSES | 0       | Enables the current to the bandgap trim fuses.<br>This must be set to 1 when writing the fuses. To<br>read the trim value, this bit must be set and then<br>reset.<br><i>Protected by security key.</i> |          |

Register D9h OSC Control

| REGISTER ADDRESS               | BIT | LABEL         | DEFAULT          | DESCRIPTION  | REFER TO |
|--------------------------------|-----|---------------|------------------|--|----------|
| R218 (DAh)<br>RTC Tick Control | 15  | RTC_TICK_ENA  | 1<br>1<br>1<br>1 | Enable RTC counting (instruction only)<br>0 = disabled<br>1 = enabled<br><i>Protected by security key. Reset by state machine. Default held in metal mask.</i>   |          |
|                                | 14  | RTC_TICKSTS   | 0                | Status of tick request. This bit can be used to ensure the RTC is using the value of RTC_TICK_ENA.<br>0 = disabled<br>1 = enabled<br><i>Protected by security key.</i>   |          |
|                                | 13  | RTC_CLKSRC    | 0<br>0<br>0<br>0 | RTC 32Khz clock source.<br>0 = take 32Khz from 32K OSC<br>1 = take 32Khz from GPIOx (Alternative GPIO function)<br><i>Protected by security key. Reset by state machine. Default held in metal mask.</i>   |          |
|                                | 12  | OSC32K_ENA    | 1<br>1<br>1<br>1 | On chip 32Khz OSC enable<br>0 = disable<br>1 = enable<br><i>Protected by security key. Reset by state machine. Default held in metal mask.</i>   |          |
|                                | 9:0 | RTC_TRIM[9:0] | 00_0000_0000     | RTC frequency trim. Used to adjust the count value of the Tick Gen block to compensate for crystal inaccuracies. RTC frequency trim is a 10bit fixed point <4,6' 2's complement number. MSB Scaling = -8Hz. The register indicates the error (in Hz) with respect to the ideal 32768Hz) of the input crystal frequency. e.g.:<br><br>Actual crystal freq: 32769.00Hz: Required trim 0xb0001_000000 (+1.000000)<br>Actual crystal freq: 32767.00Hz: Required trim 0xb1111_000000 (-1.000000)<br>Actual crystal freq: 32775.58Hz: Required trim 0xb0111_100101 (+7.578125)<br>Actual crystal freq: 32763.78Hz: Required trim 0xb1011_110010 (-4.218750)<br><i>Protected by security key.</i> |          |

Register DAh RTC Tick Control

| REGISTER ADDRESS        | BIT  | LABEL          | DEFAULT             | DESCRIPTION  | REFER TO |
|-------------------------|------|----------------|---------------------|--|----------|
| R219 (DBh)<br>Security1 | 15:0 | SECURITY[15:0] | 0000_0000_0000_0000 | The value 0013h needs to be set in this register to allow write access to the security locked registers.<br><i>Reset by state machine.</i> |          |

Register DBh Security1

| REGISTER ADDRESS               | BIT | LABEL                 | DEFAULT | DESCRIPTION   | REFER TO |
|--------------------------------|-----|-----------------------|---------|---|----------|
| R224 (E0h)<br>Signal overrides | 11  | WALL_FB_GT_BATT_OVRDE | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                                | 10  | USB_FB_GT_BATT_OVRDE  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                                | 9   | FLL_OK_OVRDE          | 0       | 0 = normal operation<br>1 = Overrides the FLL_OK  |          |
|                                | 8   | DEB_TICK_OVRDE        | 0       | Overrides the ticks in the debounce block<br>0 = normal<br>1 = All ticks are overwritten with 16KHz ticks                                     |          |
|                                | 7   | UVLO_B_OVRDE          | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                                | 6   | RTC_ALARM_OVRDE       | 0       | Override for RTC_ALARM signal<br>0 = normal<br>1 = Alarm = 1  |          |
|                                | 3   | LINE_GT_BATT_OVRDE    | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                                | 2   | LINE_GT_VRTC_OVRDE    | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                                | 1   | USB_GT_LINE_OVRDE     | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                                | 0   | BATT_GT_USB_OVRDE     | 0       | [No description available]  |          |

Register E0h Signal overrides

| REGISTER ADDRESS                 | BIT | LABEL    | DEFAULT | DESCRIPTION   | REFER TO |
|----------------------------------|-----|----------|---------|---|----------|
| R225 (E1h)<br>DCDC/LDO<br>status | 15  | LS_STS   | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.<br><i>Reset by state machine.</i> |          |
|                                  | 11  | LDO4_STS | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.<br><i>Reset by state machine.</i> |          |
|                                  | 10  | LDO3_STS | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.<br><i>Reset by state machine.</i> |          |
|                                  | 9   | LDO2_STS | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.<br><i>Reset by state machine.</i> |          |
|                                  | 8   | LDO1_STS | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.<br><i>Reset by state machine.</i> |          |
|                                  | 5   | DC6_STS  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.<br><i>Reset by state machine.</i> |          |
|                                  | 4   | DC5_STS  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.<br><i>Reset by state machine.</i> |          |
|                                  | 3   | DC4_STS  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.<br><i>Reset by state machine.</i> |          |
|                                  | 2   | DC3_STS  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.<br><i>Reset by state machine.</i> |          |
|                                  | 1   | DC2_STS  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.<br><i>Reset by state machine.</i> |          |
|                                  | 0   | DC1_STS  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1.<br><i>Reset by state machine.</i> |          |

Register E1h DCDC/LDO status

| REGISTER ADDRESS                          | BIT | LABEL                  | DEFAULT | DESCRIPTION   | REFER TO |
|---|-----|------------------------|---------|---|----------|
| R226 (E2h)<br>Charger<br>Overrides/status | 15  | CHG_BATT_HOT_OVRDE     | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|   | 14  | CHG_BATT_COLD_OVRDE    | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|   | 11  | CHG_END_OVRDE          | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|   | 2   | CHG_BATT_LT_3P9_OVRDE  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|   | 1   | CHG_BATT_LT_3P1_OVRDE  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|   | 0   | CHG_BATT_LT_2P85_OVRDE | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |

Register E2h Charger Overrides/status

| REGISTER ADDRESS                | BIT | LABEL             | DEFAULT | DESCRIPTION   | REFER TO |
|---------------------------------|-----|-------------------|---------|---|----------|
| R227 (E3h)<br>misc<br>overrides | 13  | CS2_NOT_REG_OVRDE | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                                 | 12  | CS1_NOT_REG_OVRDE | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                                 | 10  | USB_LIMIT_OVRDE   | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                                 | 7   | AUX_DCOMP4_OVRDE  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                                 | 6   | AUX_DCOMP3_OVRDE  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                                 | 5   | AUX_DCOMP2_OVRDE  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                                 | 4   | AUX_DCOMP1_OVRDE  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |



| REGISTER ADDRESS | BIT | LABEL              | DEFAULT | DESCRIPTION   | REFER TO |
|------------------|-----|--------------------|---------|---|----------|
|                  | 3   | HYST_UVLO_OK_OVRDE | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                  | 2   | CHIP_GT115_OVRDE   | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                  | 1   | CHIP_GT140_OVRDE   | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |

Register E3h misc overrides

| REGISTER ADDRESS                              | BIT | LABEL          | DEFAULT | DESCRIPTION   | REFER TO |
|---|-----|----------------|---------|---|----------|
| R228 (E4h)<br>Supply<br>overrides/status<br>1 | 5   | OVRV_DC6_OVRDE | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the CONVERTER_OV_OVRDE bit is set to 1. |          |
|   | 3   | OVRV_DC4_OVRDE | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the CONVERTER_OV_OVRDE bit is set to 1. |          |
|   | 2   | OVRV_DC3_OVRDE | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the CONVERTER_OV_OVRDE bit is set to 1. |          |
|   | 0   | OVRV_DC1_OVRDE | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the CONVERTER_OV_OVRDE bit is set to 1. |          |

Register E4h Supply overrides/status 1

| REGISTER ADDRESS                        | BIT | LABEL           | DEFAULT | DESCRIPTION   | REFER TO |
|---|-----|-----------------|---------|---|----------|
| R229 (E5h)<br>Supply overrides/status 2 | 15  | OVCR_LS_OVRDE   | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the CONVERTER_OC_OVRDE bit is set to 1. |          |
|   | 11  | UNDV_LDO4_OVRDE | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the CONVERTER_UV_OVRDE bit is set to 1. |          |
|   | 10  | UNDV_LDO3_OVRDE | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the CONVERTER_UV_OVRDE bit is set to 1. |          |
|   | 9   | UNDV_LDO2_OVRDE | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the CONVERTER_UV_OVRDE bit is set to 1. |          |
|   | 8   | UNDV_LDO1_OVRDE | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the CONVERTER_UV_OVRDE bit is set to 1. |          |
|   | 5   | UNDV_DC6_OVRDE  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the CONVERTER_UV_OVRDE bit is set to 1. |          |
|   | 4   | UNDV_DC5_OVRDE  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the CONVERTER_UV_OVRDE bit is set to 1. |          |
|   | 3   | UNDV_DC4_OVRDE  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the CONVERTER_UV_OVRDE bit is set to 1. |          |
|   | 2   | UNDV_DC3_OVRDE  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the CONVERTER_UV_OVRDE bit is set to 1. |          |
|   | 1   | UNDV_DC2_OVRDE  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the CONVERTER_UV_OVRDE bit is set to 1. |          |
|   | 0   | UNDV_DC1_OVRDE  | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the CONVERTER_UV_OVRDE bit is set to 1. |          |

Register E5h Supply overrides/status 2

| REGISTER ADDRESS                 | BIT     | LABEL    | DEFAULT  | DESCRIPTION   | REFER TO |
|----------------------------------|---------|----------|--|---|----------|
| R230 (E6h)<br>GPIO Pin<br>Status | 15      | 1        | 1  | Unused<br><i>Never reset.</i>   |          |
|                                  | 14      | 1        | 1  | Unused<br><i>Never reset.</i>   |          |
|                                  | 13      | 1        | 1  | Unused<br><i>Never reset.</i>   |          |
|                                  | 12      | GP12_LVL | 0  | Logic level of GPIO12 pin<br>Input-<br>Reads the logic level of GPIO pin<br>Writing '0' clears GP12_EINT<br><br>Output-<br>Write sets the value to drive the GPIO pin |          |
|                                  | 11      | GP11_LVL | 0  | Logic level of GPIO11 pin<br>Input-<br>Reads the logic level of GPIO pin<br>Writing '0' clears GP11_EINT<br><br>Output-<br>Write sets the value to drive the GPIO pin |          |
|                                  | 10      | GP10_LVL | 0  | Logic level of GPIO10 pin<br>Input-<br>Reads the logic level of GPIO pin<br>Writing '0' clears GP10_EINT<br><br>Output-<br>Write sets the value to drive the GPIO pin |          |
|                                  | 9       | GP9_LVL  | 0  | Logic level of GPIO9 pin<br>Input-<br>Reads the logic level of GPIO pin<br>Writing '0' clears GP9_EINT<br><br>Output-<br>Write sets the value to drive the GPIO pin   |          |
|                                  | 8       | GP8_LVL  | 0  | Logic level of GPIO8 pin<br>Input-<br>Reads the logic level of GPIO pin<br>Writing '0' clears GP8_EINT<br><br>Output-<br>Write sets the value to drive the GPIO pin   |          |
|                                  | 7       | GP7_LVL  | 0  | Logic level of GPIO7 pin<br>Input-<br>Reads the logic level of GPIO pin<br>Writing '0' clears GP7_EINT<br><br>Output-<br>Write sets the value to drive the GPIO pin   |          |
| 6                                | GP6_LVL | 0        | Logic level of GPIO6 pin<br>Input-<br>Reads the logic level of GPIO pin<br>Writing '0' clears GP6_EINT |   |          |

| REGISTER ADDRESS | BIT | LABEL   | DEFAULT | DESCRIPTION   | REFER TO |
|------------------|-----|---------|---------|---|----------|
|                  |     |         |         | Output-<br>Write sets the value to drive the GPIO pin   |          |
|                  | 5   | GP5_LVL | 0       | Logic level of GPIO5 pin<br>Input-<br>Reads the logic level of GPIO pin<br>Writing '0' clears GP5_EINT<br><br>Output-<br>Write sets the value to drive the GPIO pin |          |
|                  | 4   | GP4_LVL | 0       | Logic level of GPIO4 pin<br>Input-<br>Reads the logic level of GPIO pin<br>Writing '0' clears GP4_EINT<br><br>Output-<br>Write sets the value to drive the GPIO pin |          |
|                  | 3   | GP3_LVL | 0       | Logic level of GPIO3 pin<br>Input-<br>Reads the logic level of GPIO pin<br>Writing '0' clears GP3_EINT<br><br>Output-<br>Write sets the value to drive the GPIO pin |          |
|                  | 2   | GP2_LVL | 0       | Logic level of GPIO2 pin<br>Input-<br>Reads the logic level of GPIO pin<br>Writing '0' clears GP2_EINT<br><br>Output-<br>Write sets the value to drive the GPIO pin |          |
|                  | 1   | GP1_LVL | 0       | Logic level of GPIO1 pin<br>Input-<br>Reads the logic level of GPIO pin<br>Writing '0' clears GP1_EINT<br><br>Output-<br>Write sets the value to drive the GPIO pin |          |
|                  | 0   | GP0_LVL | 0       | Logic level of GPIO0 pin<br>Input-<br>Reads the logic level of GPIO pin<br>Writing '0' clears GP0_EINT<br><br>Output-<br>Write sets the value to drive the GPIO pin |          |

Register E6h GPIO Pin Status

| REGISTER ADDRESS                   | BIT | LABEL                 | DEFAULT | DESCRIPTION   | REFER TO |
|------------------------------------|-----|-----------------------|---------|---|----------|
| R231 (E7h)<br>comparator overrides | 15  | USB_FB_OVRDE          | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                                    | 14  | WALL_FB_OVRDE         | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                                    | 13  | BATT_FB_OVRDE         | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                                    | 11  | CODEC_JCK_DET_L_OVRDE | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                                    | 10  | CODEC_JCK_DET_R_OVRDE | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                                    | 9   | CODEC_MICSCD_OVRDE    | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |
|                                    | 8   | CODEC_MICD_OVRDE      | 0       | Readback of the raw signal value.<br>Allow direct control of this sig'al's input to the debounce logic when the ANALOG_OVRDE bit is set to 1. |          |

Register E7h comparator overrides

| REGISTER ADDRESS                   | BIT  | LABEL        | DEFAULT | DESCRIPTION   | REFER TO |
|------------------------------------|------|--------------|---------|---|----------|
| R233 (E9h)<br>State Machine status | 10:8 | USB_SM[2:0]  | 000     | Readback tell you what state the USB state machine is in. This is useful for debugging your setup.<br>0001 = 100mA Slave<br>0101 = 500mA Slave<br>0100 = Suspend<br>0010 = Master Line<br>0110 = Master DCDC  |          |
|                                    | 6:4  | CHG_SM[2:0]  | 000     | Readback tell you what state the Charger state machine is in. This is useful for debugging your setup.<br>0000 = OFF<br>0001 = TRICKLE<br>0010 = TRICKLE_CHOKE<br>0011 = TRICKLE_OVERTEMP<br>0100 = FAST<br>0110 = FAST_CHOKE<br>0101 = FAST_OVERTEMP |          |
|                                    | 3:0  | MAIN_SM[3:0] | 0000    | Readback tell you what state the MAIN state machine is in. This is useful for debugging your setup.<br>0010 = OFF<br>1101 = PRE-ACTIVE<br>1100 = HIBERNATE<br>1111 = ACTIVE   |          |

Register E9h State Machine status

| REGISTER ADDRESS                  | BIT | LABEL         | DEFAULT | DESCRIPTION   | REFER TO |
|-----------------------------------|-----|---------------|---------|---|----------|
| R248 (F8h)<br>DCDC1 Test Controls | 4   | DC1_FORCE_PWM | 0       | Force DC-DC1 PWM mode<br>0 = Normal DC-DC operation<br>1 = Force DC-DC PWM mode<br><i>Reset by state machine.</i> |          |

Register F8h DCDC1 Test Controls

| REGISTER ADDRESS                  | BIT | LABEL         | DEFAULT | DESCRIPTION   | REFER TO |
|-----------------------------------|-----|---------------|---------|---|----------|
| R250 (FAh)<br>DCDC3 Test Controls | 4   | DC3_FORCE_PWM | 0       | Force DC-DC3 PWM mode<br>0 = Normal DC-DC operation<br>1 = Force DC-DC PWM mode<br><i>Reset by state machine.</i> |          |

Register FAh DCDC3 Test Controls

| REGISTER ADDRESS                  | BIT | LABEL         | DEFAULT | DESCRIPTION   | REFER TO |
|-----------------------------------|-----|---------------|---------|---|----------|
| R251 (FBh)<br>DCDC4 Test Controls | 4   | DC4_FORCE_PWM | 0       | Force DC-DC4 PWM mode<br>0 = Normal DC-DC operation<br>1 = Force DC-DC PWM mode<br><i>Reset by state machine.</i> |          |

Register FBh DCDC4 Test Controls

| REGISTER ADDRESS                  | BIT | LABEL         | DEFAULT | DESCRIPTION   | REFER TO |
|-----------------------------------|-----|---------------|---------|---|----------|
| R253 (FDh)<br>DCDC6 Test Controls | 4   | DC6_FORCE_PWM | 0       | Force DC-DC6 PWM mode<br>0 = Normal DC-DC operation<br>1 = Force DC-DC PWM mode<br><i>Reset by state machine.</i> |          |

Register FDh DCDC6 Test Controls

## 28 DIGITAL FILTER CHARACTERISTICS

| PARAMETER                         | TEST CONDITIONS | MIN     | TYP       | MAX     | UNIT |
|-----------------------------------|-----------------|---------|-----------|---------|------|
| <b>ADC Filter</b>                 |                 |         |           |         |      |
| Passband                          | +/- 0.025dB     | 0       |           | 0.454fs |      |
|                                   | -6dB            |         | 0.5fs     |         |      |
| Passband Ripple                   |                 |         | +/- 0.025 |         | dB   |
| Stopband                          |                 | 0.546fs |           |         |      |
| Stopband Attenuation              | f > 0.546fs     |         | -60       |         | dB   |
| Group Delay                       |                 |         | 21/fs     |         |      |
| <b>ADC High Pass Filter</b>       |                 |         |           |         |      |
| High Pass Filter Corner Frequency | -3dB            |         | 3.7       |         | Hz   |
|                                   | -0.5dB          |         | 10.4      |         |      |
|                                   | -0.1dB          |         | 21.6      |         |      |
| <b>DAC Filter</b>                 |                 |         |           |         |      |
| Passband                          | +/- 0.035dB     | 0       |           | 0.454fs |      |
|                                   | -6dB            |         | 0.5fs     |         |      |
| Passband Ripple                   |                 |         | +/-0.035  |         | dB   |
| Stopband                          |                 | 0.546fs |           |         |      |
| Stopband Attenuation              | f > 0.546fs     |         | -55       |         | dB   |
| Group Delay                       |                 |         | 29/fs     |         |      |

### Terminology

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

### 28.1 DAC FILTER RESPONSES

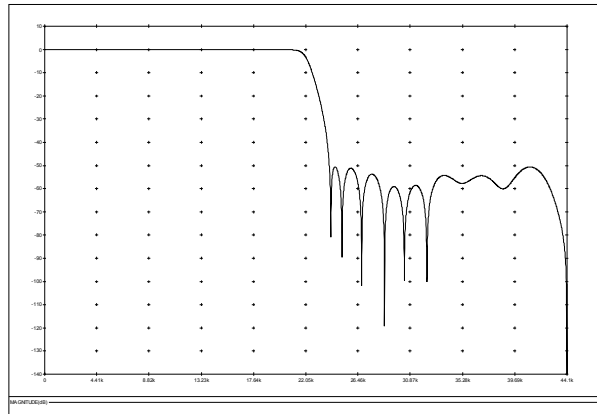


Figure 81 DAC Digital Filter Frequency Response (Normal Mode)

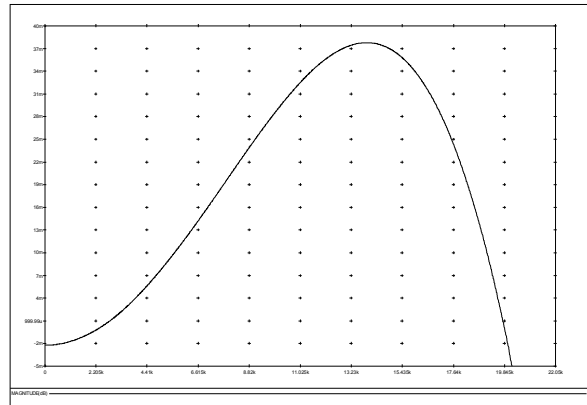


Figure 82 DAC Digital Filter Ripple (Normal Mode)

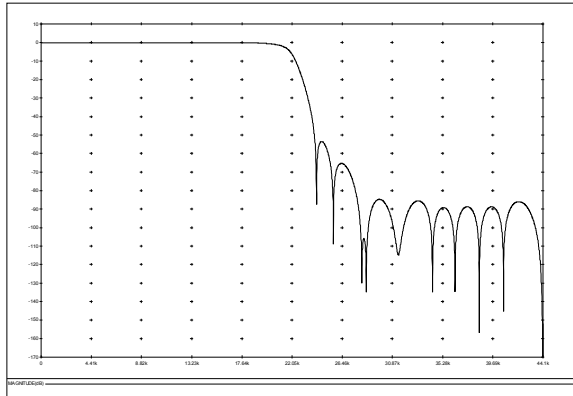


Figure 83 DAC Digital Filter Frequency Response (Sloping Stopband Mode)

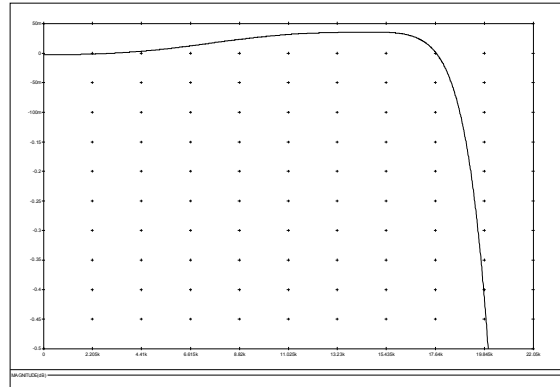


Figure 84 DAC Digital Filter Ripple (Sloping Stopband Mode)

## 28.2 ADC FILTER RESPONSES

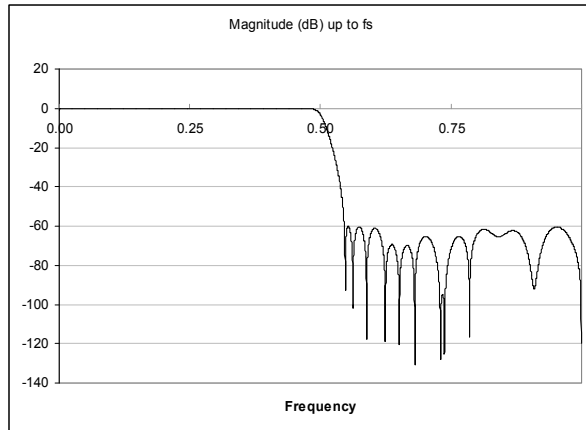


Figure 85 ADC Digital Filter Frequency Response

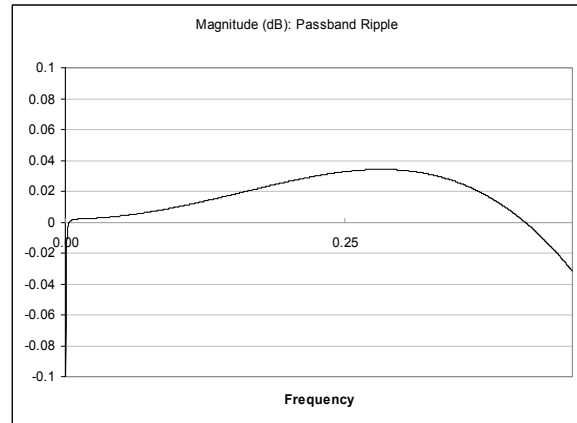


Figure 86 ADC Digital Filter Ripple



## 29 APPLICATIONS INFORMATION

### 29.1 TYPICAL CONNECTIONS

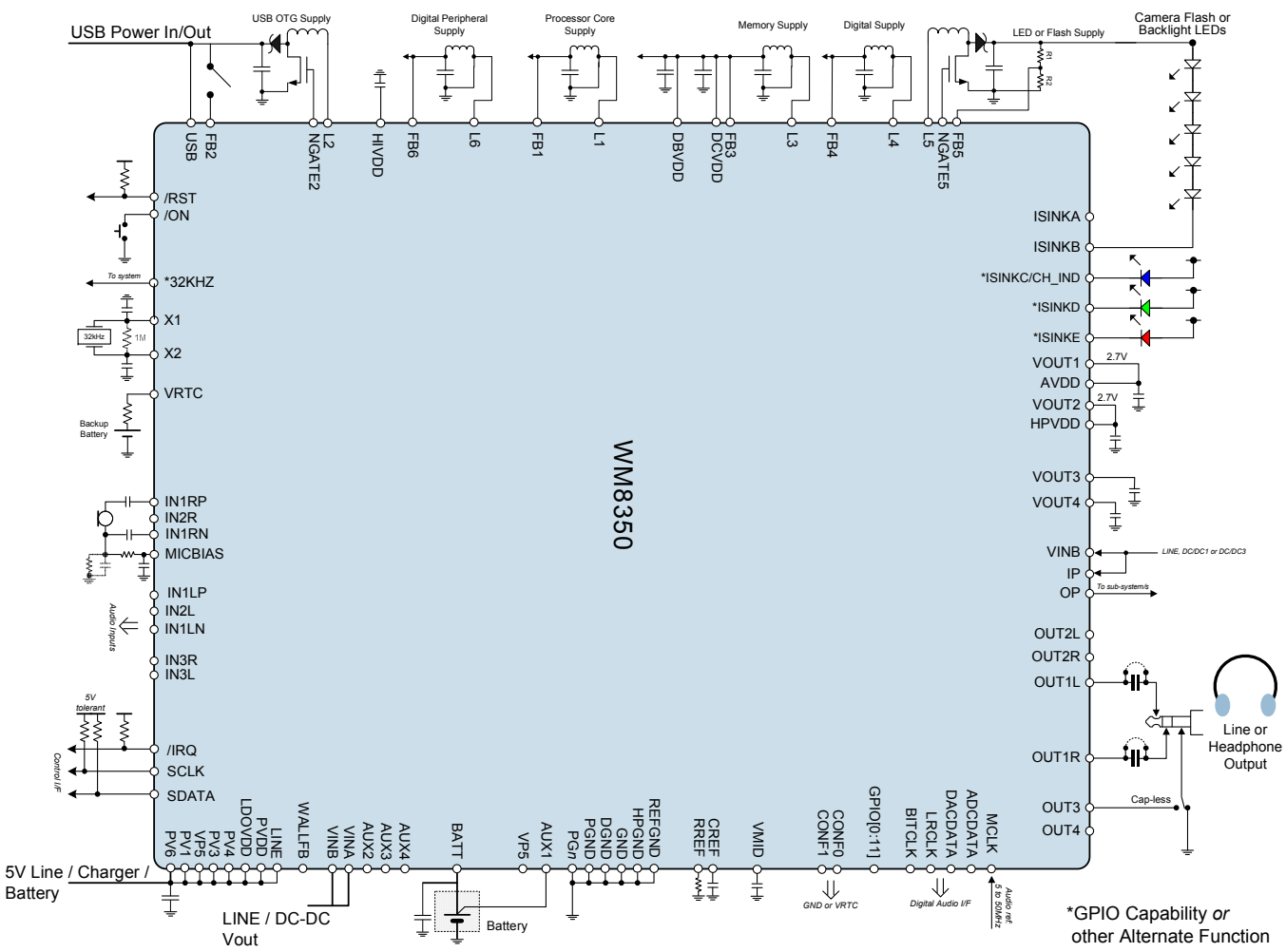


Figure 87 WM8350 Typical Connections Diagram

For detailed schematics, bill of materials and recommended external components refer to the WM8350 evaluation board users manual.

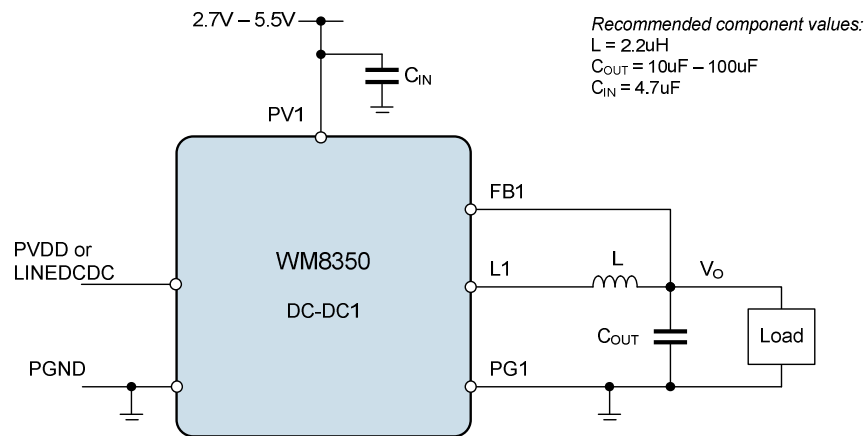
## 29.2 VOLTAGE REFERENCE (VREF) COMPONENTS

A decoupling capacitor is required between CREF and REFGND; a 2.2 $\mu$ F X5R capacitor is recommended.

A reference resistor is required between RREF and REFGND; a 100k $\Omega$  (1%) resistor is recommended.

## 29.3 DC-DC (STEP-DOWN) CONVERTER EXTERNAL COMPONENTS

The recommended connections to the DC-DC (Step-Down) Converters are illustrated in Figure 88.



Note: Equivalent circuit applies for DC-DC 3, 4 and 6.

Figure 88 DC-DC (Step-Down) Converters External Components

When selecting suitable capacitors, it is imperative that the effective capacitance is within the required limits at the applicable input/output voltage of the converter. It should be noted that some components' capacitance changes significantly depending on the DC voltage applied. Ceramic X7R or X5R types are recommended.

The choice of output capacitor for DC-DC1 and DC-DC6 varies depending on the required transient response. A value of 30 $\mu$ F is recommended in the first instance. Larger values (up to 100 $\mu$ F) may be required for optimum performance under large load transient conditions. Smaller values (down to 10 $\mu$ F) may be sufficient for a steady load in some applications.

For layout and size reasons, users may choose to implement large values of output capacitance by connecting two or more capacitors in parallel.

To ensure stable operation, the register fields DC1\_CAP and DC6\_CAP must be set according to the output capacitance, as detailed in Table 156.

| ADDRESS    | BIT       | LABEL   | DEFAULT | DESCRIPTION  |
|------------|-----------|---------|---------|--|
| R180 (B4h) | 15:1<br>4 | DC1_CAP | 00      | DC-DC1 Output Capacitor<br>00 = 10 $\mu$ F, 30 $\mu$ F, 45 $\mu$ F<br>01 = 60 $\mu$ F, 85 $\mu$ F<br>10 = Not used<br>11 = 100 $\mu$ F |
| R195 (C3h) | 15:1<br>4 | DC6_CAP | 00      | DC-DC6 Output Capacitor<br>00 = 10 $\mu$ F, 30 $\mu$ F, 45 $\mu$ F<br>01 = 60 $\mu$ F, 85 $\mu$ F<br>10 = Not used<br>11 = 100 $\mu$ F |

Table 156 Register Control for DC-DC1 and DC-DC6 Output Capacitor

When selecting a suitable output inductor, the inductance value and the saturation current must be compatible with the operating conditions of the converter.

The magnitude of the inductor current ripple is dependant on the inductor value and can be determined by the following equation:

$$\Delta I_L = \frac{V_{OUT} \cdot (1 - (V_{OUT} / V_{IN}))}{L \cdot F_{SW}}$$

$\Delta I_L$  = Inductor ripple current  
 $V_{OUT}$  = Output voltage  
 $V_{IN}$  = Input voltage  
 $L$  = Inductance  
 $F_{SW}$  = Switching frequency (2MHz)

As a minimum requirement, the DC current rating should be equal to the maximum load current plus one half of the inductor current ripple:

$$I_{Lpeak} = I_{OUTmax} + (\Delta I_L / 2)$$

$I_{Lpeak}$  = Inductor peak current  
 $I_{OUTmax}$  = Maximum load current  
 $\Delta I_L$  = Inductor ripple current

To be suitable for the application, the chosen inductor must have a saturation current that is higher than the peak inductor current given by the above equation. To maximise the converter efficiency, the inductor should also have a low DC Resistance (DCR), resulting in minimum conduction losses. Care should also be taken to ensure that the inductor is effective at the applicable operating temperature.

Wolfson recommends the following external components for use with DC-DC Converters 1 and 6. Note that the choice of output capacitor should be determined as described above.

| COMPONENT        | VALUE       | PART NUMBER                    | SIZE |
|------------------|-------------|--------------------------------|------|
| L                | 2.2 $\mu$ H | Coilcraft LPS3010-222ML (1.4A) |      |
| C <sub>OUT</sub> | 10 $\mu$ F  | Murata GRM219R60J106KE19B      | 0805 |
|                  | 22 $\mu$ F  | Murata GRM21BR60J226M          | 0805 |
|                  | 47 $\mu$ F  | Murata GRM31CR60J476M          | 1206 |
|                  | 100 $\mu$ F | Murata GRM31CR60J107M          | 1206 |
| C <sub>IN</sub>  | 4.7 $\mu$ F | Murata GRM188R60J475KE19D      | 0603 |

**Table 157 Recommended External Components - DC-DC1 and DC-DC6**

Wolfson recommends the following external components for use with DC-DC Converters 3 and 4.

| COMPONENT        | VALUE       | PART NUMBER                 | SIZE |
|------------------|-------------|-----------------------------|------|
| L                | 2.2 $\mu$ H | Murata LQM31PN2R2M00 (0.9A) | 1206 |
| C <sub>OUT</sub> | 10 $\mu$ F  | Murata GRM219R60J106KE19B   | 0805 |
| C <sub>IN</sub>  | 4.7 $\mu$ F | Murata GRM188R60J475KE19D   | 0603 |

**Table 158 Recommended External Components - DC-DC3 and DC-DC4**

## 29.4 DC-DC (STEP-UP) CONVERTER EXTERNAL COMPONENTS

The DC-DC (Step-Up) Converters can operate as Switches or as Boost Converters. In Boost mode, they operate in one of three different modes, set by the DC2\_FBSRC and DC5\_FBSRC register fields. The following subsections describe each of these modes in turn.

### 29.4.1 DC-DC (STEP-UP) CONVERTERS - CONSTANT VOLTAGE MODE

Constant voltage mode is selected by setting DCn\_FBSRC[1:0] = 00, as described in Section 14.6.4. The recommended connections to the DC-DC (Step-Up) Converters in this mode are illustrated in Figure 89.

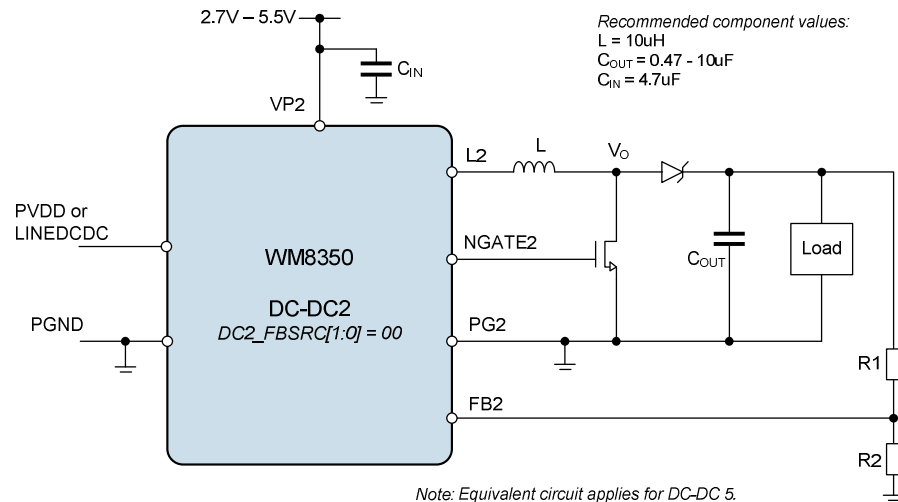


Figure 89 DC-DC (Step-Up) Converters External Components - Constant Voltage Mode

The DC-DC (Step-Up) Converters are capable of generating output voltages of up to 30V. The output voltage is determined by the two external resistors R1 and R2, which form a resistive divider between load connection and the voltage feedback pin FB2 or FB5. The output voltage is set as described in the following equation:

$$V_{\text{OUT}} = \frac{(R1/R2) + 1}{2}$$

Setting R2 to 47k $\Omega$  is recommended for most applications; R1 can be calculated using the following equation, given the required output voltage:

$$R1 = R2 \cdot (2V_{\text{OUT}} - 1)$$

When selecting suitable capacitors, it is imperative that the effective capacitance is within the required limits at the applicable input/output voltage of the converter. Ceramic X7R or X5R types are recommended.

The choice of output capacitor for DC-DC2 and DC-DC varies depending on the required output voltage. For a 20V output, 0.47 $\mu\text{F}$  is recommended. For a 5V output, 10 $\mu\text{F}$  is recommended.

When selecting a suitable output inductor, the inductance value and the saturation current must be compatible with the operating conditions of the converter.

The magnitude of the inductor current ripple is dependent on the inductor value and can be determined by the following equation:

$$\Delta I_L = \frac{V_{OUT} - V_{IN}}{L \cdot F_{SW}}$$

$\Delta I_L$  = Inductor ripple current  
 $V_{OUT}$  = Output voltage  
 $V_{IN}$  = Input voltage  
 $L$  = Inductance  
 $F_{SW}$  = Switching frequency (1MHz)

The inductor current is also a function of the DC-DC Converter maximum input current, which can be determined by the following equation:

$$I_{INmax} = \frac{I_{OUTmax}}{\text{efficiency}} \times \frac{V_{OUT}}{V_{IN}}$$

$I_{OUTmax}$  = Maximum load current  
 $I_{INmax}$  = Maximum input current  
 $V_{OUT}$  = Output voltage  
 $V_{IN}$  = Input voltage

As a minimum requirement, the DC current rating should be equal to the maximum input current plus one half of the inductor current ripple.

$$I_{Lpeak} = I_{OUTmax} + (\Delta I_L / 2)$$

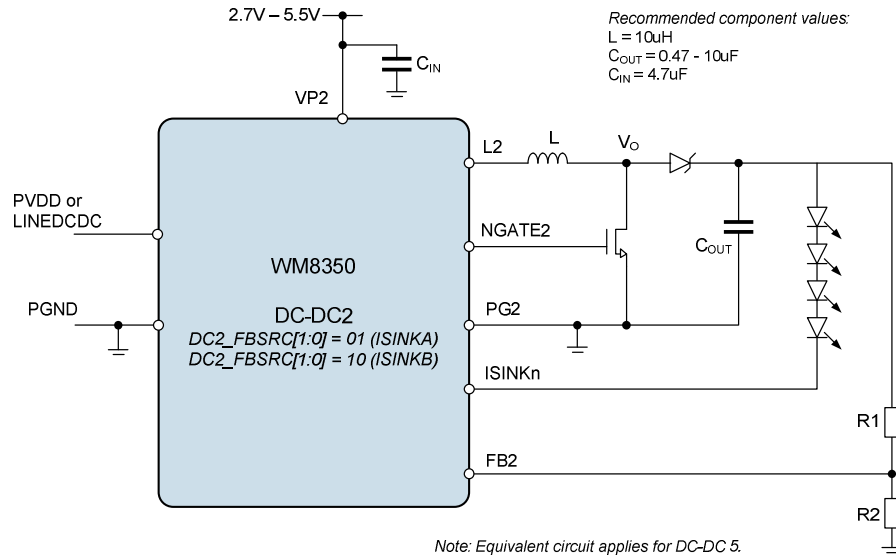
$I_{Lpeak}$  = Inductor peak current  
 $I_{OUTmax}$  = Maximum load current  
 $\Delta I_L$  = Inductor ripple current

To be suitable for the application, the chosen inductor must have a saturation current that is higher than the peak inductor current given by the above equation. To maximise the converter efficiency, the inductor should also have a low DC Resistance (DCR), resulting in minimum conduction losses. Care should also be taken to ensure that the inductor is effective at the applicable operating temperature.

See Section 29.4.4 for recommended inductor, capacitor and FET component details.

### 29.4.2 DC-DC (STEP-UP) CONVERTERS - CONSTANT CURRENT MODE

Constant current mode is selected by setting  $DCn\_FBSRC[1:0]$  as described in Section 14.6.4. Setting  $DCn\_FBSRC[1:0] = 01$  results in the DC Converter controlling the current at  $ISINKA$ , whilst setting  $DCn\_FBSRC[1:0] = 10$  controls the current at  $ISINKB$ . The recommended connections to the DC-DC (Step-Up) Converters in this mode are illustrated in Figure 90.



**Figure 90 DC-DC (Step-Up) Converters External Components - Constant Current Mode**

In the constant current mode, the DC-DC Converter output voltage is controlled by the WM8350 in order to achieve the required current in  $ISINKA$  or  $ISINKB$ . The required current is set by the  $CSn\_ISEL$  register fields, as described in Section 16.2.2. A typical application for this mode would be a white LED driver, where several LEDs are connected in series to achieve uniform brightness.

The DC-DC (Step-Up) Converters are capable of generating output voltages of up to 30V. The maximum output voltage is determined by the two external resistors  $R1$  and  $R2$ , which form a resistive divider between load connection and the voltage feedback pin  $FB2$  or  $FB5$ .

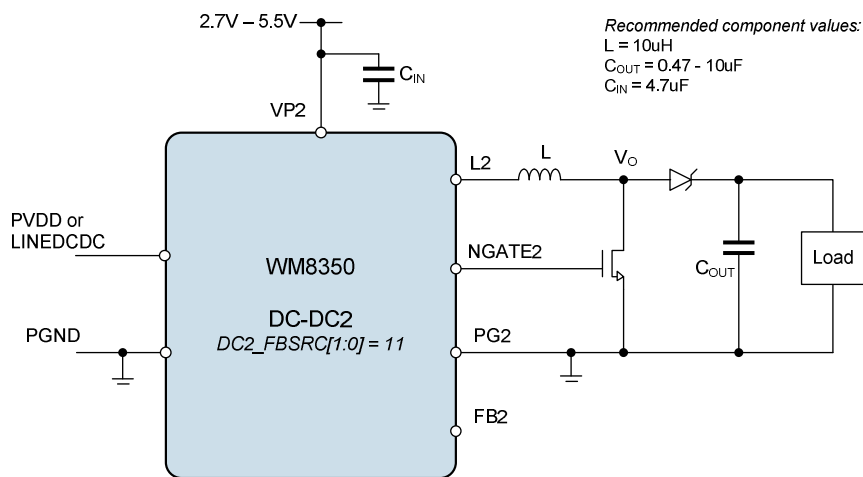
The choice of resistors  $R1$  and  $R2$  follows the same equations as for the constant voltage mode (see Section 29.4.1). Note that, in constant current mode, the resistors determine the maximum output voltage. The actual voltage will be determined by the selected  $ISINK$  current, subject to the device limits.

The choice of Capacitors, Inductor and FET in constant current mode is the same as for the constant voltage mode; see Section 29.4.4 for specific recommended component details.

When  $ISINKA$  or  $ISINKB$  is used in conjunction with DC-DC Converter 2 or 5, the  $ISINK$  should always be switched on before the DC-DC Converter is switched on. Conversely, the DC-DC Converter should always be switched off before the  $ISINK$  is switched off.

### 29.4.3 DC-DC (STEP-UP) CONVERTERS - USB MODE

USB mode is selected by setting  $DCn\_FBSRC[1:0] = 11$  as described in Section 14.6.4. This mode generates a 5V output, suitable for USB interfaces. The recommended connections to the DC-DC (Step-Up) Converters in this mode are illustrated in Figure 91.



Note: Equivalent circuit applies for DC-DC 5.

Figure 91 DC-DC (Step-Up) Converters External Components - USB Mode

In the USB mode, the DC-DC (Step-Up) Converters use an internal resistor chain to control the output voltage. This results in a fixed 5V output, suitable for USB interfaces.

The DC-DC (Step-Up) Converters may be configured as USB OTG supplement by setting  $USB\_MSTR = 1$  as described in Section 17.4. (The DC-DC Converters USB mode must also be selected by setting  $DCn\_FBSRC[1:0] = 11$ ). The output of the applicable DC-DC Converter should be connected to the USB pin in order to provide voltage feedback.

The choice of Capacitors, Inductor and FET in constant current mode is the same as for the constant voltage mode; see Section 29.4.4 for specific recommended component details.

### 29.4.4 DC-DC (STEP-UP) CONVERTERS RECOMMENDED COMPONENTS

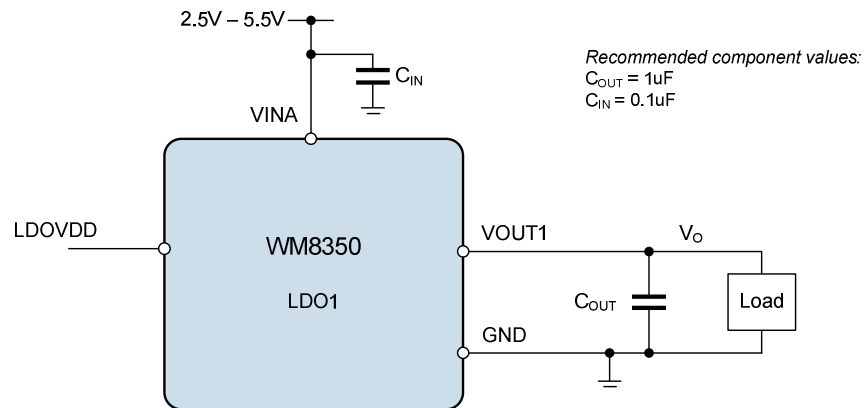
Wolfson recommends the following external components for use with DC-DC Converters 2 and 5. Note that the choice of output capacitor should be determined as described in Section 29.4.1.

| COMPONENT | VALUE              | PART NUMBER                                   | SIZE |
|-----------|--------------------|---|------|
| L         | 10 $\mu\text{H}$   | Taiyo Yuden NR4012T100M (0.7A)                |      |
| $C_{OUT}$ | 0.47 $\mu\text{F}$ | Murata GRM21BR71E474KC01L                     | 0805 |
|           | 4.7 $\mu\text{F}$  | Murata GRM188R60J475KE19D                     | 0603 |
|           | 10 $\mu\text{F}$   | Murata GRM219R60J106KE19B                     | 0805 |
| $C_{IN}$  | 4.7 $\mu\text{F}$  | Murata GRM188R60J475KE19D                     | 0603 |
| FET       |                    | On Semiconductor NTHD4N02F<br>N-Channel FETKY |      |

Table 159 Recommended External Components - DC-DC2 and DC-DC5

## 29.5 LDO REGULATOR EXTERNAL COMPONENTS

The recommended connections to the LDO Regulators are illustrated in Figure 92.



*Note: Equivalent circuit applies for LDO2, LDO3 and LDO4.  
 Input pin VINA supplies LDO1 and LDO2; Input pin VINB supplies LDO3 and LDO4.*

**Figure 92 LDO Regulators External Components**

When selecting suitable capacitors, it is imperative that the effective capacitance is within the required limits at the applicable input/output voltage of the converter. Ceramic X7R or X5R types are recommended.

Wolfson recommends the following external components for use with LDO Regulators 1, 2, 3 and 4. Note that larger capacitors will improve load transient response and power supply rejection. A maximum of  $10\mu\text{F}$  is possible at the output; a maximum of  $1\mu\text{F}$  is possible at the input.

| COMPONENT | VALUE            | PART NUMBER               | SIZE |
|-----------|------------------|---------------------------|------|
| $C_{OUT}$ | $1\mu\text{F}$   | Murata GRM155R60J105KE19D | 0402 |
| $C_{IN}$  | $0.1\mu\text{F}$ | Phycomp 06032R104K7B2     | 0603 |

**Table 160 Recommended External Components - LDO1, LDO2, LDO3 and LDO4**



## 29.6 PCB LAYOUT

Poor PCB layout will degrade the performance and be a contributory factor in EMI, ground bounce and resistive voltage losses. Poor regulation and instability can result.

Simple design rules can be implemented to negate these effects:

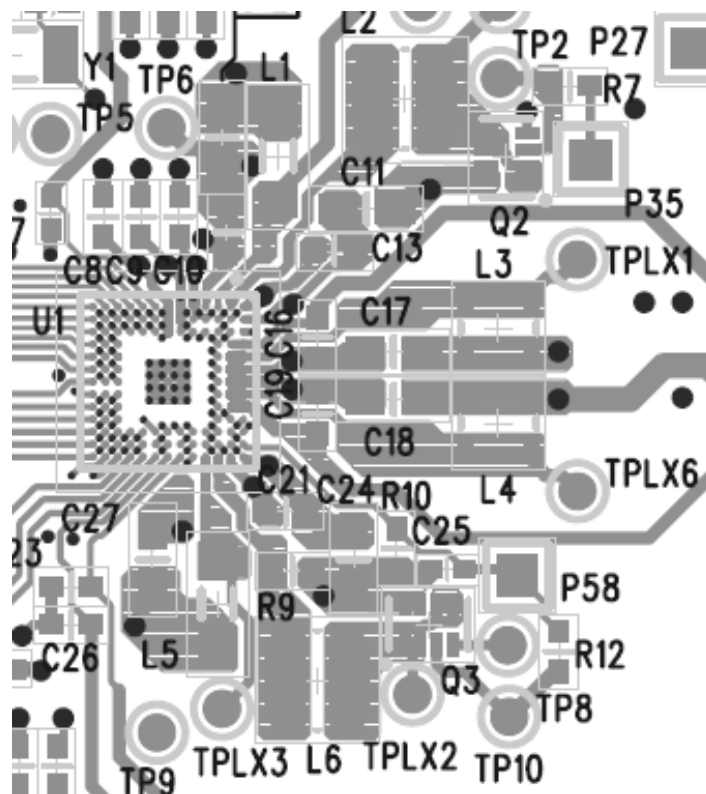
External input and output capacitors should be placed as close to the device as possible using short wide traces between the external power components.

Route output voltage feedback on an inner plane away from inductor and LX nodes to minimise noise and magnetic interference.

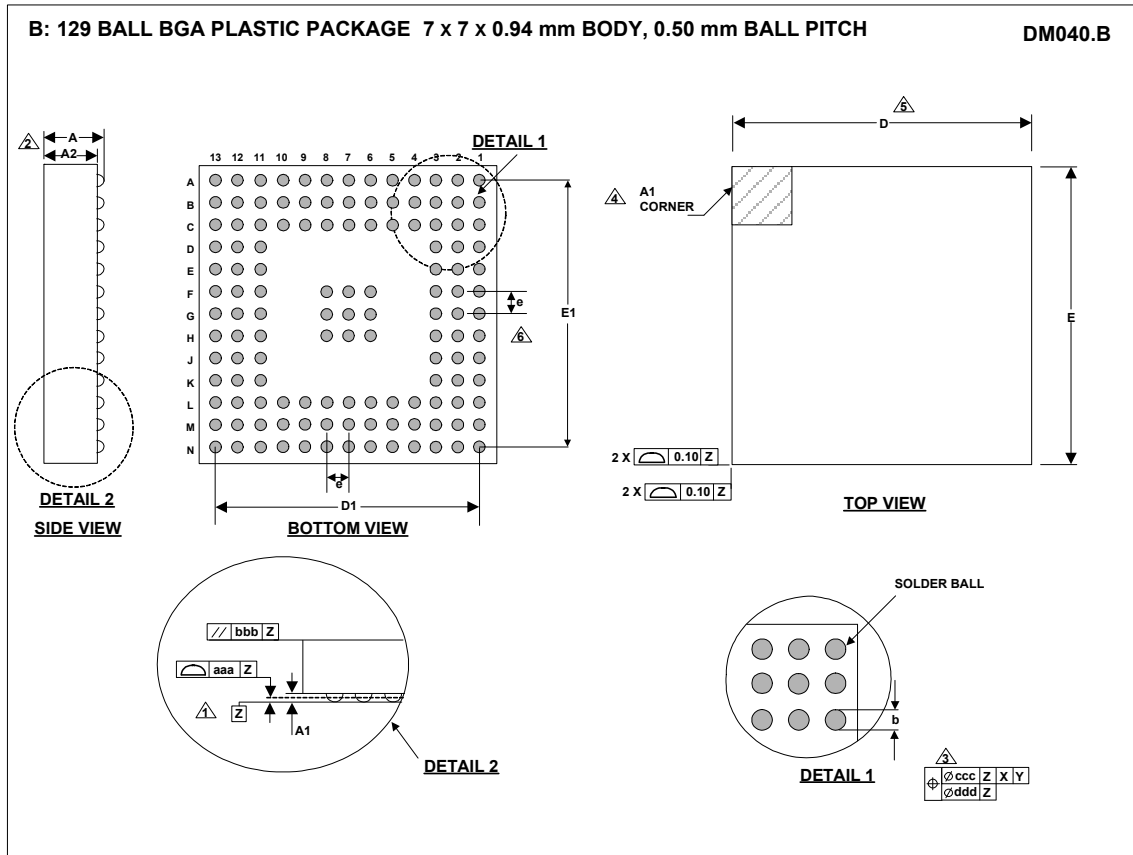
Use a local ground island for each individual converter connected at a single point onto a fully flooded ground plane.

Current loop areas should be kept as small as possible with loop areas changing little during alternating switching cycles.

Studying the layout below shows, for example, DCDC1 layout with external components C16, L3, C17. The input capacitor, C16, is close into the IC and shares a small ground island with C17 the output capacitor. The inductor, L3, is then situated in close proximity to C17 to keep loop area small and current flowing in the same direction during alternating switching cycles. Note also the use of short wide traces with all power tracking on a single (top) layer.



30 PACKAGE DIAGRAM



| Symbols                                | Dimensions (mm) |               |      |      |
|--|-----------------|---------------|------|------|
|  | MIN             | NOM           | MAX  | NOTE |
| A                                      | 0.83            | 0.94          | 1.05 |      |
| A1                                     | 0.2             | 0.24          | 0.28 |      |
| A2                                     | 0.63            | 0.70          | 0.77 |      |
| b                                      | 0.25            | 0.30          | 0.35 |      |
| D                                      |                 | 7.00 BSC      |      |      |
| D1                                     |                 | 6.00 BSC      |      |      |
| E                                      |                 | 7.00 BSC      |      |      |
| E1                                     |                 | 6.00 BSC      |      |      |
| e                                      |                 | 0.50 BSC      |      | 6    |
| <b>Tolerances of Form and Position</b> |                 |               |      |      |
| aaa                                    |                 | 0.08          |      |      |
| bbb                                    |                 | 0.10          |      |      |
| ccc                                    |                 | 0.15          |      |      |
| ddd                                    |                 | 0.05          |      |      |
| REF:                                   |                 | JEDEC, MO-195 |      |      |

- NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
  2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1'.
  3. DIMENSION 'b' IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -Z-.
  4. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
  5. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
  6. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
  7. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
  8. FALLS WITHIN JEDEC, MO-195

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**32 REVISION HISTORY**

| <b>DATE</b> | <b>REV</b> | <b>ORIGINATOR</b> | <b>CHANGES</b>                                      |
|-------------|------------|-------------------|---|
| 01/02/11    | 4.4        | PH                | REG_RESET_HIB_MODE description corrected, p111, 226 |