WM8215

60MSPS 10-bit 3-Channel CCD Digitiser

DESCRIPTION

The WM8215 is a 10-bit analogue front end/digitiser IC which processes and digitises the analogue output signals from CCD sensors or Contact Image Sensors (CIS) at pixel sample rates of up to 60MSPS.

The device includes three analogue signal processing channels each of which contains Reset Level Clamping, Correlated Double Sampling and Programmable Gain and Offset adjust functions. The output from each of these channels is time multiplexed into a single high-speed 10-bit Analogue to Digital Converter. The digital output data is available in 10-bit wide parallel format.

An internal 4-bit DAC is supplied for internal reference level generation. This may be used to reference CIS signals, in non-CDS mode or to clamp CCD signals during Reset Level Clamping. An external reference level may also be supplied. ADC references are generated internally, ensuring optimum performance from the device.

Using an analogue supply voltage of 3.3V and a digital interface supply of 3.3V, the WM8215 typically only consumes 400mW.

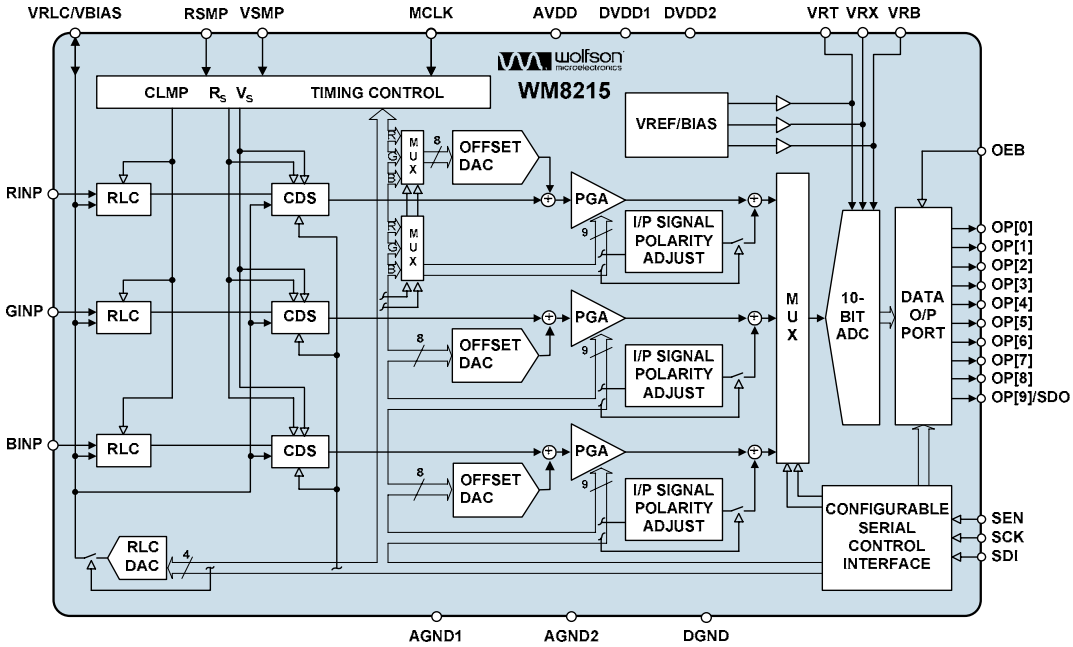
FEATURES

- 10-bit ADC
- 60MSPS conversion rate
- Low power – 400mW typical
- 3.3V single supply operation
- 3 channel operation
- Correlated double sampling
- Programmable gain (9-bit resolution)
- Programmable offset adjust (8-bit resolution)
- Flexible clamp timing
- Programmable clamp voltage
- Internally generated voltage references
- 32-lead QFN package
- Serial control interface

APPLICATIONS

- Digital Copiers
- USB2.0 compatible scanners
- Multi-function peripherals
- High-speed CCD/CIS sensor interface

BLOCK DIAGRAM



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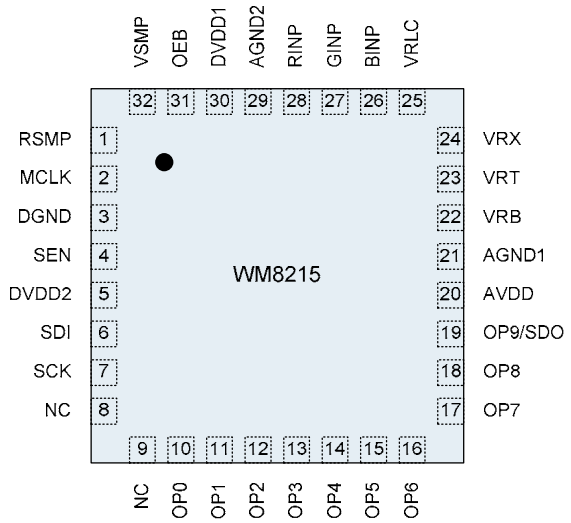
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8215SEFL	0 to 70°C	32-lead QFN (5x5x0.9mm) (Pb-free)	MSL1	260°C
WM8215SEFL/R	0 to 70°C	32-lead QFN (5x5x0.9mm) (Pb-free, tape and reel)	MSL1	260°C

Note:

Reel quantity = 3,500

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	RSMP	Digital input	Reset sample pulse (when CDS=1) or clamp control
2	MCLK	Digital input	Master (ADC) clock. This clock determines the ADC conversion rate.
3	DGND	Supply	Digital ground.
4	SEN	Digital input	Enables the serial interface when high.
5	DVDD2	Supply	Digital supply, all digital I/O pins.
6	SDI	Digital input	Serial data input.
7	SCK	Digital input	Serial clock.
8	NC	No connect	No internal connection.
9	NC	No connect	No internal connection.
			Digital output data bus. ADC output data (d9:d0) is available in 10-bit parallel format.
10	OP[0]	Digital output	d0 (LSB)
11	OP[1]	Digital output	d1
12	OP[2]	Digital output	d2
13	OP[3]	Digital output	d3
14	OP[4]	Digital output	d4
15	OP[5]	Digital output	d5
16	OP[6]	Digital output	d6
17	OP[7]	Digital output	d7
18	OP[8]	Digital output	d8
19	OP[9]/SDO	Digital output	d9 (MSB)
			Alternatively, pin OP[9]/SDO may be used to output register read-back data when OEB=0, OPD(register bit)=0 and SEN has been pulsed high. See Serial Interface description in Device Description section for further details.
20	AVDD	Supply	Analogue supply. This must be operated at the same potential as DVDD1.
21	AGND1	Supply	Analogue ground.
22	VRB	Analogue output	Lower reference voltage. This pin must be connected to AGND via a decoupling capacitor.
23	VRT	Analogue output	Upper reference voltage. This pin must be connected to AGND via a decoupling capacitor.
24	VRX	Analogue output	Input return bias voltage. This pin must be connected to AGND via a decoupling capacitor.
25	VRLC/VBIAS	Analogue I/O	Selectable analogue output voltage for RLC or single-ended bias reference. This pin would typically be connected to AGND via a decoupling capacitor. VRLC can be externally driven if programmed Hi-Z.
26	BINP	Analogue input	Blue channel input video.
27	GINP	Analogue input	Green channel input video.
28	RINP	Analogue input	Red channel input video.
29	AGND2	Supply	Analogue ground.
30	DVDD1	Supply	Digital supply for logic and clock generator. This must be operated at the same potential as AVDD.
31	OEB	Digital input	Output Hi-Z control. All digital outputs set to high-impedance state when input pin OEB=1 or register bit OPD=1.
32	VSMP	Digital input	Video sample pulse.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Analogue supply voltage: AVDD	GND - 0.3V	GND + 4.2V
Digital supply voltages: DVDD1 – 2	GND - 0.3V	GND + 4.2V
Digital ground: DGND	GND - 0.3V	GND + 0.3V
Analogue grounds: AGND1 – 2	GND - 0.3V	GND + 0.3V
Digital inputs, digital outputs and digital I/O pins	GND - 0.3V	DVDD2 + 0.3V
Analogue inputs (RINP, GINP, BINP)	GND - 0.3V	AVDD + 0.3V
Other pins	GND - 0.3V	AVDD + 0.3V
Operating temperature range: T_A	0°C	+70°C
Storage temperature after soldering	-65°C	+150°C

Notes:

1. GND denotes the voltage of any ground pin.
2. AGND1, AGND2 and DGND pins are intended to be operated at the same potential. Differential voltages between these pins will degrade performance.

RECOMMENDED OPERATING CONDITIONS

CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Operating temperature range	T_A	0		70	°C
Analogue supply voltage	AVDD	2.97	3.3	3.63	V
Digital core supply voltage	DVDD1	2.97	3.3	3.63	V
Digital I/O supply voltage	DVDD2	2.97	3.3	3.63	V

Notes:

1. DVDD2 should be operated at the same potential as DVDD1 ± 0.3V.

THERMAL PERFORMANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Performance						
Thermal resistance – junction to case	$R_{\theta JC}$	$T_{ambient}$ = 25℃		10.27		℃/W
Thermal resistance – junction to ambient	$R_{\theta JA}$			29.45		℃/W

Notes:

1. Figures given are for package mounted on 4-layer FR4 according to JESD51-5 and JESD51-7.

ELECTRICAL CHARACTERISTICS

Test Conditions
AVDD = DVDD1 = DVDD2 = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 60MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall System Specification (including 10-bit ADC, PGA, Offset and CDS functions)						
Conversion rate				60		MSPS
Full-scale input voltage range (see Note 1)		LOWREFS=0, Max Gain		0.25		Vp-p
		LOWREFS=0, Min Gain		3.03		Vp-p
		LOWREFS=1, Max Gain		0.15		Vp-p
		LOWREFS=1, Min Gain		1.82		Vp-p
Input signal limits (see Note 2)	V_{IN}		AGND-0.3		AVDD+0.3	V
Input capacitance				10		pF
Input switching impedance				45		Ω
Full-scale transition error		Gain = 0dB; PGA[8:0] = 14(hex)		20		mV
Zero-scale transition error		Gain = 0dB; PGA[8:0] = 14(hex)		20		mV
Differential non-linearity	DNL			0.75		LSB
Integral non-linearity	INL			2		LSB
Channel to channel gain matching				1%		%
Output noise		Min Gain		0.2		LSB rms
		Max Gain		2.15		LSB rms
References						
Upper reference voltage	VRT	LOWREFS=0	1.95	2.05	2.25	V
		LOWREFS=1		1.85		V
Lower reference voltage	VRB	LOWREFS=0	0.95	1.05	1.25	V
		LOWREFS=1		1.25		V
Input return bias voltage	VRX			1.25		V
Diff. reference voltage (VRT-VRB)	V_{RTB}	LOWREFS=0	0.95	1.0	1.10	V
		LOWREFS=1	0.57	0.6	0.68	V
Output resistance VRT, VRB, VRX				1		Ω
VRLC/Reset-Level Clamp (RLC)						
RLC switching impedance				45		Ω
VRLC short-circuit current				2		mA
VRLC output resistance				3		Ω
VRLC Hi-Z leakage current		VRLC = 0 to AVDD			1	µA
RLCDAC resolution				4		bits
RLCDAC step size, RLCDACRNG = 0	$V_{RLCSTEP}$			0.173		V/step
RLCDAC step size, RLCDACRNG = 1	$V_{RLCSTEP}$	LOWREFS = 0		0.11		V/step
		LOWREFS = 1		0.10		
RLCDAC output voltage at code 0(hex), RLCDACRNG = 0	V_{RLCBOT}			0.4		V
RLCDAC output voltage at code 0(hex), RLCDACRNG = 1	V_{RLCBOT}	LOWREFS = 0		0.4		V
		LOWREFS = 1				
RLCDAC output voltage at code F(hex) RLCDACRNG, = 0	V_{RLCTOP}			3.0		V
RLCDAC output voltage at code F(hex), RLCDACRNG = 1	V_{RLCTOP}	LOWREFS = 0		2.05		V
		LOWREFS = 1		1.85		
RLCDAC	DNL		-0.5		+0.5	LSB
RLCDAC	INL			+/-0.5		LSB

Notes:

1. **Full-scale input voltage** denotes the peak input signal amplitude that can be gained to match the ADC full-scale input range.

2. **Input signal limits** are the limits within which the full-scale input voltage signal must lie.

Test Conditions
AVDD = DVDD1 = DVDD2 = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 60MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Offset DAC, Monotonicity Guaranteed						
Resolution				8		bits
Differential non-linearity	DNL			0.15		LSB
Integral non-linearity	INL			0.4		LSB
Step size				2.00		mV/step
Output voltage		Code 00(hex) Code FF(hex)		-255 +255		mV mV
Programmable Gain Amplifier						
Resolution				9		bits
Gain			$0.66 + \frac{7.34}{511} * PGA[8:0]$			V/V
Max gain, each channel	G_{MAX}			8		V/V
Min gain, each channel	G_{MIN}			0.66		V/V
Gain error, each channel				3		%
Analogue to Digital Converter						
Resolution				10		bits
Speed					60	MSPS
Full-scale input range (2*(VRT-VRB))		LOWREFS=0	1.9	2	2.2	V
		LOWREFS=1		1.2		V
DIGITAL SPECIFICATIONS						
Digital Inputs						
High level input voltage	V_{IH}		0.7 ∗ DVDD2			V
Low level input voltage	V_{IL}				0.2 ∗ DVDD2	V
High level input current	I_{IH}				1	µA
Low level input current	I_{IL}				1	µA
Input capacitance	C_I			5		pF
Digital Outputs						
High level output voltage	V_{OH}	I_{OH} = 1mA	DVDD2 - 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			0.5	V
High impedance output current	I_{OZ}				1	µA
Digital IO Pins						
Applied high level input voltage	V_{IH}		0.7 ∗ DVDD2			V
Applied low level input voltage	V_{IL}				0.2 ∗ DVDD2	V
High level output voltage	V_{OH}	I_{OH} = 1mA	DVDD2 - 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			0.5	V
Low level input current	I_{IL}				1	µA
High level input current	I_{IH}				1	µA
Input capacitance	C_I			5		pF
High impedance output current	I_{OZ}				1	µA
Supply Currents						
Total supply current – active				116		mA
Analogue supply current – active (three channel mode)				105		mA
Digital supply current – active (three channel mode)				11		mA
Supply current – full power down mode				20		µA

INPUT VIDEO SAMPLING

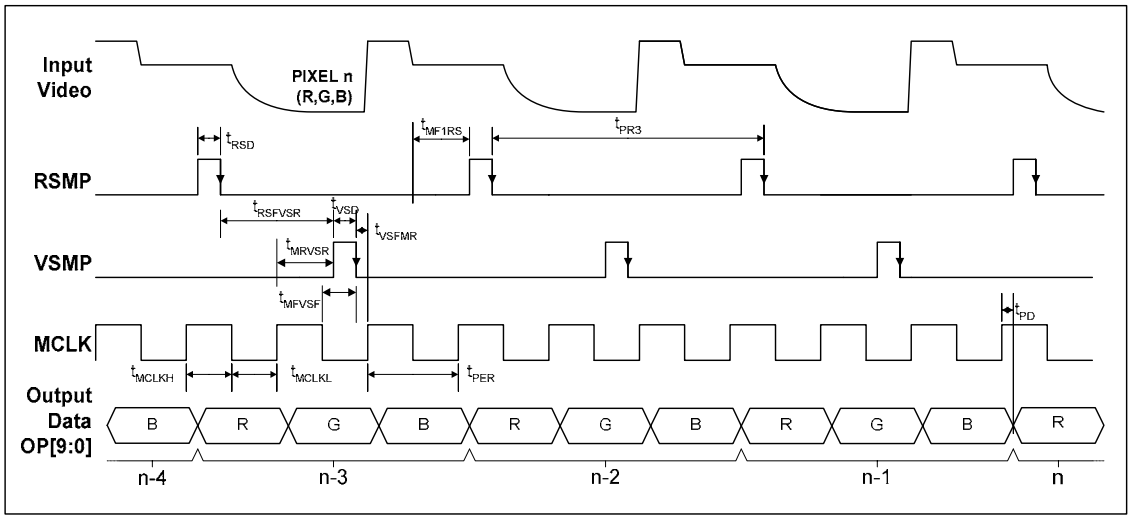


Figure 1 Three-channel CDS Input Video Timing (CDS=1)

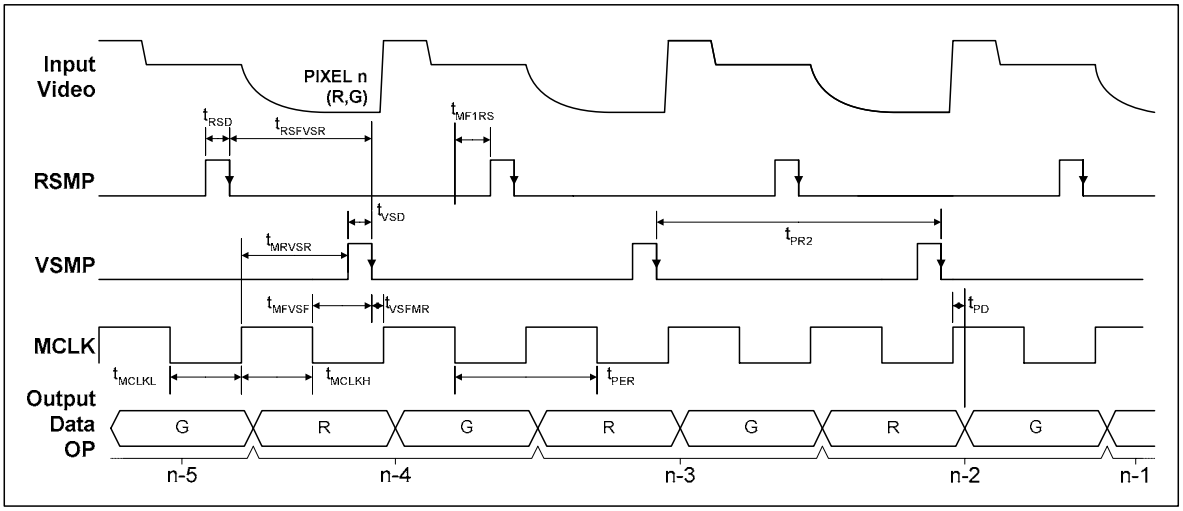


Figure 2 Two-channel CDS Operation (CDS=1)

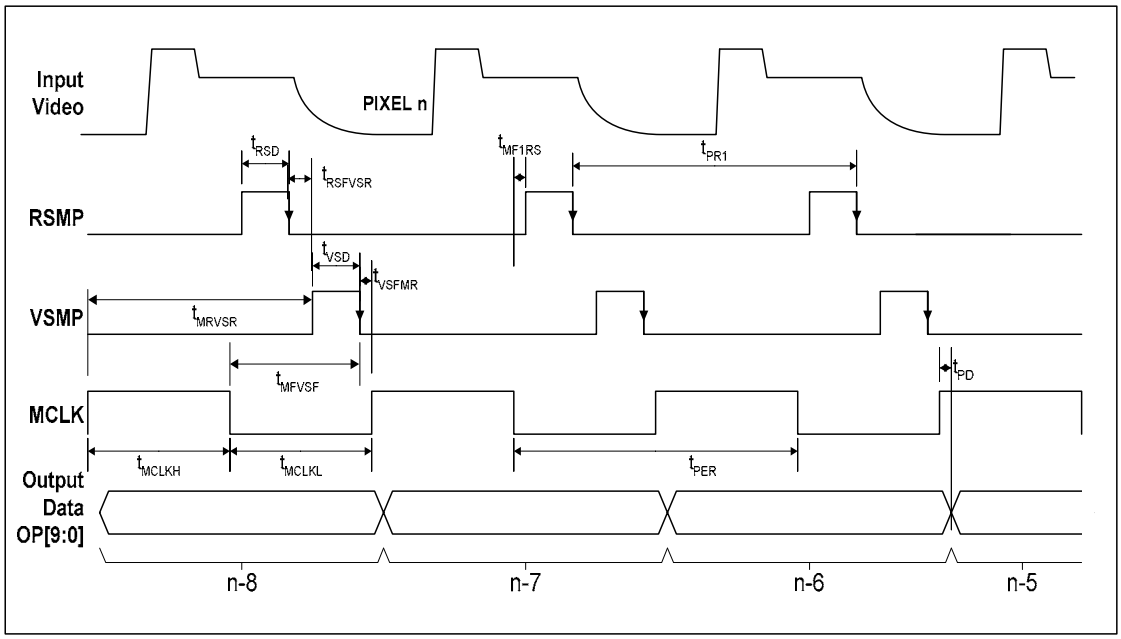


Figure 3 One-channel CDS Operation (CDS=1)

Notes:

1. The relationship between input video signal and sample points is controlled by VSMP and RSMP.
2. When VSMP is high the input video signal is connected to the Video sampling capacitors.
3. When RSMP is high the input video signal is connected to the Reset sampling capacitors.
4. RSMP must not go high before the first falling edge of MCLK after VSMP goes low.
5. It is required that the falling edge of VSMP should occur before the rising edge of MCLK.
6. In 1-channel CDS mode it is not possible to have an equally spaced Video and Reset sample points with a 45MHz MCLK.
7. Non-CDS operation is also possible; RSMP is not required in this mode but can be used to control input clamping. Timing constraints between vsmp and mclk remain unchanged for non-CDS operation.

Test Conditions

AVDD = DVDD1 = DVDD2 = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 60MHz for 3 and 2-channel mode and 45MHz for 1-channel mode unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MCLK period – 2/3 channel mode 1 channel mode	t_{PER}		16.6 22.2			ns
MCLK high period – 2/3 channel mode 1 channel mode	t_{MCLKH}		6.7	8.3 11.1		ns
MCLK low period – 2/3 channel mode 1 channel mode	t_{MCLKL}		6.7	8.3 11.1		ns
RSMP pulse high time	t_{RSD}		5			ns
VSMP pulse high time	t_{VSD}		5			ns
RSMP falling to VSMP rising time	t_{RSFVSR}		0			ns
MCLK rising to VSMP rising time	t_{MRVSR}		3			ns
MCLK falling to VSMP falling time	t_{MFVSF}		0			ns
MCLK falling to VSMP falling time in 1 channel mode	t_{MFVSF}		7			ns
VSMP falling to MCLK rising time	t_{VSFMR}		0			ns
1st MCLK falling edge after VSMP falling to RSMP rising time	t_{MF1RS}		1			ns
3-channel mode pixel period	t_{PR3}		50			ns
2-channel mode pixel period	t_{PR2}		33.3			ns
1-channel mode pixel period	t_{PR1}		22.2			ns

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output propagation delay	t_{PD}			5	10	ns
Output latency. From 1st rising edge of MCLK after VSMP falling to data output	LAT			7		MCLK periods

Notes:

1. Parameters are measured at 50% of the rising/falling edge.
2. In 1-channel mode, if t_{MFVSF} is less than 9.5ns, the output amplitude of the WM8215 will decrease.

SERIAL INTERFACE

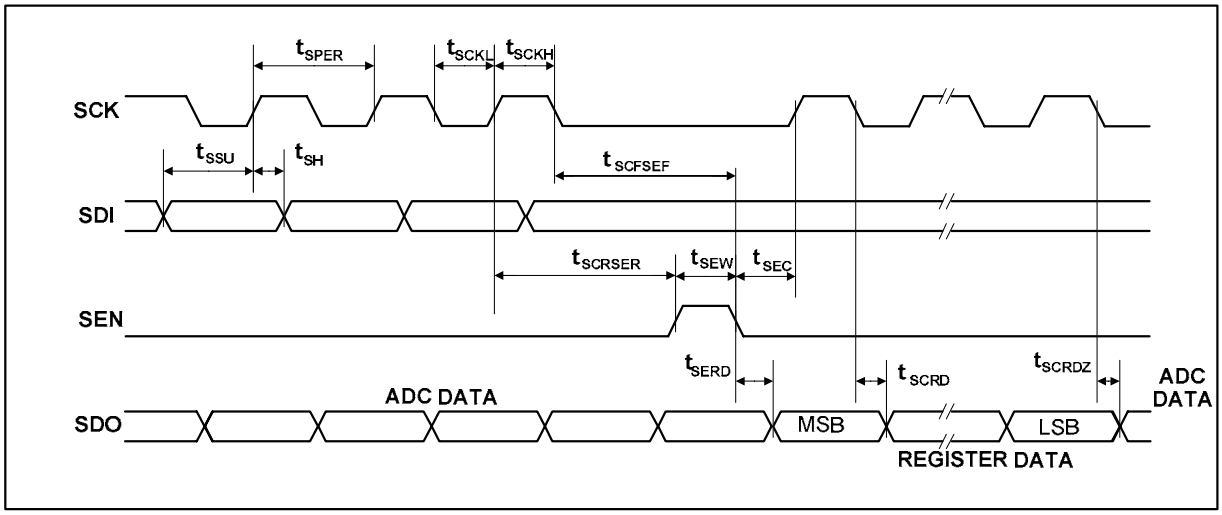


Figure 4 Serial Interface Timing

Test Conditions

AVDD = DVDD1 = DVDD2 = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 45MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SCK period	t_{SPER}		83.3			ns
SCK high	t_{SCKH}		37.5			ns
SCK low	t_{SCKL}		37.5			ns
SDI set-up time	t_{SSU}		6			ns
SDI hold time	t_{SH}		6			ns
SCK Rising to SEN Rising	t_{SCRSER}		37.5			ns
SCK Falling to SEN Falling	t_{SCFSEF}		12			ns
SEN to SCK set-up time	t_{SEC}		12			ns
SEN pulse width	t_{SEW}		60			ns
SEN low to SDO = Register data	t_{SERD}				30	ns
SCK low to SDO = Register data	t_{SCRD}				30	ns
SCK low to SDO = ADC data	t_{SCRDZ}				30	ns

Note: 1. Parameters are measured at 50% of the rising/falling edge

INTERNAL POWER ON RESET CIRCUIT

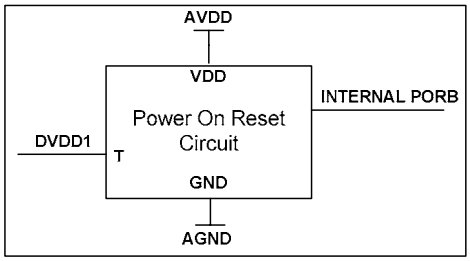


Figure 5 Internal Power On Reset Circuit Schematic

The WM8215 includes an internal Power-On-Reset Circuit, as shown in Figure 5, which is used to reset the digital logic into a default state after power up. The POR circuit is powered from AVDD and monitors DVDD1. It asserts PORB low if AVDD or DVDD1 is below a minimum threshold.

The power supplies can be brought up in any order but is important that either AVDD is brought up and is stable before DVDD comes up or vice versa as shown in Figure 6 and Figure 7.

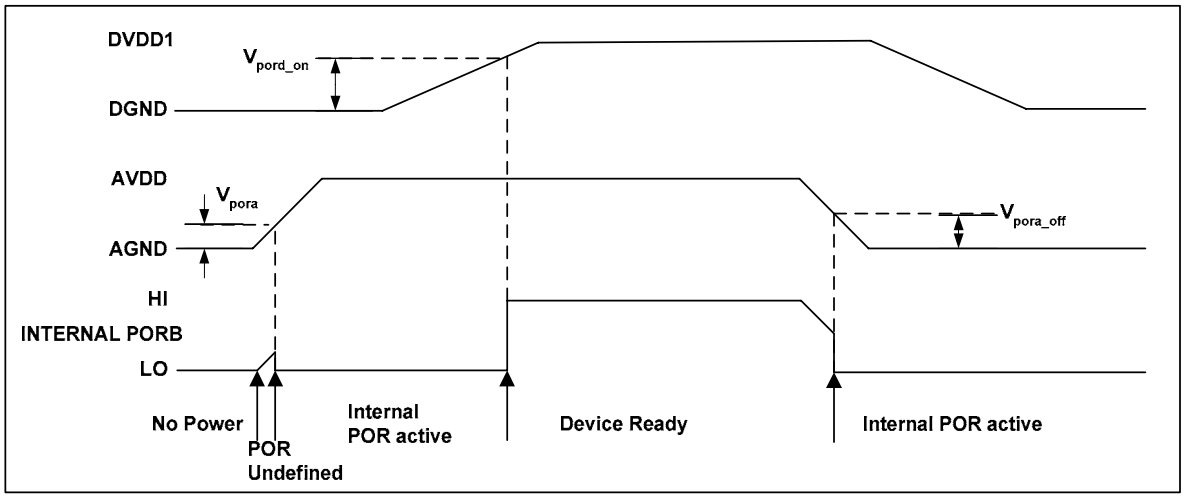


Figure 6 Typical Power up Sequence where AVDD is Powered before DVDD1

Figure 6 shows a typical power-up sequence where AVDD comes up first. When AVDD goes above the minimum threshold, Vpora, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Now AVDD is at full supply level. Next DVDD1 rises to Vpord_on and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold Vpora_off.

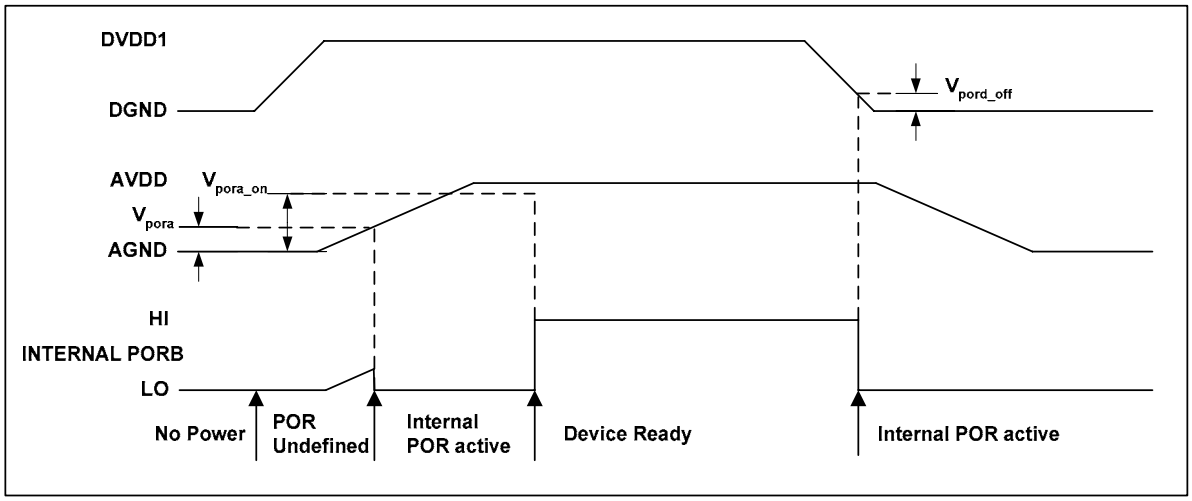


Figure 7 Typical Power up Sequence where DVDD1 is Powered before AVDD

Figure 7 shows a typical power-up sequence where DVDD1 comes up first. First it is assumed that DVDD1 is already up to specified operating voltage. When AVDD goes above the minimum threshold, Vpora, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD rises to Vpora_on, PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DVDD1 falls first, PORB is asserted low whenever DVDD1 drops below the minimum threshold Vpord_off.

SYMBOL	TYP	UNIT
V_{pora}	0.6	V
V_{pora_on}	1.2	V
V_{pora_off}	0.6	V
V_{pord_on}	0.7	V
V_{pord_off}	0.6	V

Table 1 Typical POR Operation (typical values, not tested)

Note: It is recommended that every time power is cycled to the WM8215 a software reset is written to the software register to ensure that the contents of the control registers are at their default values before carrying out any other register writes.

DEVICE DESCRIPTION

INTRODUCTION

A block diagram of the device showing the signal path is presented on the front page of this datasheet.

The WM8215 samples up to three inputs (RINP, GINP and BINP) simultaneously. The device then processes the sampled video signal with respect to the video reset level or an internally/externally generated reference level using between one and three processing channels.

Each processing channel consists of an Input Sampling block with optional Reset Level Clamping (RLC) and Correlated Double Sampling (CDS), an 8-bit programmable offset DAC and a 9-bit Programmable Gain Amplifier (PGA).

The processing channel outputs are switched alternately by a 3:1 multiplexer to the ADC input.

The ADC then converts each resulting analogue signal to a 10-bit digital word. The digital output from the ADC is presented in parallel on the 10-bit wide output bus, OP[9:0]. The ten output pins can be set to a high impedance state using either the OEB control pin or the OPD register bit.

On-chip control registers determine the configuration of the device, including the offsets and gains applied to each channel. These registers are programmable via a serial interface.

INPUT SAMPLING

The WM8215 can sample and process up to three inputs through one to three processing channels as follows:

Colour Pixel-by-Pixel: The three inputs (RINP, GINP and BINP) are simultaneously sampled for each pixel and a separate channel processes each input. The signals are then multiplexed into the ADC, which converts all three inputs within the pixel period.

Two Channel Pixel-by-pixel: Two input channels (RINP and GINP) are simultaneously sampled for each pixel and a separate channel processes each input. The signals are then multiplexed into the ADC, which converts both inputs within the pixel period. The unused Blue channel is powered down when this mode is selected.

Monochrome: A single chosen input (RINP, GINP, or BINP) is sampled, processed by the corresponding channel, and converted by the ADC. The choice of input and channel can be changed via the control interface, e.g. on a line-by-line basis if required. The unused channels are powered down when this mode is selected.

RESET LEVEL CLAMPING (RLC)

To ensure that the signal applied to the WM8215 lies within the supply voltage range (0V to AVDD) the output signal from a CCD is usually level shifted by coupling through a capacitor, $C_{IN.}$ The RLC circuit clamps the WM8215 side of this capacitor to a suitable voltage through a CMOS switch during the CCD reset period (pixel clamping) or during the black pixels (line clamping). In order for clamping to produce correct results the input voltage during the clamping must be a constant value.

The WM8215 allows the user to control the RLC switch in a variety of ways as illustrated in Figure 8 This figure shows a single channel, however all 3 channels are identical, each with its own clamp switch controlled by the common CLMP signal.

The method of control chosen depends upon the characteristics of the input video. The RLCEN register bit must be set to 1 to enable clamping, otherwise the RLC switch cannot be closed (by default RLCEN=1).

Note that unused inputs should be left floating, or grounded through a decoupling capacitor, if reset level clamping is used.

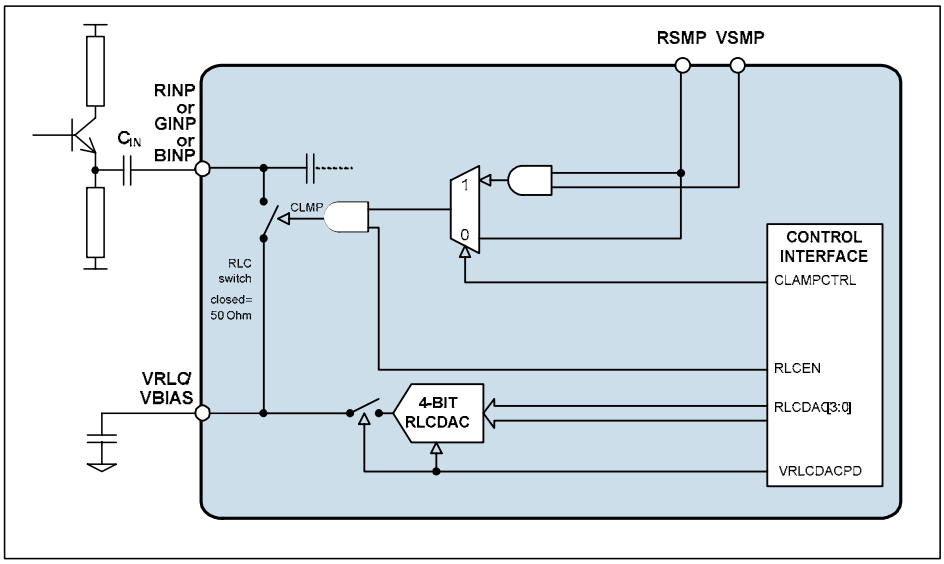


Figure 8 RLC Clamp Control Options

When an input waveform has a stable reference level on every pixel it may be desirable to clamp every pixel during this period. Setting CLAMPCTRL=0 means that the RLC switch is closed whenever the RSMP input pin is high, as shown in Figure 9.

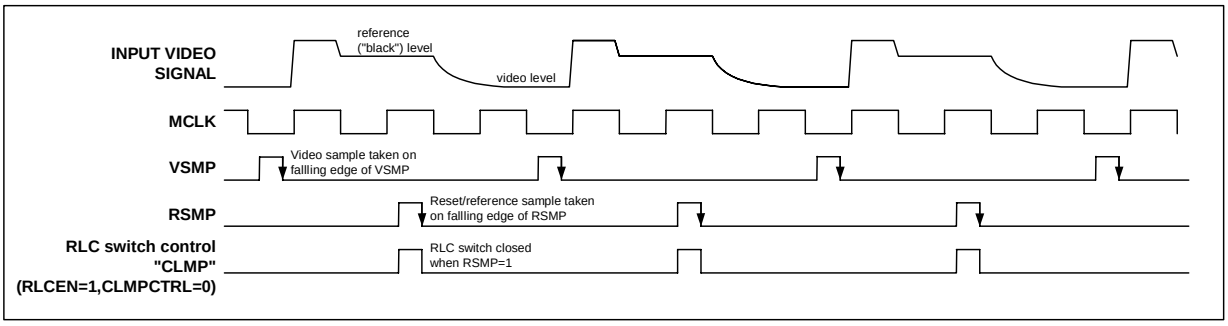


Figure 9 Reset Level Clamp Operation (CLAMPCTRL=0), CDS operation shown, non-CDS also possible

In situations where the input video signal does not have a stable reference level it may be necessary to clamp only during those pixels which have a known state (e.g. the dummy, or "black" pixels at the

start or end of a line on most image sensors). This is known as line-clamping and relies on the input capacitor to hold the DC level between clamp intervals. In non-CDS mode (CDS=0) this can be done directly by controlling the RSMP input pin to go high during the black pixels only.

Alternatively it is possible to use RSMP to identify the black pixels and enable the clamp at the same time as the input is being sampled (i.e. when VSMP is high and RSMP is high). This mode is enabled by setting CLAMPCTRL=1 and the operation is shown in Figure 10.

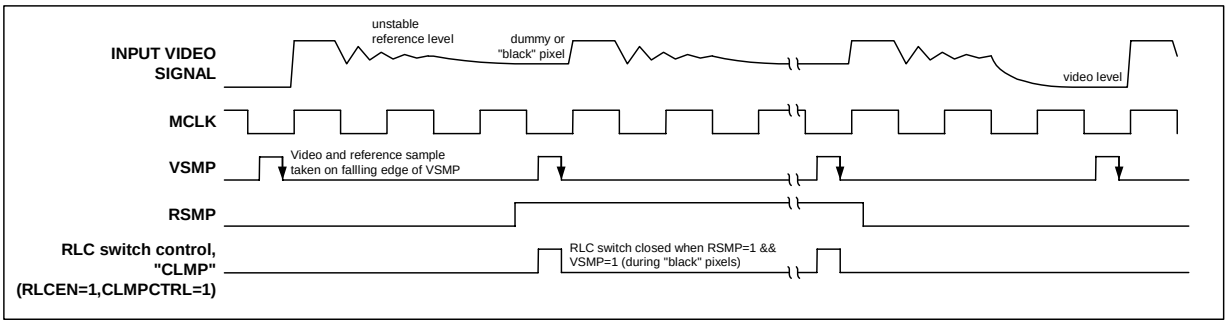


Figure 10 Reset Level Clamp Operation (CLAMPCTRL=1), non-CDS mode only

RLCEN	CLAMPCTRL	OUTCOME	USE
0	X	RLC is not enabled. RLC switch is always open.	When input is DC coupled and within supply rails.
1	0	RLC switch is controlled directly from RSMP input pin: RSMP=0: switch is open RMSP=1: switch is closed	When user explicitly provides a reset sample signal and the input video waveform has a suitable reset level.
1	1	VSMP applied as normal, RSMP is used to indicate the location of black pixels RLC switch is controlled by logical combination of RSMP and VSMP: RSMP && VSMP = 0: switch is open RSMP && VSMP = 1: switch is closed	When clamping during the video period of black pixels or there is no stable per-pixel reference level. This method of operation is generally only sensible in non-CDS mode.

Table 2 Reset Level Clamp Control Summary

CDS/NON-CDS PROCESSING

For CCD type input signals, containing a fixed reference/reset level, the signal may be processed using Correlated Double Sampling (CDS), which will remove pixel-by-pixel common mode noise. With CDS processing the input waveform is sampled at two different points in time for each pixel, once during the reference/reset level and once during the video level. To sample using CDS, register bit CDS must be set to 1 (default). This causes the signal reference to come from the video reference level as shown in Figure 11.

The video sample is always taken on the falling edge of the input VSMP signal (VS). In CDS-mode the reset level is sampled on the falling edge of the RSMP input signal (RS).

For input signals that do not contain a reference/reset level (e.g. CIS sensor signals), non-CDS processing is used (CDS=0). In this case, the video level is processed with respect to the voltage on pin VRLC/VBIAS. The VRLC/VBIAS voltage is sampled at the same time as VSMP samples the video level in this mode.

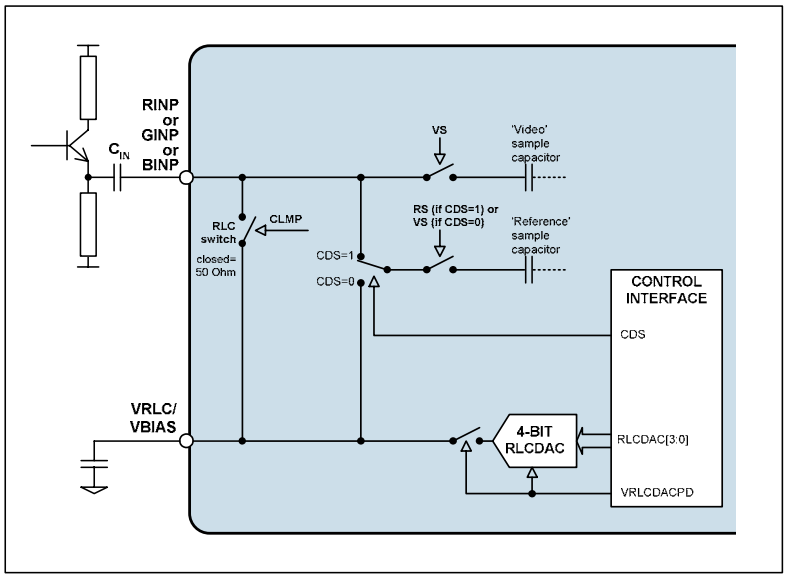


Figure 11 CDS/non-CDS Input Configuration

OFFSET ADJUST AND PROGRAMMABLE GAIN

The output from the CDS block is a differential signal, which is added to the output of an 8-bit Offset DAC to compensate for offsets and then amplified by a 9-bit PGA. The gain and offset for each channel are independently programmable by writing to control bits DAC[7:0] and PGA[8:0].

The gain characteristic of the WM8215 PGA is shown in Figure 12. Figure 13 shows the maximum device input voltage that can be gained up to match the ADC full-scale input range (default=2V).

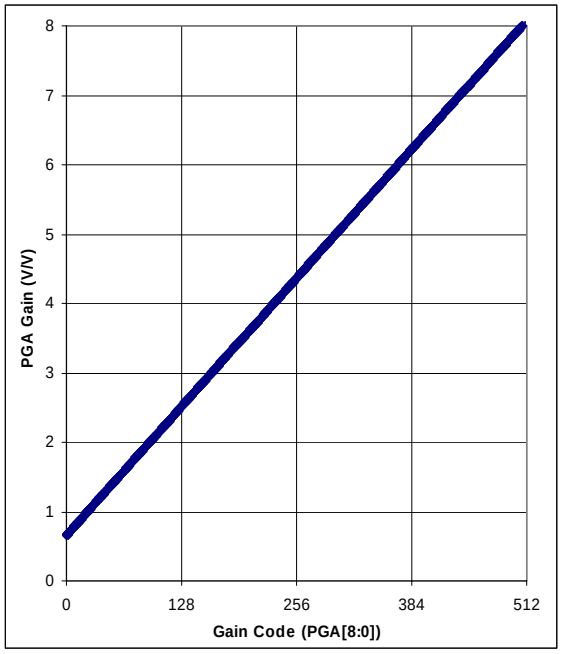


Figure 12 PGA Gain Characteristic

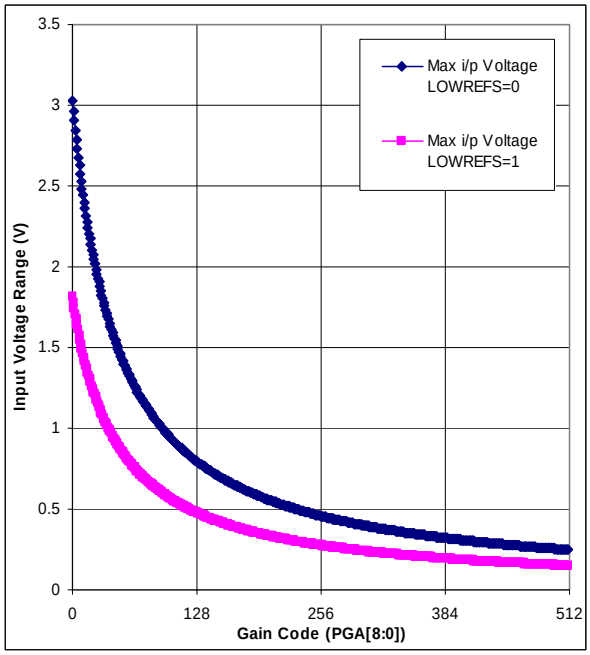


Figure 13 Peak Input Voltage to Match ADC Full-scale Range

ADC INPUT BLACK LEVEL ADJUST

The output from the PGA can be offset to match the full-scale range of the differential ADC (2*[VRT-VRB]).

For negative-going input video signals, a black level (zero differential) output from the PGA should be offset to the top of the ADC range by setting register bits PGAFS[1:0]=10. This will give an output code of 3FF (hex) from the WM8215 for zero input. If code zero is required for zero differential input then the INVOP bit should be set.

For positive going input signals the black level should be offset to the bottom of the ADC range by setting PGAFS[1:0]=11. This will give an output code of 000 (hex) from the WM8215 for zero input.

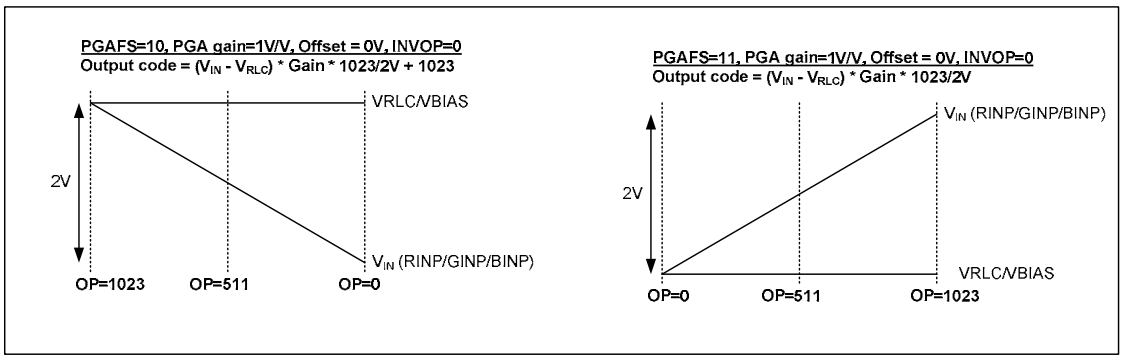


Figure 14 ADC Input Black Level Adjust Settings

OVERALL SIGNAL FLOW SUMMARY

Figure 15 represents the processing of the video signal through the WM8215.

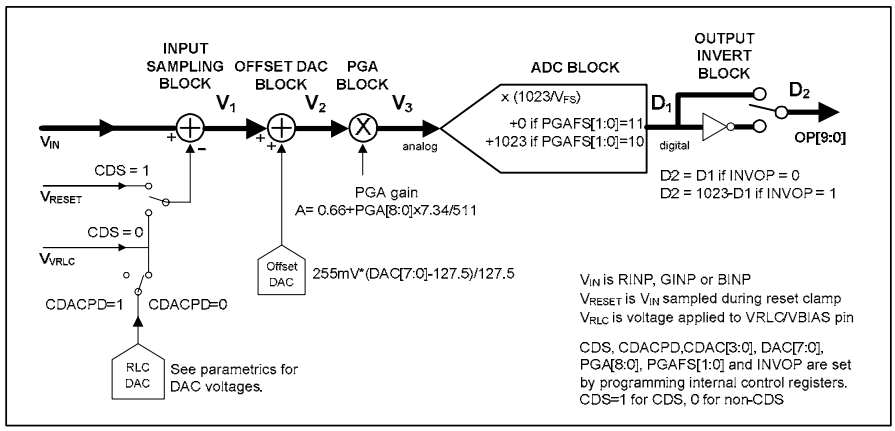


Figure 15 Overall Signal Flow

The **INPUT SAMPLING BLOCK** produces an effective input voltage $\mathbf{V_1}$. For CDS, this is the difference between the input video level V_{IN} and the input reset level V_{RESET}. For non-CDS this is the difference between the input video level V_{IN} and the voltage on the VRLC/VBIAS pin, V_{VRLC}, optionally set via the RLC DAC.

The **OFFSET DAC BLOCK** then adds the amount of fine offset adjustment required to move the black level of the input signal towards 0V, producing $\mathbf{V_2}$.

The **PGA BLOCK** then amplifies the white level of the input signal to maximise the ADC range, outputting voltage $\mathbf{V_3}$.

The **ADC BLOCK** then converts the analogue signal, $\mathbf{V_3}$, to a 10-bit unsigned digital output, $\mathbf{D_1}$.

The digital output is then inverted, if required, through the **OUTPUT INVERT BLOCK** to produce $\mathbf{D_2}$.

CALCULATING THE OUTPUT CODE FOR A GIVEN INPUT

The following equations describe the processing of the video and reset level signals through the WM8215.

INPUT SAMPLING BLOCK: INPUT SAMPLING AND REFERENCING

If CDS = 1, (i.e. CDS operation) the previously sampled reset level, V_{RESET}, is subtracted from the input video, V_{IN} (= RINP, GINP or BINP).

$$\mathbf{V_1} = V_{IN} - V_{RESET} \quad \text{Eqn. 1}$$

If CDS = 0, (non-CDS operation) the simultaneously sampled voltage on pin VRLC is subtracted instead.

$$\mathbf{V_1} = V_{IN} - V_{VRLC} \quad \text{Eqn. 2}$$

If VRLCDACPD = 1, V_{VRLC} is an externally applied voltage on pin VRLC/VBIAS.

If VRLCDACPD = 0, V_{VRLC} is the output from the internal RLC DAC.

$$V_{VRLC} = (V_{RLCSTEP} * \text{RLC DAC[3:0]}) + V_{RLCBOT} \quad \text{Eqn. 3}$$

$V_{RLCSTEP}$ is the step size of the RLC DAC and V_{RLCBOT} is the minimum output of the RLC DAC.

OFFSET DAC BLOCK: OFFSET (BLACK-LEVEL) ADJUST

The resultant signal $\mathbf{V_1}$ is added to the Offset DAC output.

$$\mathbf{V_2} = \mathbf{V_1} + \{255\text{mV} * (\text{DAC[7:0]}-127.5)\} / 127.5 \quad \text{Eqn. 4}$$

PGA NODE: GAIN ADJUST

The signal is then multiplied by the PGA gain.

$$\mathbf{V_3} = \mathbf{V_2} * (0.66 + \text{PGA[8:0]}x7.34/511) \quad \text{Eqn. 5}$$

ADC BLOCK: ANALOGUE-DIGITAL CONVERSION

The analogue signal is then converted to a 10-bit unsigned number, with input range configured by PGAFS[1:0].

$$\mathbf{D_1}[9:0] = \text{INT}\{ (\mathbf{V_3}/V_{FS}) * 1023\} \quad \text{PGAFS[1:0]} = 11 \quad \text{Eqn. 7}$$

$$\mathbf{D_1}[9:0] = \text{INT}\{ (\mathbf{V_3}/V_{FS}) * 1023\} + 1023 \quad \text{PGAFS[1:0]} = 10 \quad \text{Eqn. 8}$$

where the ADC full-scale range, V_{FS} = 2V when LOWREFS=0 and V_{FS} = 1.2V when LOWREFS=1.

OUTPUT INVERT BLOCK: POLARITY ADJUST

The polarity of the digital output may be inverted by control bit INVOP.

$$\mathbf{D_2}[9:0] = \mathbf{D_1}[9:0] \quad (\text{INVOP} = 0) \quad \text{Eqn. 9}$$

$$\mathbf{D_2}[9:0] = 1023 - \mathbf{D_1}[9:0] \quad (\text{INVOP} = 1) \quad \text{Eqn. 10}$$

REFERENCES

The ADC reference voltages are derived from an internal bandgap reference, and buffered to pins VRT and VRB where they must be decoupled to ground. Pin VRX is driven by a similar buffer, and also requires decoupling. The output buffer from the RLCDAC also requires decoupling at pin VRLC/VBIAS.

The ADC references can be switched from the default values (VRT=2.05V, VRB=1.05V, ADC input range=2V) to give a smaller ADC reference range (VRT=1.85V, VRB=1.25V, ADC input range=1.2V) under control of the LOWREFS register bit. Setting LOWREFS=1 allows smaller input signals to be accommodated.

Note:

When LOWREFS = 1 the output of the RLCDAC will scale if RLCDACRNG = 1. The max output from RLCDAC will change from 2.05 to 1.85V and the step size will proportionally reduce.

POWER MANAGEMENT

Power management for the device is performed via the Control Interface. By default the device is fully enabled. The EN bit allows the device to be fully powered down when set low. Individual blocks can be powered down using the bits in Setup Register 5. When in one or two channel mode the unused input channels are automatically disabled to reduce power consumption.

LINE-BY-LINE OPERATION

Certain linear sensors give colour output on a line-by-line basis (i.e. a full line of red pixels followed by a line of green pixels followed by a line of blue pixels). Often the sensor will have only a single output onto which these outputs are time multiplexed.

The WM8215 can accommodate this type of input by setting the LINEBYLINE register bit high. When in this mode the green and blue input PGAs are disabled to save power. The analogue input signal should be connected to the RINP pin. The offset and gain values that are applied to the Red input channel can be selected, by internal multiplexers, to come from the Red, Green or Blue offset and gain registers. This allows the gain and offset values for each of the input colours to be setup individually at the start of a scan.

When register bit ACYC=0, the gain and offset multiplexers are controlled via the INTM[1:0] register bits. When INTM=00, the red offset and gain control registers are used to control the Red input channel. Likewise, INTM=01 selects the green offset and gain registers and INTM=10 selects the blue offset and gain registers to control the Red input channel.

When register bit ACYC=1, 'auto-cycling' is enabled, and the input channel switches to the next offset and gain registers in the sequence when a pulse is applied to the RSMP input pin. The sequence is Red $\rightarrow$ Green $\rightarrow$ Blue $\rightarrow$ Red… offset and gain registers applied to the single input channel. A write to the Auto-cycle reset register (address 05h) will reset the sequence to a known state (Red registers selected).

When auto-cycling is enabled, the RSMP pin alone cannot be used to control reset level clamping. Reset level clamping may be enabled in this situation by setting the CLAMPCTRL and RLCEN bits so that the logical AND of RSMP and VSMP closes the clamp switch.

Additionally, when auto-cycling is enabled, the RSMP pin cannot be used for reset sampling (i.e. CDS must be set to 0).

CONTROL INTERFACE

The internal control registers are programmable via the serial digital control interface. The register contents can be read back via the serial interface on pin OP[9]/SDO.

It is recommended that a software reset is carried out after the power-up sequence, before writing to any other register. This ensures that all registers are set to their default values (as shown in Table 5).

SERIAL INTERFACE: REGISTER WRITE

Figure 16 shows register writing in serial mode. Three pins, SCK, SDI and SEN are used. A six-bit address (a5, 0, a3, a2, a1, a0) is clocked in through SDI, MSB first, followed by an eight-bit data word (b7, b6, b5, b4, b3, b2, b1, b0), also MSB first. Setting address bit a4 to 0 indicates that the operation is a register write. Each bit is latched on the rising edge of SCK. When the data has been shifted into the device, a pulse is applied to SEN to transfer the data to the appropriate internal register.

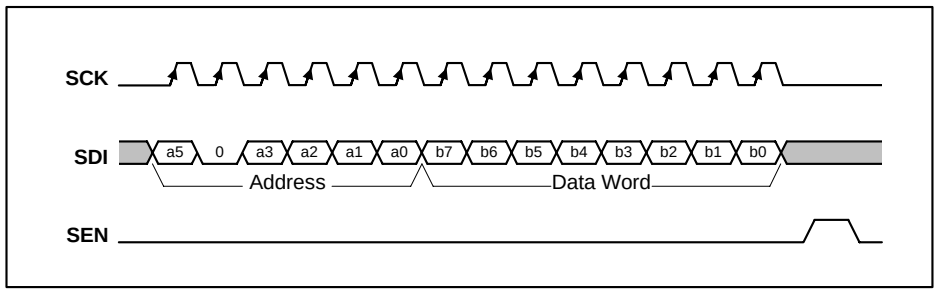


Figure 16 Serial Interface Register Write

A software reset is carried out by writing to Address “000100” with any value of data, (i.e. Data Word = XXXXXXXX).

SERIAL INTERFACE: REGISTER READ-BACK

Figure 17 shows register read-back in serial mode. Read-back is initiated by writing to the serial bus as described above but with address bit a4 set to 1, followed by an 8-bit dummy data word. Writing address (a5, 1, a3, a2, a1, a0) will cause the contents (d7, d6, d5, d4, d3, d2, d1, d0) of corresponding register (a5, 0, a3, a2, a1, a0) to be output MSB first on pin SDO (on the falling edge of SCK). Note that pin SDO is shared with an output pin, OP[9], therefore OEB should always be held low and the OPD register bit should be set low when register read-back data is expected on this pin. The next word may be read in to SDI while the previous word is still being output on SDO.

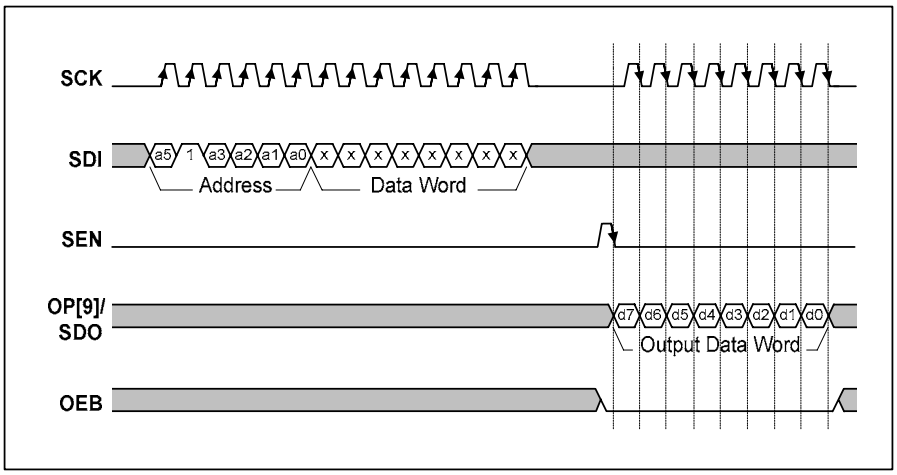


Figure 17 Serial Interface Register Read-back

NORMAL OPERATING MODES

Table 3 below shows the normal operating modes of the device. The MCLK speed can be specified along with the MCLK:VSMP ratio to achieve the desired sample rate.

NUMBER OF CHANNELS	DESCRIPTION	CDS AVAILABLE	MAXIMUM SAMPLE RATE	TIMING REQUIREMENTS	CHANNEL MODE SETTINGS
3	Three channel Pixel-by-Pixel	YES	20 MSPS	MCLK max = 60MHz Minimum MCLK:VSMP ratio = 3:1	MONO = 0 TWOCHAN = 0
2	Two channel Pixel-by-Pixel	YES	30 MSPS	MCLK max = 60MHz Minimum MCLK:VSMP ratio = 2:1	MONO = 0 TWOCHAN = 1
1	One channel Pixel-by-Pixel	YES	45 MSPS	MCLK max = 45MHz Minimum MCLK:VSMP ratio = 1:1	MONO = 1 TWOCHAN = 0

Table 3 WM8215 Normal Operating Modes

Note: In one channel mode the WM8215 can operate at 60MHz but DNL/INL values cannot be guaranteed.

Table 4 below shows the different channel mode register settings required to operate the 8215 in 1, 2 and 3 channel modes.

MONO	TWOCHAN	CHAN[1:0]	MODE DESCRIPTION
0	0	XX	3-channel (colour mode)
0	1	XX	2-channel (Blue PGA disabled)
1	0	00	1-channel (monochrome) mode. Red channel selected, Green and Blue PGAs disabled.
1	0	01	1-channel (monochrome) mode. Green channel selected, Red and Blue PGAs disabled.
1	0	10	1-channel (monochrome) mode. Blue channel selected, Red and Green PGAs disabled.
1	0	11	Invalid mode
1	1	XX	Invalid mode

Table 4 Sampling Mode Summary

Note: Unused input pins should be connected to AGND, unless reset level clamping is used.

DEVICE CONFIGURATION

REGISTER MAP

The following table describes the location of each control bit used to determine the operation of the WM8215.

ADDRESS <a5:a0>	DESCRIPTION	DEF (hex)	RW	BIT							
				b7	b6	b5	b4	b3	b2	b1	b0
000001 (01h)	Setup Reg 1	03	RW	0	0	PGAFS[1]	PGAFS[0]	TWOCHAN	MONO	CDS	EN
000010 (02h)	Setup Reg 2	20	RW	DEL[1]	DEL[0]	RLCDACRNG	LOWREFS	OPD	INVOP	0	0
000011 (03h)	Setup Reg 3	1F	RW	CHAN[1]	CHAN[0]	0	1	RLCDAC[3]	RLCDAC[2]	RLCDAC[1]	RLCDAC[0]
000100 (04h)	Software Reset	00	W								
000101 (05h)	Auto-cycle Reset	00	W								
000110 (06h)	Setup Reg 4	00	RW	0	0	0	0	INTM[1]	INTM[0]	ACYC	LINEBYLINE
000111 (07h)	Setup Reg 5	00	RW	0	VRXPD	ADCREFPD	VRLCDACPD	ADCPD	BLUPD	GRNPD	REDPD
001000 (08h)	Setup Reg 6	20	RW	0	CLAMPCTRL	RLCEN	0	0	0	0	0
001001 (09h)	Reserved	00	RW	0	0	0	0	0	0	0	0
001010 (0Ah)	Reserved	00	RW	0	0	0	0	0	0	0	0
001011 (0Bh)	Reserved	00	RW	0	0	0	0	0	0	0	0
001100 (0Ch)	Reserved	00	RW	0	0	0	0	0	0	0	0
100000 (20h)	DAC Value (Red)	80	RW	DACR[7]	DACR[6]	DACR[5]	DACR[4]	DACR[3]	DACR[2]	DACR[1]	DACR[0]
100001 (21h)	DAC Value (Green)	80	RW	DACG[7]	DACG[6]	DACG[5]	DACG[4]	DACG[3]	DACG[2]	DACG[1]	DACG[0]
100010 (22h)	DAC Value (Blue)	80	RW	DACB[7]	DACB[6]	DACB[5]	DACB[4]	DACB[3]	DACB[2]	DACB[1]	DACB[0]
100011 (23h)	DAC Value (RGB)	-	W	DACRGB[7]	DACRGB[6]	DACRGB[5]	DACRGB[4]	DACRGB[3]	DACRGB[2]	DACRGB[1]	DACRGB[0]
100100 (24h)	PGA Gain LSB (Red)	00	RW	0	0	0	0	0	0	0	PGAR[0]
100101 (25h)	PGA Gain LSB (Green)	00	RW	0	0	0	0	0	0	0	PGAG[0]
100110 (26h)	PGA Gain LSB (Blue)	00	RW	0	0	0	0	0	0	0	PGAB[0]
100111 (27h)	PGA Gain LSB (RGB)	-	W	0	0	0	0	0	0	0	PGARGB[0]
101000 (28h)	PGA Gain MSBs (Red)	0C	RW	PGAR[8]	PGAR[7]	PGAR[6]	PGAR[5]	PGAR[4]	PGAR[3]	PGAR[2]	PGAR[1]
101001 (29h)	PGA Gain (Green)	0C	RW	PGAG[8]	PGAG[7]	PGAG[6]	PGAG[5]	PGAG[4]	PGAG[3]	PGAG[2]	PGAG[1]
101010 (2Ah)	PGA Gain (Blue)	0C	RW	PGAB[8]	PGAB[7]	PGAB[6]	PGAB[5]	PGAB[4]	PGAB[3]	PGAB[2]	PGAB[1]
101011 (2Bh)	PGA Gain (RGB)	-	W	PGARGB[8]	PGARGB[7]	PGARGB[6]	PGARGB[5]	PGARGB[4]	PGARGB[3]	PGARGB[2]	PGARGB[1]

Table 5 Register Map

REGISTER MAP DESCRIPTION

The following table describes the function of each of the control bits shown in Table 5

ADDRESS <A5:A0>	REGISTER	BIT NO	BIT NAME(S)	DEFAULT	DESCRIPTION
000001 (01h)	Setup Register 1	0	EN	1	Global Enable 0 = complete power down, 1 = fully active (individual blocks can be disabled using individual powerdown bits – see setup register 5).
		1	CDS	1	Select correlated double sampling mode: 0 = single ended mode, 1 = CDS mode.
		2	MONO	0	Sampling mode select 0 = other mode (2 or 3-channel) 1 = Monochrome (1-channel) mode. Input channel selected by CHAN[1:0] register bits, unused channel is powered down. TWOCHAN and MONO should not be set concurrently
		3	TWOCHAN	0	Sampling mode select 0 = other mode (1 or 3-channel) 1 = 2-channel mode. Inputs channels are Red and Green, Blue channel is powered down. TWOCHAN and MONO should not be set concurrently
		5:4	PGAFS[1:0]	00	Offsets PGA output to optimise the ADC range for different polarity sensor output signals. Zero differential PGA input signal gives: 0x = Invalid option. Either '10' or '11' must be set. 10 = Full-scale positive output (OP=1023) – use for negative going video. NB, Set INVOP=1 if zero differential input should give a zero output code with negative going video. 11 = Full-scale negative output (OP=0) - use for positive going video
		7:6	Not Used	00	Must be set to 0

ADDRESS <A5:A0>	REGISTER	BIT NO	BIT NAME(S)	DEFAULT	DESCRIPTION
000010 (02h)	Setup Register 2	1:0	Not Used	00	Must be set to 0
		2	INVOP	0	Digitally inverts the polarity of output data. 0 = negative going video gives negative going output, 1 = negative-going video gives positive going output data.
		3	OPD	0	Output Disable. This works with the OEB pin to control the output pins. 0=Digital outputs enabled, 1=Digital outputs high impedance
					OEB (pin) / OPD / OP pins
					0 / 0 / Enabled
					0 / 1 / High Impedance
					1 / 0 / High Impedance
					1 / 1 / High Impedance
		4	LOWREFS	0	Reduces the ADC reference range (2*[VRT-VRB]), thus changing the max/min input video voltages (ADC ref range/PGA gain). 0 = ADC reference range = 2.0V 1 = ADC reference range = 1.2V
		5	RLCDACRNG	1	Sets the output range of the RLCDAC. 0 = RLCDAC ranges from 0 to AVDD (approximately), 1 = RLCDAC ranges from 0 to VRT (approximately).
		7:6	DEL[1:0]	00	Controls the latency from sample to data appearing on output pins
					DEL / Latency
					00 / 7 MCLK periods
					01 / 8 MCLK periods
					10 / 9 MCLK periods
					11 / 10 MCLK periods
000011 (03h)	Setup Register 3	3:0	RLCDAC[3:0]	1111	Controls RLCDAC driving VRLC/VBIAS pin to define single ended signal reference voltage or Reset Level Clamp voltage. See Electrical Characteristics section for ranges.
		4	Reserved	1	Must be set to one
		5	Reserved	0	Must be set to zero
		7:6	CHAN[1:0]	00	When MONO=0 this register bit has no effect Monochrome mode channel select. 00 = Red channel select 01 = Green channel select 10 = Blue channel select 11 = Reserved
000100 (04h)	Software Reset				Any write to Software Reset causes all cells to be reset. It is recommended that a software reset be performed after a power-up before any other register writes.
000101 (05h)	Auto-cycle Reset				Any write to Auto-cycle Reset causes the auto-cycle counter to reset to RINP. This function is only required when LINEBYLINE = 1.
000110 (06h)	Setup Register 4	0	LINEBYLINE	0	Selects line by line operation. Line by line operation is intended for use with systems which operate one line at a time but with up to three colours shared on that one output. 0 = normal operation, 1 = line by line operation. When line by line operation is selected MONO is forced to 1 and CHAN[1:0] to 00 internally, ensuring that the correct internal timing signals are produced. Green and Blue PGAs are also disabled to save power.

ADDRESS <A5:A0>	REGISTER	BIT NO	BIT NAME(S)	DEFAULT	DESCRIPTION
		1	ACYC	0	When LINEBYLINE = 0 this bit has no effect. When LINEBYLINE = 1 this bit determines the function of the RSMP input pin and the offset/gain register controls. 0 = RSMP pin enabled for either reset sampling (CDS) or Reset Level Clamp control. Internal selection of gain/offset multiplexers using INTM[1:0] register bits. 1 = Auto-cycling enabled by pulsing the RSMP input pin. This means that each time a pulse is applied to this pin the single input channel will switch to the next offset register and gain register in the sequence. The sequence is Red->Green->Blue->Red… offset and gain registers applied to the red input channel. When auto-cycling is enabled, the RSMP pin alone cannot be used to control reset level clamping. Reset level clamping may be enabled in this situation by setting the CLAMPCTRL and RLCEN bits so that he logical AND of RSMP and VSMP closes the clamp switch. When auto-cycling is enabled, the RSMP pin cannot be used for reset sampling (i.e. CDS must be set to 0).
		3:2	INTM[1:0]	00	When LINEBYLINE=0 or ACYC=1 this bit has no effect. When LINEBYLINE=1 and ACYC=0: Controls the PGA/offset mux selector: 00 = Red PGA/Offset registers applied to input channel 01 = Green PGA/Offset registers applied to input channel 10 = Blue PGA/Offset registers applied to input channel 11 = Reserved.
		7:4	Reserved	0000	Must be set to 0
000111 (07h)	Setup Register 5	0	REDPD	0	When set powers down red S/H, PGA
		1	GRNPD	0	When set powers down green S/H, PGA
		2	BLUPD	0	When set powers down blue S/H, PGA
		3	ADCPD	0	When set powers down ADC. Allows reduced power consumption without powering down the references which have a long time constant when switching on/off due to the external decoupling capacitors.
		4	VRLCDACPD	0	When set powers down 4-bit RLCDAC, setting the output to a high impedance state and allowing an external reference to be driven in on the VRLC/VBIAS pin.
		5	ADCREFPD	0	When set disables VRT, VRB buffers to allow external references to be used.
		6	VRXPD	0	When set disables VRX buffer to allow an external reference to be used.
		7	Not Used	0	Must be set to 0
001000 (08h)	Setup Register 6	4:0	Not Used	00000	Must be set to 0
		5	RLCEN	1	Reset Level Clamp Enable. When set Reset Level Clamping is enabled. The method of clamping is determined by CLAMPCTRL.
		6	CLAMPCTRL	0	0 = RLC switch is controlled directly from RSMP input pin: RSMP = 0: switch is open RMSP = 1: switch is closed 1 = RLC switch is controlled by logical combination of RSMP and VSMP. RSMP && VSMP = 0: switch is open RSMP && VSMP = 1: switch is closed
		7	Reserved	0	Must be set to 0

ADDRESS <A5:A0>	REGISTER	BIT NO	BIT NAME(S)	DEFAULT	DESCRIPTION
100000 (20h)	Offset DAC (Red)	7:0	DACR[7:0]	10000000	Red channel 8-bit offset DAC value (mV) = 255*(DACR[7:0]-127.5)/127.5
100001 (21h)	Offset DAC (Green)	7:0	DACG[7:0]	10000000	Green channel 8-bit offset DAC value (mV) = 255*(DACG[7:0]-127.5)/127.5
100010 (22h)	Offset DAC (Blue)	7:0	DACB[7:0]	10000000	Blue channel 8-bit offset DAC value (mV) = 255*(DACB[7:0]-127.5)/127.5
100011 (23h)	Offset DAC (RGB)	7:0	DACRGB[7:0]	-	A write to this register location causes the red, green and blue offset DAC registers to be overwritten by the new value
100100 (24h)	PGA Gain LSB (Red)	0	PGAR[0]	0	This register bit forms the LSB of the red channel PGA gain code. PGA gain is determined by combining this register bit and the 8 MSBs contained in register address 28 hex.
		7:1	Reserved	0000000	Must be set to 0
100101 (25h)	PGA Gain LSB (Green)	0	PGAG[0]	0	This register bit forms the LSB of the green channel PGA gain code. PGA gain is determined by combining this register bit and the 8 MSBs contained in register address 29 hex.
		7:1	Reserved	0000000	Must be set to 0
100110 (26h)	PGA Gain LSB (Blue)	0	PGAB[0]	0	This register bit forms the LSB of the blue channel PGA gain code. PGA gain is determined by combining this register bit and the 8 MSBs contained in register address 2A hex.
		7:1	Reserved	0000000	Must be set to 0
100111 (27h)	PGA Gain LSB (RGB)	0	PGARGB[0]	-	Writing a value to this location causes red, green and blue PGA LSB gain values to be overwritten by the new value.
		7:1	Reserved	0000000	Must be set to 0
101000 (28h)	PGA gain MSBs (Red)	7:0	PGAR[8:1]	00001100	Bits 8 to 1 of red PGA gain. Combined with red LSB register bit to form complete PGA gain code. This determines the gain of the red channel PGA according to the equation: Red channel PGA gain (V/V) = 0.66 + PGAR[8:0]x7.34/511
101001 (29h)	PGA gain MSBs (Green)	7:0	PGAG[8:1]	00001100	Bits 8 to 1 of green PGA gain. Combined with green LSB register bit to form complete PGA gain code. This determines the gain of the green channel PGA according to the equation: Green channel PGA gain (V/V) = 0.66 + PGAG[8:0]x7.34/511
101010 (2Ah)	PGA gain MSBs (Blue)	7:0	PGAB[8:1]	00001100	Bits 8 to 1 of blue PGA gain. Combined with blue LSB register bit to form complete PGA gain code. This determines the gain of the blue channel PGA according to the equation: Blue channel PGA gain (V/V) = 0.66 + PGAB[8:0]x7.34/511
101011 (2Bh)	PGA gain MSBs (RGB)	7:0	PGARGB[8:1]	-	A write to this register location causes the red, green and blue PGA MSB gain registers to be overwritten by the new value.

Table 6 Register Control Bits

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

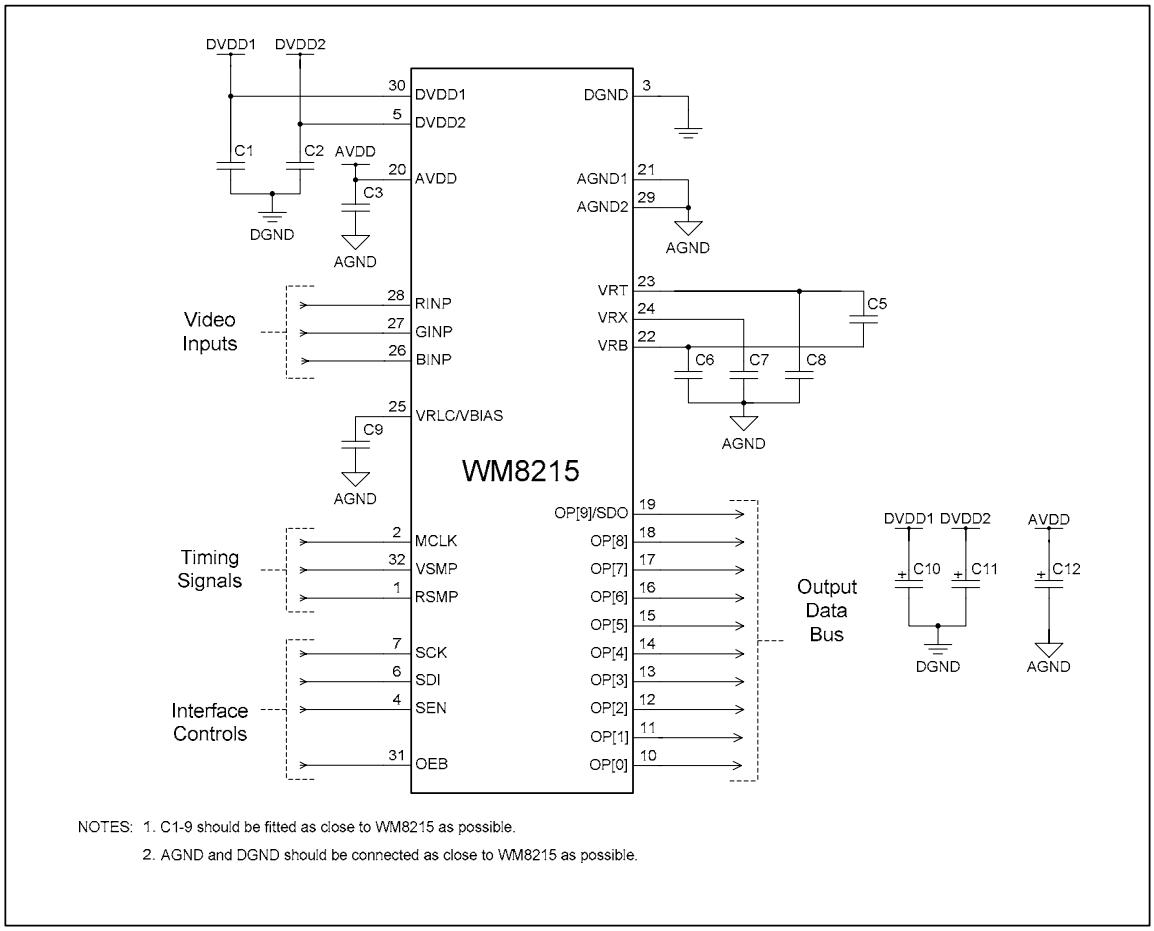


Figure 18 External Components Diagram

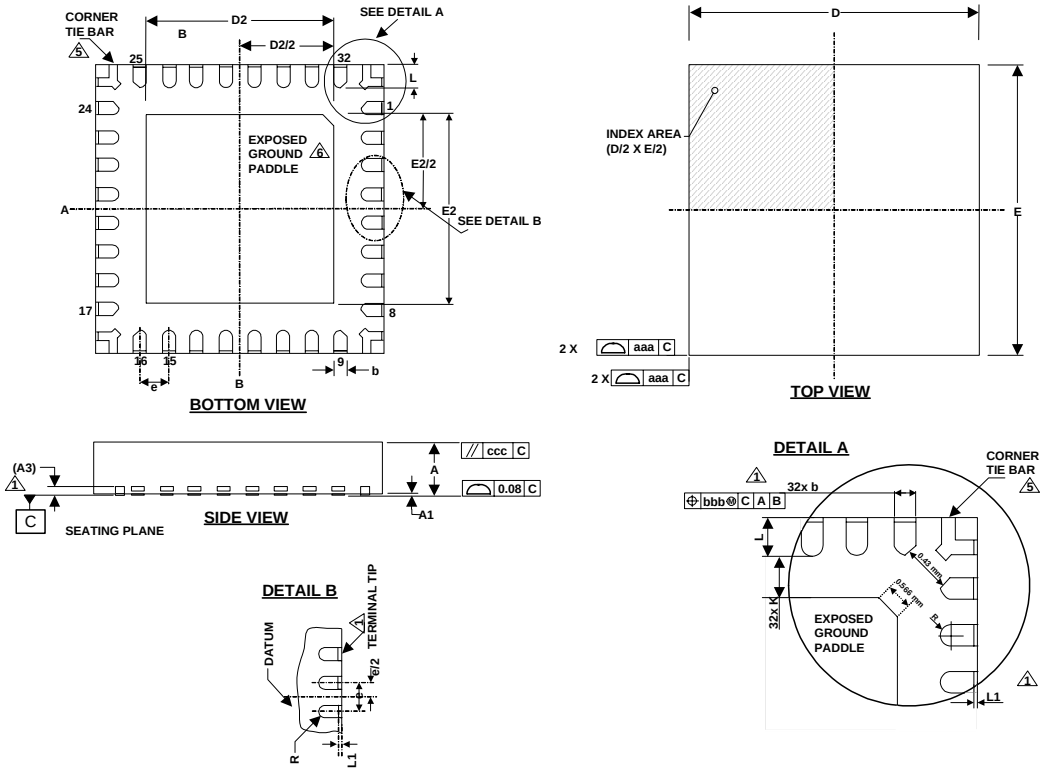
RECOMMENDED EXTERNAL COMPONENT VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1	100nF	De-coupling for DVDD1.
C2	100nF	De-coupling for DVDD2.
C3	100nF	De-coupling for AVDD.
C5	1µF	Ceramic de-coupling between VRT and VRB (non-polarised).
C6	100nF	De-coupling for VRB.
C7	100nF	De-coupling for VRX.
C8	100nF	De-coupling for VRT.
C9	100nF	De-coupling for VRLC.
C10	10µF	Reservoir capacitor for DVDD1.
C11	10µF	Reservoir capacitor for DVDD2.
C12	10µF	Reservoir capacitor for AVDD.

Table 7 External Components Descriptions

PACKAGE DIMENSIONS

FL: 32 PIN QFN PLASTIC PACKAGE 5 x 5 x 0.9 mm BODY, 0.50 mm LEAD PITCH **DM030.F**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.85	0.90	1.00	
A1	0	0.02	0.05	
A3		0.2 REF		
b	0.18	0.23	0.30	1
D		5.00 BSC		
D2	3.2	3.3	3.4	2
E		5.00 BSC		
E2	3.2	3.3	3.4	2
e		0.5 BSC		
L	0.35	0.4	0.45	
L1			0.1	1
R	b(min)/2			
K	0.20			
Tolerances of Form and Position				
aaa	0.15			
bbb	0.10			
ccc	0.10			
REF:	JEDEC, MO-220, VARIATION VHHD-2			

NOTES:
1. DIMENSION b APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL PULL BACK FROM PACKAGE SIDE WALL. MAXIMUM OF 0.1mm IS ACCEPTABLE. WHERE TERMINAL PULL BACK EXISTS, ONLY UPPER HALF OF LEAD IS VISIBLE ON PACKAGE SIDE WALL DUE TO HALF ETCHING OF LEADFRAME.
2. FALLS WITHIN JEDEC, MO-220 WITH THE EXCEPTION OF D2, E2:
   D2,E2: LARGER PAD SIZE CHOSEN WHICH IS JUST OUTSIDE JEDEC SPECIFICATION
3. ALL DIMENSIONS ARE IN MILLIMETRES
4. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
5. SHAPE AND SIZE OF CORNER TIE BAR MAY VARY WITH PACKAGE TERMINAL COUNT. CORNER TIE BAR IS CONNECTED TO EXPOSED PAD INTERNALLY.
6. REFER TO APPLICATION NOTE WAN_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.

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ADDRESS:

Wolfson Microelectronics plc

Westfield House

26 Westfield Road

Edinburgh

EH11 2QB

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

Email :: sales@wolfsonmicro.com