CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX866
V.22 bis Modem with AT Commands

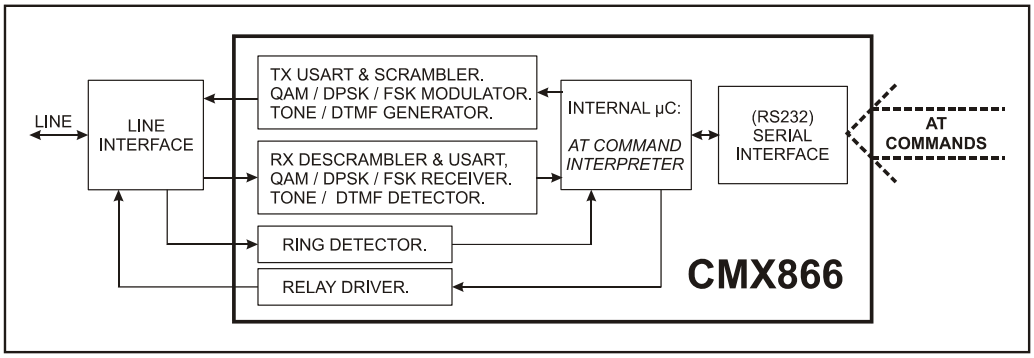
D/866/5 May 2008 Provisional Issue

Features

- **V.22 bis, V.22 and Bell 212A QAM/DPSK**
- **V.23, Bell 202, V.21 and Bell 103 FSK**
- **Integral AT Command Set with 'Fast Connect'**
- **V.23 and Bell 202 'Fast Turnaround'**
- **Support for Type 1 Caller Line Identification**
- **DTMF/Programmable Tones: Transmit and Receive**
- **'Zero-Power' and Powersave Standby Modes**
- **Low Power Operation**

Applications

- **Telephone Telemetry Systems**
- **Remote Utility Meter Reading**
- **Security Systems**
- **Industrial Control Systems**
- **Electronic Cash Terminals / ATMs**
- **Pay-Phones**
- **Cable TV Set-Top Boxes**
- **EPOS Terminals**



1.1 Brief Description

The CMX866 is a multi-standard modem for use in telephone based information and telemetry systems.

Control of the device is via AT commands over a simple 9600b/s serial interface, compatible with most types of host µController. An RS232 compatible interface can be created by the addition of a Level Converter. The data transmitted and received by the modem is also transferred over the same serial interface. The on-chip µController interprets these AT commands and controls an internal DSP, which provides the modem and anciliary functions such as Ring Detection, Call Progress Detection, Hook Switch control and DTMF autodialling. User-specific DSP functions are also available via the AT command set.

Hardware support is provided for V.23 and Bell 202 Fast Turnaround and for rapid return to AT Command mode. A Fast Connect mode has been implemented to reduce modem connection time. Flexible line driver and receive hybrid circuits are integrated on chip, requiring only passive external components to build a 2 or 4-wire line interface. Complete examples of 2-wire line interfaces to an external host µC and to an RS232 interface, including the additional components required for Type 1 CLI, are provided.

The device features a Hook Switch relay drive output and a Ring Detector circuit that remain operational when the CMX866 is in 'Zero-Power' or Powersave mode, providing an interrupt which can be used to wake up an external host µC, as well as the CMX866, when line voltage reversal or ringing is detected. The device is also able to detect off-hook parallel phones by monitoring voice activity on the line.

The CMX866 takes 5mA (typ.) from a single 2.7–5.5V supply and comes in 28-pin SSOP/SOIC packages.

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It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

1.2 Block Diagram

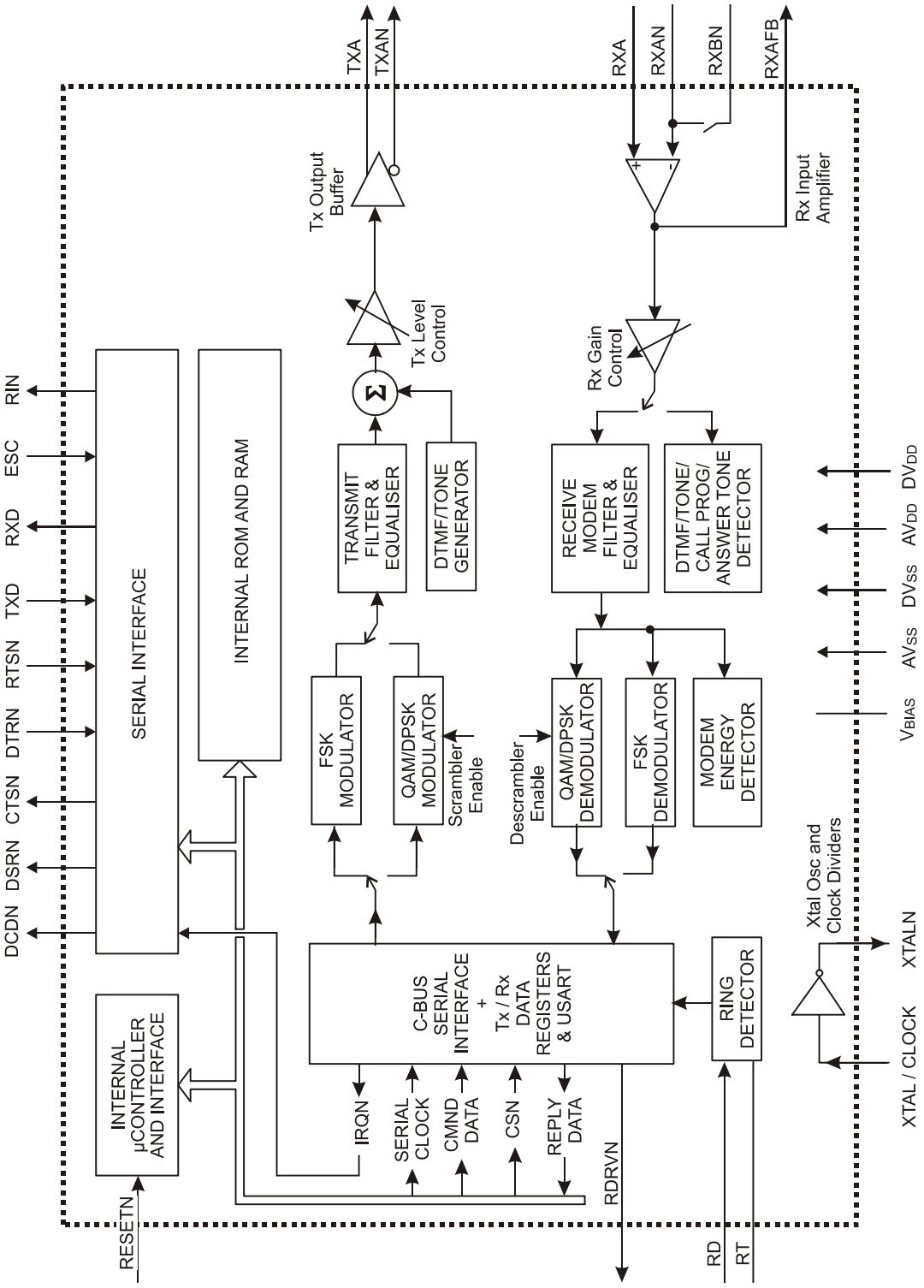


Figure 1 Block Diagram

1.3 Signal List

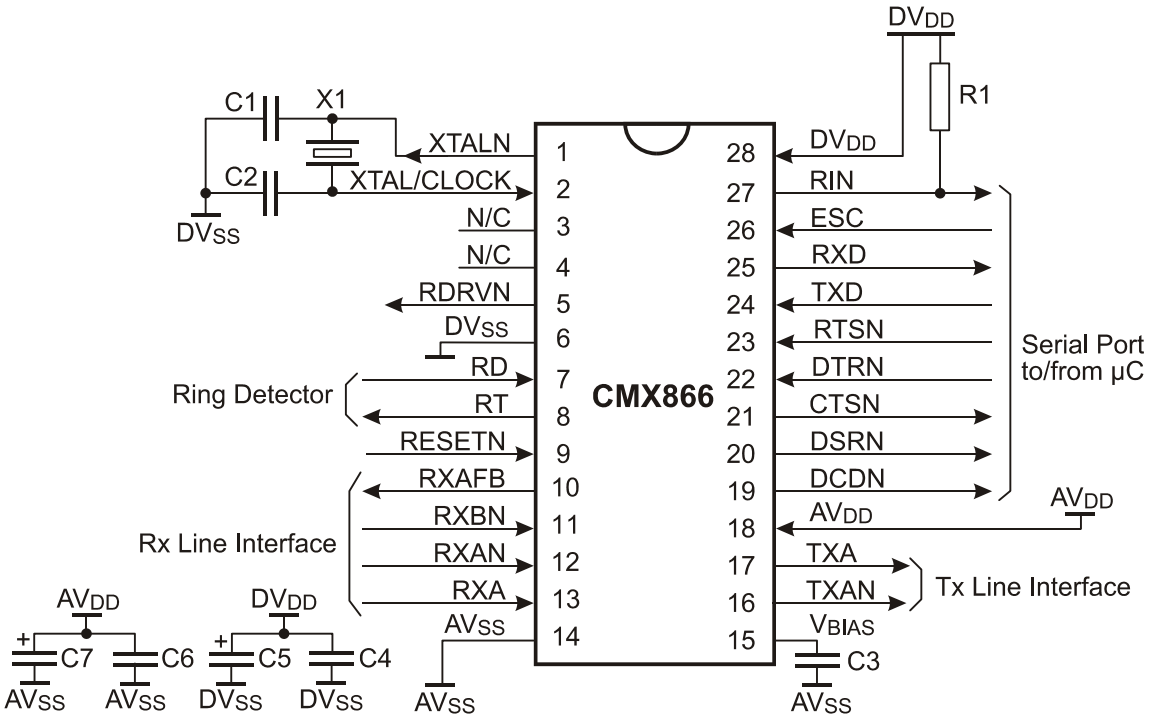
CMX866 D1/D6	Signal		Description
Pin No.	**Name**	**Type**	
1	XTALN	O/P	The output of the on-chip Xtal oscillator inverter.
2	XTAL/CLOCK	I/P	The input to the oscillator inverter from the Xtal circuit or external clock source.
3	N/C	~	Reserved for future use. Connect this pin to DVSS.
4	N/C	~	Reserved for future use. Connect this pin to DVSS.
5	RDRVN	O/P	Relay drive output, low resistance pull down to DVSS when active and medium resistance pull up to DVDD when inactive.
6	DVSS	Power	The negative supply rail for the digital on-chip blocks.
7	RD	I/P	Schmitt trigger input to the Ring signal detector. Connect to DVSS if Ring Detector not used.
8	RT	BI	Open drain output and Schmitt trigger input forming part of the Ring signal detector. Connect to DVDD if Ring Detector not used.
9	RESETN	I/P	Schmitt trigger input to an active-low reset pin. Connect to DVDD if no external reset signal used
10	RXAFB	O/P	The output of the Rx Input Amplifier.
11	RXBN	I/P	An alternative, switched inverting input to the Rx Input Amplifier, used to increase the amplifier gain for the detection of on-hook signals. If this input is not required, leave the pin disconnected.
12	RXAN	I/P	The inverting input to the Rx Input Amplifier
13	RXA	I/P	The non-inverting input to the Rx Input Amplifier. If this pin is to be connected to VBIAS then it should also be decoupled to AVSS locally.
14	AVSS	Power	The negative supply rail for the analogue on-chip blocks.
15	VBIAS	O/P	Internally generated bias voltage of approximately AVDD /2, except when the device is in Powersave or 'Zero-Power' modes, when VBIAS will discharge to AVSS. This pin should be decoupled to AVSS by a capacitor mounted close to the device pins.
16	TXAN	O/P	The inverted output of the Tx Output Buffer.
17	TXA	O/P	The non-inverted output of the Tx Output Buffer.

CMX866 D1/D6	Signal		Description
18	AVDD	Power	The positive supply rail for the analogue on-chip blocks. Levels and thresholds within the device are proportional to this voltage.
19	DCDN	O/P	The inverted DCD signal used for an RS232 interface with a Level Converter.
20	DSRN	O/P	The inverted DSR signal used for an RS232 interface with a Level Converter.
21	CTSN	O/P	The inverted CTS signal used for an RS232 interface with a Level Converter.
22	DTRN	I/P	The inverted DTR signal used for an RS232 interface with a Level Converter.
23	RTSN	I/P	The inverted RTS signal used for an RS232 interface with a Level Converter.
24	TXD	I/P	The non-inverted TD signal used for an RS232 interface with a Level Converter. This pin accepts data from the external host µC for transmission over the phone line.
25	RXD	O/P	The non-inverted RD signal used for an RS232 interface with a Level Converter. This pin sends data to the external host µC which was received over the phone line.
26	ESC	I/P	An auxiliary pin to force the CMX866 into Command Mode from Data Mode and remain off-hook. The ATO command will return the CMX866 to Data Mode. This pin should be connected to DVSS if not required.
27	RIN	O/P	The inverted RI signal used for an RS232 interface with a Level Converter. This is a 'wire-ORable' output for connection to an external host µC Interrupt Request input. This output is pulled down to DVSS when active and is high impedance when inactive. An external pullup resistor is required (eg. R1 in Figure 2a).
28	DVDD	Power	The positive supply rail for the digital on-chip blocks. Levels and thresholds within the device are proportional to this voltage.

Notes:

I/P = Input
O/P = Output
BI = Bidirectional
T/S = 3-state Output
NC = No Connection

1.4 External Components



C1, C2	22pF	C3, C4, C6	100nF
R1	100kΩ	C5, C7	10uF
X1	11.0592MHz	L1, L2	100nH (optional)

Resistors ±5%, capacitors ±20% unless otherwise stated.

Figure 2a Recommended External Components for Typical Application

This device is capable of detecting and decoding small amplitude signals. To achieve this DV_{DD}, AV_{DD} and V_{BIAS} should be decoupled and the receive path protected from extraneous in-band signals. It is recommended that the printed circuit board is laid out with both AV_{SS} and DV_{SS} ground planes in the CMX866 area, as shown in Figure 2b, with provision to make a link between them close to the CMX866. To provide a low impedance connection to ground, the decoupling capacitors (C3 – C7) must be mounted as close to the CMX866 as possible and connected directly to their respective ground plane. This will be achieved more easily by using surface mounted capacitors.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity. Apart from the decoupling capacitor shown (C3), no other loads are allowed. If V_{BIAS} needs to be used to set external analogue levels, it must be buffered with a high input impedance buffer.

The DV_{SS} connections to the Xtal oscillator capacitors C1 and C2 should also be of low impedance and preferably be part of the DV_{SS} ground plane to ensure reliable start up of the oscillator.

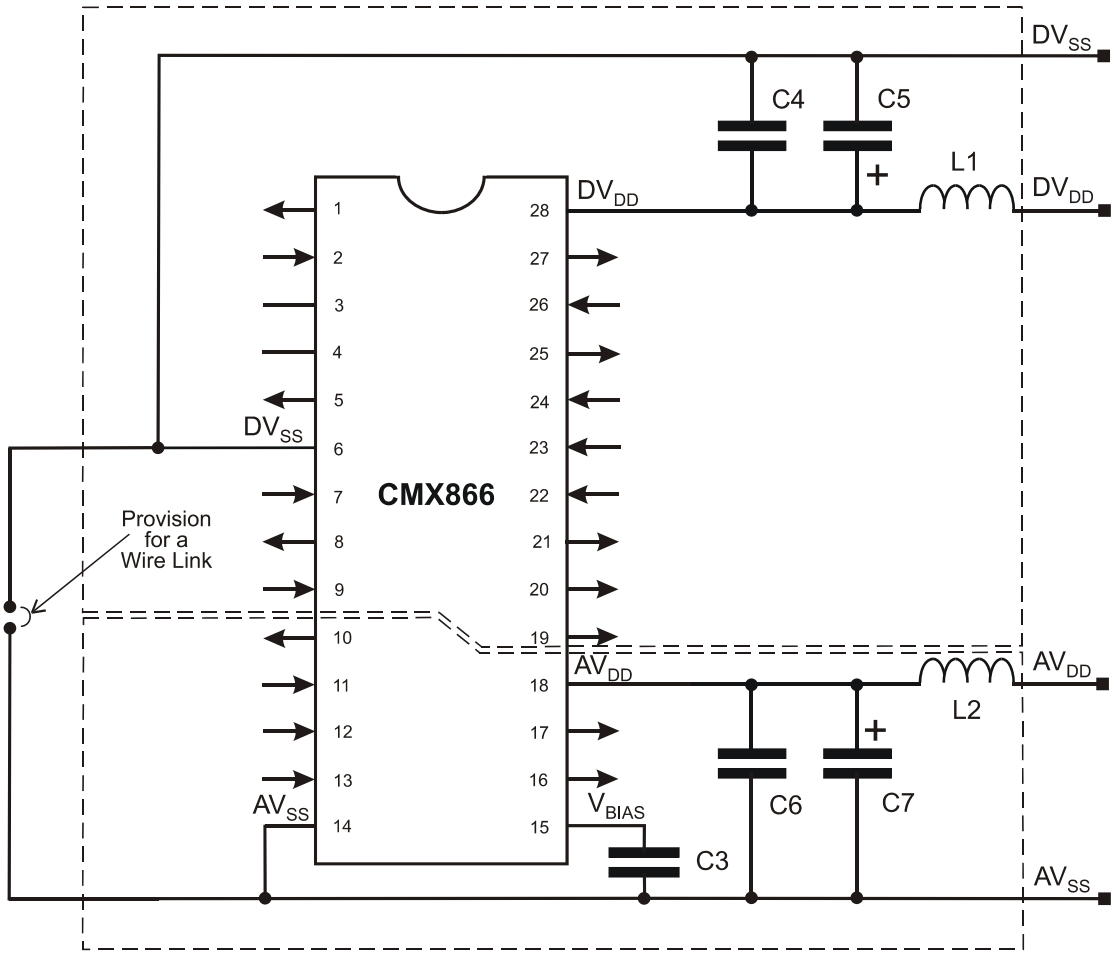


Figure 2b Recommended Power Supply Connections and De-coupling

ANALOGUE		**DIGITAL**	
C3, C6	100nF	C4	100nF
C7	10uF	C5	10uF
L2	100nH (optional, see note)	L1	100nH (optional, see note)

Note: The inductors L1 and L2 and the electrolytic capacitor C7 can be omitted without significantly degrading the system performance.

1.4.1 Ring Detector Interface

Figure 3 shows how the CMX866 may be used to detect the large amplitude Ringing signal voltage present on the 2-wire line at the start of an incoming telephone call.

The ring signal is usually applied at the subscriber's exchange as an ac voltage inserted in series with one of the telephone wires and will pass through either C20 and R20 or C21 and R21 to appear at the top end of R22 (point X in Figure 3) in a rectified and attenuated form.

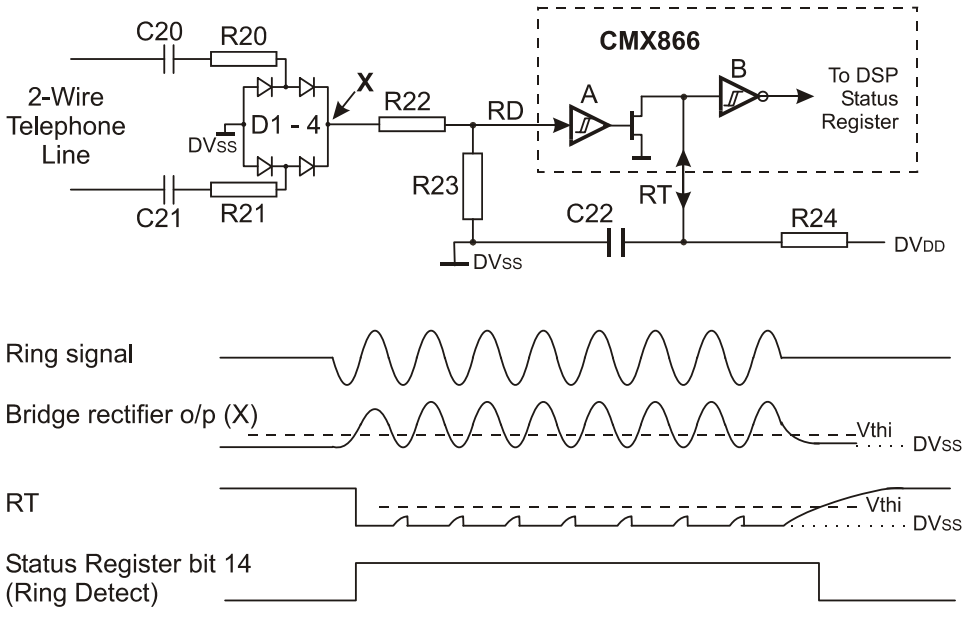
The signal at point X is further attenuated by the potential divider formed by R22 and R23 before being applied to the CMX866 RD input. If the amplitude of the signal appearing at RD is greater than the input threshold (Vthi) of Schmitt trigger 'A' then the N transistor connected to RT will be turned on, pulling the voltage at RT to DV_{SS} by discharging the external capacitor C22. The output of the Schmitt trigger 'B' will then go high, setting bit 14 (Ring Detect) of the DSP Status Register. The on-chip µController will then respond by setting pin RIN low.

The minimum amplitude ringing signal that is certain to be detected is:

$$(0.7 + Vthi \times [R20 + R22 + R23] / R23) \times 0.707 \quad Vrms$$

where Vthi is the high-going threshold voltage of the Schmitt trigger A (see section 1.7.1).

With R20-22 all 470kΩ as Figure 3, setting R23 to 68kΩ will guarantee detection of ringing signals of 40Vrms and above for DV_{DD} over the range 3 to 5V.



R20, 21, 22	470kΩ	C20, 21	0.1µF
R23	See text	C22	0.33µF
R24	470kΩ	D1-4	1N4004

Resistors ±5%, capacitors ±20%

Figure 3 Ring Signal Detector Interface Circuit

If the time constant of R24 and C22 is large enough then the voltage on RT will remain below the threshold of the 'B' Schmitt trigger for the duration of a ring cycle. The time for the voltage on RT to charge from DV_{SS} towards DV_{DD} can be derived from the formula:

$$V_{RT} = DV_{DD} \times [1 - \exp(-t/(R24 \times C22))]$$

As the Schmitt trigger high-going input threshold voltage (Vthi) has a minimum value of 0.56 x DV_{DD}, then the Schmitt trigger B output will remain high for a time of at least 0.821 x R24 x C22 following a pulse at RD. The values of R24 and C22 given in Figure 3 (470kΩ and 0.33μF) give a minimum RT charge time of 100msec, which is adequate for ring frequencies of 10Hz or above.

Note that this circuit will also respond to a telephone line voltage reversal. The external host μC can distinguish between a Ring signal and a line voltage reversal by measuring the time that pin RIN is low.

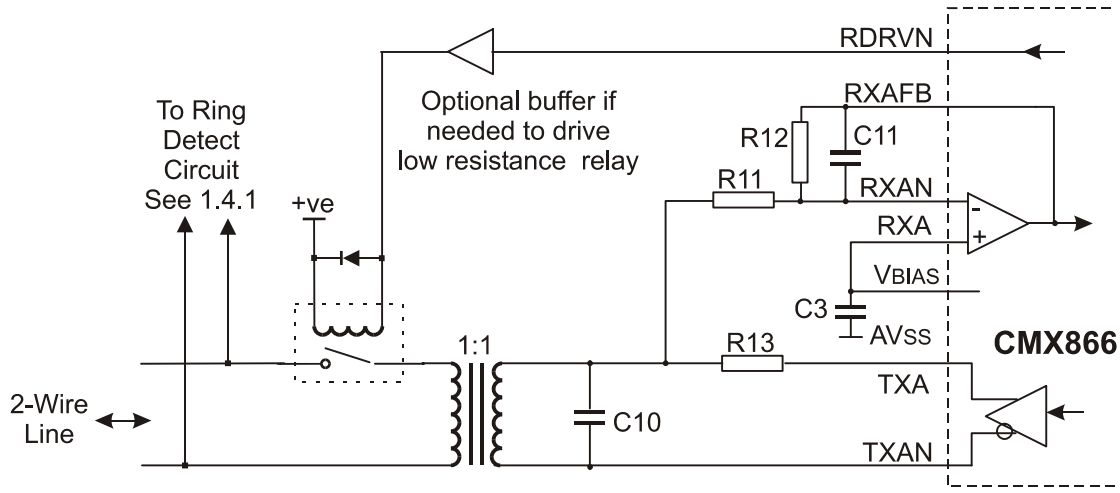
If the Ring detect function is not used then pin RD should be connected to DVSS and RT to DVDD.

1.4.2 Line Interface

A line interface circuit is needed to provide dc isolation and to terminate the line.

2-Wire Line Interface

Figure 4a shows a simplified interface for use with a 600Ω 2-wire line. The complex line termination is provided by R13 and C10, high frequency noise is attenuated by C10 and C11, while R11 and R12 set the receive signal level into the modem. For clarity the 2-wire line protection circuits and the connection to RXBN (for on-hook CLI applications) have not been shown.



R11	See text	C3	See Figure 2
R12	100kΩ	C10	33nF
R13	600Ω	C11	100pF

Resistors ±5%, capacitors ±20%

Figure 4a 2-Wire Line Interface Circuit

The transmit line signal level is determined by the voltage swing between the TXA and TXAN pins, less 6dB due to the line termination resistor R13, and less the loss in the line coupling transformer. Allowing for 1dB loss in the transformer, then with the DSP Tx Mode Register set for a Tx Level Control gain of 0dB (S25 register set to 'xxxxx111') the nominal transmit line levels will be:

	AVDD = 3.0V	**AVDD = 5.0V**
QAM, DPSK and FSK Tx modes (no guard tone)	-10dBm	-5.5dBm
Single tone transmit mode	-10dBm	-5.5dBm
DTMF transmit mode	-6 and -8 dBm	-1.5 and -3.5 dBm

For a line impedance of 600Ω, 0dBm = 775mVrms. See also section 1.7.1.3

In the receive direction, the signal detection thresholds within the CMX866 are proportional to AVDD and are affected by the Rx Gain Control gain setting in the DSP Rx Mode Register (as indicated by the value held in the S26 register). The signal level into the CMX866 is affected by the line coupling transformer loss and the values of R11 and R12 of Figure 4a.

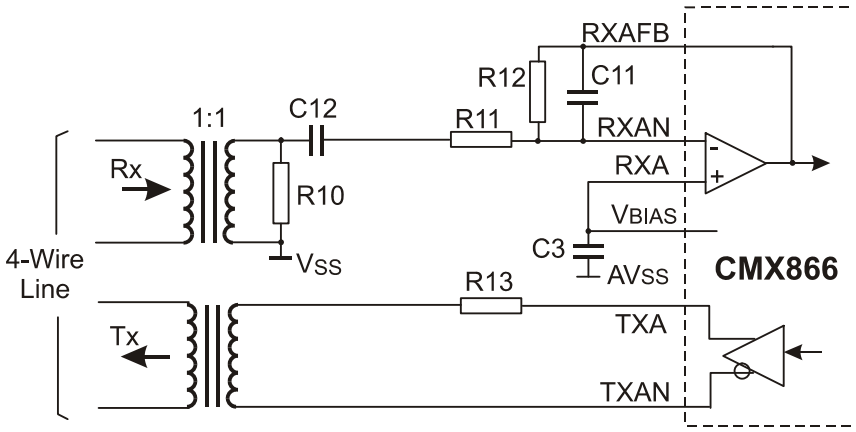
Assuming 1dB transformer loss, the Rx Gain Control programmed to 0dB (S26 register set to 'xxxxx111') and R12 = 100kΩ, then for correct operation (see section 1.7.1.3) the value of R11 should be equal to:

500 / AVDD kΩ i.e. 160kΩ at 3.0V, falling to 100kΩ at 5.0V

When the RDRVN pin is high impedance (= on-hook = inactive) the auxiliary receive input pin RXBN is internally connected to the RXAN pin. This can be used to increase the Rx gain (required for Type 1 Caller Line Identification reception) by reducing the effective value of R11, as shown in Figures 11 and 12. When the RDRVN pin is low (= off-hook = active) the RXBN pin is not connected.

4-Wire Line Interface

Figure 4b shows an interface for use with a 600Ω 4-wire line. The line terminations are provided by R10 and R13, high frequency noise is attenuated by C11 while R11 and R12 set the receive signal level into the modem. Transmit and receive line level settings and the value of R11 are as for the 2-wire circuit.



R10, 13	600Ω	C3	See Figure 2
R11	See text	C11	100pF
R12	100kΩ	C12	33nF

Resistors ±5%, Capacitors ±20%

Figure 4b 4-Wire Line Interface Circuit

1.4.3 Serial Interface

The CMX866 is controlled by sending AT commands over the serial interface from an external host µC. For simplicity, an asynchronous protocol has been adopted: 9600 baud, 8-bit words, no parity, 1 stop-bit. Since this communications rate exceeds that over the phone line, it is necessary to use CTS flow control to moderate the data rate, so that on average it equals the baud rate for the communications standard adopted. The CTS flow control method provided on the CMX866 will also work with the RTS/CTS handshake protocol used by some µControllers. AT commands and phone numbers need to be stored for future use and the CMX866 provides four internal buffers for phone number and command storage and for data buffering (see Figure 5a).

When the external host µC is ready to transmit AT commands or data it should take the Request To Send signal active (RTSN pin goes low) and place the information to be sent on the Transmit Data (TXD) pin. When the CMX866 is ready to accept this information from the external host µC it will take the Clear To Send signal active (CTSN pin goes low). The information should be sent as 8-bit bytes, encapsulated by a start bit (low) and a stop bit (high). The CMX866 should be presented with continuous mark (stop bits) when the host µC has no information to send. As each byte is received it is stored in a 48-byte AT command buffer when in Command mode or in a 16-byte receive data buffer when in Data Transfer mode. The CMX866 will take the CTSN pin high when either buffer is full. The TXD pin must then be taken high (continuous mark) until the on-chip µController in the CMX866 is ready to accept further data, which it will signify by taking the CTSN pin low, providing the RTSN pin is already low. If the external host µC does not have an Request To Send signal, the RTSN pin should be permanently wired low. When RTSN is inactive high, CTSN follows RTSN and becomes inactive high, thus there is no data flow from the host µC to the CMX866, but data flow from the CMX866 to the host µC is allowed and will take place if data is received from the phone line. As the incoming AT command is being interpreted, any phone number is identified and stored separately in the 24-byte phone number buffer.

When the CMX866 is in Data Transfer mode and it receives a signal from the phone line which exceeds the minimum amplitude threshold, it will attempt to demodulate the signal and place the received data on the RXD pin. At the same time it will make the Data Carrier Detected signal active (DCDN pin goes low). Received data is presented to the RXD pin at 9600 baud (with the same protocol as for transmission, regardless of the format that was used over the phone line), after a complete byte has been demodulated. There is a 24-byte message buffer in the receive path but, as the received data always arrives at slower than 9600 baud, there is no need for a flow control handshake in the receive path. It is assumed that the external host µC will absorb all of the data presented to it without the need for flow control and will ignore continuous mark (stop bits) when there is no received data. If the received signal is below the detection threshold or the CMX866 is not in Data Transfer mode, the DCDN and RXD pins will be taken high.

If the CMX866 receives a RING signal on the RD and RT pins, such that the detection threshold is exceeded, then the device will forward this condition to the external host µC by taking the RIN pin low. This pin follows the output of the ring detector, so will go low for each burst of RING signal. If the CMX866 is in a Powersave or 'Zero-Power' state, it will be woken up and the DSRN pin will go low once the on-chip µController is ready to receive communications through the serial port. This wake up process takes about 30ms from 'Zero-Power' state, as the V_{BIAS} pin has to charge the external reservoir capacitor and the crystal oscillator has to start up and stabilise before the CMX866 can initialise itself. From the Powersave state this wake up process takes about 10µs, as the oscillator and the V_{BIAS} pin are already stable.

The DSRN and DTRN pins do not act as a handshake with the external host µC. The DSRN pin indicates the operational status of the on-chip µController (low = ready to communicate with an external host µC). The DTRN pin is used for taking the CMX866 out of a Powersave or 'Zero-Power' state. It acts as a device wake up, in the same manner as the RING signal, and becomes active on the high to low transition. A high to low transition on the DTRN pin is ignored if the device is already 'woken up'. If the external host µC does not have a DTR signal, the DTRN pin should be permanently wired to the TXD pin. When the CMX866 is in a Powersave or 'Zero-Power' state, the RXD, CTSN, DSRN, DCDN and RIN pins will be permanently high. The condition of the TXD, RTSN and DTRN pins is not important.

Depending on the &Dn configuration, if the DTRN pin is taken high at any time whilst the CMX866 is in Data Transfer mode, a fixed, 100ms timeout is started. On completion of the timeout, the CMX866 will return to Command mode, enabling further AT commands to be sent. If the DTRN pin goes high whilst the CMX866 is in Command mode, the action is ignored. AT commands can be sent providing CTSN and RTSN are low (ie DTRN can be either high or low). A low to high transition on the ESC pin also has the same effect of returning the CMX866 from Data Transfer mode to Command mode, but with immediate effect. The &Dn command configures these options, see section 1.5.4.4 for more details.

If the RTSN pin is taken high at any time whilst the CMX866 is in Data Transfer mode, a timeout is started whose value is set in the S28 register (0 = timeout disabled). On completion of the timeout, the CMX866 will return to Command mode and take CTSN high. If the RTSN pin goes high whilst the CMX866 is in Command mode, the CTSN pin goes high and the action on the RTSN pin is ignored. Information transfer can only restart when the RTSN pin is taken low again and the CMX866 responds by taking CTSN low.

1.4.4 RESETN pin

The CMX866 has an internal power-up reset function which is activated whenever power is first applied to the device. This reset function resets all of the on-chip µController registers, including the S-Register settings, and then performs an initialisation sequence which resets the internal DSP and subsequently places it in a powersave state, loads the factory default values into the S-Registers and places the on-chip µController into an operating state. This internal power-up reset function is OR-ed with the RESETN pin. The state of the CMX866, including its outputs, is undefined for approximately 4.7ms, until this reset operation is complete.

When the RESETN pin is taken low, the on-chip µcontroller is reset and its program counter held at address $0000. It remains in this condition until the RESETN pin is taken high, at which time the software reset operation described above is performed. The RESETN pin must be held low for at least 5.0µs.

When the CMX866 first enters the operating state, it reports its configuration as follows:

- CMX866 waits for DTRN to go active (low)
- CMX866 takes the DSRN pin active (low) to indicate its readiness to communicate with an external host µC
- CMX866 waits for RTSN to go active (low)
- CMX866 sends "CMX866" identification message to external host µC (equivalent to the host µC issuing an ATI0 command)
- The on-chip µController now powers up the DSP part of the CMX866
- The DSP is automatically reset then requested to perform an internal diagnostic self-check, which takes about 2.9ms to complete
- On successful completion, CMX866 sends "DSP checksum OK" identification message to the external host µC. If not successful, CMX866 sends "DSP Error" message to the external host µC. In the latter case, the CMX866 should be reset again by taking the RESETN pin low
- The on-chip µController now powers down the DSP part of the CMX866
- The on-chip µController is now in the Command mode operating state and is ready to accept AT commands from the serial interface, approximately 55ms after DTRN went low
- CMX866 takes the CTSN pin active (low) to indicate its readiness to communicate with an external host µC

Note that the on-chip µController does not perform its own internal diagnostic self-check as this is not considered necessary.

1.5 General Description

1.5.1 Internal Structure

Internally, the CMX866 consists of a dedicated DSP which is controlled by an on-chip µController. This µController is preprogrammed to interpret the AT commands provided by the user into instructions for controlling the dedicated DSP. It also handles the CMX866 power management and other functions. The DSP is preprogrammed with algorithms to implement the various modem functions, but also has Tone Generators and Detectors which are user programmable with AT commands, via the on-chip µController.

The CMX866's DSP transmit and receive operating modes are independently programmable by means of AT commands which write values into the S-Registers. The on-chip µController then interprets the values in these registers and programs the corresponding registers in the dedicated DSP.

The DSP transmit mode can be set to any one of the following:

- V.22 bis modem. 2400bps QAM (Quadrature Amplitude Modulation)
- V.22 and Bell 212A modem. 1200 bps DPSK (Differential Phase Shift Keying)
- V.21 modem. 300bps FSK (Frequency Shift Keying)
- Bell 103 modem. 300bps FSK
- V.23 modem. 1200 or 75 bps FSK
- Bell 202 modem. 1200 or 150 bps FSK
- DTMF transmit
- Single tone transmit (from a range of modem calling, answer and other tone frequencies)
- User programmed tone or tone pair transmit (programmable frequencies and levels)
- Disabled

The DSP receive mode can be set to any one of the following:

- V.22 bis modem. 2400bps QAM
- V.22 and Bell 212A modem. 1200 bps DPSK
- V.21 modem. 300bps FSK
- Bell 103 modem. 300 bps FSK
- V.23 modem. 1200 or 75 bps FSK
- Bell 202 modem. 1200 or 150 bps FSK
- DTMF detect
- 2100Hz and 2225Hz answer tone detect
- Call progress signal detect
- Dual alert tone pair detect (for Caller Line Identification)
- User programmed tone or tone pair detect
- Disabled

The CMX866 can also be set into 'Zero-Power' or Powersave states, which disable all circuitry except for the Ring Detector. The S-Register settings and the CMX866's configuration are remembered when in 'Zero-Power' or Powersave states. The 'Zero-Power' state stops the crystal oscillator and removes power from the V_{BIAS} pin, for minimum power consumption. It takes about 30ms for the CMX866 to become operational from the 'Zero-Power' state. The Powersave state stops the internal clock distribution, but retains power to the crystal oscillator and V_{BIAS} circuit. Consequently, the CMX866 can become operational from this state in about 10µs. If the TXD pin is tied to the DTRN pin (to implement a reduced RS232 interface) any activity on the TXD pin will also take the CMX866 into an operational state. In this case, however, data may be corrupted until the CMX866 is fully operational.

1.5.2 Operating States and Data Flow

The following diagram shows the flow of data in the CMX866:

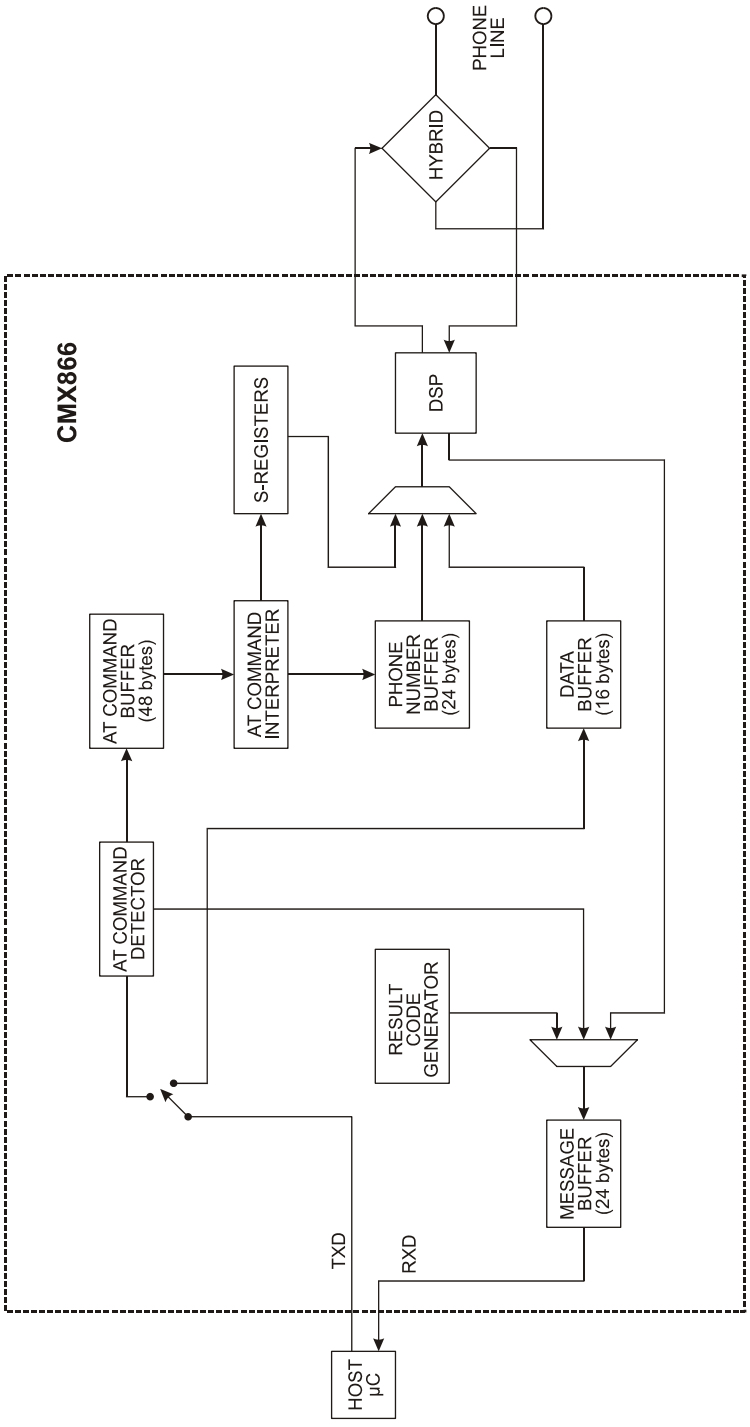


Figure 5a CMX866 Data Flow Diagram

The following state transition chart shows the various modes of operation for the CMX866:

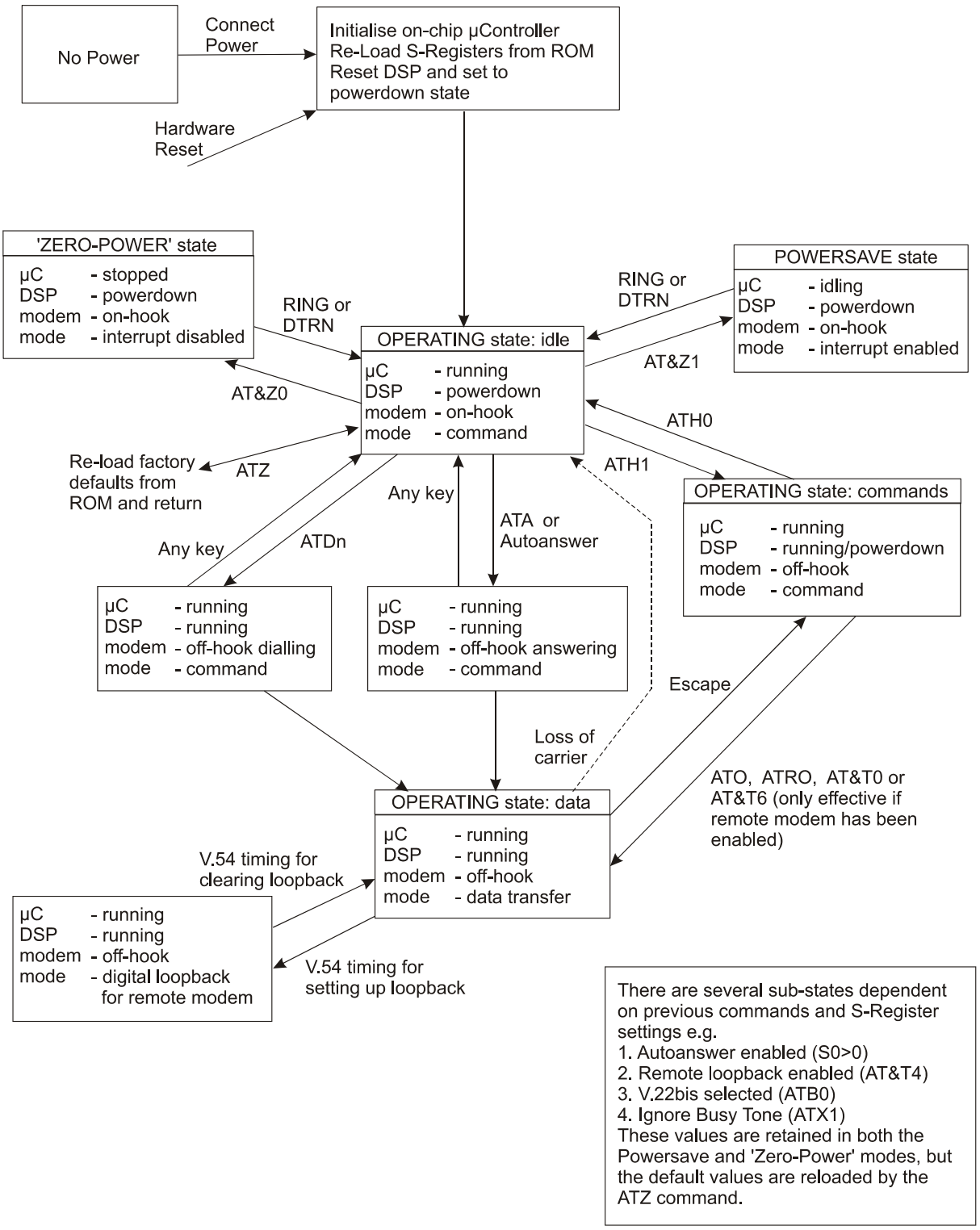


Figure 5b CMX866 State Transition Chart

1.5.3 Functional Description

The CMX866 is a multi-functional integrated modem chip which requires simple telephone line and RS232 interfaces to implement a complete, low-power modem that can be controlled by widely used AT commands. A list of the main features of this product is given below:

Function	Commands	Registers
• Set modem line communication functions, software protocol and control characters for AT commands	Bn, &Gn	S2, S3, S4, S5, S10, S23, S24, S27
• Select automatic or no fallback from V.22bis to V.22	Nn	S24
• Select V.23 or Bell 202 fast turnaround	RO	S14, S24
• Return to Command mode by: 1) Issuing an escape sequence: <delay> +++ <delay> 2) Taking the DTRN pin high (active low) 3) Taking the ESC pin high (active high) 4) Taking the RTSN pin high (active low)		 S12 S24 S14 S28
• Bypass the answertone detection sequence to give "Fast Connect"		S14
• Set modem into answer or originate mode, independently of whether a call is being initiated or answered		S14
• Detect dual alert tones or FSK whilst on-hook (for Type 1 CLI)	@Rn, @RR, @F8	
• Place the CMX866 into either 'Zero-Power' or Powersave states. When in these states, the CMX866 can be "woken-up" by either: 1) activity on the DTRN pin (including transmitted data, if this is also wired to the DTRN pin) 2) detection of a Ringing condition on the RD and RT pins	&Z0, &Z1	S21
• Make local and remote digital loopback connections and allow remote modems to digitally loopback the CMX866. This facilitates the provision of loopback tests by the external host µController	&Tn	S15, S16, S18, S21
• Automatically dial a directory number and monitor call progress tones before entering the modem function	Dn, DTn, DL, Hn, Xn	S6, S7, S8, S11, S22, S29
• Automatically answer an incoming call	A, Hn	S0, S1, S17
• Independently set the Rx and Tx path gain		S25, S26
• Perform internal confidence tests on the CMX866 and report back the device revision, status and configuration	In, &V	
• Perform miscellaneous line communications functions, such as repeating the last command, selecting alphabetic or numeric result codes, etc.	A/, En, Qn, Vn	S14
• Restore the default 'factory profile', placing the CMX866 into a known state without resetting the device	Z	
• Set the serial interface (RS232) communications protocol and CMX866 hardware configurations	&Cn, &Dn	S24
• Enter Data mode from Command mode	O, RO, &Tn	

1.5.4 AT Command and Register Set

1.5.4.1 AT Command and S-Register Summary

AT Command	Parameters	Function	Default
A		Answer Command - Answer and establish a connection when off-hook	
A/		Re-execute last command	
Bn	n = 0..9	Select Communications Standard	n=0
Dn ... n or DTn ... n	n = 0..9, A..D, *,#	Dial Command - DTMF dials the subsequent Directory Number	
	,	Dial Command Modifier - Delay during dialling - time in S8 register	
	!	Dial Command Modifier- Send a line break - time in S29 register	
	;	Dial Command Modifier - command mode after dialling, no handshake	
DL		Dial Command - Redial last number	
En	n = 0,1	Command echo, 0=off, 1=on	n=1
Hn	n = 0,1	Switch Hook Control, 0=on-hook, 1=off-hook	n=0
In	n = 0	Identification - Returns the modem's product identification	
Nn	n = 0,1	V.22bis Fallback to V.22 option, 0=none, 1=automatic	n=1
O		Go online in Data mode (from Command mode)	
Qn	n = 0,1	Enable(n=0)/Disable(n=1) return of modem result codes	n=0
RO		Execute V.23 or Bell 202 turnaround if enabled (see S14 and S24) then go online in Data mode	
Sn?	n = 0..29	S-Register "n" Read - Display specified S Register contents	
Sn=x	n = 0..29	S-Register "n" Write - Write to specified S Register	
Vn	n =0,1	Return result codes as numbers (n=0) or words (n=1)	n=0
Xn	n = 0..3	Calling and Response Characteristics	n=3
Z		Restore factory profile for CMX866	
&Cn	n = 0,1	DCD always on (n=0) or DCD follows carrier (n=1)	n=1
&Dn	n= 0..2	DTR signal procedure	n=2
&Gn	n = 0..2	Guard Tone Select - Disable (n=0), Enable 550Hz (n=1) or 1800Hz (n=2)	n=0
&Tn	n = 0,3..6	User accessible Loopback Tests and Diagnostics	n=0
&V		Returns current configuration	
&Zn	n = 0,1	'Zero-Power' state (n=0) or Powersave state (n=1)	
@Rn?	n = 00..FF	DSP Register "n" Read - Display specified DSP Register contents	
@Rn=x	n = 00..FF	DSP Register "n" Write - Write to specified DSP Register	

S Registers	Parameters	Function	Default
S0	0…255	Number of rings before answering, 0 = Auto-answer disabled	2
S1	0…255	Number of rings received	0
S2	0-127	Escape character value	+
S3	0-127	Carriage return character value	CR
S4	0-127	Line feed character value	LF
S5	0-127	Backspace character value	BS
S6	2…255	Waiting time in seconds for dial tone or before blind dialling	4s
S7	2…255	Maximum waiting time in seconds for carrier	50s
S8	0...255	Pause time in seconds for "," dial modifier	2s
S9	1...255	Reserved	
S10	1…255	Lost carrier to hang up delay in units of 100ms	700ms

S Registers	Parameters	Function	Default
S11	5…255	DTMF tone duration and interdigit pause duration in units of 10ms	100ms
S12	0…255	Escape code guard time in units of 50ms	1s
S13		Reserved	
S14	0…255	General Options	$92
S15	0…255	Loopback carrier off time in units of 10ms	80ms
S16	0…255	Drop time for loopback in units of 10ms	60ms
S17	0…255	Handshake timeout (Answering) in seconds	30s
S18	0…255	Loopback timer (0= no timeout) in seconds	0s
S19		Reserved for test functions	
S20		Reserved	
S21	0…255	Loopback and Power states	$10
S22	0…255	Calling and response characteristics selection	$C0
S23	0…255	Guard tone selection	$00
S24	0…255	Equaliser, DCD, DTR status and modulation fallback	$A9
S25	0…255	TX Gain, TX data format	$B0
S26	0…255	RX Gain, RX data format, overspeed (2.3% default) setting	$30
S27	0…255	Communications Protocol	$00
S28	0…255	RTSN Timeout for return to Command mode from Data mode in seconds	0s
S29	0…255	Timed Break Recall period in units of 10ms	300ms

Bn Register	Parameter	Communications Protocol	Fallback
	n	(Mapped to S27 register)	
	0	V.22bis 2400bps QAM	V.22
	1	V.22 1200bps DPSK	
	2	V.23 Tx 75bps, Rx 1200bps (Master)	
	3	V.23 Tx 1200bps, Rx 75bps (Slave)	
	4	Reserved	
	5	V.21 300bps FSK	
	6	Bell 212A 1200bps DPSK	
	7	Bell 202 Tx 150bps Rx 1200bps	
	8	Bell 202 Tx 1200bps Rx 150bps	
	9	Bell 103 300bps FSK	

Xn Register	Parameter	Calling and Response Characteristics
	n	(Mapped to S22 register)
	0	Ignore dial tones and busy tones, return CONNECTxxxx or NO CARRIER
	1	Ignore busy tone, wait for dial tone to dial. Return NO DIAL TONE or CONNECT xxxx or NO CARRIER
	2	Ignore dial tone. If busy tone detected, return BUSY. Return CONNECT xxxx
	3	Return NO DIAL TONE, BUSY, CONNECT xxxx, or NO CARRIER

&Dn Register	Parameter	DTR action
	n	(Mapped to S24 register)
	0	Ignore DTR signal
	1	Go to command state when on to off transition occurs
	2	Hang up and go to command state when on to off transition occurs

&Gn Register	Parameter	Guard Tone action
	n	(Mapped to S23 register)
	0	Disabled
	1	Enabled 550Hz
	2	Enabled 1800Hz

&Tn Register	Parameter	Test function
	n	(Mapped to S21 register)
	0	Terminate test
	1	Reserved
	2	Reserved
	3	Local digital loopback
	4	Enable remote request for digital loopback
	5	Disable remote request for digital loopback
	6	Request remote digital loopback & initiate

1.5.4.2 General Description of AT Commands

Only the AT commands listed above are supported. Valid commands will generate an 'OK' result code (see section 1.5.4.6) and invalid commands will be rejected with an 'ERROR' result code, when command echoing and word result codes are enabled. The on-chip µController will send a <LF> character directly after a <CR> character to ensure compatibility with external host µControllers. Any commands which are not fully implemented will return the result code 'NYI' (Not Yet Implemented). AT commands should not be sent to the on-chip µController until the previous result code (if enabled) has been received.

Every line of commands (except for A/ and the escape sequence) must begin with the AT prefix and be terminated with a carriage return <CR>. The on-chip µController waits to receive a complete AT command line before processing it. Embedded spaces are ignored and the case (upper or lower) of characters including the 'AT' does not matter. The command line must not exceed 48 characters (excluding the 'AT' characters). The on-chip µController will ignore the command line and return an 'ERROR' result code if the line is not terminated correctly.

All characters in the AT command, including the 'AT' and <CR> terminator are echoed (if E1 is set) by the CMX866 in the order in which they are sent by the external host µC.

If when entering an AT command, no command or register name suffix is supplied, a suffix of zero is assumed. If when changing a register value, no value is supplied a value of zero or an empty string is assumed: eg ATS0=<CR> is equivalent to ATS0=0<CR>.

Receipt of a back space will cause the CMX866 to send a "back space, space, back space" sequence of characters to the external host µC, to allow any terminal which may be connected to the latter to clear its screen of the last character. Also the last character received will be discarded unless the last characters received were 'AT', ie the 'AT' is never deleted.

The escape sequence '+++' (with Guard Time = 1s [see S12 register] before and after the sequence) will cause the CMX866 to enter Command mode from Data Transfer mode and to return an 'OK' response.

1.5.4.3 AT Commands in Detail

Command	*Description*
A	**Answer Command** The CMX866 will go off-hook and attempt to answer an incoming call by establishing a connection with a remote modem. The command is not valid if there is no incoming call and it will return the 'ERROR' result code. Syntax: **ATA**<*CR*>
A/	**Re-Execute Previous Command Line** Re-executes the last issued command line. This command does not require the AT prefix or a carriage return. If the last issued command line contained several AT commands, each of these will be repeated. Syntax: **A/**
Bn	**Select Communications Standard** Selects the communications standard specified by the parameter n. Syntax: **ATBn**<*CR*> ***Modifier Usage*** **n=0** Selects ITU-T V.22bis at 2400bps QAM (default). **n=1** Selects ITU-T V.22 at 1200bps DPSK. **n=2** Selects ITU-T V.23 with Tx 75bps and Rx 1200bps FSK. **n=3** Selects ITU-T V.23 with Tx 1200bps and Rx 75bps FSK. **n=4** Reserved for future use. **n=5** Selects ITU-T V.21 at 300bps FSK. **n=6** Selects Bell 212A at 1200bps DPSK. **n=7** Selects Bell 202 with Tx 150bps and Rx 1200bps FSK. **n=8** Selects Bell 202 with Tx 1200bps and Rx 150bps FSK. **n=9** Selects Bell 103 at 300bps FSK.
Dn **or DTn**	**Dial Command** This command directs the CMX866 to go off-hook, dial the directory number entered and attempt to establish a connection with a remote modem by going into Data Transfer mode. The n represents an ASCII string composed of dial digits and dial modifiers and must not exceed the 23 character buffer limit. The DTMF tone dialling digits include 0 through 9, A, B, C, D, and the symbols # and *. Loop-disconnect (pulse) dialling is not implemented. For example: **ATD9,01621875500**<*CR*> ***Modifier Usage*** **n=L** Re-dial last number. **n=,** Delay dial sequence (pause setting contained in S8 register). **n=!** Send a timed break recall (duration in S29 register). **n=;** Remain in command mode after dialling, no handshake.

En	**Echo Command Characters** Syntax: **ATEn**<*CR*> ***Modifier Usage*** **n=0** Disables the echoing of commands to the external host µC. **n=1** Enables echoing of commands to the external host µC (default**)**.
Hn	**Hook Switch Control** Syntax: **ATHn**<*CR*> ***Modifier Usage*** **n=0** Instructs the CMX866 to go on-hook (RDRVN pin goes high). This disconnects the CMX866 from the line (default). **n=1** Instructs the CMX866 to go off-hook (RDRVN pin goes low). Line disconnection also occurs if the CMX866 is placed in 'Zero-Power' or Powersave mode, if the RESETN pin is taken low or, in certain cases, if the DTRN pin is taken high (see &Dn command).
In	**Identification** Requests the CMX866 to return its product identification information. Syntax: **ATIn**<*CR*> ***Modifier Usage*** **n=0** Displays the product identification: "CMX866"
Nn	**Modulation Fallback Option** Syntax: **ATNn**<*CR*> ***Modifier Usage*** **n=0** When originating or answering, the CMX866 negotiates only at the specified communications standard. **n=1** When originating or answering, the CMX866 falls back from V.22bis to V.22, as required (default).
O	**Change to Data Transfer Mode** Used during on-line AT Command mode, this command changes the CMX866 operation to Data Transfer mode, without initiating any retrain sequence. Syntax: **ATO**<*CR*>
Qn	**Enable/Disable Modem Responses** Syntax: **ATQn**<*CR*> ***Modifier Usage*** **n=0** Enables result codes. Codes are issued to the external host µC (default). **n=1** Disables result codes. Codes are not issued to the external host µC.

RO	**Change to Data Transfer Mode in Reverse Direction** Used during on-line AT Command mode to execute a V.23 turnaround if enabled (see S14 and S24 registers), then returns to Data Transfer mode, like the O command above. Syntax: **ATRO**<*CR*>
Sn?	**S-Register Read** Command for displaying the contents of an S-Register (See S-Register Table). Syntax: **ATSn?**<*CR*> where **n** is the S-Register to be interrogated (decimal). Value returned is either in decimal or hex (default) format depending on the setting of Bit 4 in the S14 register. Note that a **?** command on its own is invalid.
Sn=x	**S-Register Write** Command for writing to an S-Register (See S-Register Table). Syntax: **ATSn=x**<*CR*> where **n** is the S-Register (decimal) and **x** is the value to be written (decimal, 0-255). Note that a **=x** command on its own is invalid.
Vn	**Result Code Format** Syntax: **ATVn**<*CR*> ***Modifier Usage*** **n=0** Instructs the CMX866 to display result codes as numbers (default). **n=1** Instructs the CMX866 to display result codes as words.
Xn	**Calling Characteristics** Determines which set of responses and calling characteristics are used. Syntax: **ATXn**<*CR*> ***Modifier Usage*** **n=0** The CMX866 will ignore dial tones and busy tones. Dial tone wait time is zero, and blind dialling is enabled after the delay in register S6. The CMX866 returns a CONNECT xxxx result code when a connection is established, where xxxx is the Tx/Rx line speed, otherwise it returns a NO CARRIER result code. **n=1** The CMX866 waits for a dial tone before dialling but will ignore busy tone. If a dial tone is not detected within the time in register S6, a NO DIAL TONE result code is returned. The CMX866 returns a CONNECT xxxx result code when a connection is established, where xxxx is the Tx/Rx line speed, otherwise it returns a NO CARRIER result code. **n=2** The CMX866 will ignore dial tone. If busy tone is detected, a BUSY result code is returned. Blind dialling is enabled after the delay in register S6. The CMX866 returns a CONNECT xxxx result code when a connection is established, where xxxx is the Tx/Rx line speed, otherwise it returns a NO CARRIER result code. **n=3** If a dial tone is not detected within the time in register S6, a NO DIAL TONE result code is returned. If a busy tone is detected, a BUSY result code is returned.

	The CMX866 returns a CONNECT xxxx result code when a connection is established, where xxxx is the Tx/Rx line speed, otherwise it returns a NO CARRIER result code (default).

Z	**Factory Reload** Reloads the factory default S-Register settings (See S-Register Table). Syntax: **ATZ**<*CR*>

1.5.4.4 Extended AT Commands

Command	***Description***
&Cn	**Carrier Detect** Determines the action of the DCDN pin. Syntax: **AT&Cn**<*CR*> ***Modifier Usage*** **n=0** DCD is always on (DCDN pin is held permanently low). **n=1** DCD follows the received carrier. If a carrier is present on the line, then DCD is on (DCDN pin is held low). Otherwise DCD is off (DCDN pin is held high) (default).
&Dn	**Data Terminal Ready** Determines the meaning of the DTRN pin. Syntax: **AT&Dn**<*CR*> ***Modifier Usage*** **n=0** DTRN pin is ignored **n=1** When an on to off transition of DTR occurs (DTRN pin goes from low to high), the CMX866 goes into Command mode (if it was in Data Transfer mode), after a fixed delay of 100ms, during which time the transition is qualified. Whilst in Command mode, if DTRN remains high for more than 500ms, then the CMX866 goes on-hook. **n=2** Same as above (n=1), except that the CMX866 also goes on-hook when the DTRN transition is qualified.
&Gn	**Guard Tone Select** Selects the Guard tone to be transmitted with highband QAM or DPSK. Syntax: **AT&Gn**<*CR*> ***Modifier Usage*** **n=0** Disable guard tone (default). **n=1** Enable 550Hz guard tone. **n=2** Enable 1800Hz guard tone.

&Tn	**Loopback Connection** Instructs the CMX866 to make local or remote loopback connections, or to action a remote request to make loopback connections. Syntax: **AT&Tn**<*CR*> ***Modifier Usage*** **n=0** Remove all loopbacks and return to Data Transfer mode. **n=1** Reserved. **n=2** Reserved. **n=3** Make a local digital loopback connection to loopback the received data stream from the remote modem. **n=4** Enable remote requests for a local digital loopback connection. **n=5** Disable remote requests for a local digital loopback connection. **n=6** Request a remote digital loopback connection. Note that if the CMX866 is in Data Transfer mode, an escape sequence must be issued (+++) to return the CMX866 to Command mode before this loopback connection command can be given. The AT&T0, AT&T3 and AT&T6 commands can only be issued when off-hook. The AT&T4 and AT&T5 commands can be issued when either on-hook or off-hook. After the loopback command (AT&T3 or AT&T6) has been actioned, the CMX866 will be in Data Transfer mode. In order to cancel the loopback, it is first necessary to return to Command mode by locally issuing a CMX866 escape sequence (+++). The AT&T0 command can then be given to cancel the loopback. Alternatively, the ATO command can be given to re-instate the loopback and return to Data Transfer mode. Note that no other characters may precede the escape sequence (+++). This is because the CMX866 will not be looking for data sent over the RS232 interface when a loopback connection is active. Any RS232 data sent which does not begin with the escape sequence will be ignored and will prevent any subsequent escape sequence from being recognised. Also note that any escape sequence sent from the remote end will not be recognised by the CMX866, irrespective of mode.
&V	**Current Configuration** Returns the current CMX866 configuration by reading the S-Registers. The register data is output on the RXD pin in the form (where xxx is decimal data): S00: xxx S01: xxx S02: xxx S03: xxx S04: xxx S05: xxx S06: xxx S07: xxx S08: xxx S09: xxx<CR> S10: xxx S11: xxx S12: xxx S13: xxx S14: xxx S15: xxx S16: xxx S17: xxx S18: xxx S19: xxx<CR> S20: xxx S21: xxx S22: xxx S23: xxx S24: xxx S25: xxx S26: xxx S27: xxx S28: xxx S29: xxx<CR> This register data is also available in hexadecimal form, by setting bit 4 of S14 register. Syntax: **AT&V**<*CR*>

&Zn	**Sleep States** Instructs the CMX866 to enter one of the following sleep states: Syntax: **AT&Zn**<*CR*> ***Modifier Usage*** **n=0** 'Zero-Power' state. **n=1** Powersave state. The 'Zero-Power' state stops the crystal oscillator and removes power from the VBIAS pin, for minimum power consumption. It takes about 30ms for the CMX866 to become fully operational from the 'Zero-Power' state. However, the crystal oscillator only takes about 1.4ms to become stable, so commands which do not require the analogue parts of the DSP to be stable (VBIAS at ½VDD) can be given to the on-chip µController after this time. The Powersave state stops the internal clock distribution, but retains power to the crystal oscillator and VBIAS circuit. Consequently, the CMX866 can become operational from this state in about 10µs. To enter either sleep state, the DTRN pin must already be inactive (high) and the RD and RT pins inactive (low).

1.5.4.5 S-Registers

The following table gives a more detailed description of the available S-Registers and their functions. The register range, units and default values are also listed.

S-Register				
Reg	***Range***	***Units***	***Description***	***Default***
S0	0-255	Rings	**Automatic answer** - Number of rings until automatic answer. If the register is zero the modem will not automatically answer.	2
S1	0-255	Rings	**Count incoming rings** - This register is read only and contains the number of rings detected by the CMX866.	0
S2	0-127	ASCII Decimal	**Escape character value** - Contains the ASCII decimal value of the escape character. The default setting is an ASCII + and the escape sequence is +++. A value over 127 disables the escape sequence.	43
S3	0-127	ASCII Decimal	**Carriage return character** - Contains the ASCII decimal value of the character recognised as the command line terminator. This character will also be sent at the end of result codes. The default setting is <CR>.	13
S4	0-127	ASCII Decimal	**Line feed character** - Contains the ASCII decimal value of the character recognised as a line feed. This character is ignored if present in a command string. The default setting is <LF>. The CMX866 sends the line feed character after a carriage return only when word responses are sent.	10
S5	0-127	ASCII Decimal	**Backspace character** - Contains the ASCII decimal value of the character recognised as a backspace. The default setting is <BS>.	8
S6	2-255	1s	**Wait time for blind dialling -** If Blind Dialling is enabled (see Xn command, Register S22), sets the length of time to pause after the CMX866 goes off-hook before dialling the first digit of the directory number. If Blind Dialling is disabled, sets the length of time to wait for a dial tone after the CMX866 goes off-hook. If a dial tone is not received in this time, an 'ERROR' result code is returned.	4
S7	1-255	1s	**Wait for carrier after dial** - Sets the length of time the CMX866 waits for a carrier before returning on-hook.	50
S8	0-255	1s	**Pause Time for Comma Dial Modifier** - Specifies the number of seconds to pause for each comma (,) encountered in a dial string.	2
S9	1-255		**Reserved**	

S-Register				
Reg	***Range***	***Units***	***Description***	***Default***
S10	1-255	100ms	**Lost carrier to hang up delay** - Sets the length of time that the CMX866 waits before hanging up after the loss of a carrier. This allows the CMX866 to distinguish between disturbances that momentarily break the connection and the remote modem hanging up.	7
S11	5-25	10ms	**DTMF tone duration** - Defines the duration of DTMF tones for tone dialling. The length of pause between each DTMF tone is the same as this duration time.	10
S12	0-255	50ms	**Escape code guard time** - Specifies the minimum time of no data before and after entry of the escape sequence.	20
S13	0-255		**Reserved**	
S14	0-255	Hex	**General options** - provides the following functions: Bit 0 - V.23/Bell 202 Turnaround, 0 Disabled, 1 Enabled Bit 1 - Echo command character, 0 Disables echoing (ATE0), 1 Enables echoing (ATE1) Bit 2 - Result code display, 0 Send responses (ATQ0), 1 Do not send responses (ATQ1) Bit 3 - Word or number responses, 0 Send number responses (ATV0), 1 Send word responses (ATV1) Bit 4 - DSP or S-Register o/p format, 0 Decimal, 1 Hex Bit 5 - Fast Connect, 0 Disabled, 1 Enabled Bit 6 - ESC pin, 0 Disabled, 1 Enabled Bit 7 - Answer/originate operation, 0 Answer (ATA), 1 Originate (ATD)	92
S15	0-255	10ms	**Loopback Carrier Off Time** - To terminate a loopback test at a remote modem, the CMX866 turns off the carrier sent to that modem for the time specified in this register.	8
S16	0-255	10ms	**Drop Time for Loopback** - If a loopback test is being performed by a remote modem, detection of a drop in the carrier from that modem which exceeds the time set in this register will cause the local loopback to be removed.	6
S17	0-255	1s	**Handshake Timeout -** If the handshake sequence, when answering, exceeds this duration, the handshake will be aborted and the modem will return to Command mode.	30
S18	0-255	1s	**Loopback Timer** - Defines the duration in seconds for which the modem performs diagnostic tests. On timeout, the test is terminated and the modem returns to Command mode. The default value of 0s disables the loopback timer, so that tests will run indefinitely. A test can also be terminated from Command mode at any time by issuing the AT&T0 command, which then returns the modem to Data Transfer mode.	0

S-Register				
Reg	***Range***	***Units***	***Description***	***Default***
S19	0-255		**Reserved** – Reserved for test functions	
S20	0-255		**Reserved**	
S21	0-255	Hex	**Loopback and Power States** - controls the operation of remote loopback and operational states: Bit 4 - Remote loopback, 0 Disabled, 1 Enabled (See &Tn command) Bit 6 - Powersave state, 0 Not powersaved, 1 Powersaved Bit 7 - 'Zero-Power' state, 0 Not 'Zero-Power', 1 'Zero-Power' All other bits Reserved	10
S22	0-255	Hex	**Calling and Response Characteristics (see section 1.5.4.1):** Bit 4-0 - Reserved Bit 7-5 - Calling and Response Characteristics: 000 Ignore Dial Tone and Busy Tone (ATX0), 100 Ignore Busy Tone, wait for Dial Tone (ATX1), 101 Ignore Dial Tone, wait for Busy Tone (ATX2), 110 Wait for Dial Tone and Busy Tone (ATX3)	C0
S23	0-255	Hex	**Guard Tone Selection (see section 1.5.4.1):** Bit 5-0 - Reserved Bit 7-6 - Guard Tone Activity: 00 Disabled (AT&G0), 11 Enabled, guard tone = 550Hz (AT&G1) 10 Enabled, guard tone = 1800Hz (AT&G2)	00
S24	0-255	Hex	**Equaliser, DCD and DTR status (see section 1.5.4.1):** Bit 0 - Reserved. Permanently set to 1 Bit 1 - Fixed Compromise Equaliser, 0 Enabled, 1 Disabled Bit 2 - Auto-Equaliser, 0 Disabled, 1 Enabled Bit 3 - DCDN pin function, 0 DCDN always low, 1 DCDN follows inverse of carrier Bit 5-4 - DTRN pin function, 00 Ignore DTRN signal (AT&D0), 01 Go to Command mode when low to high transition has been qualified (AT&D1) 10 Go on-hook then go to Command mode when low to high transition has been qualified (AT&D2) Bit 6 - Reserved for use with the V.23 or Bell 202 turnaround function (used by the ATRO command) Bit 7 - Fallback mechanism from V.22bis to V.22 (equivalent to ATN1 command), 0 Disabled, 1 Enabled	A9

S-Register				
Reg	***Range***	***Units***	***Description***	***Default***
S25	0-255	Hex	**Tx Gain, Tx data format on phone line**: Bit 2-0 - Tx Gain, 000 (-10.5dB) through to 111 (0dB) in 1.5dB steps Bit 5-3 - Tx Data/Stop bits: 000 (5 data, 1 stop), 001 (5 data, 2 stop), 010 (6 data, 1 stop), 011 (6 data, 2 stop), 100 (7 data, 1 stop), 101 (7 data, 2 stop), 110 (8 data, 1 stop) - default, 111 (8 data, 2 stop) Bit 7-6 - Tx Data Format: 00 (start/stop mode - odd parity), 01 (start/stop mode - even parity), 10 (start/stop mode - no parity) - default, 11 (Synchronous mode)	B0
S26	0-255	Hex	**Rx Gain, Rx data format, Rx overspeed on phone line**: Bit 2-0 - Rx Gain, 000 (-10.5dB) through to 111 (0dB) in 1.5dB steps Bit 5-3 - Rx Data/Parity bits: 000 (5 data, no parity), 001 (5 data, parity), 010 (6 data, no parity), 011 (6 data, parity), 100 (7 data, no parity), 101 (7 data, parity), 110 (8 data, no parity) - default, 111 (8 data, parity) Bit 7-6 - Rx USART overspeed mode: 00 (start/stop mode 2.3% overspeed) - default, 01 (start/stop mode 1.0% overspeed), 10 (start/stop mode no overspeed), 11 (Synchronous mode)	30

S-Register				
Reg	***Range***	***Units***	***Description***	***Default***
S27	0-255	Hex	**Communications Protocol**: Bit 3-0 - Reserved Bit 7-4 - Communications standard: 0000 (ATB0) Selects ITU-T V.22bis at 2400bps QAM, 0001 (ATB1) Selects ITU-T V.22 at 1200bps DPSK, 0010 (ATB2) Selects ITU-T V.23 with Tx 75bps and Rx 1200bps FSK, 0011 (ATB3) Selects ITU-T V.23 with Tx 1200bps and Rx 75bps FSK, 0100 (ATB4) No function. Reserved for future use, 0101 (ATB5) Selects ITU-T V.21 at 300bps FSK, 0110 (ATB6) Selects Bell 212A at 1200bps DPSK, 0111 (ATB7) Selects Bell 202 with Tx 150bps and Rx 1200bps FSK, 1000 (ATB8) Selects Bell 202 with Tx 1200bps and Rx 150bps FSK, 1001 (ATB9) Selects Bell 103 at 300bps FSK	00
S28	0-255	1s	**RTSN Timeout -** The timeout for validation of a change on the RTSN pin before it is actioned by returning to Command mode from Data Transfer mode. (0 = timeout disabled).	0
S29	0-255	10ms	**Timed Break Recall Period** - Sets the length of time that the CMX866 breaks the line before reconnecting it and continuing to dial the directory number.	30

1.5.4.6 Result Codes

Numeric Response (Decimal)	*Word Response*	
00	**OK**	
01	**CONNECT**	
02	**RING**	
03	**NO CARRIER**	
04	**ERROR**	
05	**NO DIAL TONE**	
06	**BUSY**	
07	**CONNECT 2400**	
08	**CONNECT 1200**	
09	**DUAL TONE DETECT**	
10	**CONNECT 300**	
11	**CONNECT 1200/75**	
12	**CONNECT 75/1200**	
13	**CONNECT 1200/150**	
14	**CONNECT 150/1200**	
15	**NYI**	**(Not Yet Implemented)**

1.5.5 Tx USART

A flexible Tx USART is provided for all CMX866 modes. It can be programmed to transmit continuous patterns, Start-Stop characters or Synchronous Data.

In both Synchronous Data and Start-Stop modes the data to be transmitted is written by the on-chip µController into the 8-bit DSP Tx Data Register from which it is transferred to the Tx Data Buffer.

If Synchronous Data mode has been selected the 8 data bits in the Tx Data Buffer are transmitted serially in the order in which they are received, ie. b0 being sent first.

In Start-Stop mode a single Start bit is transmitted, followed by 5, 6, 7 or 8 data bits from the Tx Data Buffer - b0 first - followed by an optional Parity bit then - normally - one or two Stop bits. The Start, Parity and Stop bits are generated by the USART as determined by the Tx Mode Register settings and are not taken from the DSP Tx Data Register.

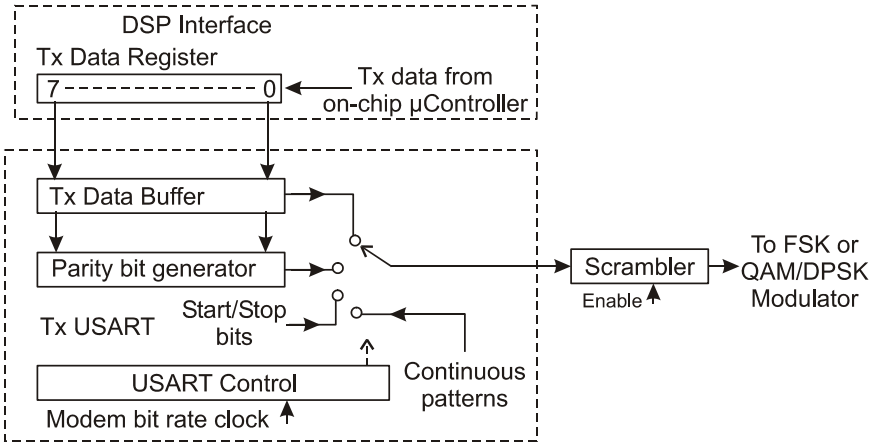


Figure 6a Tx USART

Every time the contents of the DSP Tx Data Register are transferred to the Tx Data Buffer, the Tx Data Ready flag bit of the DSP Status Register is set to 1 to indicate that a new value should be loaded into the DSP Tx Data Register. This flag bit is cleared to 0 when a new value is loaded into the DSP Tx Data Register. The interpretation of this flag is handled automatically by the on-chip µController.

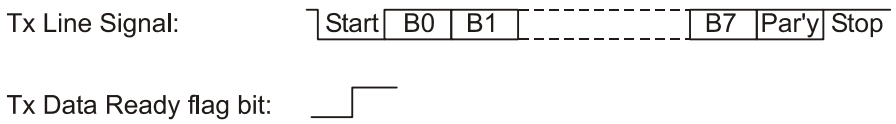


Figure 6b Tx USART Function (Start-Stop mode, 8 Data Bits + Parity)

If a new value is not loaded into the DSP Tx Data Register in time for the next DSP Tx Data Register to Tx Data Buffer transfer then the DSP Status Register Tx Data Underflow bit will be set to 1. In this event the contents of the Tx Data Buffer will be re-transmitted if Synchronous Data mode has been selected, or if Start-Stop mode was selected then a continuous Stop signal (1) will be transmitted until a new value is loaded into the DSP Tx Data Register.

In all modes the transmitted bit and baud rates are the nominal rates for the selected modem type, with an accuracy determined by the XTAL frequency accuracy. Underspeed transmission is automatically handled by the CMX866 in Start-Stop mode as it inserts extra Stop bit(s) if it has to wait for new data to be loaded into the DSP Tx Data Register.

The optional V.22/V.22 bis compatible data scrambler is enabled in V.22 and V.22bis handshake and data transfer modes. Its function is to invert the next input bit in the event of 64 consecutive ones appearing at its input. The scrambler uses the generating polynomial:

$$1 + x^{-14} + x^{-17}$$

1.5.6 FSK and QAM/DPSK Modulators

Serial data from the USART is fed via the optional scrambler to the FSK modulator if V.21, V.23, Bell 103 or Bell 202 mode has been selected or to the QAM/DPSK modulator for V.22, V.22 bis and Bell 212A modes.

The FSK modulator generates one of two frequencies according to the transmit mode and the value of current transmit data bit.

The QAM/DPSK modulator generates a carrier of 1200Hz (Low Band, Calling modem) or 2400Hz (High Band, Answering modem) which is modulated at 600 symbols/sec as described below:

For V.22 and Bell 212A 1200bps DPSK the transmit data stream is divided into groups of two consecutive bits (dibits) which are encoded as a carrier phase change:

Dibit (left-hand bit is the first of the pair)	**Phase change**
00	+90°
01	0°
11	+270°
10	+180°

For V.22 bis 2400bps QAM the transmit data stream is divided into groups of 4 consecutive data bits. The first two bits of each group are encoded as a phase quadrant change and the last two bits define one of four elements within a quadrant:

First two bits of group (left-hand bit is the first of the pair)	Phase quadrant change
00	+90° (e.g. quadrant 1 to 2)
01	0° (no change of quadrant)
11	+270° (e.g. quadrant 1 to 4)
10	+180° (e.g. quadrant 1 to 3)

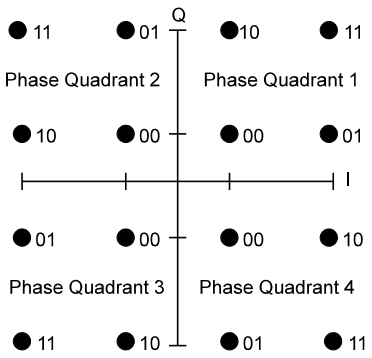


Figure 7 V.22 bis Signal Constellation

1.5.7 Tx Filter and Equaliser

The FSK or QAM/DPSK modulator output signal is fed through the Transmit Filter and Equaliser block which limits the out-of-band signal energy to acceptable limits. In 1200 and 2400 bps FSK, DPSK and QAM modes this block includes a fixed compromise line equaliser which is automatically set for the particular modulation type and frequency band being employed. This fixed compromise line equaliser may be enabled or disabled by bit 1 of the S24 register. The amount of Tx equalisation provided compensates for one quarter of the relative amplitude and delay distortion of ETS Test Line 1 over the frequency band used.

1.5.8 DTMF/Tone Generator

In DTMF/Tones mode this block generates DTMF signals or single or dual frequency tones. In QAM/DPSK modem modes it is used to generate the optional 550 or 1800Hz guard tone (see &Gn command and S23 register).

1.5.9 Tx Level Control and Output Buffer

The outputs (if present) of the Transmit Filter and DTMF/Tone Generator are summed then passed through the programmable Tx Level Control and Tx Output Buffer to the pins TXA and TXAN. The Tx Output Buffer has symmetrical outputs to provide sufficient line voltage swing at low values of V_{DD} and to reduce harmonic distortion of the signal. The output level is adjusted by bits 0-2 of the S25 register.

1.5.10 Rx DTMF/Tones Detectors

In Rx Tones Detect mode the received signal, after passing through the Rx Gain Control block, is fed to the DTMF / Tones / Call Progress / Answer Tone detectors. The selection of the four separate detectors is handled automatically by the on-chip µController:

The DTMF detector detects standard DTMF signals. A valid DTMF signal will set bit 5 of the DSP Status Register to 1 for as long as the signal is detected. The output of this detector is not currently used by the on-chip µController, however, this register can be accessed by the @R command.

The programmable tone pair detector includes two separate tone detectors. The first detector will set bit 6 of the DSP Status Register for as long as a valid signal is detected, the second detector sets bit 7, and bit 10 of the DSP Status Register will be set when both tones are detected. By default, this programmable tone pair detector is set to detect the dual alert tone pair (2130Hz and 2750Hz) used on some Type 1 CLI systems. The output of this detector is not currently used by the on-chip µController, however, this register can be accessed by the @R command.

The Call Progress detector measures the amplitude of the signal at the output of a 275 - 665 Hz bandpass filter and sets bit 10 of the DSP Status Register to 1 when the signal level exceeds the measurement threshold. This is handled automatically by the on-chip µController. When the CMX866 is on-hook, the Call Progress detector can be enabled so that it will detect voice activity arising from a parallel phone connection which is off-hook. The output of the DSP Status Register will need to be monitored by the external host µC, using an @R command, for several seconds and decision taken on whether there is voice activity.

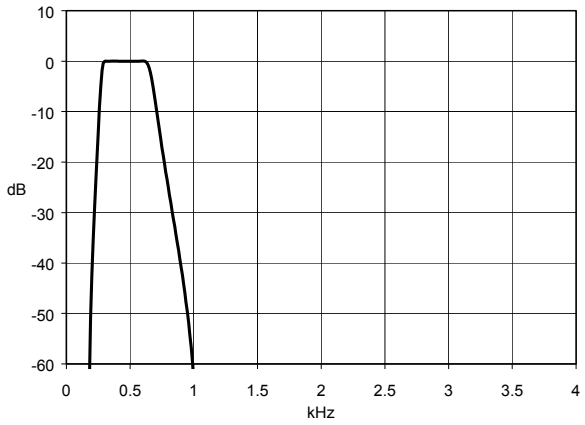


Figure 8a Response of Call Progress Filter

The Answer Tone detector measures both amplitude and frequency of the received signal and sets bit 6 or bit 7 of the DSP Status Register respectively when a valid 2225Hz or 2100Hz signal is received. This is handled automatically by the on-chip µController, which looks for either of the Answer Tones.

1.5.11 Rx Modem Filterering and Demodulation

When the receive part of the CMX866 is operating as a modem, the received signal is fed to a bandpass filter to attenuate unwanted signals and to provide fixed compromise line equalisation for 1200 and 2400 bps FSK, DPSK and QAM modes. The characteristics of the bandpass filter and equaliser are determined by the chosen receive modem type and frequency band. The fixed compromise line equaliser may be enabled or disabled by bit 1 of the S24 register and compensates for one quarter of the relative amplitude and delay distortion of ETS Test Line 1.

The responses of these filters, including the line equaliser and the effect of external components used in Figures 4a and 4b, are shown in Figures 8b-e:

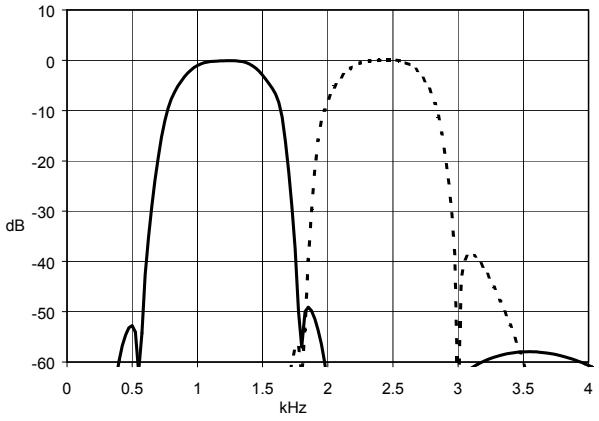


Figure 8b QAM/DPSK Rx Filters

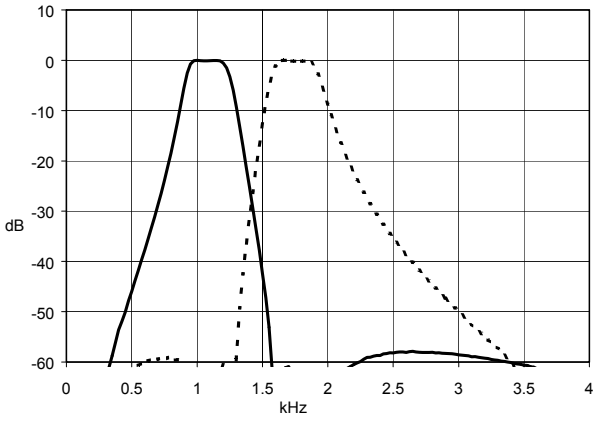


Figure 8c V.21 Rx Filters

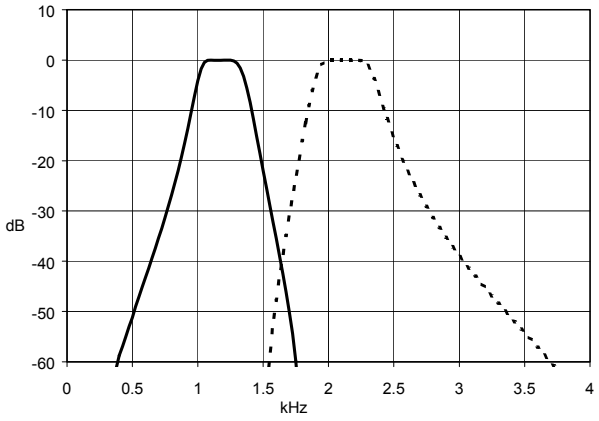


Figure 8d Bell 103 Rx Filters

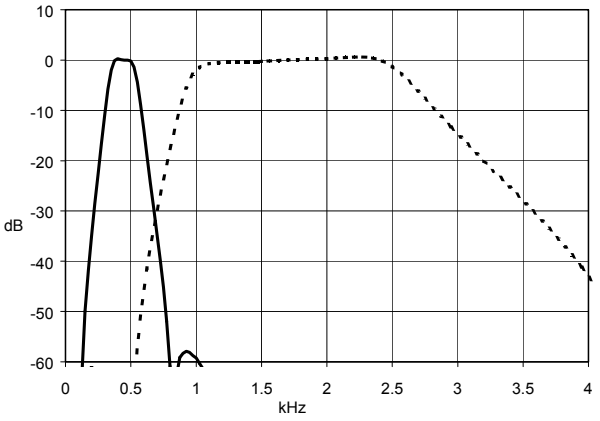


Figure 8e V.23/Bell 202 Rx Filters

The signal level at the output of the Receive Modem Filter and Equaliser is measured in the Modem Energy Detector block, compared to a threshold value, and the result is automatically handled by the on-chip µController.

The output of the Receive Modem Filter and Equaliser is also applied to the FSK or QAM/DPSK demodulator depending on the selected modem type.

The FSK demodulator recognises individual frequencies as representing received ‘1’ or ‘0’ data bits:

The QAM/DPSK demodulator decodes QAM or DPSK modulation of a 1200Hz or 2400Hz carrier and is used for V.22, V.22 bis and Bell 212A modes. It includes an adaptive receive signal equaliser (auto-

equaliser) that will automatically compensate for a wide range of line conditions in both QAM and DPSK modes. It must be enabled when receiving 2400bps QAM by setting bit 2 of the S24 register. The auto-equaliser can provide a useful improvement in performance in 1200bps DPSK as well as 2400bps QAM modes, so although it must be disabled at the start of a handshake sequence, it can be enabled as soon as scrambled 1200bps 1s have been detected.

Both FSK and QAM/DPSK demodulators produce a serial data bit stream which is fed to the Rx pattern detector, descrambler and USART block (see Figure 9a). In QAM/DPSK modes the demodulator input is also monitored for the V.22 bis handshake 'S1' signal.

The QAM/DPSK demodulator also estimates the received bit error rate by comparing the actual received signal against an ideal waveform. This estimate is placed in bits 2-0 of the DSP Status Register. However, the estimate is not required for CMX866 operation and so is ignored by the on-chip µController.

1.5.12 Rx Modem Pattern Detectors and Descrambler

See Figure 9a.

The 1010.. pattern detector operates only in FSK modes and will set bit 9 of the DSP Status Register when 32 bits of alternating 1's and 0's have been received.

The 'Continuous Unscrambled 1's' detector operates in all modem modes and will set bits 8 and 7 of the DSP Status Register to 01 when 32 consecutive 1's have been received.

The descrambler operates only in DPSK/QAM modes and is enabled automatically by the on-chip µController.

The 'Continuous Scrambled 1's' detector operates only in DPSK/QAM modes when the descrambler is enabled and will set bits 8 and 7 of the DSP Status Register to 11 when 32 consecutive 1's appear at the output of the descrambler. To avoid possible ambiguity, the 'Scrambled 1's' detector is disabled when continuous unscrambled 1's are detected.

The 'Continuous 0's' detector will set bits 8 and 7 of the DSP Status Register to 10 when NX consecutive 0's have been received, NX being 32 except when DPSK/QAM Start-Stop mode has been selected, in which case NX = 2N + 4 where N is the number of bits per character including the Start, Stop and any Parity bits.

All of these pattern detectors will hold the 'detect' output for 12 bit times after the end of the detected pattern unless the received bit rate or operating mode is changed, in which case the detectors are reset within 2ms.

The DSP Status Register is automatically polled by the on-chip µController, which then interprets the results of these pattern detectors.

1.5.13 Rx Data Register and USART

A flexible Rx USART is provided for all modem modes. It can be programmed by bits 6 and 7 of the S26 register to treat the received data bit stream as Synchronous data or as Start-Stop characters.

In Synchronous mode the received data bits are all sent to the Rx Data Buffer, which is copied into the DSP Rx Data Register after every 8 bits.

In Start-Stop mode the USART Control logic looks for the start of each character, then sends only the required number of data bits (not parity) to the Rx Data Buffer. The parity bit (if used) and the presence of a Stop bit are then checked and the data bits in the Rx Data Buffer copied into the DSP Rx Data Register.

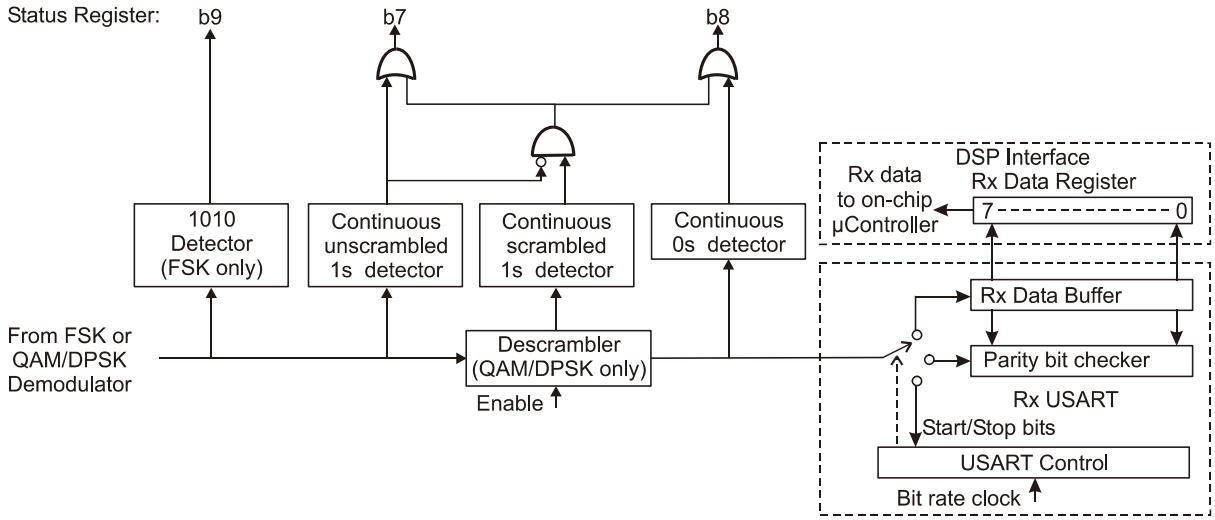


Figure 9a Rx Modem Data Paths

Whenever a new character is copied into the DSP Rx Data Register, the Rx Data Ready flag bit of the DSP Status Register is set to 1 to prompt the on-chip µController to read the new data and, in Start-Stop mode, the Even Rx Parity flag bit of the DSP Status Register is updated.

In Start-Stop mode, if the Stop bit is missing (received as a 0 instead of a 1) the received character will still be placed into the DSP Rx Data Register and the Rx Data Ready flag bit set, but the DSP Status Register Rx Framing Error bit will also be set to 1 and the USART will re-synchronise onto the next 1 – 0 (Stop – Start) transition. The Rx Framing Error bit will remain set until the next character has been received.

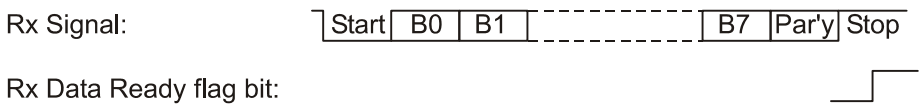


Figure 9b Rx USART Function (Start-Stop mode, 8 Data Bits + Parity)

If, for any reason, the on-chip µController has not read the previous data from the DSP Rx Data Register by the time that new data is copied to it from the Rx Data Buffer, then the Rx Data Overflow flag bit of the DSP Status Register will be set to 1.

The Rx Data Ready flag and Rx Data Overflow bits are automatically cleared to 0 when the DSP Rx Data Register is read by the on-chip µController. The handling of these low-level status flags is performed automatically by the on-chip µController and is transparent to the user.

1.6 Application Notes

1.6.1 Hardware Interface

The CMX866 can be interfaced to an external host µC, as shown in Figure 11, or to an RS232 computer port (via a level shifter IC, to generate ±6V), as shown in Figure 12. These are complete phone line interface circuits for operation at V_{DD} = 5.0V. Figure 12 includes the additional gyrator components which may be required for CTR21 compliance.

It is recommended that the full, 9-wire interface should be used, where practical. This is illustrated functionally in Figure 10a. In some applications it will be necessary to move the safety barrier to the serial port interface of the CMX866. If opto-couplers are used to achieve the safety isolation required, a reduced RS232 interface, shown in Figure 10b, may be preferred for economic reasons.

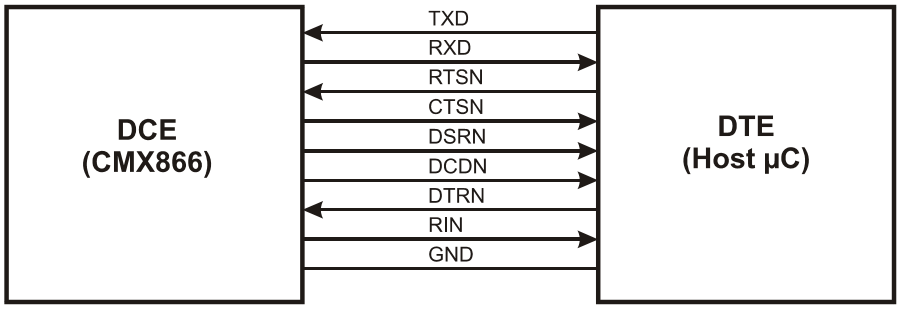


Figure 10a Full RS232 Link

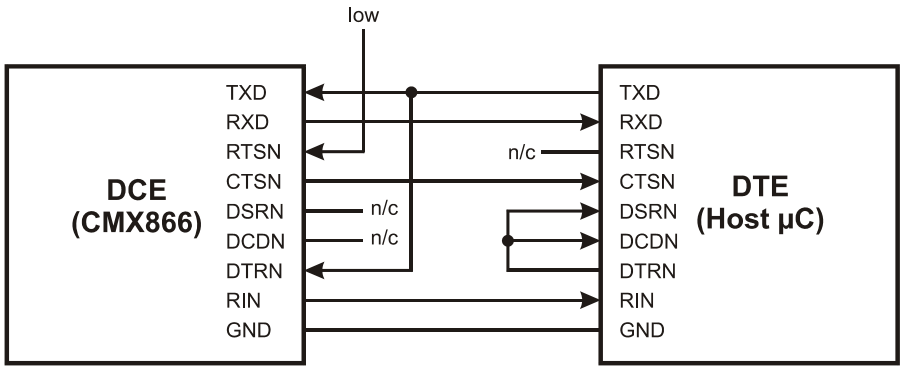


Figure 10b Reduced RS232 Link

The TXD signal can be used to wake up the CMX866 from Powersave or 'Zero-Power' states, as shown above. The external host µC should ignore CTSN and write a character byte to the CMX866 via the TXD pin, which is connected to the DTRN pin. This will wake up the CMX866 because the DTRN pin is pulled low. The byte written, and any further activity on the TXD pin for up to 30ms when coming out of 'Zero-Power' state (or up to 10µs when coming out of Powersave state), will be corrupted. Normal data transfer can commence when the CTSN pin goes low, providing the RTSN pin is already low.

If the DTRN pin is not connected to the TXD pin, the TXD signal cannot be used on its own to wake up the CMX866. If the DTRN pin is permanently wired low it will not be possible to wake up the CMX866 from an external host µC. Moreover, it will not be possible to put the CMX866 into either a Powersave or 'Zero-Power' state in the first place, so the device will remain permanently operational.

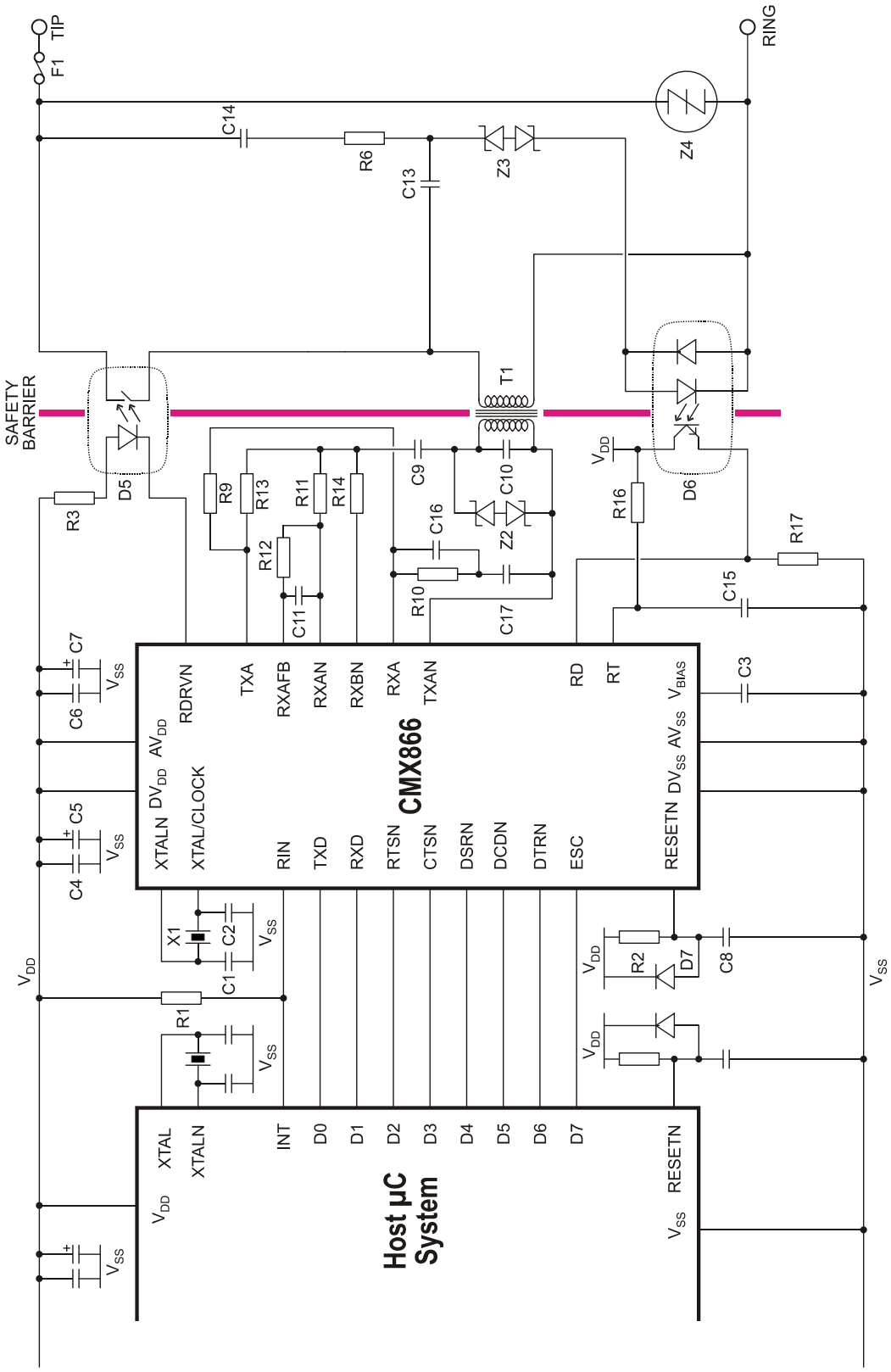


Figure 11 Host µC Example (FCC68)

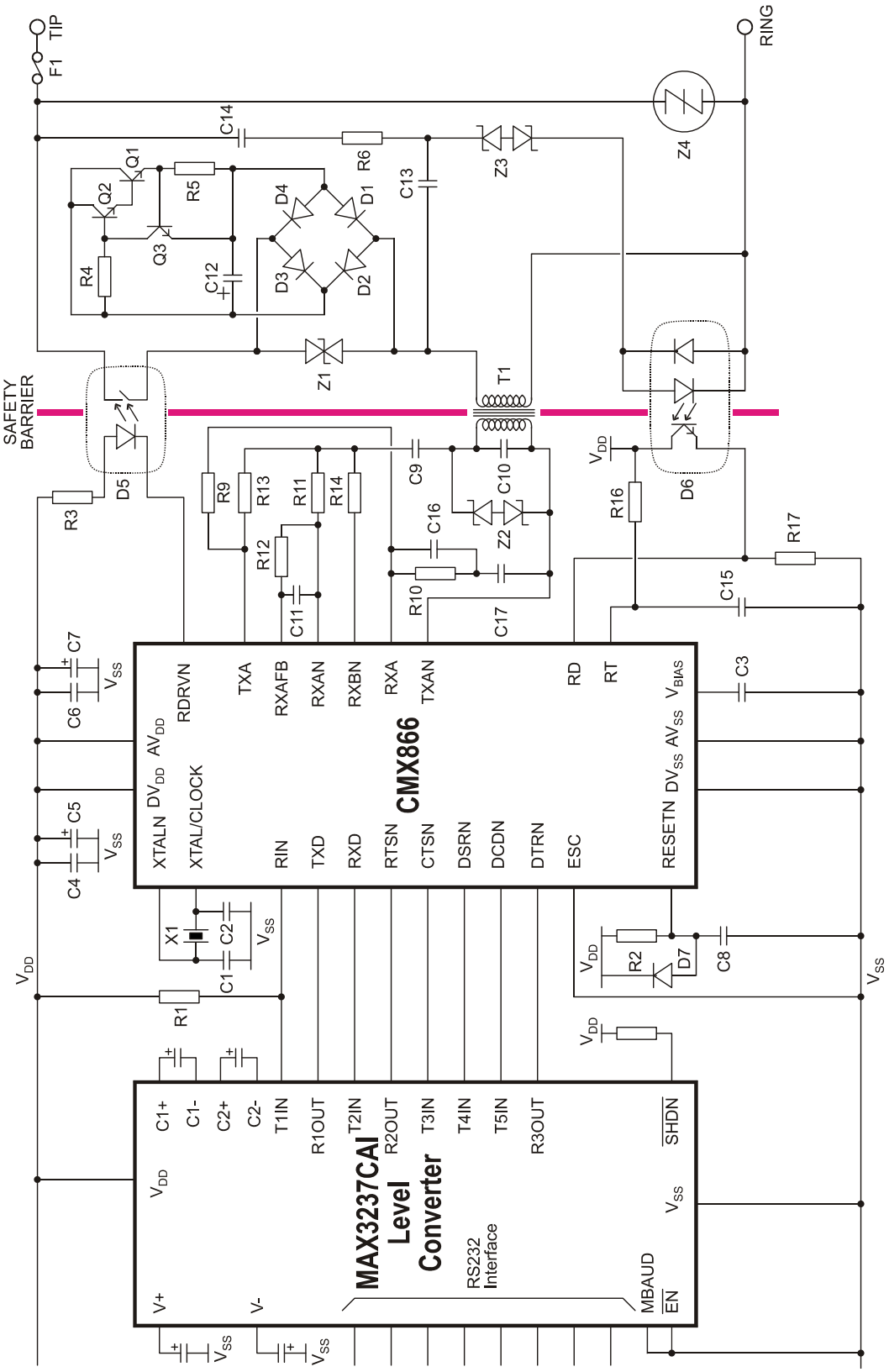


Figure 12 RS232 Level Converter Example (CTR21)

Figures 11 and 12 - Component List:

Reference	Value	Tolerance	Supplier	Comment
C1, C2	22pF	±20%	Generic	
C3, C4, C6	100nF	±20%	Generic	
C5, C7	10µF	±20%	Generic	
C8	100nF	±20%	Generic	user selectable
C9 (FCC)	not fitted			replace with wire link
C9 (CTR21)	2.2µF, 16V	±20%	Generic	non-polarised
C10 (FCC)	33nF	±20%	Generic	
C10 (CTR21)	100nF	±20%	Generic	
C11	100pF	±20%	Generic	
C12 (FCC)	not used			
C12 (CTR21)	10µF, 50V	±20%	Generic	polarised, electrolytic
C13	100nF	±20%	Generic	
C14	330nF, 250V	±20%	Syfer 1812J250	
C15	330nF	±20%	Generic	
C16 (FCC)	47pF	±10%	Generic	
C16 (CTR21)	220pF	±10%	Generic	
C17	100nF	±10%	Generic	
D1, D2, D3, D4	not used			(FCC)
D1, D2, D3, D4	CBRHD-02	~	CENTRAL SEMI	(CTR21)
D5	LCA110S	~	CLARE	
D6	PS2701-1	~	NEC	also use a BAS16 diode
D7	BAS16	~	Generic	
F1	C515-1.25	~	BUSSMANN	1.25A slow blow
Q1, Q2 (FCC)	not used			
Q1, Q2 (CTR21)	FZT605	~	ZETEX	
Q3 (FCC)	not used			
Q3 (CTR21)	BC846ALT1	~	MOTOROLA	
R1	100kΩ	±5%	Generic	
R2	100kΩ	±5%	Generic	user selectable
R3	620Ω	±5%	Generic	
R4 (FCC)	not used			
R4 (CTR21)	33kΩ	±5%	Generic	
R5 (FCC)	not used			
R5 (CTR21)	11.5Ω, 125mW	±1%	Generic	
R6	10kΩ, 0.5W	±5%	Generic	
R7, R8	not used			
R9	120kΩ	±1%	Generic	
R10	180kΩ	±1%	Generic	

Reference	Value	Tolerance	Supplier	Comment
R11 (FCC)	62kΩ	±1%	Generic	optimum value = 64k9Ω
R11 (CTR21)	56kΩ	±1%	Generic	optimum value = 57k6Ω
R12	100kΩ	±1%	Generic	
R13	390Ω	±1%	Generic	optimum value = 392Ω
R14	5k6Ω	±1%	Generic	optimum value = 6k04Ω
R15	not used			
R16	470kΩ	±5%	Generic	
R17	20kΩ	±5%	Generic	
T1 (FCC)	82111	~	MIDCOM	
T1 (CTR21)	82107	~	MIDCOM	
X1	11.0592MHz	±0.01%	RALTRON	
Z1 (FCC)	not used			
Z1 (CTR21)	P6SMB33CAT3	~	MOTOROLA	
Z2	CMPZDA4V3	~	CENTRAL SEMI	
Z3	CMPZDA18V	~	CENTRAL SEMI	
Z4	P3100SC	~	TECCOR	310V SIDACTOR
MAX3237CAI	MAX3237CAI	~	MAXIM	LEVEL CONVERTER
CMX866	CMX866	~	CML	MODEM IC

1.6.2 Calling Modem AT Commands

General Commands for Initialisation

- wake-up CMX866 from 'Zero-Power' state (pull DTRN pin low)
- restore factory defaults ATZ
- set Tx gain and data format ATS25=x
- set communications standard ATS27=x or ATBn
- set Rx gain and data format ATS26=x
- set guard time (if required) ATS23=x or AT&Gn
- set lost carrier to hang-up delay ATS10=x
- set other features (as required) (S12, S14, S24, S28 and S29 registers)

Specific Tx Commands

- set calling and response characteristics ATS22=x or ATXn
- set DTMF tone duration ATS11=x
- set pause time for comma dial modifier ATS8=x
- set wait for carrier after dial ATS7=x
- set wait time for blind dialling ATS6=x
- check correct settings AT&V

Call Setup

- go off-hook and dial directory number ATD<number>
- progress call and go to data mode when call established. (This is automatic)
- return to command mode <escape sequence>
- go on-hook ATH0
- return CMX866 to 'Zero-Power' state AT&Z0

1.6.3 Answering Modem AT Commands

General Commands for Initialisation

- wake-up CMX866 from 'Zero-Power' state (pull DTRN pin low)
- set features (as required) (see above)

Specific Rx Commands

- set handshake timeout ATS17=x
- enable automatic answer ATS0=x
- check correct settings AT&V

Call Answer

- go off-hook and answer an incoming call on RING ATA
- progress call and go to data mode when call established. (This is automatic)
- return to command mode <escape sequence>
- go on-hook ATH0
- return CMX866 to 'Zero-Power' state AT&Z0

1.6.4 RS232 Transaction Sequence

A typical RS232 transaction sequence is shown in Figure 13 below:

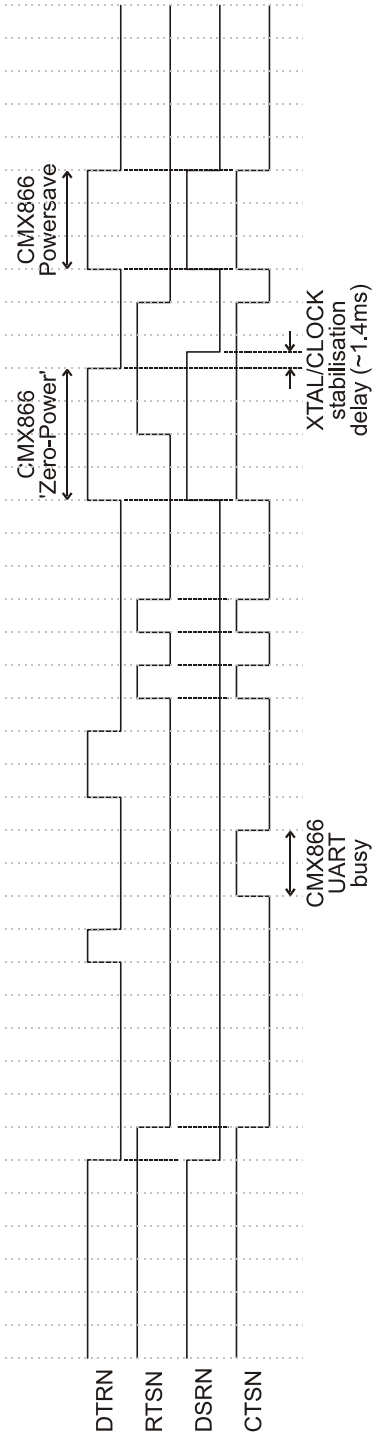


Figure 13 RS232 Transaction Sequence

1.7 Performance Specification

1.7.1 Electrical Performance

1.7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-50	+50	mA
Current into RDRVN pin (RDRVN pin low)		+50	mA
Current into or out of any other pin	-20	+20	mA

D1 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		740	mW
... Derating		7.4	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

D6 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		1490	mW
... Derating		14.9	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

1.7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		2.7	5.5	V
Operating Temperature		-40	+85	°C

1.7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
V_{DD} = 2.7V to 5.5V at Tamb = -40 to +85°C,
Xtal Frequency = 11.0592MHz ± 0.01% (100ppm)
0dBm corresponds to 775mVrms.

DC Parameters	Notes	Min.	Typ.	Max.	Units
I_{DD} ('Zero-Power' mode)	1, 2	-	3.0	10.0	µA
I_{DD} (Powersave mode, V_{DD} = 3.0V)	1, 2	-	0.6	1.5	mA
I_{DD} (Powersave mode, V_{DD} = 5.0V)	1, 2	-	1.5	3.0	mA
I_{DD} (µC operating, DSP powerdown, V_{DD} = 3.0V)	1	-	1.7	3.5	mA
I_{DD} (µC operating, DSP powerdown, V_{DD} = 5.0V)	1	-	3.7	7.5	mA
I_{DD} (µC and DSP operating, V_{DD} = 3.0V)	1, 3	-	3.4	7.0	mA
I_{DD} (µC and DSP operating, V_{DD} = 5.0V)	1, 3	-	6.2	12.5	mA
I_{DD} (µC and DSP operating, V_{DD} = 3.0V)	1	-	5.0	10.0	mA
I_{DD} (µC and DSP operating, V_{DD} = 5.0V)	1	-	9.0	18.0	mA
Logic '1' Input Level	4	70%	-	-	V_{DD}
Logic '0' Input Level	4	-	-	30%	V_{DD}
Logic Input Leakage Current (Vin = 0 to V_{DD}), (excluding XTAL/CLOCK input)		-1.0	-	+1.0	µA
Output Logic '1' Level (I_{OH} = 2 mA)		80%	-	-	V_{DD}
Output Logic '0' Level (I_{OL} = -3 mA)		-	-	0.4	V
IRQN O/P 'Off' State Current (Vout = V_{DD})		-	-	1.0	µA
RD and RT pin Schmitt trigger input high-going threshold (Vthi) (see Figure 14)		$0.56V_{DD}$	-	$0.56V_{DD}$ + 0.6V	V
RD and RT pin Schmitt trigger input low-going threshold (Vtlo) (see Figure 14)		$0.44V_{DD}$ - 0.6V	-	$0.44V_{DD}$	V
RDRVN 'ON' resistance to V_{SS} (V_{DD}= 3.0V)		-	50	70	Ω
RDRVN 'OFF' resistance to V_{DD} (V_{DD}= 3.0V)		-	1300	3000	Ω

XTAL/CLOCK Input (timings for an external clock input)	Notes	Min.	Typ.	Max.	Units
'High' Pulse Width		30	-	-	ns
'Low' Pulse Width		30	-	-	ns

Transmit QAM and DPSK Modes (V.22, Bell 212A, V.22 bis)	Notes	Min.	Typ.	Max.	Units
Carrier frequency, high band	5	-	2400	-	Hz
Carrier frequency, low band	5	-	1200	-	Hz
Baud rate	6	-	600	-	Baud
Bit rate (V.22, Bell 212A)	6	-	1200	-	bps
Bit rate (V.22 bis)	6	-	2400	-	bps
550Hz guard tone frequency		548	550	552	Hz
550Hz guard tone level wrt data signal		-4.0	-3.0	-2.0	dB
1800Hz guard tone frequency		1797	1800	1803	Hz
1800Hz guard tone level wrt data signal		-7.0	-6.0	-5.0	dB

Transmit V.21 FSK Mode	Notes	Min.	Typ.	Max.	Units
Baud rate	6	-	300	-	Baud
Mark (logical 1) frequency, high band		1647	1650	1653	Hz
Space (logical 0) frequency, high band		1847	1850	1853	Hz
Mark (logical 1) frequency, low band		978	980	982	Hz
Space (logical 0) frequency, low band		1178	1180	1182	Hz

Transmit Bell 103 FSK Mode	Notes	Min.	Typ.	Max.	Units
Baud rate	6	-	300	-	Baud
Mark (logical 1) frequency, high band		2222	2225	2228	Hz
Space (logical 0) frequency, high band		2022	2025	2028	Hz
Mark (logical 1) frequency, low band		1268	1270	1272	Hz
Space (logical 0) frequency, low band		1068	1070	1072	Hz

Transmit V.23 FSK Mode	Notes	Min.	Typ.	Max.	Units
Baud rate	6	-	1200/75	-	Baud
Mark (logical 1) frequency, 1200 baud		1298	1300	1302	Hz
Space (logical 0) frequency, 1200 baud		2097	2100	2103	Hz
Mark (logical 1) frequency, 75 baud		389	390	391	Hz
Space (logical 0) frequency, 75 baud		449	450	451	Hz

Transmit Bell 202 FSK Mode	Notes	Min.	Typ.	Max.	Units
Baud rate	6	-	1200/150	-	Baud
Mark (logical 1) frequency, 1200 baud		1198	1200	1202	Hz
Space (logical 0) frequency, 1200 baud		2197	2200	2203	Hz
Mark (logical 1) frequency, 150 baud		386	387	388	Hz
Space (logical 0) frequency, 150 baud		486	487	488	Hz

DTMF/Single Tone Transmit	Notes	Min.	Typ.	Max.	Units
Tone frequency accuracy		-0.2	-	+0.2	%
Distortion	7	-	1.0	2.0	%

Transmit Output Level	Notes	Min.	Typ.	Max.	Units
Modem and Single Tone modes	7	-4.0	-3.0	-2.0	dBm
DTMF mode, Low Group tones	7	-2.0	-1.0	0.0	dBm
DTMF: level of High Group tones wrt Low Group	7	+1.0	+2.0	+3.0	dB
Tx output buffer gain control accuracy	7	-0.25	-	+0.25	dB

Receive QAM and DPSK Modes (V.22, Bell 212A, V.22 bis)	Notes	Min.	Typ.	Max.	Units
Carrier frequency (high band)		2392	2400	2408	Hz
Carrier frequency (low band)		1192	1200	1208	Hz
Baud rate	9	-	600	-	Baud
Bit rate (V.22, Bell 212A)	9	-	1200	-	bps
Bit rate (V.22 bis)	9	-	2400	-	bps

Receive V.21 FSK Mode	Notes	Min.	Typ.	Max.	Units
Acceptable baud rate		297	300	303	Baud
Mark (logical 1) frequency, high band		1638	1650	1662	Hz
Space (logical 0) frequency, high band		1838	1850	1862	Hz
Mark (logical 1) frequency, low band		968	980	992	Hz
Space (logical 0) frequency, low band		1168	1180	1192	Hz

Receive Bell 103 FSK Mode	Notes	Min.	Typ.	Max.	Units
Acceptable baud rate		297	300	303	Baud
Mark (logical 1) frequency, high band		2213	2225	2237	Hz
Space (logical 0) frequency, high band		2013	2025	2037	Hz
Mark (logical 1) frequency, low band		1258	1270	1282	Hz
Space (logical 0) frequency, low band		1058	1070	1082	Hz

Receive V.23 FSK Mode	Notes	Min.	Typ.	Max.	Units
1200 baud	16				
Acceptable baud rate		1188	1200	1212	Baud
Mark (logical 1) frequency		1280	1300	1320	Hz
Space (logical 0) frequency		2080	2100	2120	Hz
75 baud	16				
Acceptable baud rate		74	75	76	Baud
Mark (logical 1) frequency		382	390	398	Hz
Space (logical 0) frequency		442	450	458	Hz

Receive Bell 202 FSK Mode	Notes	Min.	Typ.	Max.	Units
1200 baud	16				
Acceptable baud rate		1188	1200	1212	Baud
Mark (logical 1) frequency		1180	1200	1220	Hz
Space (logical 0) frequency		2180	2200	2220	Hz
150 baud	16				
Acceptable baud rate		148	150	152	Baud
Mark (logical 1) frequency		377	387	397	Hz
Space (logical 0) frequency		477	487	497	Hz

Rx Modem Signal (FSK, DPSK and QAM Modes)	Notes	Min.	Typ.	Max.	Units
Signal level	10	-45	-	-9	dBm
Signal to Noise Ratio (noise flat 300-3400Hz)		20	-	-	dB

Rx Modem S1 Pattern Detector (DPSK and QAM modes)	Notes	Min.	Typ.	Max.	Units
Will detect S1 pattern lasting for		90.0	-	-	ms
Will not detect S1 pattern lasting for				72.0	
Hold time (minimum detector 'On' time)		5.0	-	-	ms

Rx Modem Energy Detector	Notes	Min.	Typ.	Max.	Units
Detect threshold ('Off' to 'On)	10,11	-	-	-43.0	dBm
Undetect threshold ('On' to 'Off')	10,11	-48.0	-	-	dBm
Hysteresis	10,11	2.0	-	-	dB
Detect ('Off' to 'On') response time					
QAM and DPSK modes	10,11	10.0	-	35.0	ms
300 and 1200 baud FSK modes	10,11	8.0	-	30.0	ms
150 and 75 baud FSK modes	10,11	16.0	-	60.0	ms
Undetect ('On' to 'Off') response time					
QAM and DPSK modes	10,11	10.0	-	55.0	ms
300 and 1200 baud FSK modes	10,11	10.0	-	40.0	ms
150 and 75 baud FSK modes	10,11	20.0	-	80.0	ms

Rx Answer Tone Detectors	Notes	Min.	Typ.	Max.	Units
Detect threshold ('Off' to 'On)	10,12	-	-	-43.0	dBm
Undetect threshold ('On' to 'Off')	10,12	-48.0	-	-	dBm
Hysteresis	10,12	2.0	-	-	dB
Detect ('Off' to 'On') response time	10,12	30.0	33.0	45.0	ms
Undetect ('On' to 'Off') response time	10,12	7.0	18.0	25.0	ms
2100Hz detector					
'Will detect' frequency		2050	-	2160	Hz
'Will not detect' frequency		-	-	2000	Hz
2225Hz detector					
'Will detect' frequency		2160	-	2285	Hz
'Will not detect' frequency		2335	-	-	Hz

Rx Call Progress Energy Detector	Notes	Min.	Typ.	Max.	Units
Bandwidth (-3dB points) See Figure 8a		275	-	665	Hz
Detect threshold ('Off' to 'On)	10,13	-	-	-37.0	dBm
Undetect threshold ('On' to 'Off')	10,13	-42.0	-	-	dBm
Detect ('Off' to 'On') response time	10,13	30.0	36.0	45.0	ms
Undetect ('On' to 'Off') response time	10,13	6.0	8.0	50.0	ms

Receive Input Amplifier	Notes	Min.	Typ.	Max.	Units
Input impedance (at 100Hz)		10.0			Mohm
Open loop gain (at 100Hz)			10000		V/V
Rx Gain Control Block accuracy		-0.25		+0.25	dB

DTMF Decoder	Notes	Min.	Typ.	Max.	Unit
Valid input signal levels (each tone of composite signal)	10	-30.0	-	0.0	dBm
Not decode level (either tone of composite signal)	10	-	-	-36.0	dBm
Twist = High Tone/Low Tone		-10.0	-	6.0	dB
Frequency Detect Bandwidth		±1.8	-	-	%
Frequency Not Detect Bandwidth		-	-	±3.5	%
Max level of low frequency noise (i.e dial tone)					
Interfering signal frequency <= 550Hz	14	-	-	0.0	dB
Interfering signal frequency <= 450Hz	14	-	-	10.0	dB
Interfering signal frequency <= 200Hz	14	-	-	20.0	dB
Max. noise level wrt. signal	14,15	-	-	-10.0	dB
DTMF detect response time	17	-	40.0	-	ms
DTMF de-response time		-	-	30.0	ms
Status Register b5 high time		14.0	-	-	ms
'Will Detect' DTMF signal duration		40.0	-	-	ms
'Will Not Detect' DTMF signal duration		-	25.0	-	ms
Pause length detected		30.0	-	-	ms
Pause length ignored		-	-	15.0	ms

Notes:

1. At 25°C, not including any current drawn from the CMX866 pins by external circuitry other than X1, C1 and C2.
2. All logic inputs at V_{SS} except for RT, DTRN and RTSN inputs which are at DV_{DD}.
3. DSP is powered up but in a reset state.
4. Excluding RD and RT pins.
5. % carrier frequency accuracy is the same as XTAL/CLOCK % frequency accuracy.
6 Tx signal % baud or bit rate accuracy is the same as XTAL/CLOCK % frequency accuracy.
7. Measured between TXA and TXAN pins with Tx Level Control gain set to 0dB, 1k2Ω load between TXA and TXAN, at V_{DD} = 3.0V (levels are proportional to V_{DD} - see section 1.4.2). Level measurements for all modem modes are performed with random transmitted data and without any guard tone. 0dBm = 775mVrms.
8. Measured on the 2 or 4-wire line using the line interface circuits described in section 1.4.2 with the Tx line signal level set to -10dBm for QAM, DPSK, FSK or single tones, -6dBm and -8dBm for DTMF tones. Excludes any distortion due to external components such as the line coupling transformer.
9. These are the bit and baud rates of the line signal, the acceptable tolerance is ±0.01%.
10. Rx 2 or 4-wire line signal level assuming 1dB loss in line coupling transformer with Rx Gain Control block set to 0dB and external components as section 1.4.2.
11. Thresholds and times measured with random data for QAM and DPSK modes, continuous binary '1' for all FSK modes. Fixed compromise line equaliser enabled. Signal switched between off and -33dBm
12. 'Typical' value refers to 2100Hz or 2225Hz signal switched between off and -33dBm. Times measured with respect to the received line signal
13. 'Typical' values refers to 400Hz signal switched between off and -33dBm
14. Referenced to DTMF tone of lower amplitude.
15. Flat Gaussian Noise in 300-3400Hz band.
16. For V.23r (Tx1200/Rx75) and Bell 202r (Tx1200/Rx150) the calling modem carrier detect time is typically 1700ms.
17. The decode time is directly affected by signal quality but, for good signals, will always be much less than the 100ms required for PSTN use.

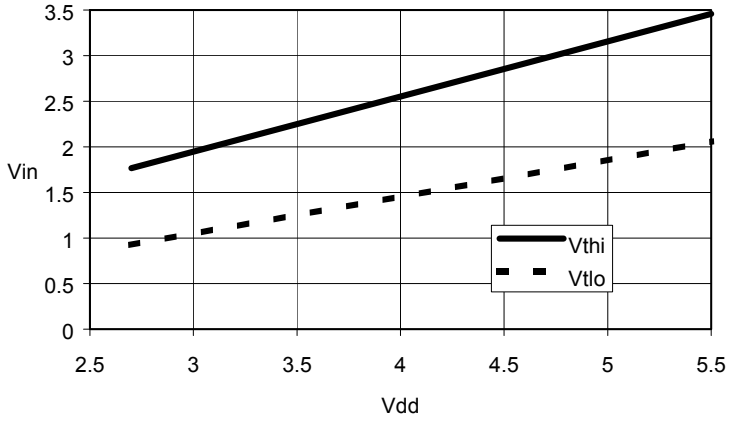


Figure 14 Typical Schmitt Trigger Input Voltage Thresholds vs. V_{DD}

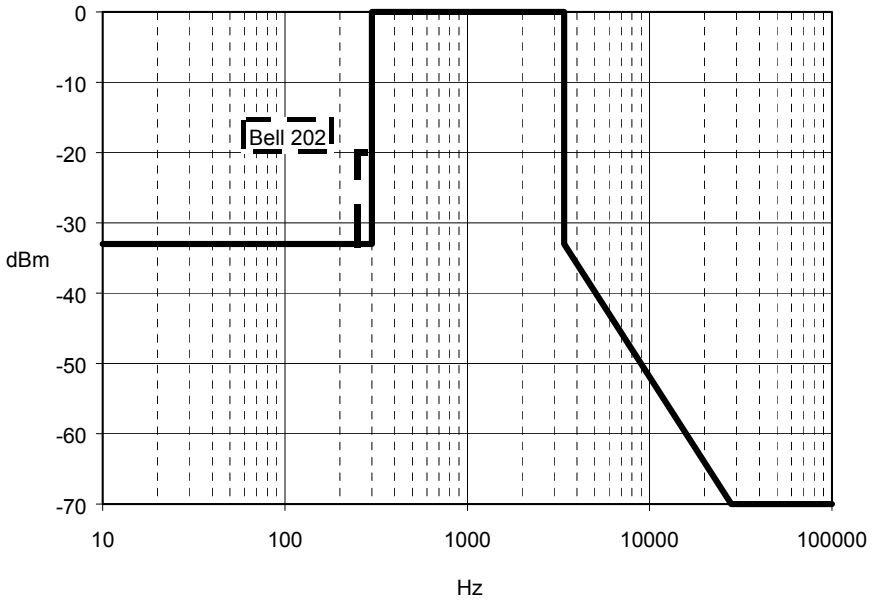
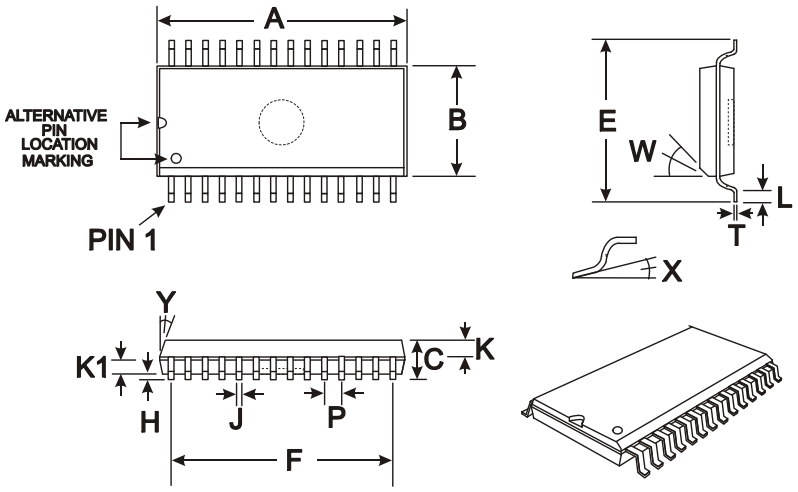


Figure 15 Maximum Out of Band Tx Line Energy Limits (see note 8)

1.7.2 Packaging



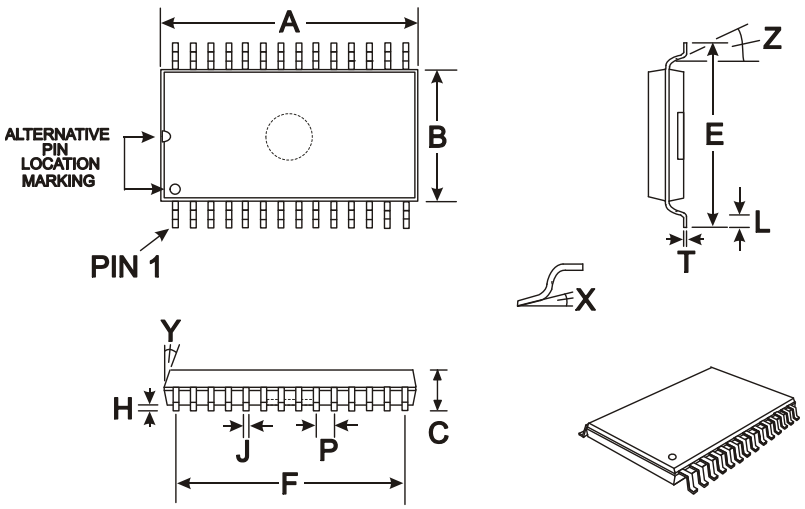
	DIM.	MIN.	TYP.	MAX.
*	A	0.697 (17.70)		0.711 (18.06)
*	B	0.286 (7.26)		0.299 (7.59)
	C	0.088 (2.24)		0.105 (2.67)
	E	0.390 (9.90)		0.419 (10.64)
	F		0.650 (16.51)	
	H	0.003 (0.08)		0.020 (0.51)
	J	0.013 (0.33)		0.018 (0.46)
	K		0.041 (1.04)	
	K1		0.041 (1.04)	
	L	0.016 (0.41)		0.050 (1.27)
	P		0.050 (1.27)	
	T	0.009 (0.23)		0.0125 (0.32)
	W		45°	
	X	0°		10°
	Y		7°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees
Co-Planarity of leads within 0.004" (0.1mm)

Figure 16a 28-pin SOIC (D1) Mechanical Outline: *Order as part no. CMX866D1*



	DIM.	MIN.	TYP.	MAX.
*	A	9.90		10.50
*	B	5.00		5.60
	C	1.67		2.00
	E	7.40		8.20
	F		8.45	
	H	0.05		0.21
	J	0.22		0.38
	L	0.55		0.95
	P		0.65	
	T	0.09		0.25
	X	0°		8°
	Y	7°		9°
	Z	4°		12°

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 16b 28-pin SSOP (D6) Mechanical Outline: *Order as part no. CMX866D6*

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