Preferred Device

Sensitive Gate Silicon Controlled Rectifiers Reverse Blocking Thyristors

Designed for industrial and consumer applications such as temperature, light and speed control; process and remote controls; warning systems; capacitive discharge circuits and MPU interface.

Features

- Center Gate Geometry for Uniform Current Density
- All Diffused and Glass-Passivated Junctions for Parameter Uniformity and Stability
- Small, Rugged Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Low Trigger Currents, 200 µA Maximum for Direct Driving from Integrated Circuits
- Pb-Free Packages are Available*

MAXIMUM RATINGS (T_J = 25° C unless otherwise noted)

Rating	Symbol	Value	Unit
$\begin{array}{l} \mbox{Peak Repetitive Off-State Voltage (Note 1)} \\ (T_J = -40 \ to \ 110^\circ C, \ Sine \ Wave, \\ 50 \ Hz \ to \ 60 \ Hz) & MCR72-3 \\ MCR72-6 \\ MCR72-8 \end{array}$	V _{DRM,} V _{RRM}	100 400 600	V
On-State RMS Current (180° Conduction Angles; T _C = 83°C)	I _{T(RMS)}	8.0	Α
Peak Non-Repetitive Surge Current (1/2 Cycle, 60 Hz, T _J = 110°C)	I _{TSM}	100	Α
Circuit Fusing Considerations (t = 8.3 ms)	l ² t	40	A ² s
Forward Peak Gate Voltage (t \leq 10 µs, T _C = 83°C)	V _{GM}	±5.0	V
Forward Peak Gate Current (t \leq 10 µs, T _C = 83°C)	I _{GM}	1.0	А
Forward Peak Gate Power (t \leq 10 μ s, T _C = 83°C)	P _{GM}	5.0	W
Average Gate Power (t = 8.3 ms, T_C = 83°C)	P _{G(AV)}	0.75	W
Operating Junction Temperature Range	TJ	-40 to +110	°C
Storage Temperature Range	T _{stg}	-40 to +150	°C
Mounting Torque	-	8.0	in. lb.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

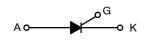
 V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking

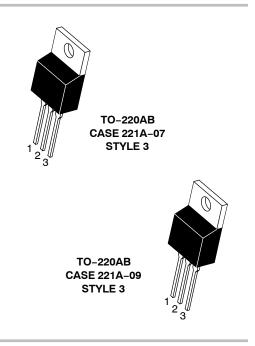


ON Semiconductor®

http://onsemi.com

SCRs 8 AMPERES RMS 100 thru 600 VOLTS





PIN ASSIGNMENT			
1	Cathode		
2	Anode		
3	Gate		
4	Anode		

MARKING AND ORDERING INFORMATION

See detailed marking, ordering, and shipping information in the package dimensions section on page 5 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Мах	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.2	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	60	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Secs	TL	260	°C

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted.)

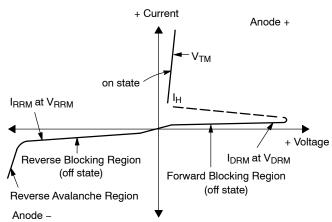
				1	1	r
Characteristic		Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS						
Peak Repetitive Forward or Reverse Blocking Current (Note 2) $(V_{AK} = Rated V_{DRM} \text{ or } V_{RRM}; R_{GK} = 1 k\Omega)$	T _J = 25°C T _J = 110°C	I _{DRM} , I _{RRM}			10 500	μΑ μΑ
High Logic Level Supply Current from V_{CC}		I _{CCH}	4	4	μA	μA
ON CHARACTERISTICS						
Peak Forward On-State Voltage (I_{TM} = 16 A Peak, Pulse Width \leq 1 ms, Duty Cycle \leq 2%)		V _{TM}	-	1.7	2.0	V
Gate Trigger Current (Continuous dc) (Note 3) $(V_D = 12 \text{ V}, \text{ R}_L = 100 \Omega)$		I _{GT}	-	30	200	μΑ
Gate Trigger Voltage (Continuous dc) (Note 3) $(V_D = 12 \text{ V}, \text{ R}_L = 100 \Omega)$		V _{GT}	-	0.5	1.5	V
Gate Non-Trigger Voltage (V_D = 12 Vdc, R_L = 100 Ω , T_J = 110°C)		V _{GD}	0.1	-	-	V
Holding Current (V _D = 12 V, Initiating Current = 200 mA, R _{GK} = 1 k Ω)		I _H	-	-	6.0	mA
Gate Controlled Turn-On Time $(V_D = Rated V_{DRM}, I_{TM} = 16 A, I_G = 2 mA)$		t _{gt}	-	1.0	-	μs
DYNAMIC CHARACTERISTICS						
Critical Rate-of-Rise of Off-State Voltage		dv/dt	-	10	-	V/μs

Critical Rate-of-Rise of Off-State Voltage	dv/dt	-	10	-	V/μs
(V _D = Rated V _{DRM} , R _{GK} = 1 k Ω , T _J = 110°C, Exponential Waveform)					-

Ratings apply for negative gate voltage or R_{GK} = 1 kΩ. Devices shall not have a positive gate voltage concurrently with a negative voltage on the anode. Devices should not be tested with a constant current source for forward and reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.
R_{GK} current not included in measurement.

Voltage Current Characteristic of SCR

Symbol	Parameter
V _{DRM}	Peak Repetitive Off State Forward Voltage
I _{DRM}	Peak Forward Blocking Current
V _{RRM}	Peak Repetitive Off State Reverse Voltage
I _{RRM}	Peak Reverse Blocking Current
V _{TM}	Peak On State Voltage
Ι _Η	Holding Current



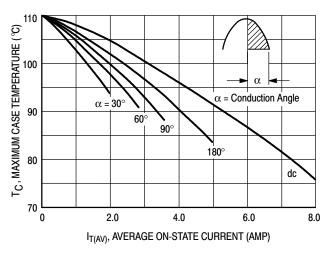


Figure 1. Average Current Derating

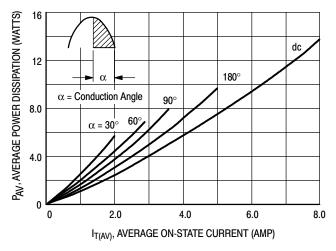


Figure 2. On-State Power Dissipation

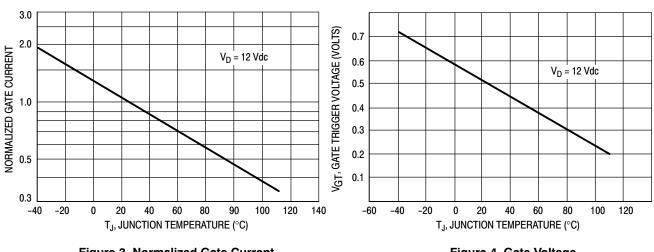
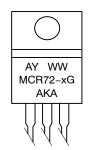


Figure 3. Normalized Gate Current



MARKING DIAGRAMS

TO-220AB CASE 221A-07



=	Assembly Location
=	Year
=	Work Week
=	Device Code
	x = 3, 6, 8, or 8T
=	Pb-Free Package
=	Diode Polarity
	= = =

TO-220AB CASE 221A-09



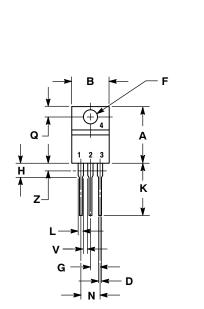
A	= Assembly Location
Y	= Year
WW	= Work Week
MCR72-6T	= Device Code
G	= Pb-Free Package
AKA	= Diode Polarity

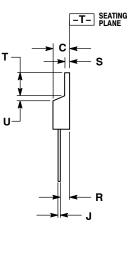
ORDERING INFORMATION

Device	Package	Shipping
MCR72-3	TO-220AB	
MCR72-3G	TO-220AB (Pb-Free)	500 H - H - (D -
MCR72-6	TO-220AB	500 Units / Box
MCR72-6G	TO-220AB (Pb-Free)	
MCR72-6T	TO-220AB	
MCR72-6TG	TO-220AB (Pb-Free)	50 Units / Rail
MCR72-8	TO-220AB	
MCR72-8G	TO-220AB (Pb-Free)	500 Units / Box
MCR72-8T	TO-220AB	
MCR72-8TG	TO-220AB (Pb-Free)	50 Units / Rail

PACKAGE DIMENSIONS

TO-220 CASE 221A-07 ISSUE O





т

NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

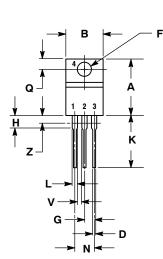
	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.570	0.620	14.48	15.75
В	0.380	0.405	9.66	10.28
С	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
Н	0.110	0.155	2.80	3.93
J	0.014	0.022	0.36	0.55
Κ	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
Ν	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
Т	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
۷	0.045		1.15	
Ζ		0.080		2.04

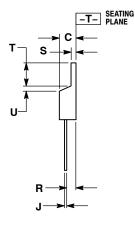
STYLE 3: PIN 1. CATHODE

2. ANODE

3. GATE 4. ANODE

TO-220 CASE 221A-09 **ISSUE AF**





NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI

Y14.5M, 1982. CONTROLLING DIMENSION: INCH. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE 2 3.

ALLOWED.
 INCHES

 DIM
 MIN
 MAX

 A
 0.570
 0.620

 B
 0.380
 0.405

 C
 0.190
 0.190
 MILLIMETERS MIN MAX 14.48 15.75 9.66 10.28 4.07 4.82 D 0.025 0.035 F 0.142 0.161 0.64 0.88 3.61 4.09 G 0.095 0.105 2.42 2.66 H 0.110 0.155 2.80 3.93
 J
 0.014
 0.025

 K
 0.500
 0.562
 L

 L
 0.045
 0.060
 0.36 0.64 12.70 14.27 1.15 1.52
 N
 0.190
 0.210

 Q
 0.100
 0.120
 4.83 5.33 2.54 3.04 **R** 0.080 0.110 2.04 2.79
 S
 0.045
 0.055
 1.15
 1.39

 T
 0.235
 0.255
 5.97
 6.47

 U
 0.000
 0.050
 0.00
 1.27
 V 0.045 Z ---1.15 0.080 2.04 STYLE 3: PIN 1. CATHODE

2. ANODE GATE

GATE
ANODE

ON Semiconductor and IIII are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any provided in SCILLC data sheets and/or specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is a Equal Opportunity/Affirmative Action Employer. This literature is subject to all application ecopyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada Email: orderlit@onsemi.com N. American Technical Support: 800–282–9855 Toll Free USA/Canada Europe, Middle East and Africa Technical Support:

Phone: 421 33 790 2910 Japan Customer Focus Center Phone: 81–3–5773–3850 ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative