

40V COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET

Product Summary

Device	V _{(BR)DSS}	R _{DS(on)} max	I _D max (A) T _A = 25°C (Notes 3 & 5)
Q1	40V	25mΩ @ V _{GS} = 10V	7.5
		40mΩ @ V _{GS} = 4.5V	6.2
Q2	-40V	25mΩ @ V _{GS} = -10V	-7.3
		45mΩ @ V _{GS} = -4.5V	-5.7

Description and Applications

This MOSFET has been designed to ensure that R_{DS(on)} of N and P channel FET are matched to minimize losses in both arms of the bridge. The DMC4040SSD is optimized for use in 3 phases brushless DC motor circuits (BLDC), CCFL backlighting.

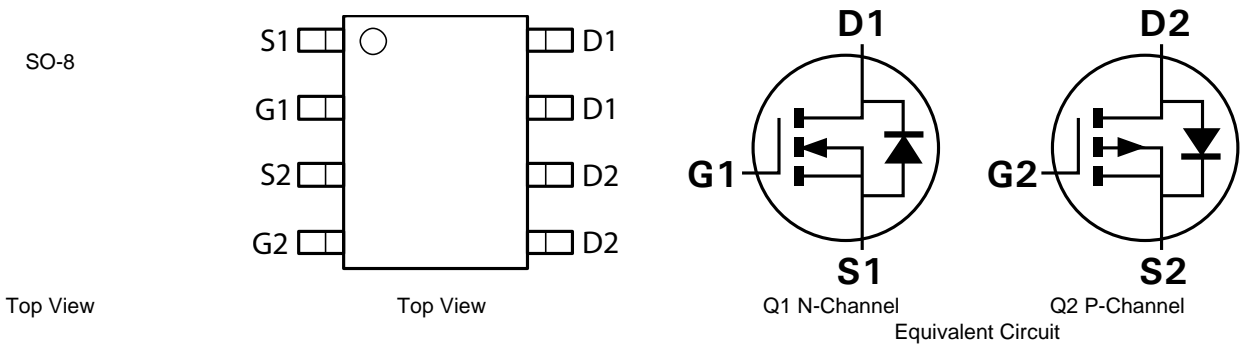
- 3 phases BLDC motor
- CCFL backlighting

Features and Benefits

- Matched N & P R_{DS(on)} - Minimizes power losses
- Fast switching – Minimizes switching losses
- Dual device – Reduces PCB area
- "Green" component and RoHS compliant (Note 1)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0 (Note 1)
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208
- Weight: 0.074 grams (approximate)

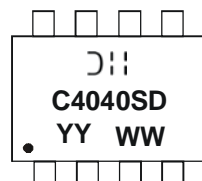


Ordering Information (Note 1)

Product	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
DMC4040SSD-13	C4040SD	13	12	2,500

Note: 1. Diodes, Inc. defines "Green" products as those which are RoHS compliant and contain no halogens or antimony compounds; further information about Diodes Inc.'s "Green" Policy can be found on our website. For packaging details, go to our website.

Marking Information



D = Manufacturer's Marking
 C4040SD = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Year (ex: 10 = 2010)
 WW = Week (01 - 53)

Maximum Ratings @ $T_A = 25^\circ\text{C}$ unless otherwise specified

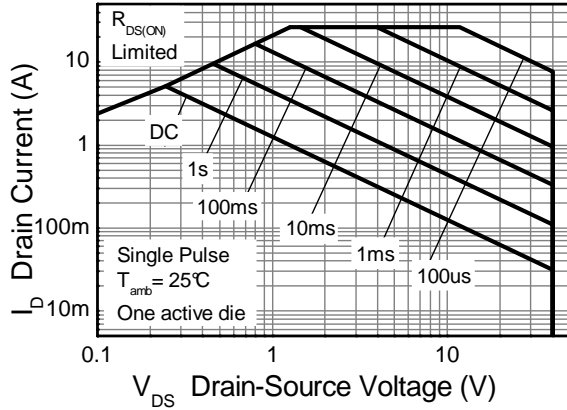
Characteristic			Symbol	N-Channel - Q1	P-Channel - Q2	Unit
Drain-Source Voltage			V_{DSS}	40	-40	V
Gate-Source Voltage			V_{GSS}	± 20	± 20	
Continuous Drain Current	$V_{GS} = 10\text{V}$	(Notes 3 & 5)	I_D	7.5	-7.5	A
		$T_A = 70^\circ\text{C}$ (Notes 3 & 5)		5.8	-5.8	
		(Notes 2 & 5)		5.7	-5.7	
		(Notes 2 & 6)		6.8	-6.8	
Pulsed Drain Current	$V_{GS} = 10\text{V}$	(Notes 4 & 5)	I_{DM}	29.0	-29.0	
Continuous Source Current (Body diode)			(Notes 3 & 5)	I_S	3.0	
Pulsed Source Current (Body diode)			(Notes 4 & 5)	I_{SM}	29.0	-29.0

Thermal Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

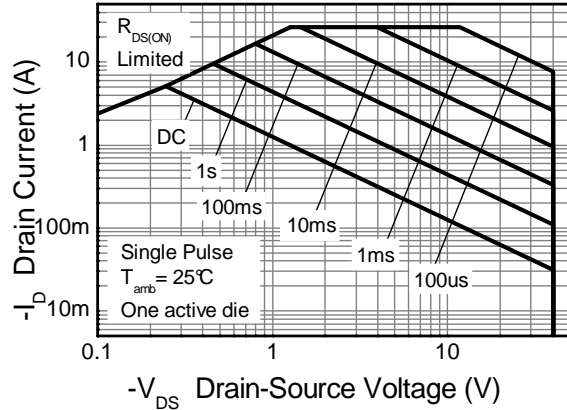
Characteristic		Symbol	N-Channel - Q1	P-Channel - Q2	Unit
Power Dissipation Linear Derating Factor	(Notes 2 & 5)	P_D	1.25		W mW/ $^\circ\text{C}$
			10		
	(Notes 2 & 6)		1.8		
			14.3		
Thermal Resistance, Junction to Ambient	(Notes 3 & 5)	$R_{\theta JA}$	2.14		$^\circ\text{C}/\text{W}$
			17.2		
	(Notes 2 & 5)		100		
	(Notes 2 & 6)		70		
Thermal Resistance, Junction to Lead	(Notes 3 & 5)	$R_{\theta JL}$	58		
	(Notes 5 & 7)		51		
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150		$^\circ\text{C}$

- Notes:
- For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
 - Same as note (2), except the device is measured at $t \leq 10$ sec.
 - Same as note (2), except the device is pulsed with $D = 0.02$ and pulse width 300 μs .
 - For a dual device with one active die.
 - For a device with two active die running at equal power.
 - Thermal resistance from junction to solder-point (at the end of the drain lead).

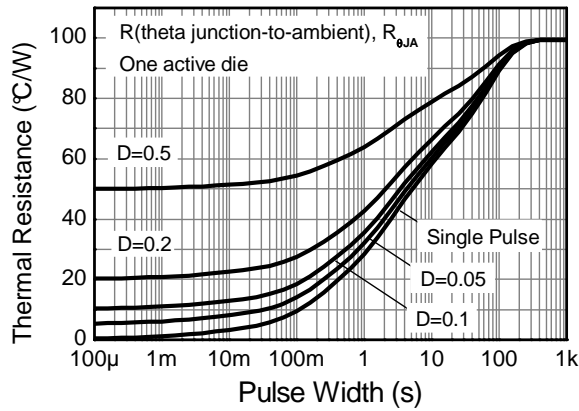
Thermal Characteristics



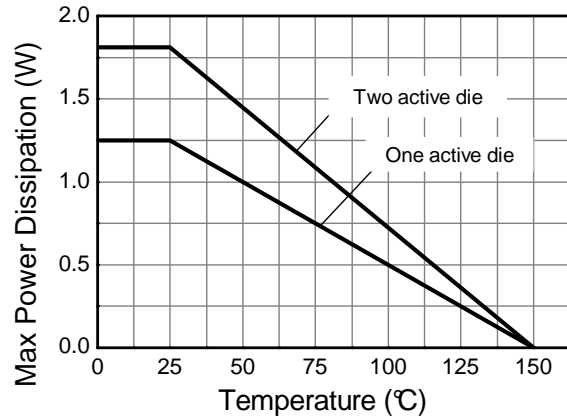
N-channel Safe Operating Area



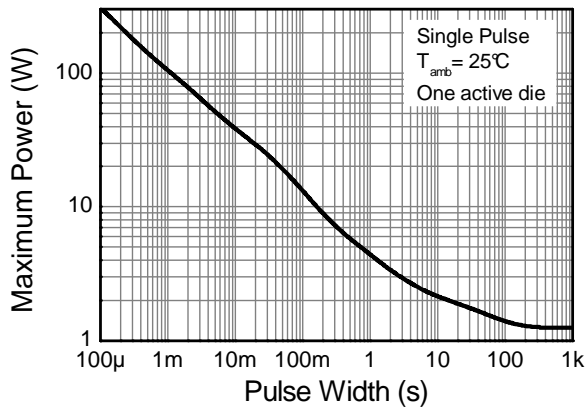
P-channel Safe Operating Area



Transient Thermal Impedance



Derating Curve



Pulse Power Dissipation

Electrical Characteristics – Q1 N-CHANNEL @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	40	—	—	V	I _D = 250μA, V _{GS} = 0V
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1.0	μA	V _{DS} = 40V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(th)}	0.8	1.3	1.8	V	I _D = 250μA, V _{DS} = V _{GS}
Static Drain-Source On-Resistance (Note 8)	R _{DS(on)}	—	0.013	0.025	Ω	V _{GS} = 10V, I _D = 3A
			0.028	0.040		V _{GS} = 4.5V, I _D = 3A
Forward Transconductance (Notes 8 & 9)	g _{fs}	—	12.6	—	S	V _{DS} = 5V, I _D = 3A
Diode Forward Voltage (Note 8)	V _{SD}	—	0.7	1.0	V	I _S = 1A, V _{GS} = 0V
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	—	1790	—	pF	V _{DS} = 20V, V _{GS} = 0V f = 1MHz
Output Capacitance	C _{oss}	—	160	—		
Reverse Transfer Capacitance	C _{rss}	—	120	—		
Gate Resistance	R _g	—	1.03	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge (Note 10)	Q _g	—	16.0	—	nC	V _{GS} = 4.5V V _{GS} = 10V V _{DS} = 20V I _D = 3A
Total Gate Charge (Note 10)	Q _g	—	37.6	—		
Gate-Source Charge (Note 10)	Q _{gs}	—	7.8	—		
Gate-Drain Charge (Note 10)	Q _{gd}	—	6.6	—		
Turn-On Delay Time (Note 10)	t _{D(on)}	—	8.1	—	ns	V _{DD} = 20V, V _{GS} = 10V I _D = 3A
Turn-On Rise Time (Note 10)	t _r	—	15.1	—		
Turn-Off Delay Time (Note 10)	t _{D(off)}	—	24.3	—		
Turn-Off Fall Time (Note 10)	t _f	—	5.3	—		

Notes: 8. Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%
 9. For design aid only, not subject to production testing.
 10. Switching characteristics are independent of operating junction temperatures.

Typical Characteristics – Q1 N-Channel

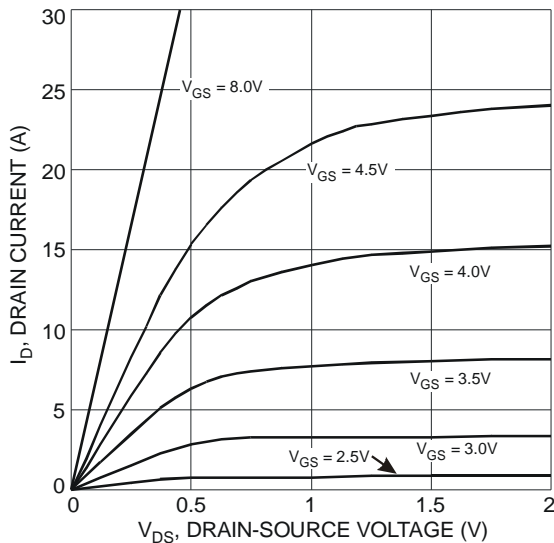


Fig. 1 Typical Output Characteristic

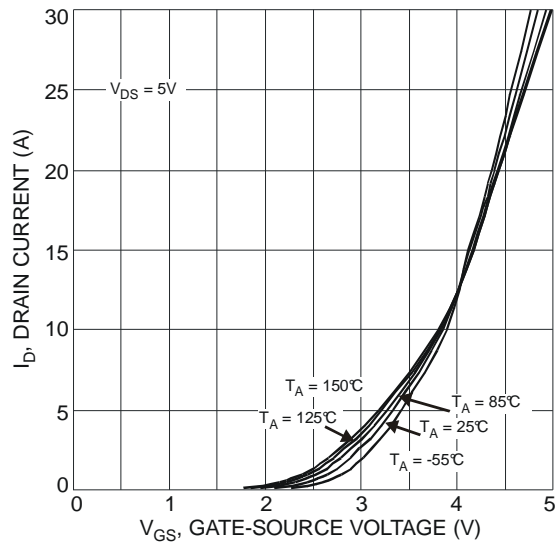


Fig. 2 Typical Transfer Characteristic

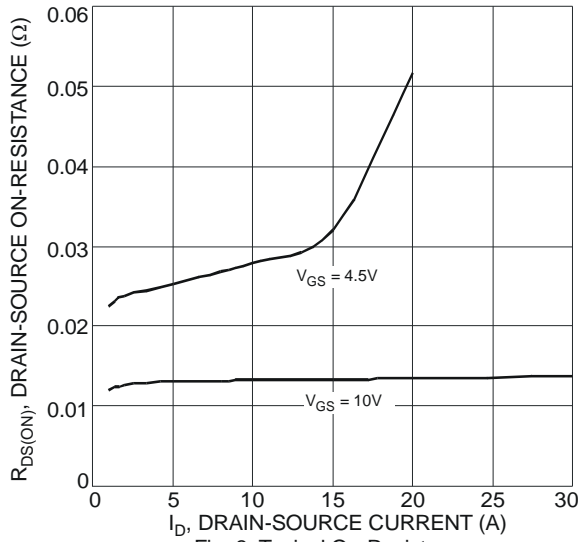


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

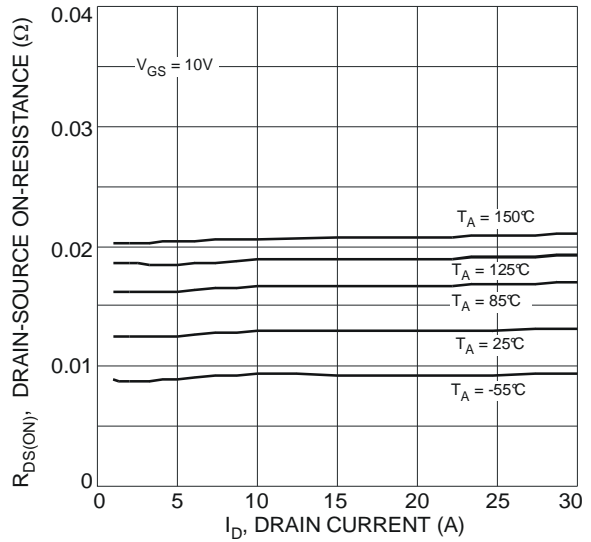


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

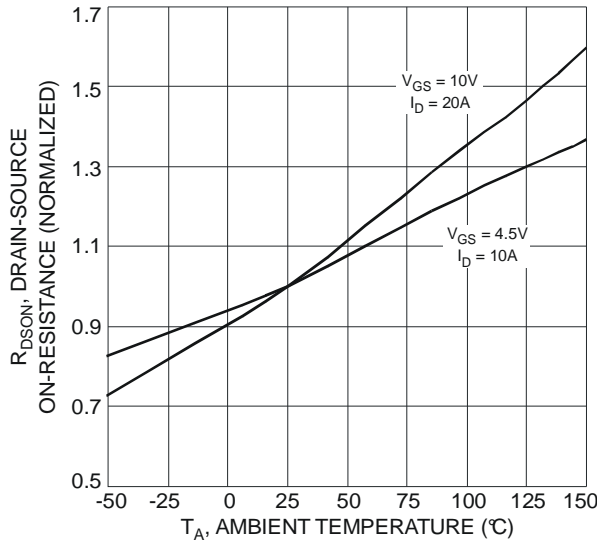


Fig. 5 On-Resistance Variation with Temperature

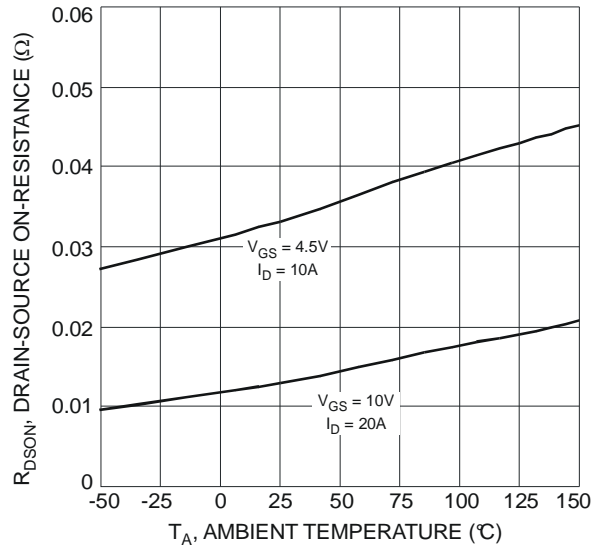


Fig. 6 On-Resistance Variation with Temperature

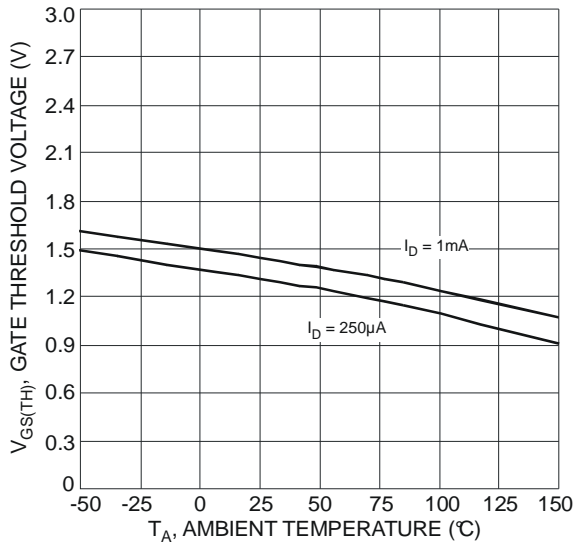


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

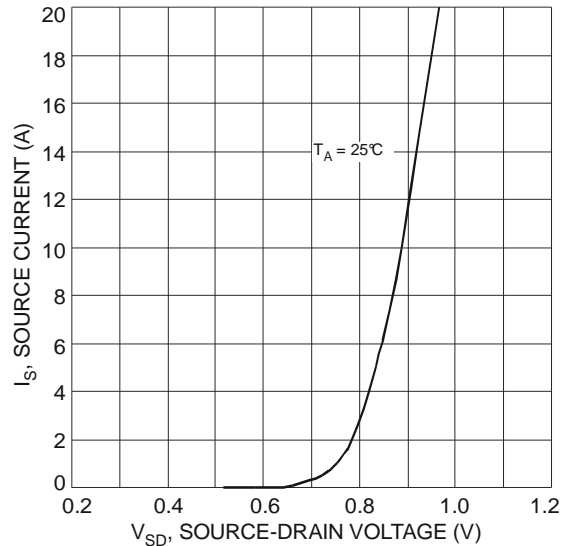


Fig. 8 Diode Forward Voltage vs. Current

DMC4040SSD

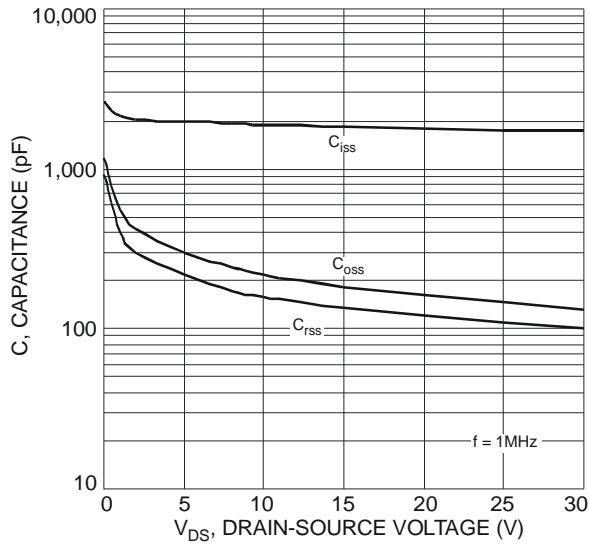


Fig. 9 Typical Total Capacitance

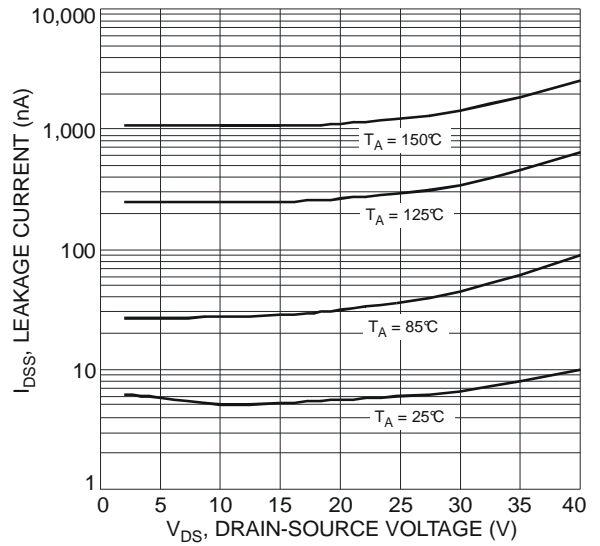


Fig. 10 Typical Leakage Current vs. Drain-Source Voltage

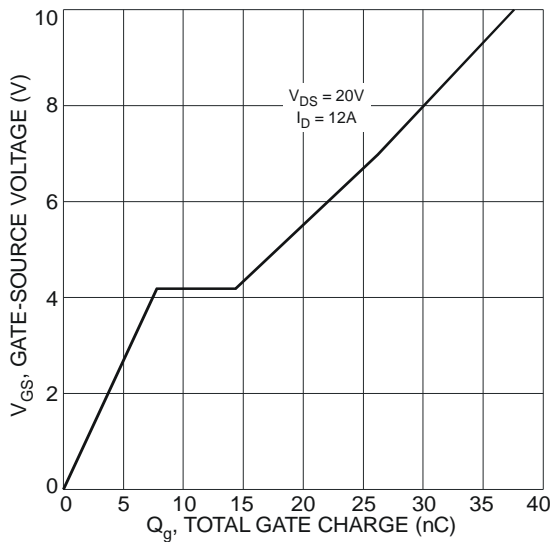


Fig. 11 Gate-Charge Characteristics

Electrical Characteristics – Q2 P-CHANNEL @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	-40	–	–	V	I _D = -250μA, V _{GS} = 0V
Zero Gate Voltage Drain Current	I _{DSS}	–	–	-1.0	μA	V _{DS} = -40V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	–	–	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(th)}	-0.8	-1.3	-1.8	V	I _D = -250μA, V _{DS} = V _{GS}
Static Drain-Source On-Resistance (Note 11)	R _{DS(on)}	–	0.018	0.025	Ω	V _{GS} = -10V, I _D = -3A
			0.030	0.045		V _{GS} = -4.5V, I _D = -3A
Forward Transconductance (Notes 11 & 12)	g _{fs}	–	16.6	–	S	V _{DS} = -5V, I _D = -3A
Diode Forward Voltage (Note 11)	V _{SD}	–	-0.7	-1.0	V	I _S = -1A, V _{GS} = 0V
DYNAMIC CHARACTERISTICS (Note 12)						
Input Capacitance	C _{iSS}	–	1643	–	pF	V _{DS} = -20V, V _{GS} = 0V f = 1MHz
Output Capacitance	C _{oss}	–	179	–		
Reverse Transfer Capacitance	C _{rss}	–	128	–		
Gate Resistance	R _g	–	6.43	–	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge (Note 13)	Q _g	–	14.0	–	nC	V _{GS} = -4.5V V _{DS} = -20V I _D = -3A
Total Gate Charge (Note 13)	Q _g	–	33.7	–		
Gate-Source Charge (Note 13)	Q _{gs}	–	5.5	–		
Gate-Drain Charge (Note 13)	Q _{gd}	–	7.3	–		
Turn-On Delay Time (Note 13)	t _{D(on)}	–	6.9	–	ns	V _{DD} = -20V, V _{GS} = -10V I _D = -3A
Turn-On Rise Time (Note 13)	t _r	–	14.7	–		
Turn-Off Delay Time (Note 13)	t _{D(off)}	–	53.7	–		
Turn-Off Fall Time (Note 13)	t _f	–	30.9	–		

Notes: 11. Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%
 12. For design aid only, not subject to production testing.
 13. Switching characteristics are independent of operating junction temperatures.

Typical Characteristics – Q2 P-Channel

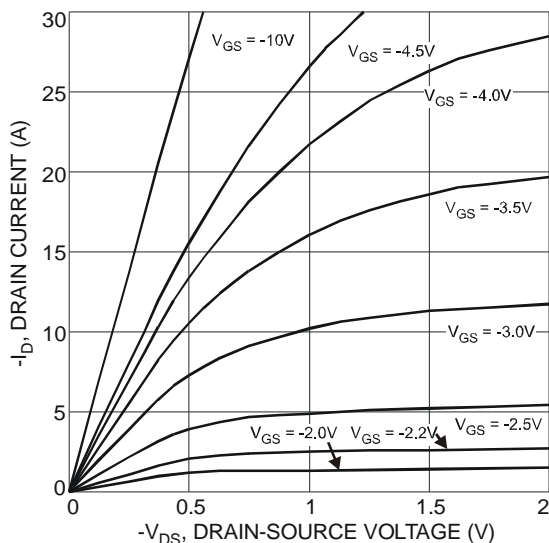


Fig. 12 Typical Output Characteristic

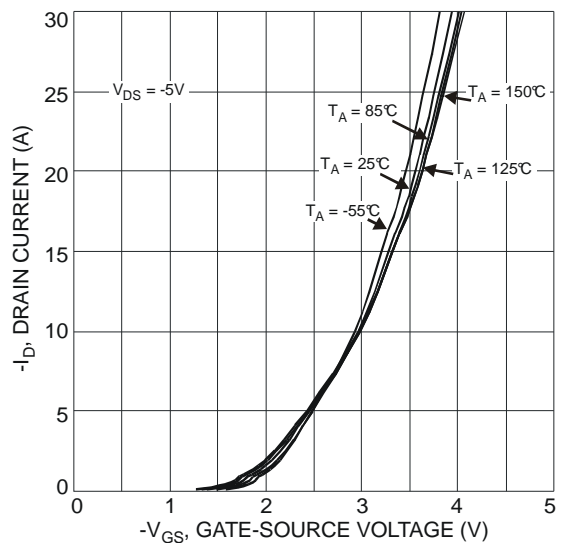


Fig. 13 Typical Transfer Characteristic

DMC4040SSD

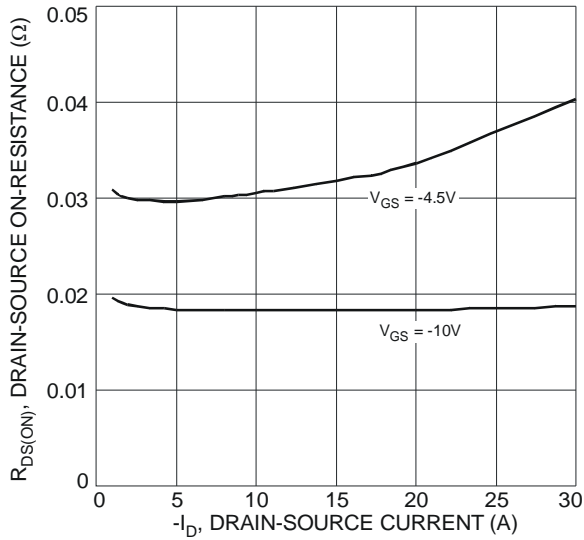


Fig. 14 Typical On-Resistance vs. Drain Current and Gate Voltage

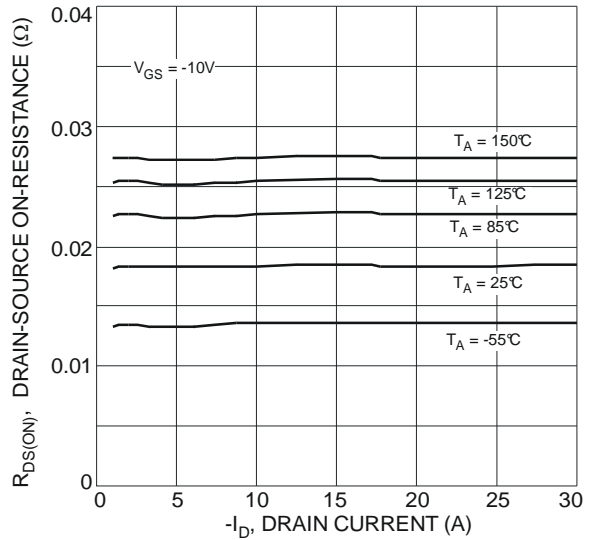


Fig. 15 Typical On-Resistance vs. Drain Current and Temperature

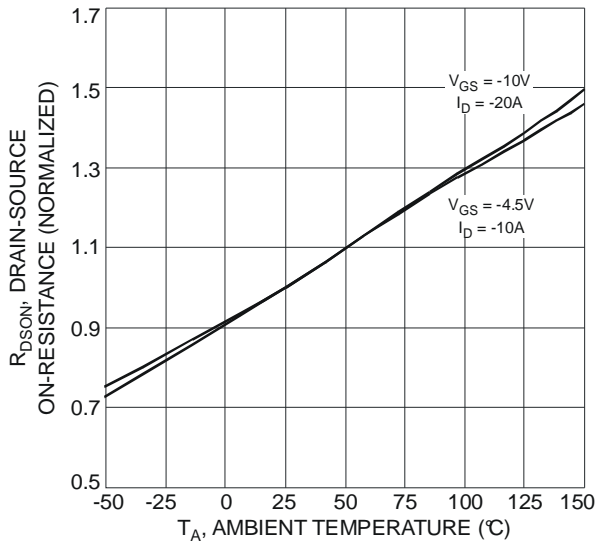


Fig. 16 On-Resistance Variation with Temperature

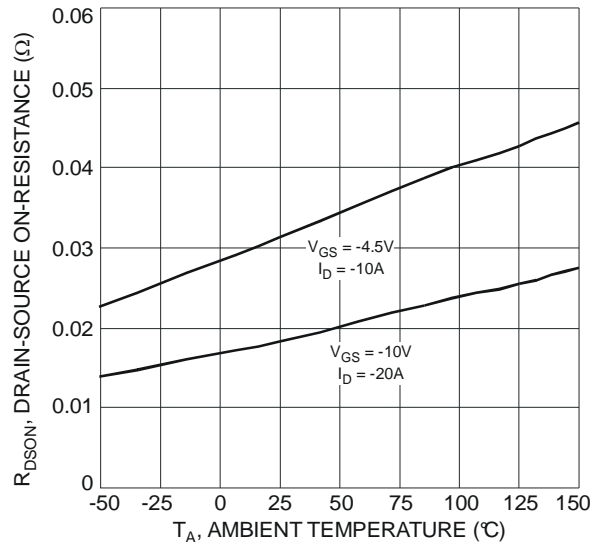


Fig. 17 On-Resistance Variation with Temperature

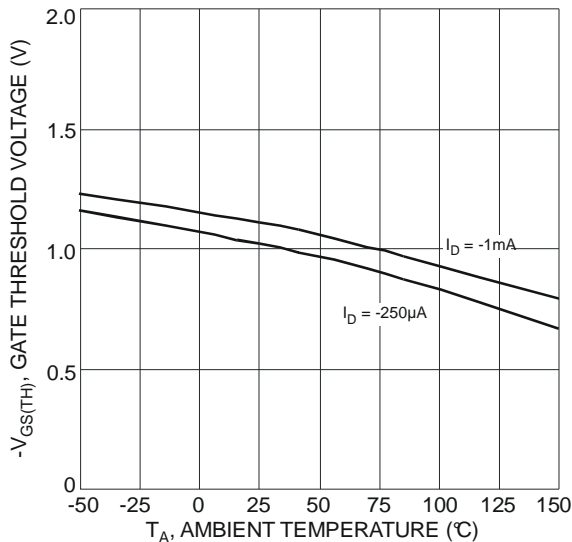


Fig. 18 Gate Threshold Variation vs. Ambient Temperature

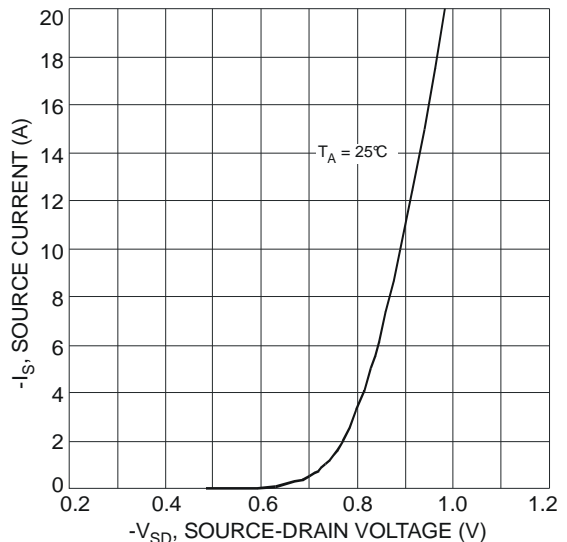


Fig. 19 Diode Forward Voltage vs. Current

DMC4040SSD

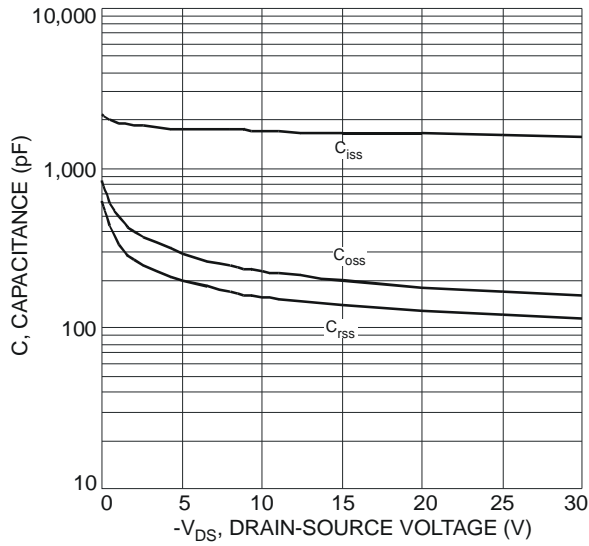


Fig. 20 Typical Total Capacitance

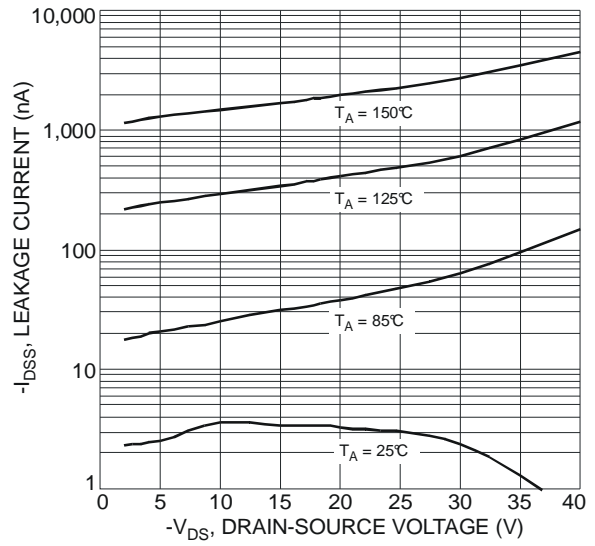


Fig. 21 Typical Leakage Current vs. Drain-Source Voltage

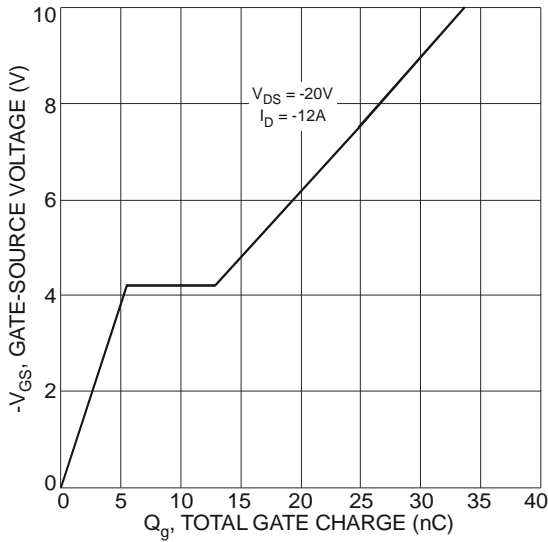
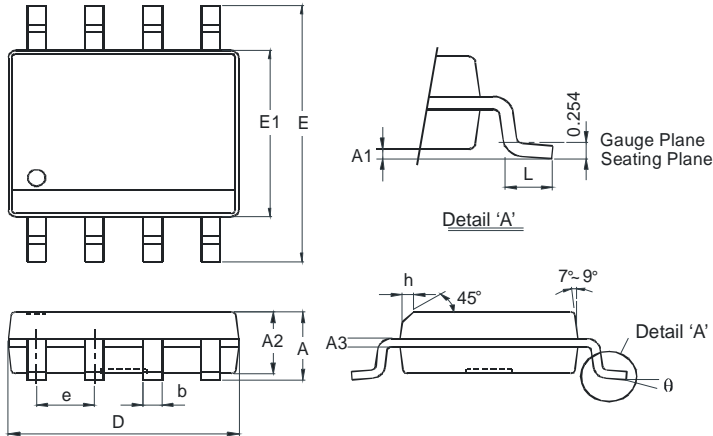


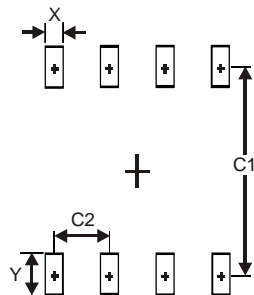
Fig. 22 Gate-Charge Characteristics

Package Outline Dimensions



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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