

**DMP21D0UFD**
**20V P-CHANNEL ENHANCEMENT MODE MOSFET**
**Product Summary**

$V_{(BR)DSS}$	$R_{DS(on)}$ Max	$I_D$ max $T_A = 25^\circ\text{C}$ (Notes 4)
-20V	495m $\Omega$ @ $V_{GS} = -4.5\text{V}$	-1.14A
	730m $\Omega$ @ $V_{GS} = -2.5\text{V}$	-0.94A
	960m $\Omega$ @ $V_{GS} = -1.8\text{V}$	-0.85A
	1300m $\Omega$ @ $V_{GS} = -1.5\text{V}$	-0.75A

**Description and Applications**

This MOSFET has been designed to minimize the on-state resistance ( $R_{DS(on)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Portable electronics

**Features and Benefits**

- Low Gate Threshold Voltage
- Fast Switching Speed
- **ESD Protected Gate 3KV**
- **Totally Lead-Free & Fully RoHS compliant (Note 1)**
- **Halogen and Antimony Free. "Green" Device (Note 2)**
- **Qualified to AEC-Q101 Standards for High Reliability**

**Mechanical Data**

- Case: X1-DFN1212-3
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.005 grams (approximate)

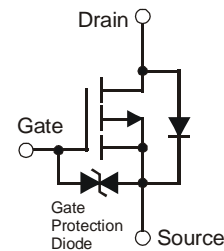
X1-DFN1212-3



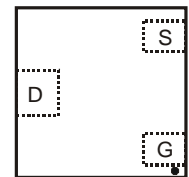
ESD PROTECTED TO 3kV

Top View

Bottom View



Equivalent Circuit

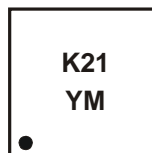


Pin-out Top view

**Ordering Information (Note 3)**

Part Number	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
DMP21D0UFD-7	K21	7	8	3000

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. Halogen and Antimony free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  3. For packaging details, go to our website at <http://www.diodes.com>.

**Marking Information**


K21 = Product Type Marking Code  
 YM = Date Code Marking  
 Y = Year (ex: Y = 2011)  
 M = Month (ex: 9 = September)

**Date Code Key**

Year	2011	2012	2013	2014	2015	2016	2017
Code	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

## Maximum Ratings @T<sub>A</sub> = 25°C unless otherwise specified

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V <sub>DSS</sub>	-20	V
Gate-Source Voltage			V <sub>GSS</sub>	±8	V
Continuous Drain Current	Steady State	T <sub>A</sub> = 25°C (Note 4)	I <sub>D</sub>	-1.14	A
		T <sub>A</sub> = 85°C (Note 4)		-0.83	
		T <sub>A</sub> = 25°C (Note 5)		-0.82	
Pulsed Drain Current (Note 6)			I <sub>DM</sub>	-4.0	A

## Thermal Characteristics @T<sub>A</sub> = 25°C unless otherwise specified

Characteristic		Symbol	Value	Unit
Power Dissipation	(Note 4)	P <sub>D</sub>	930	mW
	(Note 5)		490	mW
Thermal Resistance, Junction to Ambient	(Note 4)	R <sub>θJA</sub>	135	°C/W
	(Note 5)		256	°C/W
Operating and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

- Notes:
4. For a device surface mounted on 15mm x 15mm x 1.6mm FR4 PCB with high coverage of 2oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
  5. Same as note 4, except the device is mounted on minimum recommended pad layout.
  6. Device mounted on minimum recommended pad layout test board, 10μs pulse duty cycle = 1%.

## Thermal Characteristics

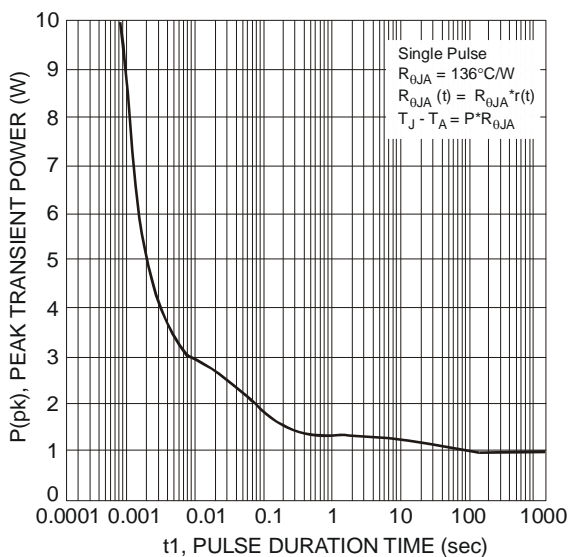


Fig. 1 Single Pulse Maximum Power Dissipation

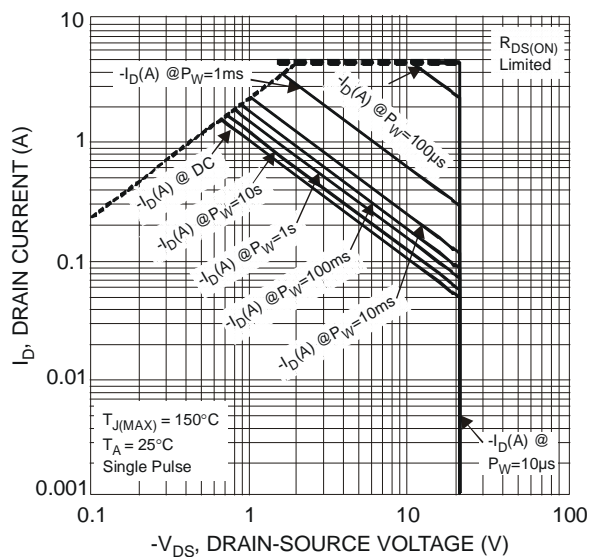


Fig. 2 SOA, Safe Operation Area

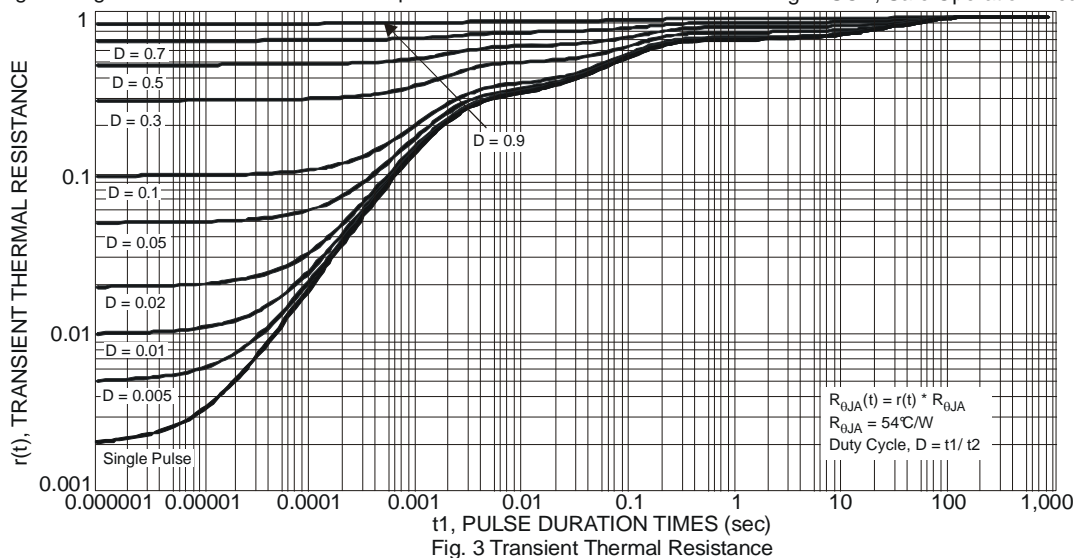


Fig. 3 Transient Thermal Resistance

**Electrical Characteristics** @  $T_A = 25^\circ\text{C}$  unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	-20	-	-	V	$V_{GS} = 0V, I_D = -250\mu A$
Zero Gate Voltage Drain Current $T_J = 25^\circ\text{C}$	$I_{DSS}$	-	-	-1	$\mu A$	$V_{DS} = -20V, V_{GS} = 0V$
Gate-Source Leakage	$I_{GSS}$	-	-	$\pm 10$	$\mu A$	$V_{GS} = \pm 8V, V_{DS} = 0V$
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	-0.45	-0.7	-1.2	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
Static Drain-Source On-Resistance	$R_{DS(on)}$	-	-	495	$m\Omega$	$V_{GS} = -4.5V, I_D = -800mA$
				730		$V_{GS} = -2.5V, I_D = -700mA$
				960		$V_{GS} = -1.8V, I_D = -100mA$
				1300		$V_{GS} = -1.5V, I_D = -100mA$
Forward Transfer Admittance	$ Y_{fs} $	50	-	-	mS	$V_{DS} = -3V, I_D = -300mA$
Diode Forward Voltage	$V_{SD}$	-	-	-1.2	V	$V_{GS} = 0V, I_S = -300mA$
<b>DYNAMIC CHARACTERISTICS</b>						
Input Capacitance	$C_{iss}$	-	76.5	-	pF	$V_{DS} = -10V, V_{GS} = 0V, f = 1.0MHz$
Output Capacitance	$C_{oss}$	-	13.7	-	pF	
Reverse Transfer Capacitance	$C_{rss}$	-	10.7	-	pF	
Gate Resistance	$R_g$	-	195	-	$\Omega$	$V_{DS} = 0V, V_{GS} = 0V, f = 1MHz$
Total Gate Charge (Note 8)	$Q_g$	-	1.5	-	nC	$V_{GS} = -8V, V_{DS} = -15V, I_D = -1A$
Total Gate Charge (Note 8)	$Q_g$	-	1.0	-	nC	$V_{GS} = -4.5V, V_{DS} = -15V, I_D = -1A$
Gate-Source Charge	$Q_{gs}$	-	0.2	-	nC	
Gate-Drain Charge	$Q_{gd}$	-	0.3	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	7.1	-	ns	$V_{DS} = -10V, -I_D = 1A, V_{GS} = -4.5V, R_G = 6\Omega$
Turn-On Rise Time	$t_r$	-	8.0	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	31.7	-	ns	
Turn-Off Fall Time	$t_f$	-	18.5	-	ns	

Notes: 7. Short duration pulse test used to minimize self-heating effect.  
 8. Guarantee by design.

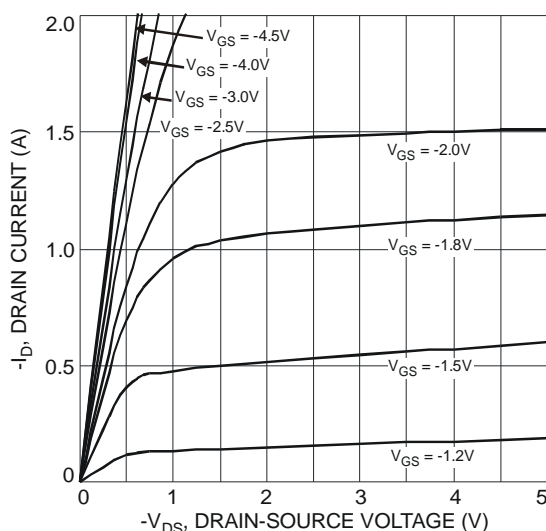


Fig. 4 Typical Output Characteristic

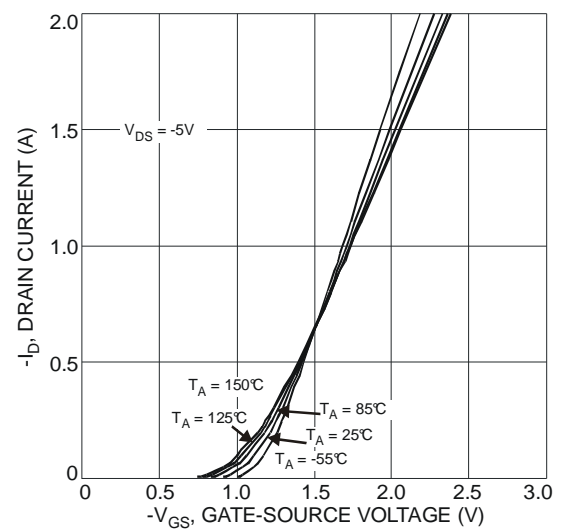


Fig. 5 Typical Transfer Characteristic

**DMP21D0UFD**

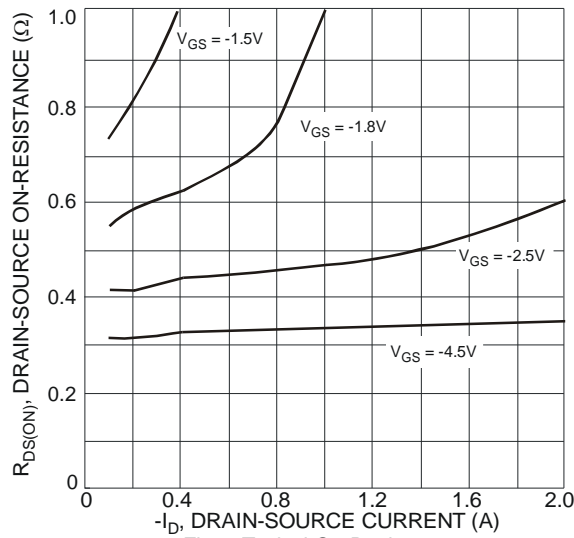


Fig. 6 Typical On-Resistance  
vs. Drain Current and Gate Voltage

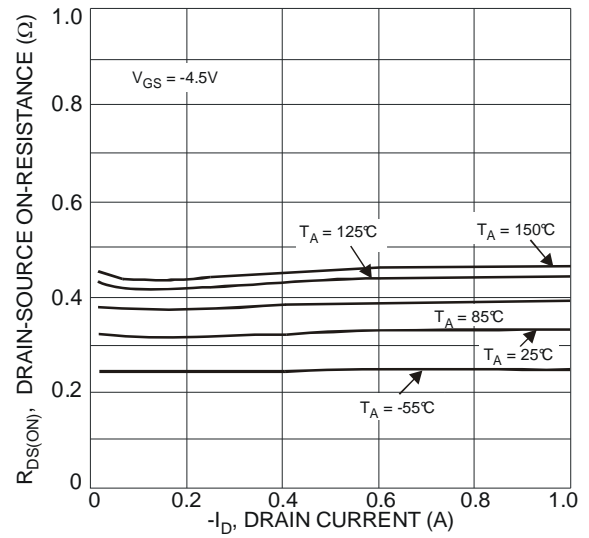


Fig. 7 Typical On-Resistance  
vs. Drain Current and Temperature

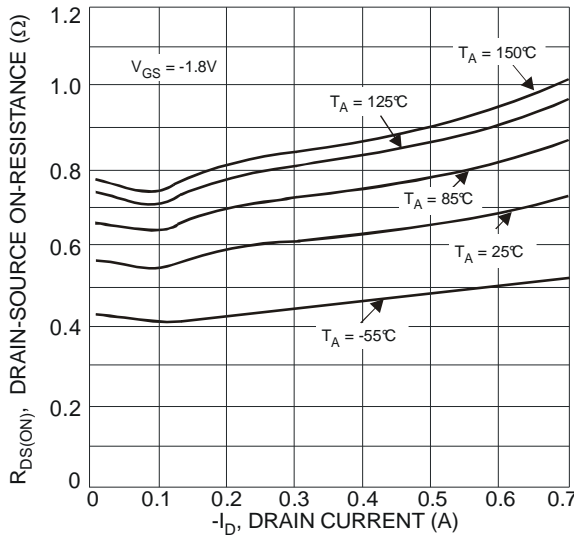


Fig. 8 Typical On-Resistance  
vs. Drain Current and Temperature

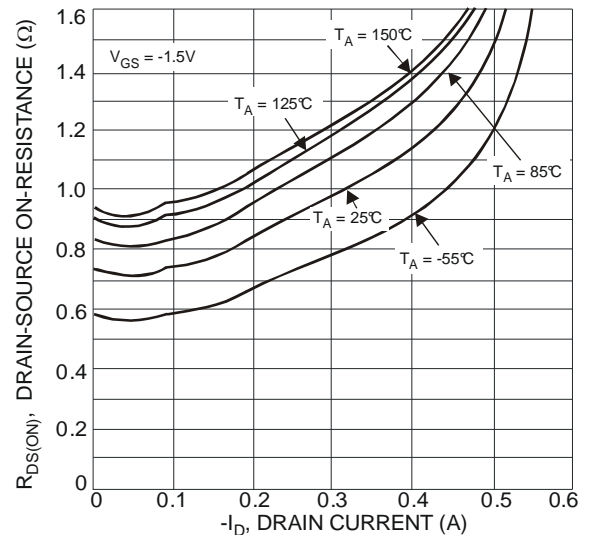


Fig. 9 Typical On-Resistance  
vs. Drain Current and Temperature

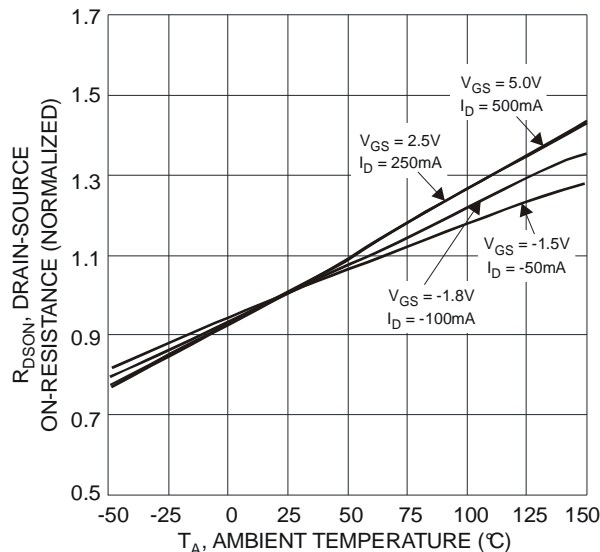


Fig. 10 On-Resistance Variation with Temperature

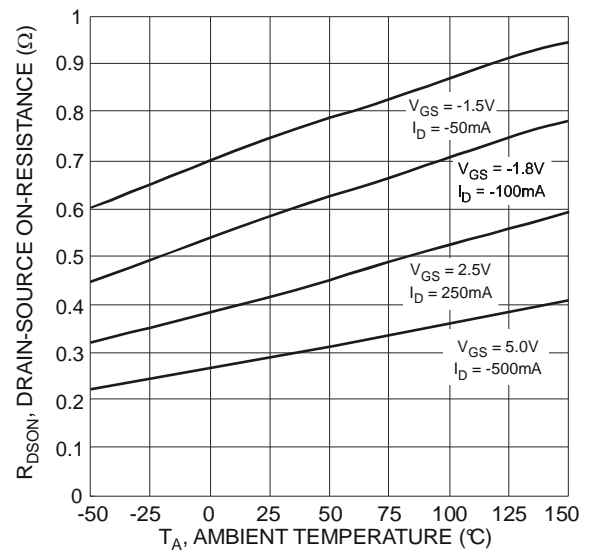


Fig. 11 On-Resistance Variation with Temperature

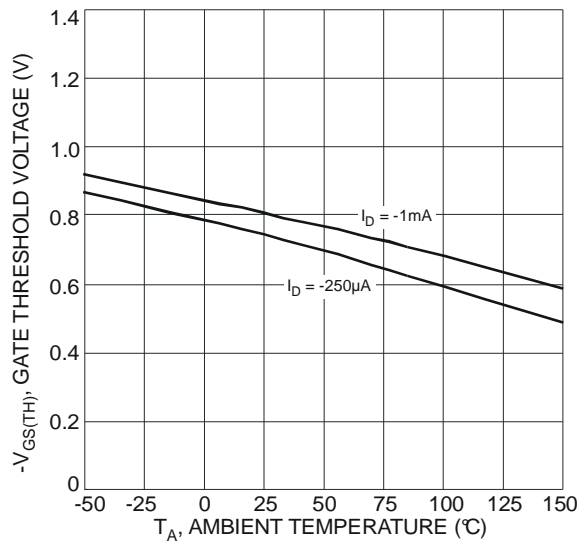


Fig. 12 Gate Threshold Variation vs. Ambient Temperature

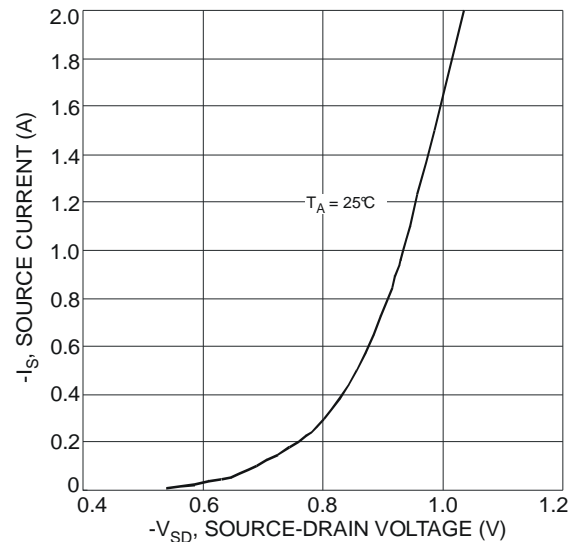


Fig. 13 Diode Forward Voltage vs. Current

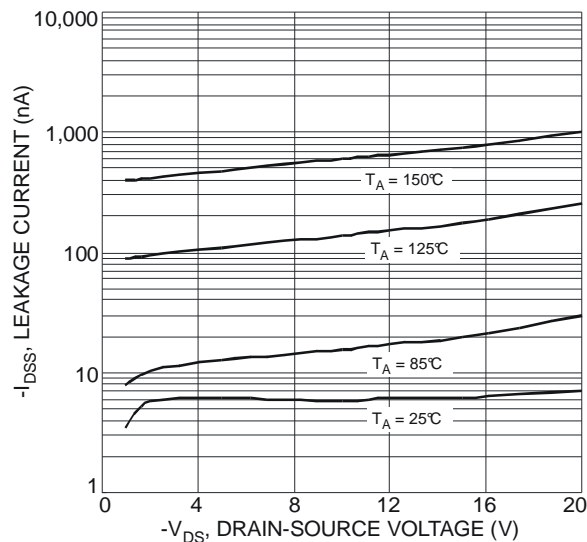


Fig. 14 Typical Leakage Current vs. Drain-Source Voltage

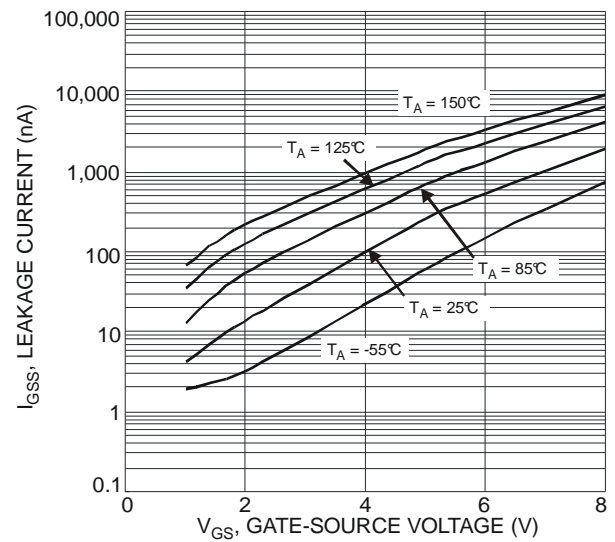


Fig. 15 Leakage Current vs. Gate-Source Voltage

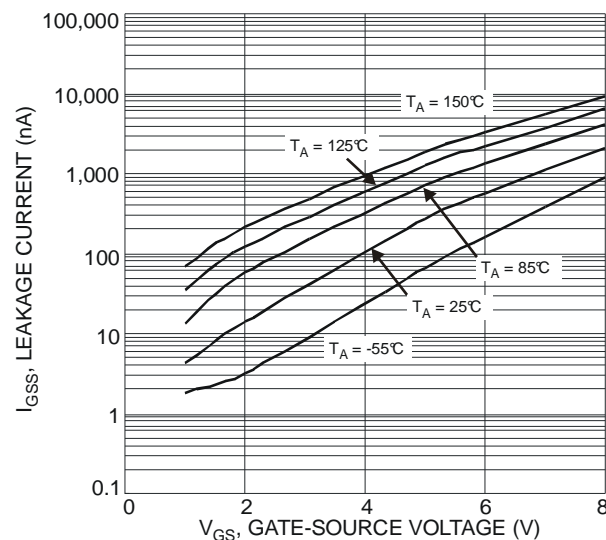


Fig. 16 Leakage Current vs. Gate-Source Voltage

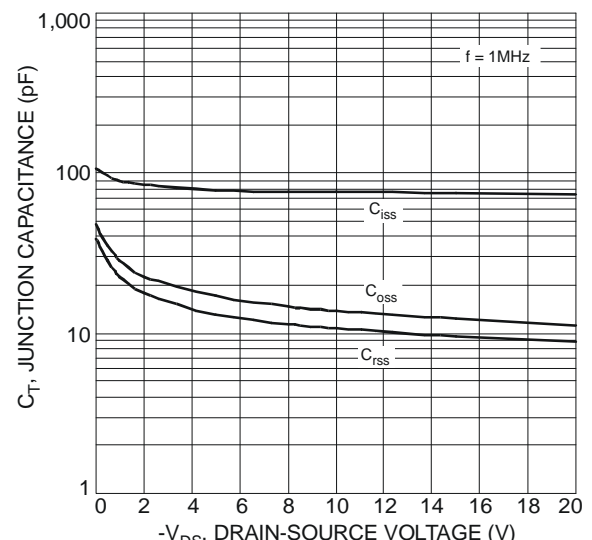


Fig. 17 Typical Junction Capacitance

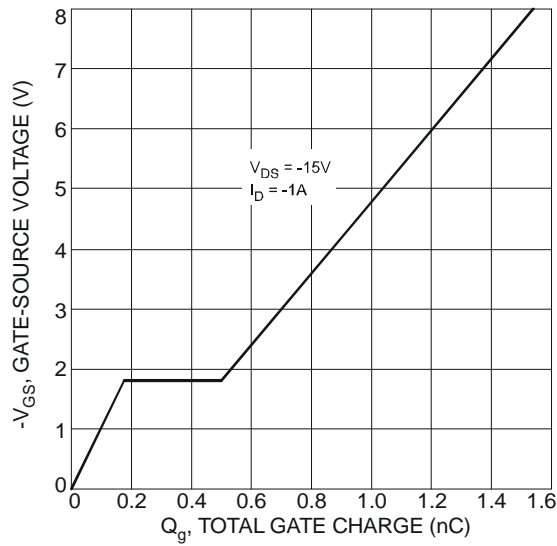
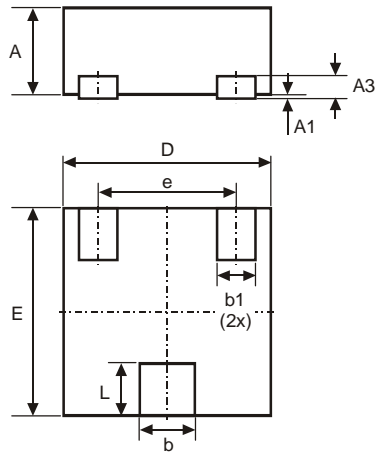


Fig. 18 Gate-Charge Characteristics

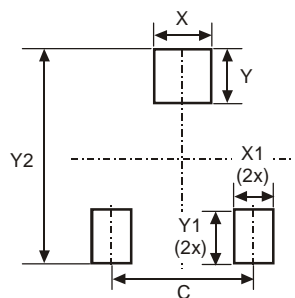
## Package Outline Dimensions



X1-DFN1212-3			
Dim	Min	Max	Typ
A	0.47	0.53	0.50
A1	0	0.05	0.02
A3	-	-	0.13
b	0.27	0.37	0.32
b1	0.17	0.27	0.22
D	1.15	1.25	1.20
E	1.15	1.25	1.20
e	-	-	0.80
L	0.25	0.35	0.30

All Dimensions in mm

## Suggested Pad Layout



Dimensions	Value (in mm)
C	0.80
X	0.42
X1	0.32
Y	0.50
Y1	0.50
Y2	1.50

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