# 2-Wire Bus Buffers with High Noise Margin

## FEATURES

- **Bidirectional Buffer Increases Fanout**
- **High Noise Margin with $V_{IL}$ = 0.3•$V_{CC}$**
- **Compatible with Non-Compliant $I^2C$ Devices That Drive a High $V_{OL}$**
- **Strong (LTC4313-1) and 2.5mA (LTC4313-2) Rise Time Accelerator Current**
- **Level Shift 1.5V, 1.8V, 2.5V, 3.3V and 5V Busses**
- Prevents SDA and SCL Corruption During Live Board Insertion and Removal from Backplane
- Stuck Bus Disconnect and Recovery
- Compatible with $I^2C$, $I^2C$ Fast Mode and SMBus
- ±4kV Human Body Model ESD Ruggedness
- High Impedance SDA, SCL Pins When Unpowered
- 8-Lead MSOP and 8-Lead (3mm × 3mm) DFN Packages

## APPLICATIONS

- Capacitance Buffers/Bus Extender
- Live Board Insertion
- Telecommunications Systems Including ATCA
- Level Translation
- PMBus
- Servers

## DESCRIPTION

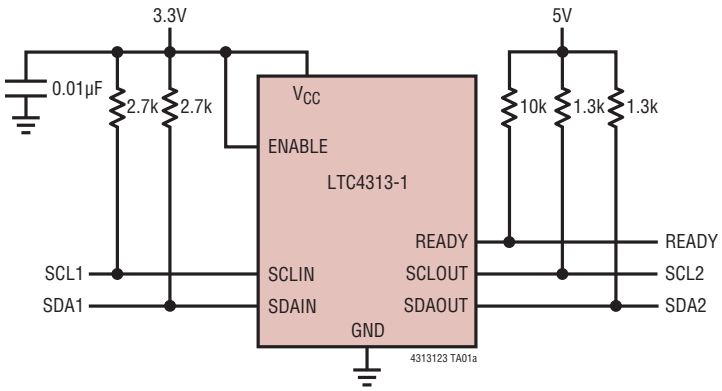
The LTC®4313 is a hot swappable 2-wire bus buffer that provides bidirectional buffering while maintaining a low offset voltage and high noise margin up to 0.3 • $V_{CC}$. The high noise margin allows the LTC4313 to be interoperable with devices that drive a high $V_{OL}$ (>0.4V) and allows multiple LTC4313s to be cascaded. The LTC4313-1 and LTC4313-2 support level translation between 3.3V and 5V busses. In addition to these voltages, the LTC4313-3 also supports level translation to 1.5V, 1.8V and 2.5V.

During insertion, the SDA and SCL lines are pre-charged to 1V to minimize bus disturbances. Connection is established between the input and output after ENABLE is asserted high and a stop bit or bus idle condition has been detected on the SDA and SCL pins.

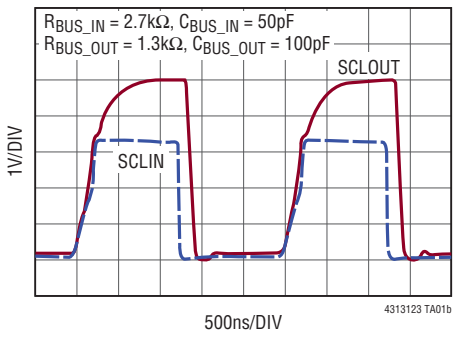
If both data and clock are not simultaneously high at least once in 45ms, the input is disconnected from the output. Up to 16 clock pulses are subsequently generated to free the stuck bus. Rise time accelerators (RTAs) provide pull-up currents on SDA and SCL rising edges to meet rise time specifications in heavily loaded systems. The RTAs are configured as slew limited switches in the LTC4313-1 and 2.5mA current sources in the LTC4313-2. The LTC4313-3 does not have RTAs.



## TYPICAL APPLICATION




**400kHz Operation**



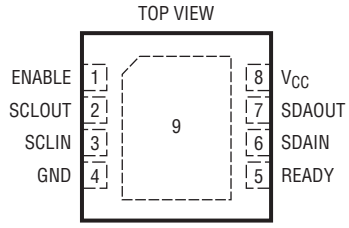
## ABSOLUTE MAXIMUM RATINGS

**(Notes 1, 2)**

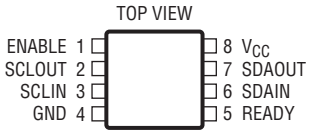
Supply Voltage $V_{CC}$ ..... –0.3V to 6V
Input Voltage ENABLE..... –0.3V to 6V
Input/Output Voltages SDAIN, SDAOUT,
SCLIN, SCLOUT ..... –0.3V to 6V
Output Voltage READY..... –0.3V to 6V
Output Sink Current READY.....50mA

Operating Ambient Temperature Range
LTC4313C ..... 0°C to 70°C
LTC4313I..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MS Package..... 300°C

## PIN CONFIGURATION




DD8 PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 39.7°C/W
EXPOSED PAD (PIN 9) PCB CONNECTION TO GND IS OPTIONAL




MS8 PACKAGE
8-LEAD PLASTIC MSOP
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 163°C/W

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC4313CDD-1#PBF | LTC4313CDD-1#TRPBF | LFYZ | 8-Lead (3mm × 3mm) Plastic DFN | 0°C to 70°C |
| LTC4313IDD-1#PBF | LTC4313IDD-1#TRPBF | LFYZ | 8-Lead (3mm × 3mm) Plastic DFN | –40°C to 85°C |
| LTC4313CMS8-1#PBF | LTC4313CMS8-1#TRPBF | LTFYZ | 8-Lead Plastic MSOP | 0°C to 70°C |
| LTC4313IMS8-1#PBF | LTC4313IMS8-1#TRPBF | LTFYZ | 8-Lead Plastic MSOP | –40°C to 85°C |
| LTC4313CDD-2#PBF | LTC4313CDD-2#TRPBF | LFZB | 8-Lead (3mm × 3mm) Plastic DFN | 0°C to 70°C |
| LTC4313IDD-2#PBF | LTC4313IDD-2#TRPBF | LFZB | 8-Lead (3mm × 3mm) Plastic DFN | –40°C to 85°C |
| LTC4313CMS8-2#PBF | LTC4313CMS8-2#TRPBF | LTFZC | 8-Lead Plastic MSOP | 0°C to 70°C |
| LTC4313IMS8-2#PBF | LTC4313IMS8-2#TRPBF | LTFZC | 8-Lead Plastic MSOP | –40°C to 85°C |
| LTC4313CDD-3#PBF | LTC4313CDD-3#TRPBF | LGDD | 8-Lead (3mm × 3mm) Plastic DFN | 0°C to 70°C |
| LTC4313IDD-3#PBF | LTC4313IDD-3#TRPBF | LGDD | 8-Lead (3mm × 3mm) Plastic DFN | –40°C to 85°C |
| LTC4313CMS8-3#PBF | LTC4313CMS8-3#TRPBF | LTGDF | 8-Lead Plastic MSOP | 0°C to 70°C |
| LTC4313IMS8-3#PBF | LTC4313IMS8-3#TRPBF | LTGDF | 8-Lead Plastic MSOP | –40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 3.3V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Power Supply/Start-Up** | | | | | | | |
| $V_{CC}$ | Input Supply Voltage | | ● | 2.9 | | 5.5 | V |
| $V_{DD,BUS}$ | 2-Wire Bus Supply Voltage | LTC4313-1, LTC4313-2 | ● | 2.9 | | 5.5 | V |
| | | LTC4313-3 | ● | 1.4 | | 5.5 | V |
| $I_{CC}$ | Input Supply Current | $V_{ENABLE}$ = $V_{CC}$ = 5.5V, $V_{SDAIN,SCLIN}$ = 0V (Note 3) | ● | 6 | 8.1 | 10 | mA |
| $I_{CC(DISABLED)}$ | Input Supply Current | $V_{ENABLE}$ = 0V, $V_{CC}$ = 5.5V, $V_{SDAIN,SCLIN}$ = 0V | ● | 2.5 | 3.5 | 4.5 | mA |
| $V_{TH\_UVLO}$ | $V_{CC}$ UVLO Threshold | $V_{CC}$ Rising | ● | 2.55 | 2.7 | 2.85 | V |
| $V_{CC\_UVLO(HYST)}$ | UVLO Threshold Hysteresis Voltage | | | | 200 | | mV |
| $V_{PRE}$ | Precharge Voltage | SDA, SCL Pins Open | ● | 0.8 | 1 | 1.2 | V |
| **Buffers** | | | | | | | |
| $V_{OS(SAT)}$ | Buffer Offset Voltage | $I_{OL}$ = 4mA, Driven $V_{SDA,SCL}$ = 50mV | ● | 100 | 190 | 280 | mV |
| | | $I_{OL}$ = 500µA, Driven $V_{SDA,SCL}$ = 50mV | ● | 15 | 60 | 120 | mV |
| $V_{OS}$ | Buffer Offset Voltage | $I_{OL}$ = 4mA, Driven $V_{SDA,SCL}$ = 200mV | ● | 50 | 120 | 180 | mV |
| | | $I_{OL}$ = 500µA, Driven $V_{SDA,SCL}$ = 200mV | ● | 15 | 60 | 115 | mV |
| $V_{IL,\ FALLING}$ | Buffer Input Logic Low Voltage | $V_{CC}$ = 2.9V, 3.3V, 5.5V | ● | 0.3•$V_{CC}$ | 0.33•$V_{CC}$ | 0.36•$V_{CC}$ | V |
| $\Delta V_{IL(HYST)}$ | $V_{IL}$ Hysteresis Voltage | | | | 50 | | mV |
| $I_{LEAK}$ | Input Leakage Current | SDA, SCL Pins = 5.5V, $V_{CC}$ = 5.5V, 0V | ● | | | ±10 | µA |
| $C_{IN}$ | Input Capacitance | SDA, SCL Pins (Note 4) | ● | | | 10 | pF |
| **Rise Time Accelerators (LTC4313-1 and LTC4313-2 Only)** | | | | | | | |
| $dV/dt_{(RTA)}$ | Minimum Slew Rate Requirement | SDA, SCL Pins, $V_{CC}$ = 5V | ● | 0.1 | 0.2 | 0.4 | V/µs |
| $V_{RTA(TH)}$ | Rise Time Accelerator DC Threshold Voltage | $V_{CC}$ = 5V | ● | 0.38•$V_{CC}$ | 0.41•$V_{CC}$ | 0.44•$V_{CC}$ | V |
| $\Delta V_{ACC}$ | Buffers Off to Accelerator On Voltage | SDA, SCL Pins, $V_{CC}$ = 5V | ● | 0.05•$V_{CC}$ | 0.07•$V_{CC}$ | | mV |
| $I_{RTA}$ | Rise Time Accelerator Pull-Up Current | SDA, SCL Pins, $V_{CC}$ = 5V (Note 5) LTC4313-1 | ● | 15 | 25 | 40 | mA |
| | | LTC4313-2 | ● | 1.5 | 2.5 | 3.5 | mA |
| **Enable/Control** | | | | | | | |
| $V_{EN(TH)}$ | ENABLE Threshold Voltage | | ● | 1 | 1.4 | 1.8 | V |
| $I_{LEAK}$ | ENABLE Leakage Current | $V_{ENABLE}$ = 5.5V | ● | | 0.1 | ±10 | µA |
| $V_{READY(OL)}$ | READY Output Low Voltage | $I_{READY}$ = 3mA, $V_{CC}$ = 5V | ● | | | 0.4 | V |
| $I_{READY(OH)}$ | READY Off Leakage Current | $V_{CC}$ = $V_{READY}$ = 5V | ● | | 0.1 | ±5 | µA |
| **Stuck Low Timeout Circuitry** | | | | | | | |
| $t_{TIMEOUT}$ | Bus Stuck Low Timer | | ● | 35 | 45 | 55 | ms |
| **I²C Interface Timing** | | | | | | | |
| $f_{SCL(MAX)}$ | I²C Frequency Max | | ● | 400 | | | kHz |
| $t_{PDHL}$ | SCL, SDA Fall Delay | $V_{CC}$ = $V_{DD,BUS}$ = 5V, $C_{BUS}$ = 100pF, $R_{BUS}$ = 10kΩ (Note 4) | | | 130 | 250 | ns |
| $t_f$ | SCL, SDA Fall Times | $V_{CC}$ = $V_{DD,BUS}$ = 5V, $C_{BUS}$ = 100pF, $R_{BUS}$ = 10kΩ (Note 4) | | 20 | | 300 | ns |
| $t_{IDLE}$ | Bus Idle Time | | ● | 55 | 95 | 175 | µs |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into pins are positive and all voltages are referenced to GND unless otherwise indicated.

**Note 3:** Test performed with SDA, SCL buffers active.

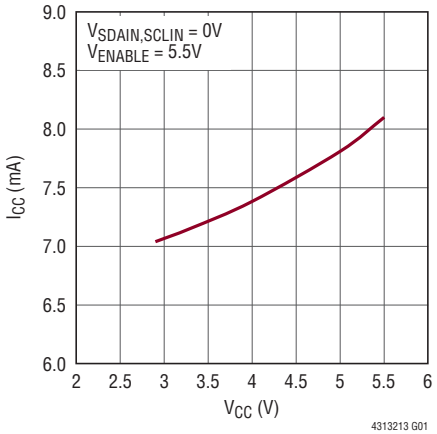
**Note 4:** Guaranteed by design and not tested.

**Note 5:** Measured in a special DC mode with $V_{SDA,SCL}$ = $V_{RTA(TH)}$ + 1V. The transient $I_{RTA}$ during rising edges for the LTC4313-1 will depend on the bus loading condition and the slew rate of the bus. The LTC4313-1's internal slew rate control circuitry limits the maximum bus rise rate to 75V/µs by controlling the transient $I_{RTA}$.

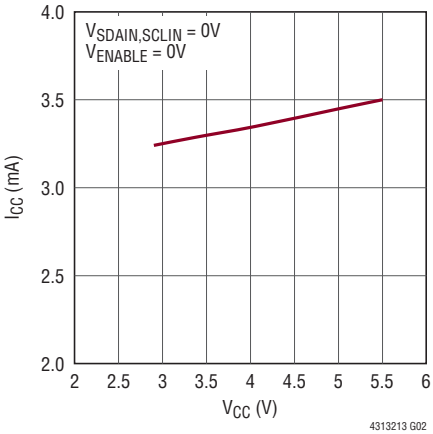
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, $V_{CC}$ = 3.3V unless otherwise noted.

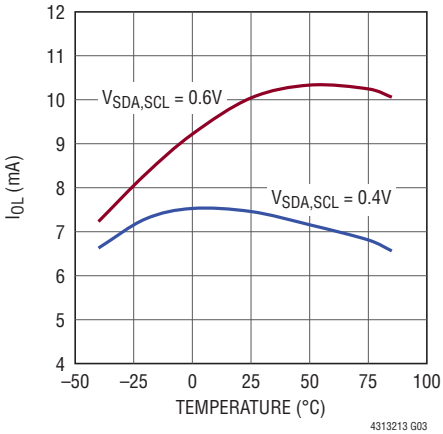
**$I_{CC}$ Enabled Current vs Supply Voltage**



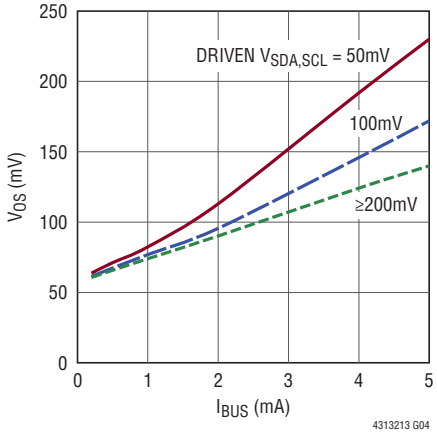

**$I_{CC}$ Disabled Current vs Supply Voltage**



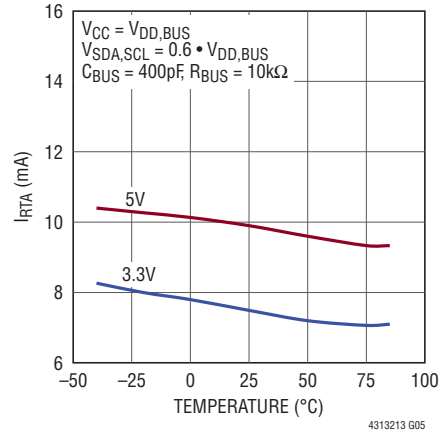

**Buffer DC $I_{OL}$ vs Temperature**



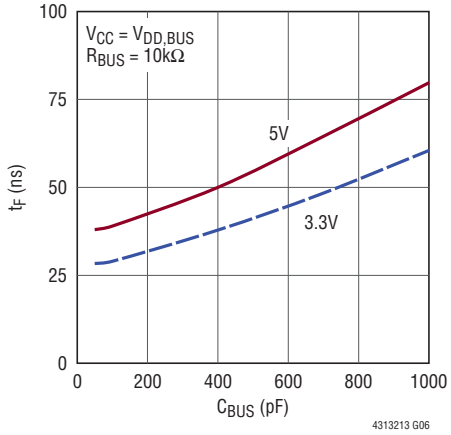

**$V_{OS}$ vs $I_{BUS}$ for Different Driven Voltage Levels**



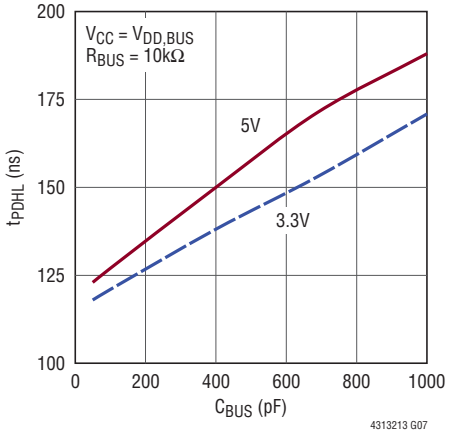

**LTC4313-1 $I_{RTA}$ vs Temperature**



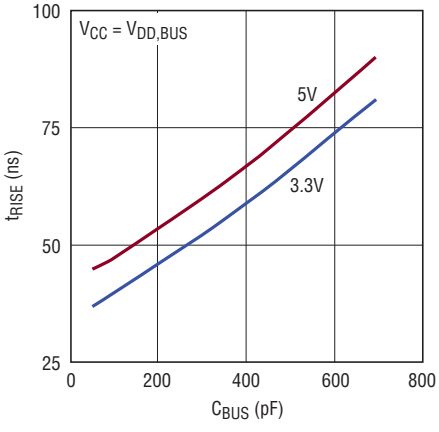

**$t_F$ (70% to 30%) vs Bus Capacitance**




**$t_{PDHL}$ (50% to 50%) vs Bus Capacitance**




**LTC4313-1 Bus Rise Time (40% to 70%) vs $C_{BUS}$**



## PIN FUNCTIONS

**ENABLE (Pin 1):** Connection Enable Input. When driven low, the ENABLE pin isolates SDAIN and SCLIN from SDAOUT and SCLOUT, asserts READY low, disables rise time accelerators and inhibits automatic clock and stop bit generation during a stuck low fault condition. When driven high, the ENABLE pin connects SDAIN and SCLIN to SDAOUT and SCLOUT after a stop bit or bus idle has been detected on both busses. Driving ENABLE high also enables automatic clock generation during a stuck low fault condition. During a stuck low fault condition, a rising edge on the ENABLE pin forces a connection between SDAIN and SDAOUT and SCLIN and SCLOUT. When using the LTC4313 in a Hot Swap™ application with staggered connector pins, connect a 10k resistor between ENABLE and GND to ensure correct functionality. Connect to $V_{CC}$ if unused.

**SCLOUT (Pin 2):** Serial Bus 2 Clock Input/Output. Connect this pin to the SCL bus segment where stuck low recovery is desired. Connect an external pull-up resistor or current source between this pin and the bus supply. The bus supply needs to be ≥ $V_{CC}$ for the LTC4313-1 and LTC4313-2, but not for the LTC4313-3. Refer to the Applications Information section for more details. Do not leave open.

**SCLIN (Pin 3):** Serial Bus 1 Clock Input/Output. Connect this pin to the SCL line on the upstream bus. Connect an external pull-up resistor or current source between this pin and the bus supply. The bus supply needs to be ≥ $V_{CC}$ for the LTC4313-1 and LTC4313-2, but not for the LTC4313-3. Refer to the Applications Information section for more details. Do not leave open.

**GND (Pin 4):** Device Ground.

**READY (Pin 5):** Connection Ready Status Output. This open drain N-channel MOSFET output pulls low when the input and output sides are disconnected. READY is pulled high when ENABLE is high and a connection has been established between the input and output. Connect a pull-up resistor, typically 10k from this pin to the bus pull-up supply. Leave open or tie to GND if unused.

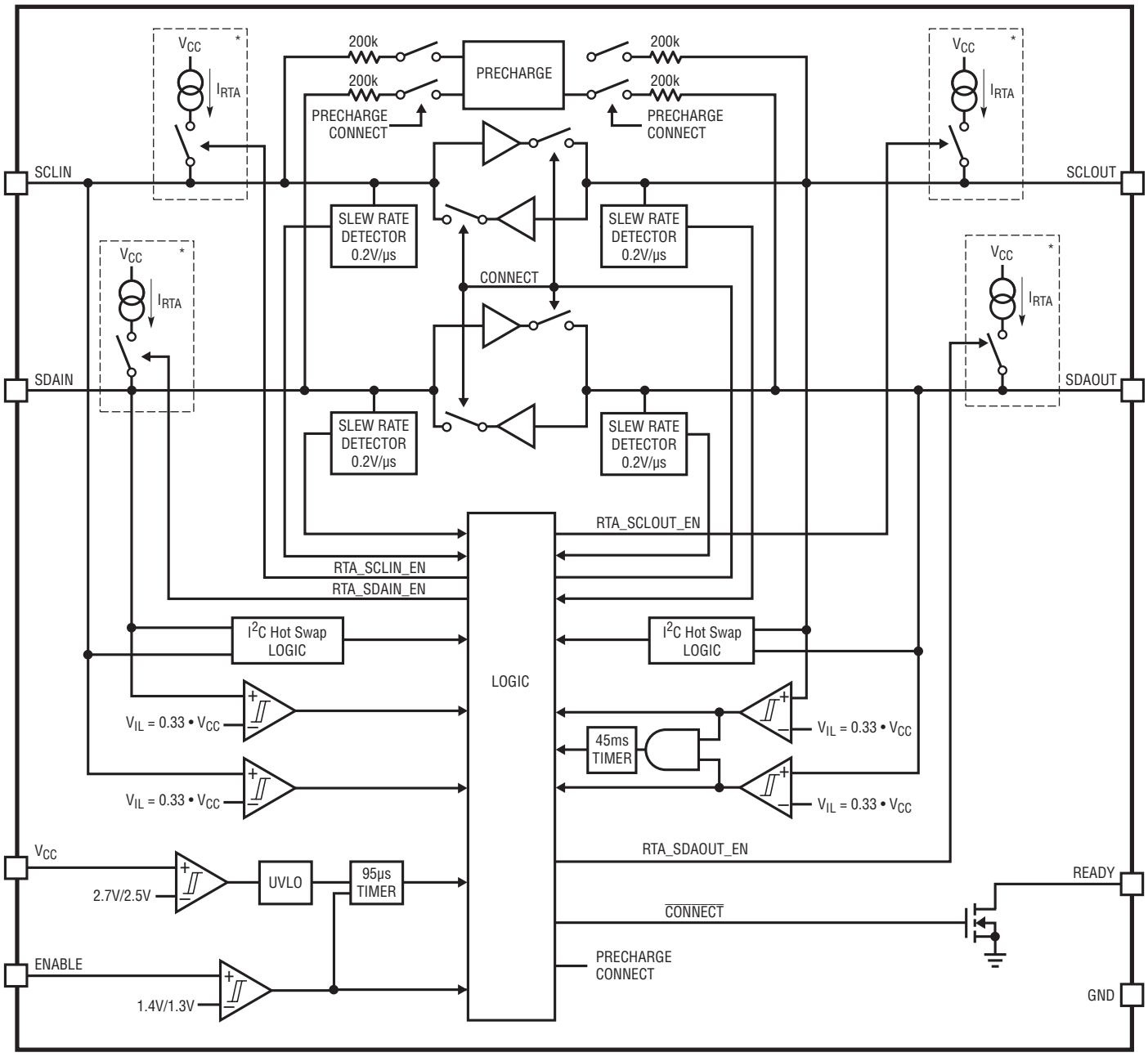
**SDAIN (Pin 6):** Serial Bus 1 Data Input/Output. Connect this pin to the SDA line on the upstream bus. Connect an external pull-up resistor or current source between this pin and the bus supply. The bus supply needs to be ≥ $V_{CC}$ for the LTC4313-1 and LTC4313-2, but not for the LTC4313-3. Refer to the Applications Information section for more details. Do not leave open.

**SDAOUT (Pin 7):** Serial Bus 2 Data Input/Output. Connect this pin to the SDA bus segment where stuck low recovery is desired. Connect an external pull-up resistor or current source between this pin and the bus supply. The bus supply needs to be ≥ $V_{CC}$ for the LTC4313-1 and LTC4313-2, but not for the LTC4313-3. Refer to the Applications Information section for more details. Do not leave open.

**$V_{CC}$ (Pin 8):** Power Supply Voltage. Power this pin from a supply between 2.9V and 5.5V. Bypass with at least 0.01µF to GND.

**Exposed Pad (Pin 9, DD8 Package Only):** Exposed pad may be left open or connected to device GND.

## BLOCK DIAGRAM




*INSIDE DASHED BOX APPLIES ONLY TO THE LTC4313-1 AND LTC4313-2.

## OPERATION

The LTC4313 is a high noise margin bus buffer which provides capacitance buffering for I$^2$C signals. Capacitance buffering is achieved by using back to back buffers on the clock and data channels which isolate the SDAIN and SCLIN capacitances from the SDAOUT and SCLOUT capacitances respectively. All SDA and SCL pins are fully bidirectional. The high noise margin allows the LTC4313 to operate with non-compliant I$^2$C devices that drive a high $V_{OL}$, permits a number of LTC4313s to be connected in series and improves the reliability of I$^2$C communications in large noisy systems. Rise time accelerator (RTA) pull-up currents ($I_{RTA}$) turn on during rising edges to reduce bus rise time for the LTC4313-1 and LTC4313-2. In a typical application the input and output busses are pulled up to $V_{CC}$ although this is not a requirement. If $V_{DD,BUS}$ is not tied to $V_{CC}$, $V_{DD,BUS}$ must be greater than $V_{CC}$ to prevent overdrive of the bus by the RTAs for the LTC4313-1 and LTC4313-2. See the Applications Information section for $V_{DD,BUS}$ requirements for the LTC4313-3.

When the LTC4313 first receives power on its $V_{CC}$ pin, it starts out in an undervoltage lockout mode (UVLO) until its $V_{CC}$ exceeds 2.7V. The buffers and RTAs are disabled and the LTC4313 ignores the logic state of its clock and data pins. During this time the precharge circuit forces a nominal voltage of 1V on the SDA and SCL pins through 200k resistors.

Once the LTC4313 exits UVLO and its ENABLE pin has been asserted high, it monitors the clock and data pins for a stop bit or a bus idle condition. When a combination of either condition is detected simultaneously on the input and output sides, the LTC4313 activates the connection between SDAIN and SDAOUT, and SCLIN and SCLOUT, respectively, asserts READY high and deactivates the precharge circuit. RTAs for the LTC4313-1 and LTC4313-2 are also enabled at this time.

When a SDA/SCL pin is driven below the $V_{IL}$ level, the buffers are turned on and the logic low level is propagated though the LTC4313 to the other side. A high occurs when all devices on the input and output sides release high. Once the bus voltages rise above the $V_{IL}$ level, the buffers are turned off. The RTAs are turned on at a slightly higher voltage. The RTAs accelerate the rising edges of the SDA/SCL inputs and outputs up to a voltage of 0.9•$V_{CC}$, provided that the busses on their own are rising at a minimum rate of 0.4V/µs as determined by the slew rate detectors. The RTAs are configured to operate in a strong slew limited switch mode in the LTC4313-1 and in the current source mode in the LTC4313-2.

The LTC4313 detects a bus stuck low (fault) condition when both clock and data busses are not simultaneously high at least once in 45ms. When a stuck bus occurs, the LTC4313 disconnects the input and output sides and after waiting at least 40µs, generates up to sixteen 5.5kHz clock pulses on the SCLOUT pin and a stop bit to attempt to free the stuck bus. Should the stuck bus release high during this period, automatic clock generation is terminated.

Once the stuck bus recovers, connection is re-established between the input and output after a stop bit or bus idle condition is detected. Toggling ENABLE after a fault condition has occurred forces a connection between the input and output. When powering into a stuck low condition, the input and output sides remain disconnected even after the LTC4313 has exited the UVLO mode as a stop bit or bus idle condition is not detected on the stuck busses. After the timeout period, a stuck low fault condition is detected and the behavior is as described previously.

## APPLICATIONS INFORMATION

The LTC4313 provides capacitance buffering, data and clock Hot Swap capability and level translation. The high noise margin of the LTC4313 permits interoperability with $I^2C$ devices that drive a high $V_{OL}$ permits series connection of multiple LTC4313s and improves $I^2C$ communication reliability. The LTC4313 isolates backplane and card capacitances and provides slew control of falling edges while level translating 3.3V and 5V busses. The LTC4313-1 and LTC4313-2 also provide pull-up currents to accelerate rising edges. These features are illustrated in the following subsections.

### Rise Time Accelerator (RTA) Pull-Up Current Strength (LTC4313-1 and LTC4313-2)

After an input and output connection has been established, the RTAs on both the input and output sides of the SDA and SCL busses are activated. During positive bus transitions of at least 0.4V/µs, the RTAs provide pull-up currents to reduce rise time. The RTAs allow users to choose larger bus pull-up resistors to reduce power consumption and improve logic low noise margins, design with bus capacitances outside of the $I^2C$ specification or to operate at a higher clock frequency. The LTC4313-1 regulates its RTA current to limit the bus rise rate to a maximum of 75V/µs. The current is therefore directly proportional to the bus capacitance. The LTC4313-1 RTA is capable of sourcing up to 40mA of current. Rise time acceleration for the LTC4313-2 is provided by a 2.5mA current source.

Figures 1 and 2 show the rising waveforms of heavily loaded SDAIN and SDAOUT busses for the LTC4313-1 and LTC4313-2 respectively. In both figures, during a rising edge, the buffers are active and the input and output sides are connected, until the bus voltages on both the input and output sides are greater than 0.3 • $V_{CC}$. When each individual bus voltage rises above 0.41 • $V_{CC}$, the RTA on that bus turns on. The effect of the acceleration strength is shown in the waveforms in Figures 1 and 2 for identical bus loads. The RTAs of the LTC4313-1 and LTC4313-2 supply 10mA and 2.5mA of pull-up current respectively for the bus conditions shown in Figures 1 and 2. For identical bus loads, the bus rises faster in Figure 1 compared to Figure 2 because of the higher $I_{RTA}$.

The RTAs are internally disabled during power-up and during a bus stuck low event. The RTAs when activated pull the bus up to 0.9•$V_{CC}$ on the input and output sides of the SDA and SCL pins. In order to prevent bus overdrive by the RTA, the bus supplies on the input and output sides

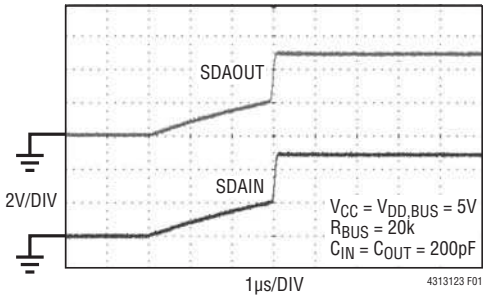



Figure 1. Bus Rising Edge for the LTC4313-1. $V_{CC} = V_{DD,BUS} = 5V$

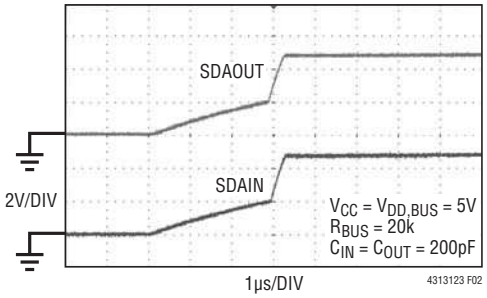



Figure 2. Bus Rising Edge for the LTC4313-2. $V_{CC} = V_{DD,BUS} = 5V$

## APPLICATIONS INFORMATION

of the LTC4313-1 and LTC4313-2 must be greater than or equal to 0.9•$V_{CC}$. An example is shown in Figure 3 where the input bus voltage is greater than $V_{CC}$. During a rising edge, the input bus rise rate will be accelerated by the RTA up to a voltage of 2.97V after which the bus rise rate will reduce to a value that is determined by the bus current and bus capacitance. The RTA turn-off voltage is less than the bus supply and the bus is not overdriven.

### Pull-Up Resistor Value Selection

To guarantee that the RTAs are activated during a rising edge, the bus must rise on its own with a positive slew rate of at least 0.4V/µs. To achieve this, choose a maximum $R_{BUS}$ using the formula:

$$R_{BUS} \le \frac{\left(V_{DD,BUS(MIN)} - V_{RTA(TH)}\right)}{0.4\frac{V}{\mu s} \bullet C_{BUS}} \quad (1)$$

$R_{BUS}$ is the pull-up resistor, $V_{DD,BUS(MIN)}$ is the minimum bus pull-up supply voltage, $V_{RTA(TH)}$ is the voltage at which the RTA turns on and $C_{BUS}$ is the equivalent bus capacitance. $R_{BUS}$ must also be large enough to guarantee that:

$$R_{BUS} \ge \frac{\left(V_{DD,BUS(MAX)} - 0.4V\right)}{4mA} \quad (2)$$

This criterion ensures that the maximum bus current is less than 4mA.

### Input to Output Offset Voltage

While propagating a logic low voltage on its SDA and SCL pins, the LTC4313 introduces a positive offset voltage between the input and output. When a logic low voltage ≥200mV is driven on any of the LTC4313's clock or data pins, the LTC4313 regulates the voltage on the opposite side to a slightly higher value. This is illustrated in Equation 3, which uses SDA as an example:

$$V_{SDAOUT} = V_{SDAIN} + 50mV + 15\Omega \bullet \frac{V_{DD,BUS}}{R_{BUS}} \quad (3)$$

In Equation 3, $V_{DD,BUS}$ is the output bus supply voltage and $R_{BUS}$ is the SDAOUT bus pull-up resistance.

For driven logic low voltages < 200mV Equation 3 does not apply as the saturation voltage of the open collector output transistor results in a higher offset. For a driven input logic low voltage below 220mV, the output is guaranteed to be below a $V_{OL}$ of 400mV for bus pull-up currents up to 4mA. See the Typical Performance Characteristics section for offset variation as a function of the driven logic low voltage and bus pull-up current.

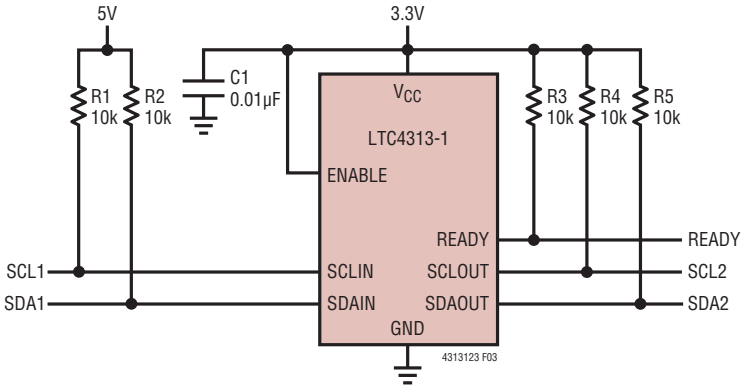



**Figure 3. Level Shift Application Where the SDAIN and SCLIN Bus Pull-Up Supply Voltage Is Higher Than the Supply Voltage of the LTC4313**

## APPLICATIONS INFORMATION

### Falling Edge Characteristics

The LTC4313 introduces a propagation delay on falling edges due to the finite response time and the finite current sink capability of the buffers. In addition the LTC4313 also slew limits the falling edge to an edge rate of 45V/µs (typ). The slew limited falling edge eliminates fast transitions on the busses and minimizes transmission line effects in systems. Refer to the Typical Performance Characteristics section for the propagation delay and fall times as a function of the bus capacitance.

### Stuck Bus Disconnect and Recovery

During an output bus stuck low condition (SCLOUT and SDAOUT have not been simultaneously high at least once in 45ms), the LTC4313 attempts to unstick the bus by first breaking the connection between the input and output. After 40µs the LTC4313 generates up to sixteen 5.5KHz clock pulses on the SCLOUT pin. Should the stuck bus release high during this period, clock generation is stopped and a stop bit is generated. This process is shown in Figure 4 for the case where SDAOUT starts out stuck low and then recovers. As seen from Figure 4, the LTC4313 pulls READY low and breaks the connection between the input and output sides, when a stuck low condition on SDA is detected. Clock pulses are then issued on SCLOUT to attempt to unstick the SDAOUT bus. When SDAOUT recovers, clock pulsing is stopped, a stop bit is generated on the output and READY is released high. When powering up into a stuck low condition, a connection is never made between the input and the output, as a stop bit or bus idle condition is never detected. After a timeout period of 45ms, the behavior is the same as described previously.

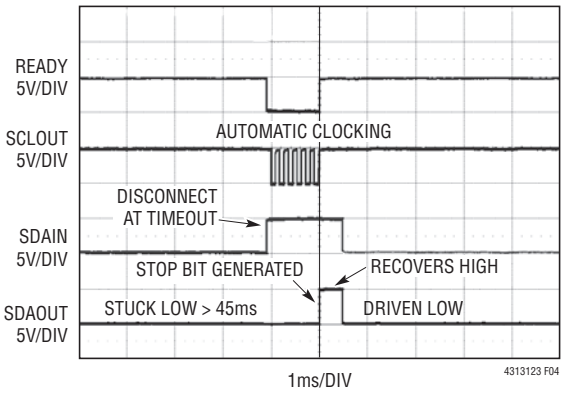



**Figure 4. Bus Waveforms During SDAOUT Stuck Low and Recovery Event**

## APPLICATIONS INFORMATION

### Live Insertion and Capacitance Buffering Application

Figure 5 illustrates an application of the LTC4313 that takes advantage of the LTC4313's Hot Swap, capacitance buffering and precharge features. If the I/O cards were plugged directly into the backplane without LTC4313 buffers, all of the backplane and card capacitances would directly add together, making rise time requirements difficult to meet. Placing an LTC4313 on the edge of each card isolates the card capacitance from the backplane. For a given I/O card, the LTC4313 drives the capacitance of everything on the card and the devices on backplane must drive only the small capacitance of the LTC4313 which is < 10pF.

In Figure 5 a staggered connector is used to connect the LTC4313 to the backplane. $V_{CC}$ and GND are the longest pins to ensure that the LTC4313 is powered and forcing a 1V precharge voltage on the medium length SDA and SCL pins before they contact the backplane. The 1V precharge voltage is applied to the SDA and SCL pins through 200k resistors. Since cards are being plugged into a live backplane whose SDA and SCL busses could be at any voltage between 0 and $V_{CC}$, precharging the LTC4313's SDA and SCL pins to 1V minimizes disturbances to the backplane bus when cards are being plugged in. The low (<10pF) input capacitance of the LTC4313 also contributes to minimizing bus disturbance as cards are being plugged in. With ENABLE being the shortest pin and also pulled to GND by a resistor, the staggered approach provides additional time for transients associated with live insertion to settle before the LTC4313 can be enabled. A 10k or lower pull-down resistor from ENABLE to GND is recommended.

If a connector is used where all pins are of equal length, the benefit of the precharge circuit is lost. Also, the ENABLE signal to the LTC4313 must be held low until all the transients associated with card insertion into a live system die out.

### Level Translating to Voltages < 2.9V (LTC4313-3 Only)

The LTC4313-3 can be used for level translation to bus voltages below 2.9V. Since the maximum buffer turn-on and turn-off voltages are 0.36•$V_{CC}$, the minimum bus supply voltage is determined by the following equation,

$$V_{DD,BUS(MIN)} \geq \frac{0.36 \bullet V_{CC}}{0.7} \quad (4)$$

in order to meet the $V_{IH} = 0.7 \bullet V_{DD,BUS}$ requirement and not impact the high side noise margin. Users willing to live with a lower logic high noise margin can level translate down to 1.4V. An example of voltage level translation from 3.3V to 1.8V is illustrated in Figure 6, where a 3.3V input voltage bus is translated to a 1.8V output voltage bus. Tying $V_{CC}$ to 3.3V satisfies Equation 4. A similar voltage translation can also be performed going from a 3.3V bus supply on the output side to a 1.8V input if the $V_{CC}$ pin of the LTC4313-3 is tied to the 3.3V output supply.

## APPLICATIONS INFORMATION

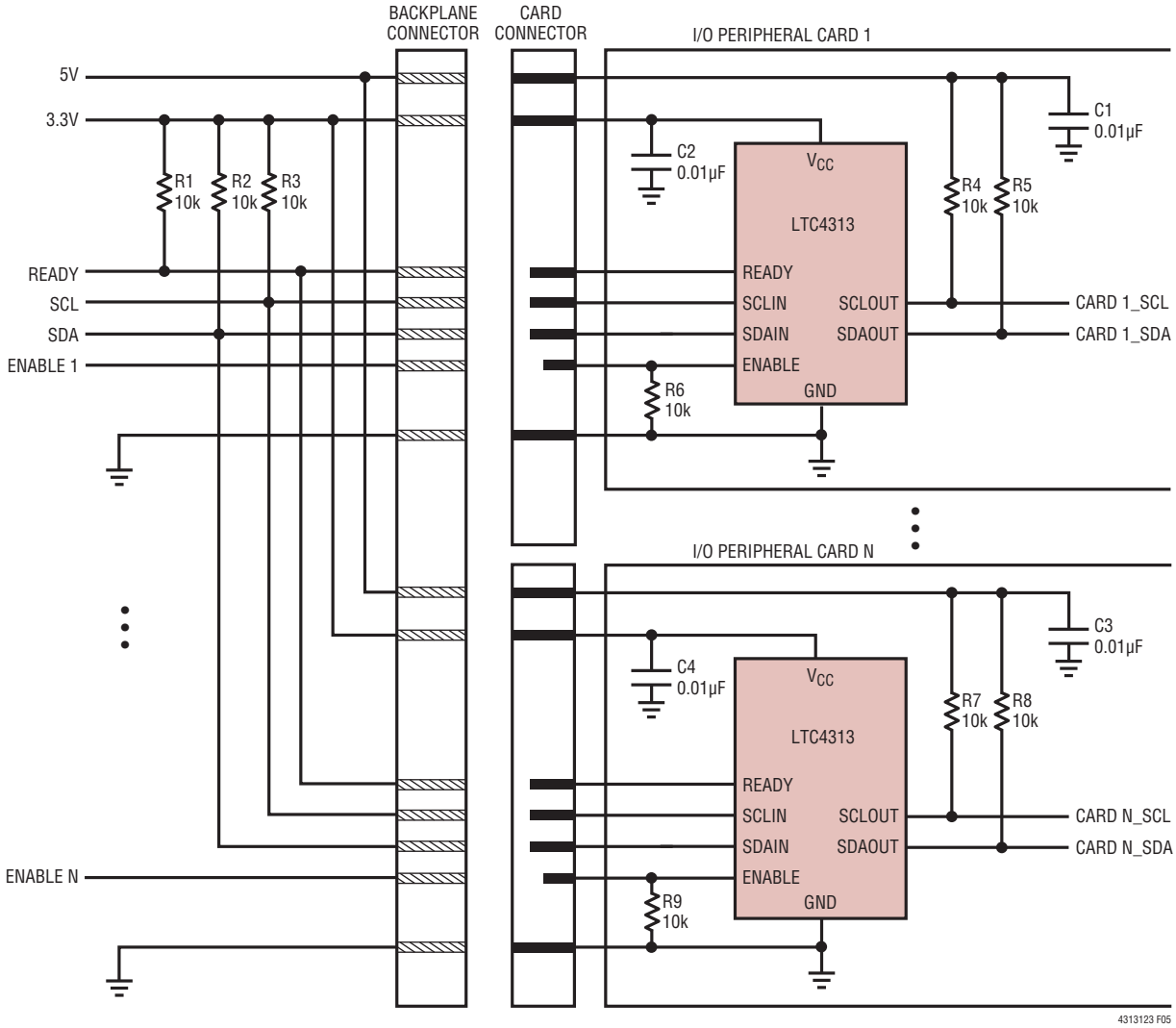



**Figure 5. LTC4313 in an I²C Hot Swap Application with a Staggered Connector**

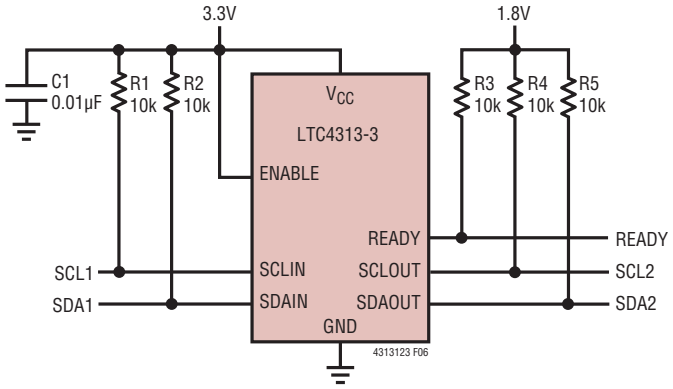



**Figure 6. Voltage Level Translation from 3.3V to 1.8V Using the LTC4313-3**

## APPLICATIONS INFORMATION

### Telecommunications Systems

The LTC4313 has several features that make it an excellent choice for use in telecommunication systems such as ATCA. Referring to Figures 7 and 8, buffers are used on the edges of the field replaceable units (FRU) and shelf managers to shield devices on these cards from the large backplane capacitance. The input capacitance of the LTC4313 is less than the 10pF maximum specification for buffers used in bussed ATCA applications. The LTC4313 buffers can drive capacitances >1nF, which is greater than the maximum backplane capacitance of 690pF in bussed ATCA systems. The precharge feature, low input capacitance and high impedance of the SDA and SCL pins of the LTC4313 when it is unpowered, minimize disturbances to the bus when cards are being hot swapped. In Figure 7, the RTA of the LTC4313-2 on the shelf manager supplies sufficient pull-up current, allowing the 1µs rise time requirement to be met on the heavily loaded backplane for loads well beyond the 690pF maximum specification. The 0.33 • $V_{CC}$ turn-off voltage of the LTC4313's buffers provides a large logic low noise margin in these systems. In the bussed ATCA application shown in Figure 7, the LTC4313s located on the shelf managers #1 and #2 and on the FRUs, drive the large backplane capacitance while the microcontrollers on the shelf managers and the $I^2C$ slave devices on the FRUs drive the small input capacitance of the LTC4313-3.

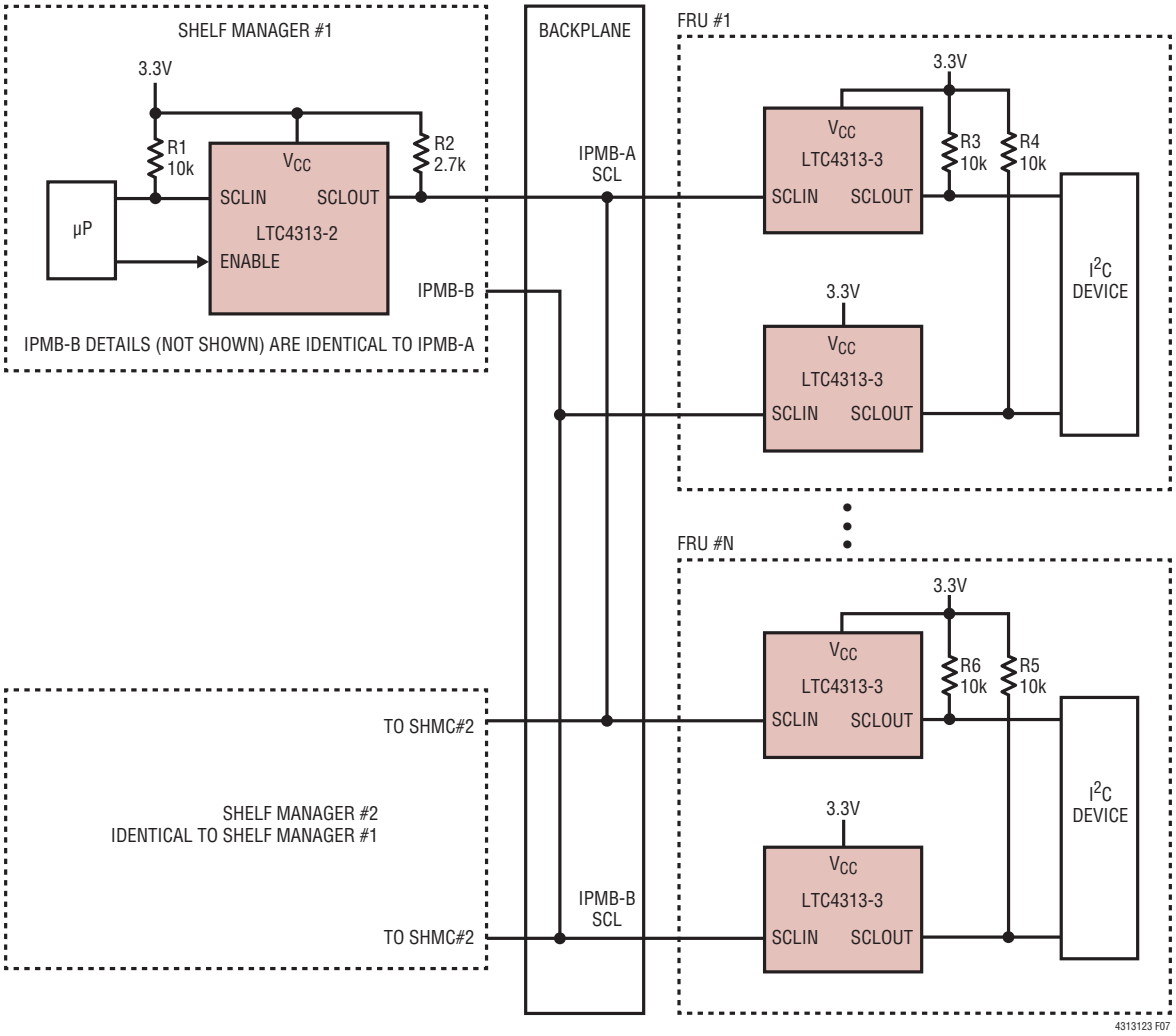



**Figure 7. LTC4313s Used in a Bussed ATCA Application. Only the Clock Path is Shown for Simplicity**

## APPLICATIONS INFORMATION

The LTC4313-2 on only one of the shelf managers is enabled at any given time. The hot insertion logic on the LTC4313-3 allows the FRUs to be plugged or unplugged from a live backplane. The features mentioned previously provide noise immunity and allow timing specifications to be met for a wide range of backplane loading conditions.

In the 6 × 4 radial configuration shown in Figure 8, the LTC4314s on the shelf managers and the LTC4313-2s on the FRUs drive the large backplane capacitance while the $I^2C$ slave devices on the FRUs only drive the small input capacitance of the LTC4313-2s. The LTC4314s on only one of the shelf managers are enabled at a given time. All the benefits provided by the LTC4313-2 in Figure 7 apply to Figure 8 as well.

### Cascading and Interoperability with Other LTC Buffers and Non-Compliant $I^2C$ Devices

Multiple LTC4313s can be cascaded or the LTC4313 can be cascaded with other LTC bus buffers. Cascades often exist in large $I^2C$ systems, where multiple I/O cards having bus buffers connect to a common backplane bus. Two issues need to be considered when using such cascades – the additive nature of the buffer logic low offset voltages and the impact of the RTA-buffer interaction on the noise margin.

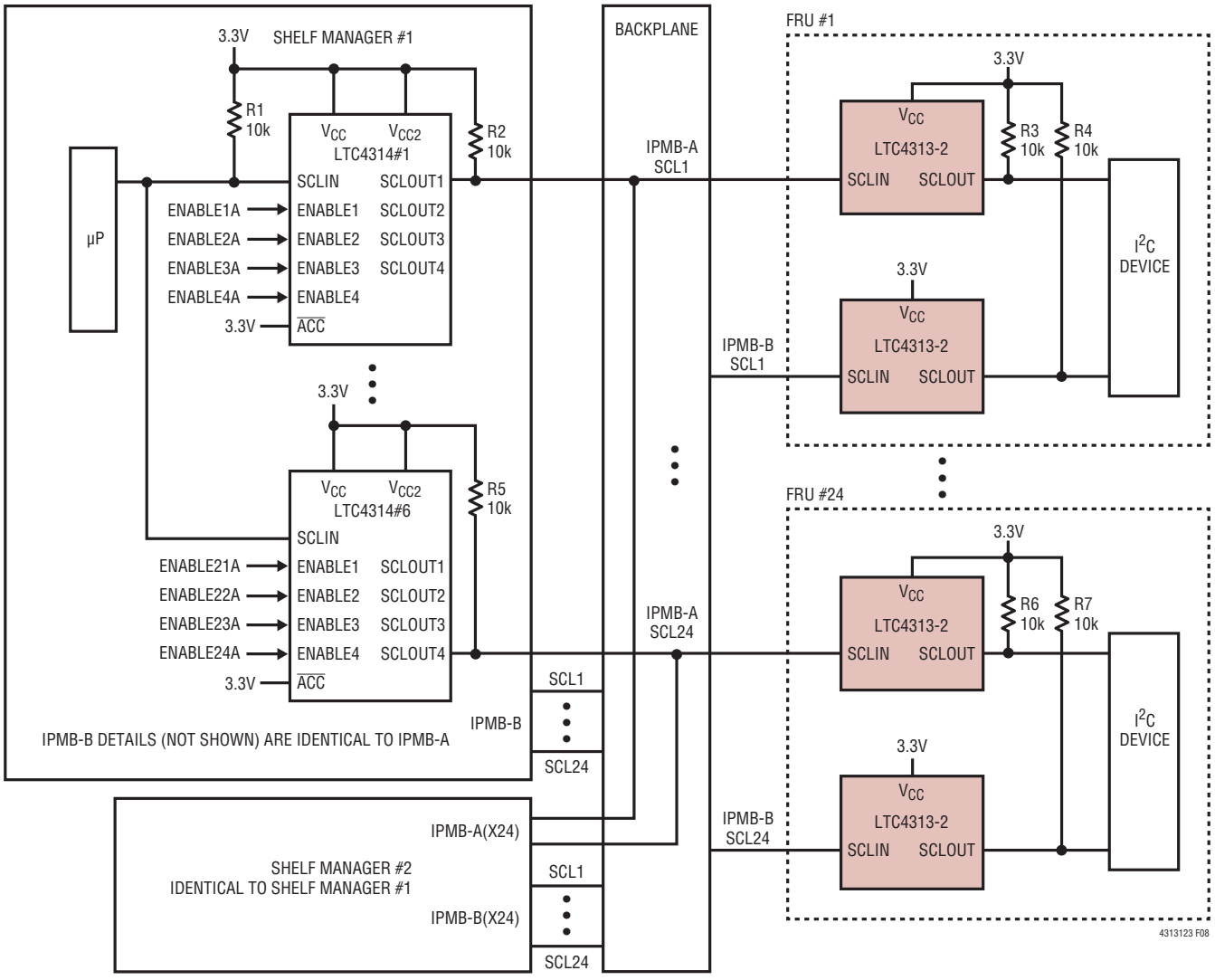



**Figure 8. LTC4313-2 Used in a Radially Connected Telecommunication System in a 6 × 4 Arrangement. Only the Clock Path is Shown for Simplicity. The Data Pathway is Identical**

## APPLICATIONS INFORMATION

First, when two or more buffers are connected in a cascade configuration, if the sum of the offsets across the cascade (refer to Equation 3 and the data sheets of the corresponding buffers) plus the worst-case driven logic low voltage exceeds the minimum buffer turn-off voltage, signals will not be propagated across the cascade. The maximum driven logic low voltage must be set accordingly, for correct operation in such cascades.

Second, noise margin is affected by cascading the LTC4313 with buffers whose RTA turn-on voltage is lower than the LTC4313 buffer turn-off voltage. The $V_{IL}$ for the LTC4313 is set to 0.3 • $V_{CC}$ to achieve high noise margin provided that the LTC4313 buffers do not contend with RTAs of other products. To maximize logic low noise margin, disable the RTAs of the other LTC buffers if possible and use the RTAs of the LTC4313 in cascading applications. To permit interoperability with other LTC buffers whose RTAs cannot be disabled, the LTC4313 senses the RTA current and turns off its buffers below 0.3 • $V_{CC}$. This eliminates contention between the LTC4313 buffers and other RTAs, making the SDA/SCL waveforms monotonic.

Figures 9 shows the LTC4313-1 operating on a bus shared with LTC4300A and LTC4307 buffers. The corresponding SCL waveforms are shown in Figure 10. The RTAs on the LTC4300A and the LTC4307 cannot be disabled. The backplane in Figure 9 has five I/O cards connected to it. Each I/O card has a LTC bus buffer on its outside edge for SDA/SCL Hot Swap onto the backplane. In this example, there are three LTC4300As, one LTC4307 and one LTC4313-1. The SCL1 bus is driven by an $I^2C$ master (master not shown). When the SCL2 voltage crosses 0.6V and 0.8V, the RTAs on the LTC4300A and LTC4307 turn on respectively and source current into SCL2. The LTC4313-1 detects this and turns off its buffers, releasing SCL1 and SCL2 high. Contention between the LTC4313-1 buffers and the LTC4300A and LTC4307 RTAs is prevented and the SCL1, SCL2 and SCL3 waveforms in Figure 10 are monotonic. The logic low noise margin is reduced because the LTC4313-1 buffers turn off when the SCL1 voltage is approximately 0.6V.

Generally, noise margin will be reduced if other RTAs turn on at a voltage less than 0.3•$V_{CC}$. The reduction in noise margin is a function of the number of LTC4313s and the number and turn-on voltage of other RTAs, whose current must be sunk by the LTC4313 buffers. The same arguments apply for non-LTC buffer products whose RTA turn-on voltage is less than 0.3•$V_{CC}$.

Interoperability is improved by reducing the interaction time between the LTC4313 buffers and other RTAs by reducing R1 and $C_{B1}$. The following guidelines are recommended for single supply systems,

a. For 5V systems choose R1 < 20kΩ and $C_{B1}$ < 1nF. There are no other constraints.

b. For 3.3V systems, refer to Figures 11 and 12 for operation with LTC4300As and LTC4307s. In the figures,

$$M = \frac{\text{Number of LTC4300As or LTC4307s}}{\text{Number of LTC4313s}}$$

R1 and $C_{B1}$ must be chosen to be below the curves for a specific value of M. For M greater than the values shown in the figures, non-idealities do not result. R1 <20kΩ and $C_{B1}$ <1nF are still recommended.

The LTC4313 is interoperable with non-compliant $I^2C$ devices that drive a high $V_{OL}$ > 0.4V. Figure 13 shows the LTC4313-1 in an application where a microcontroller communicates through the LTC4313-1 with a non-compliant $I^2C$ device that drives a $V_{OL}$ of 0.6V. The LTC4313 buffers are active up to a bus voltage of 0.3•$V_{CC}$ which is 1.089V in this case, yielding a noise margin of 0.489V.

### Repeater Application

Multiple LTC4313s can be cascaded in a repeater application where a large 2-wire system is broken into smaller sections as shown in Figure 14. The high noise margin and low offset of the LTC4313 allows multiple devices to be cascaded while still providing good system level noise margin. In the repeater circuit shown in Figure 14 if SCL1/SDA1 is driven externally to 200mV, SCL2/SDA2 is regulated to ~440mV worst-case by the cascade of LTC4313-1s. The buffer turn-off voltage is 1.089V, yielding a minimum logic low noise margin of ~650mV. In Figure 14, use of the RTAs combined with an increased level of buffering reduces transition times and permits operation at a higher frequency.

## APPLICATIONS INFORMATION

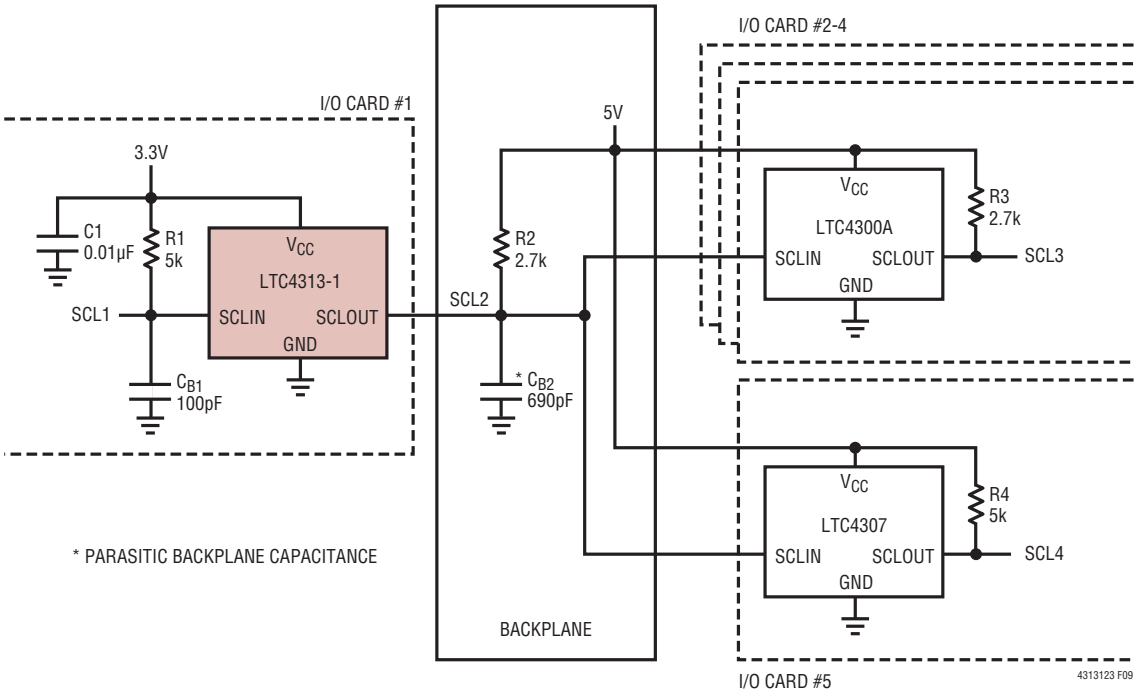



**Figure 9. The LTC4313-1 Operating in a Cascade with Other LTC Buffers with Active RTAs. Only the Clock Pathway is Shown for Simplicity**

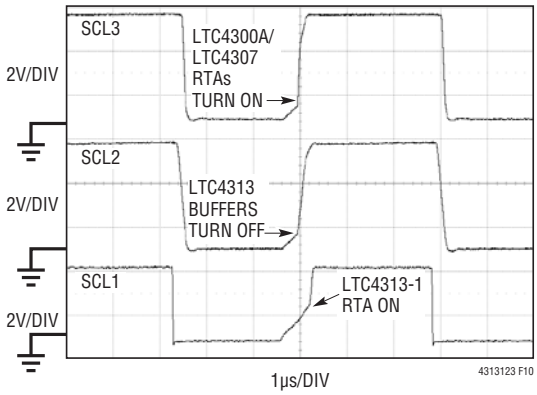



**Figure 10. Corresponding SCL Switching Waveforms. No Glitches Are Seen**

## APPLICATIONS INFORMATION

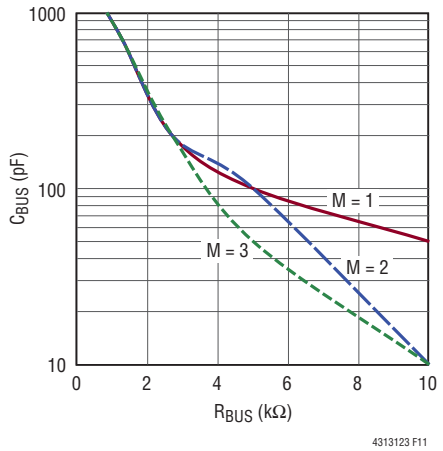



Figure 11. Recommended Maximum R1 and $C_{B1}$ Values for the LTC4313 Operating with Multiple LTC4300As in a 3.3V System

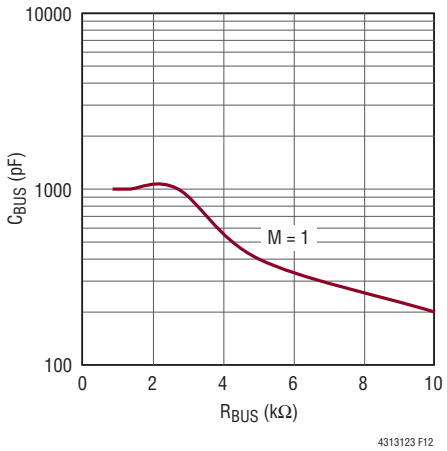



Figure 12. Recommended Maximum R1 and $C_{B1}$ Values for the LTC4313 Operating with Multiple LTC4307s in a 3.3V System

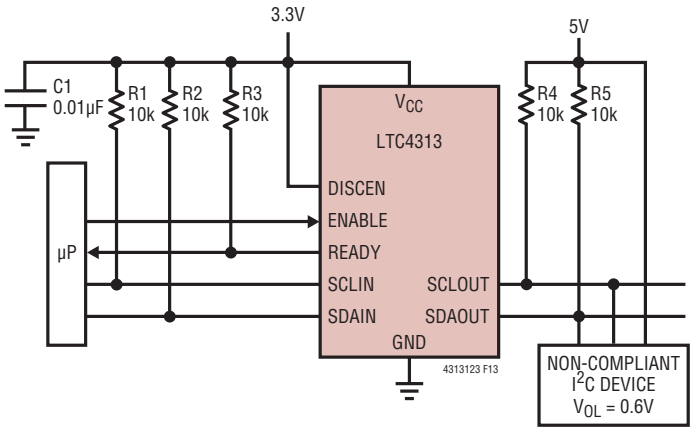



Figure 13. Communication with a Non-Compliant $I^2C$ Device Using the LTC4313

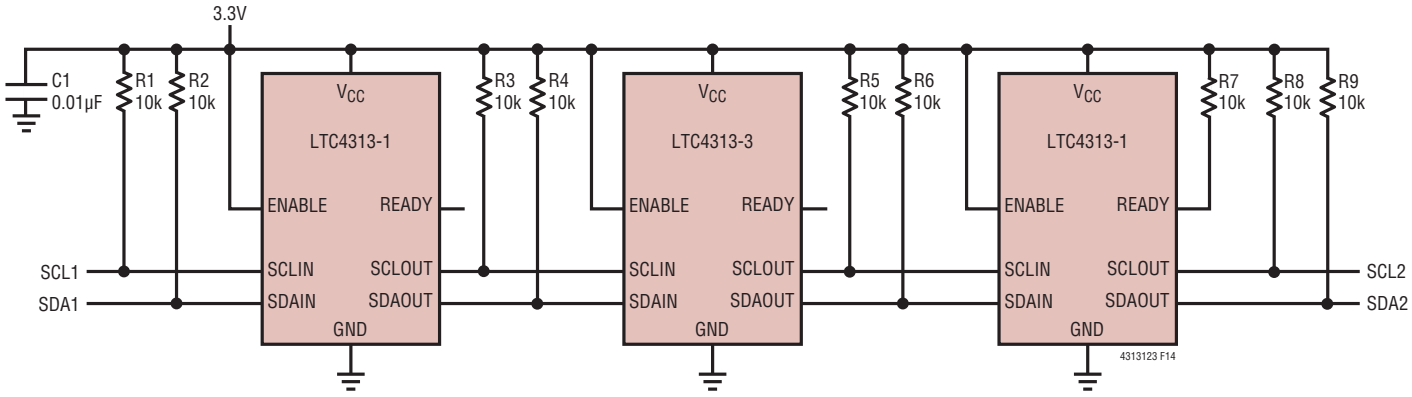
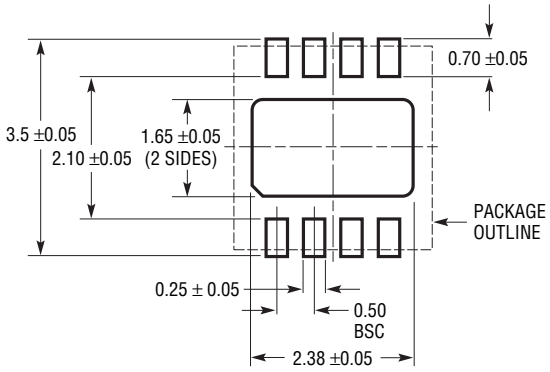



Figure 14. LTC4313-1s in a Repeater Application

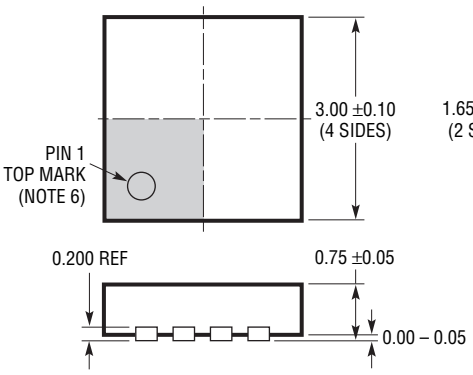
## PACKAGE DESCRIPTION

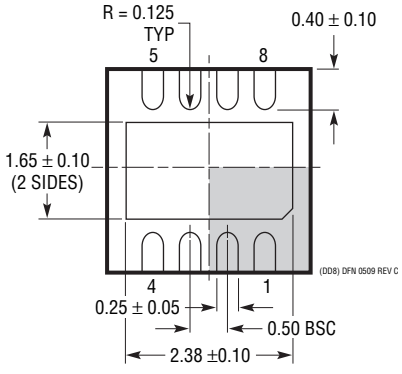
**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

**DD8 Package**
**8-Lead Plastic DFN (3mm × 3mm)**
(Reference LTC DWG # 05-08-1698 Rev C)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



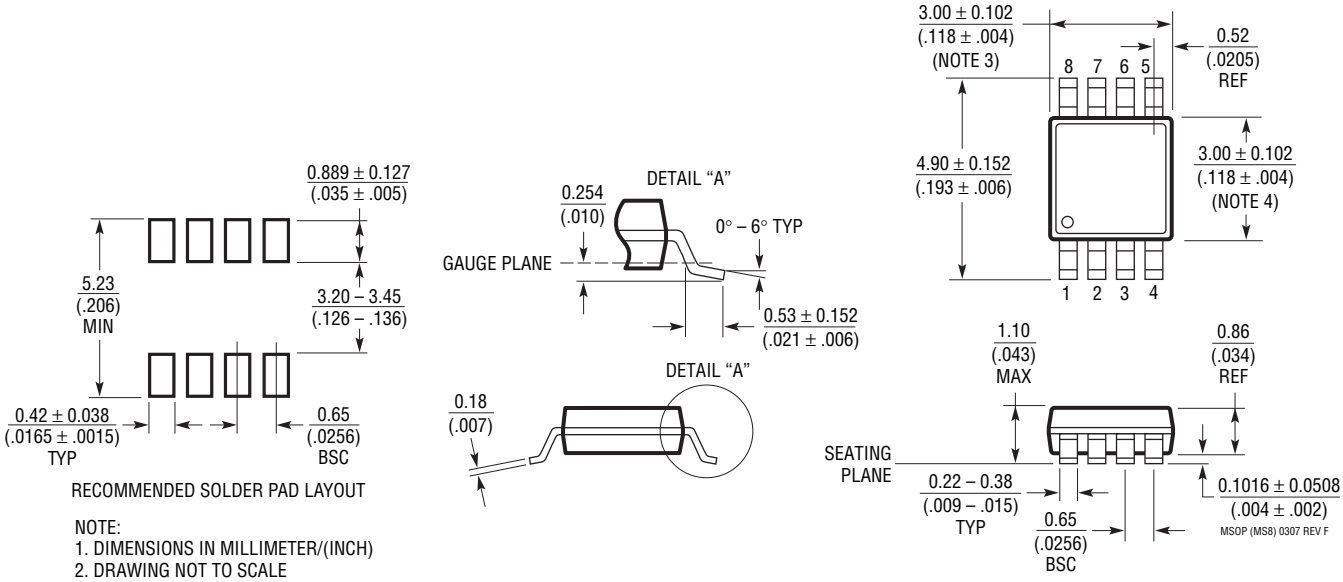

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

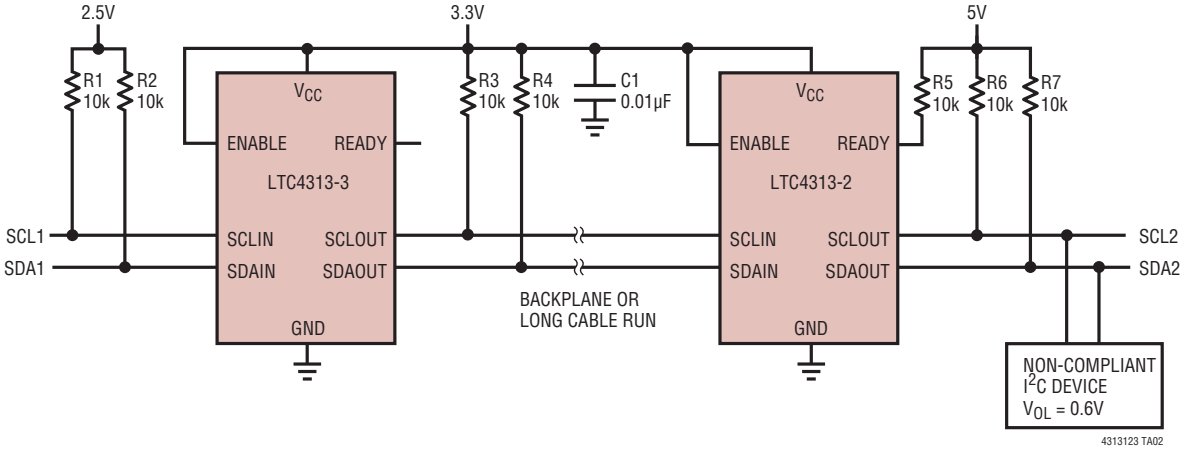
**MS8 Package**
**8-Lead Plastic MSOP**
(Reference LTC DWG # 05-08-1660 Rev F)




NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

## TYPICAL APPLICATION

**Cascaded Application with Level Shifting and Operation with a Non-Compliant I²C Device**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC4300A-1/<br>LTC4300A-2/<br>LTC4300A-3 | Hot Swappable 2-Wire Bus Buffers | -1: Bus Buffer with READY and ENABLE<br>-2: Dual Supply Buffer with ACC<br>-3: Dual Supply Buffer and ENABLE |
| LTC4302-1/<br>LTC4302-2 | Addressable 2-Wire Bus Buffer | Address Expansion, GPIO, Software Controlled |
| LTC4303/<br>LTC4304 | Hot Swappable 2-Wire Bus Buffer with Stuck Bus Recovery | Provides Automatic Clocking to Free Stuck I²C Busses |
| LTC4305/<br>LTC4306 | 2- or 4-Channel, 2 Wire Bus Multiplexers with Capacitance Buffering | Two or Four Software Selectable Downstream Busses, Stuck Bus Disconnect, Rise Time Accelerators, Fault Reporting, ±5kV HBM ESD |
| LTC4307 | Low Offset Hot Swappable 2-Wire Bus Buffer with Stuck Bus Recovery | 60mV Bus Offset, Rise Time Accelerators, ±5kV HBM ESD |
| LTC4307-1 | High Definition Multimedia Interface (HDMI) Level Shifting 2-Wire Bus Buffer | 60mV Buffer Offset, 3.3V to 5V Level Shifting, 30ms Stuck Bus Disconnect and Recovery, ±5kV HBM ESD |
| LTC4308 | Low Voltage, Level Shifting Hot Swappable 2-Wire Bus Buffer with Stuck Bus Recovery | Bus Buffer with 1V Precharge, ENABLE and READY, 0.9V to 5.5V Level Translation, 30ms Stuck Bus Disconnect and Recovery, Output Side Rise Time Accelerators, ±6kV HBM ESD |
| LTC4309 | Low Offset Hot Swappable 2-Wire Bus Buffer with Stuck Bus Recovery | 60mV Buffer Offset, 30ms Stuck Bus Disconnect and Recovery, Rise Time Accelerators, ±5kV HBM ESD, 1.8V to 5.5V Level Translation |
| LTC4310-1<br>LTC4310-2 | Hot Swappable I²C Isolators | Bidirectional I²C Communication Between Two Isolated Busses, LTC4310-1: 100kHz Bus, LTC4310-2: 400kHz Bus |
| LTC4311 | Low Voltage I²C/SMBus Accelerator | Rise Time Acceleration with ENABLE and ±8kV HBM ESD |
| LTC4312/<br>LTC4314 | 2- or 4-Channel, Hardware Selectable 2 Wire Bus Multiplexers with Capacitance Buffering | Two or Four Pin Selectable Downstream Busses, $V_{IL}$ Up to 0.3•$V_{CC}$, Stuck Bus Disconnect, Rise time Accelerators, 45ms Stuck Bus Disconnect and Recovery, ±4kV HBM ESD |
| LTC4315 | High Noise Margin 2-Wire Bus Buffer | $V_{IL}$ = 0.3•$V_{CC}$, Rise Time Accelerators, Stuck Bus Disconnect, 1V Precharge, ENABLE and READY Pins, ±4kV HBM ESD |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