

Helping Customers Innovate, Improve & Grow



VC-501

Description

The VC-501 is a voltage controlled crystal oscillator that is housed in a hermetic 14.0 x 9.0 x 4.5mm ceramic package. Depending upon the frequency and application requirements, one of three various oscillator designs is available for use yielding very low jitter and phase noise characteristics.

Features

- CMOS or LVPECL outputs
- Output Frequencies from 77.76 MHz to 1 GHz
- 3.3 V Operation
- Fundamental Crystal, Crystal Multiplier w/SAW, or Fundamental SAW Design for Low Jitter Performance
- Output Disable Feature
- ± 20 ppm Temperature Stability Available
- 0/70°C or -40/85°C Operating Temperature
- Industry Standard Package, 14.0 x 9.0 x 4.5 mm
- Product is free of lead and compliant to EC RoHS Directive



Applications

- SONET/SDH/DWDM
- Ethernet, SyncE, GE
- xDSL, PCMA
- Digital Video
- Broadband Access
- Base Stations, Picocells

Block Diagrams

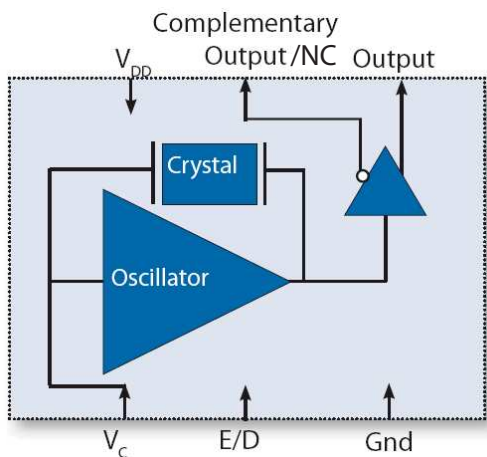


Figure 1a. Crystal-Based

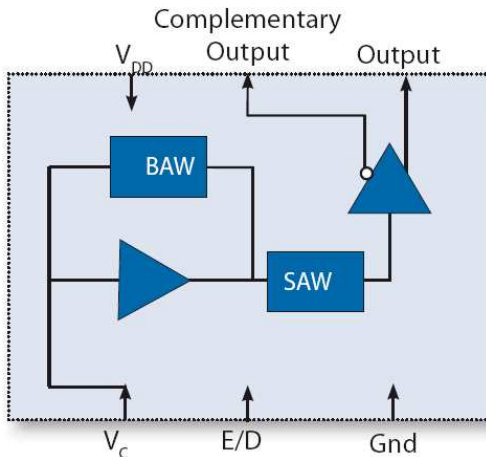


Figure 1b. Crystal-Based Multiplier w/SAW

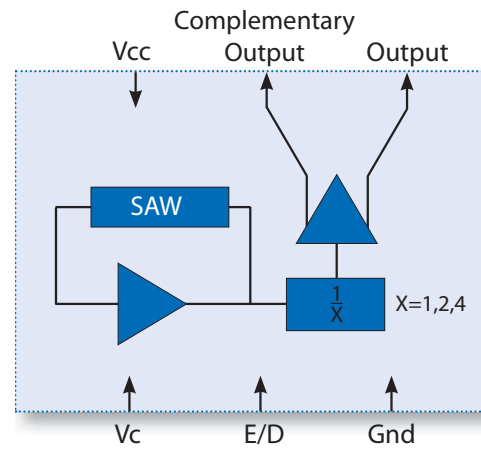


Figure 1c. SAW-Based

Performance Specifications

Table 1. Electrical Performance - 3.3V CMOS (77.76 MHz to 160 MHz) Crystal-Based

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage ¹	V_{DD}	3.135	3.3	3.465	V
Current ²	I_{DD}			40	mA
Frequency					
Nominal Frequency ³	f_N	77.76		160.00	MHz
Absolute Pull Range ^{2,6} , <i>ordering option</i>	APR	±50			ppm
Linearity ²	Lin		5		%
Gain Transfer ²	K_V	+80			ppm/V
Temperature Stability	f_{STAB}		±20		ppm
Outputs					
Output Logic Levels ² Output Logic High Output Logic Low	V_{OH} V_{OL}	0.9* V_{DD}		0.1* V_{DD}	V
Load	I_{OUT}			15	pF
Rise Time ^{2,4}	t_R			5	ns
Fall Time ^{2,4}	t_F			5	ns
Symmetry ²	SYM	45	50	55	%
Jitter, RMS ^{5,7} (12kHz to 20 MHz)	ϕ_J		80	200	fsec
Phase Noise ⁸ (122.88 MHz) 10Hz 100Hz 1kHz 10kHz 100kHz 1MHz 10MHz			-66 -98 -124 -138 -151 -158 -161		dBc/Hz
Control Voltage					
Control Voltage Range for Pull Range	V_C	0.3		3.0	V
Control Voltage Input Impedance	Z_{IN}		100		K Ω
Control Voltage Modulation BW	BW	10			kHz
Output Enable/Disable ⁹ Output Enabled Output Disabled	V_{IH} V_{IL}	0.9* V_{DD}		0.1* V_{DD}	V
Start-Up Time	T_S			10	ms
Operating Temp, Ordering Option	T_{OP}	0/70 or -40/85			°C
Package Size		14.0 x 9.0 x 4.5			mm

- 1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for examples 0.1 and 0.01 uF
- 2] Parameters are tested with production test circuit as shown in Figure 2.
- 3] See Standard Frequencies and Ordering Information tables for more specific information
- 4] Measured from 20% to 80% of a full output swing as shown in Figure 4.
- 5] Not tested in production, guaranteed by design, verified at qualification.
- 6] Tested with $V_C = 0.3V$ to $3.0V$ unless otherwise stated in part description
- 7] Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples.
- 8] Phase Noise is measured with an Agilent E5052A.
- 9] The Output is Enabled if the Enable/Disable is left open.

Performance Specifications

Table 2. Electrical Performance - 3.3V LVPECL (77.76 MHz to 200 MHz) Crystal-Based

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage ¹		3.135	3.3	3.465	V
Current ²	I_{DD}			90	mA
Frequency					
Nominal Frequency ³	f_N	77.76		200	MHz
Absolute Pull Range ^{2,6} , <i>ordering option</i>	APR	±50			ppm
Linearity ²	Lin		5		%
Gain Transfer ² (77.76 - 200 MHz)	K_V	+80			ppm/V
Temperature Stability	f_{STAB}		±20		ppm
Outputs					
Output Logic Levels ² Output Logic High Output Logic Low	V_{OH} V_{OL}	$V_{DD}-1.025$ $V_{DD}-1.810$	$V_{DD}-0.950$ $V_{DD}-1.700$	$V_{DD}-0.880$ $V_{DD}-1.620$	V
Rise Time ^{2,4}	t_R			1	ns
Fall Time ^{2,4}	t_F			1	ns
Symmetry ²	SYM	45	50	55	%
Jitter, RMS ^{5,8} (12kHz to 20 MHz)	ϕ_J		0.3	1	ps
Jitter, RMS ^{5,8} (10kHz to 1MHz)	ϕ_J			0.3	ps
Phase Noise ⁸ (122.88 MHz) 10Hz 100Hz 1kHz 10kHz 100kHz 1MHz 10MHz			-60 -93 -118 -131 -145 -149 -151		dBc/Hz
Control Voltage					
Control Voltage Range for Pull Range	V_C	0.3		3.0	V
Control Voltage Input Impedance	Z_{IN}	10			MΩ
Control Voltage Modulation BW	BW	10			kHz
Output Enable/Disable ⁹ Output Enabled, Option A Output Disabled, Option A	V_{IH} V_{IL}	$0.9 \cdot V_{DD}$		$0.1 \cdot V_{DD}$	V
Start-Up Time	T_S			10	ms
Operating Temp, Ordering Option	T_{OP}	0/70 or -40/85			°C
Package Size		14.0 x 9.0 x 4.5			mm

- 1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for examples 0.1 and 0.01uF
- 2] Parameters are tested with production test circuit below as shown in Figure 3.
- 3] See Standard Frequencies and Ordering Information tables for more specific information
- 4] Measured from 20% to 80% of a full output swing as shown in Figure 4.
- 5] Not tested in production, guaranteed by design, verified at qualification.
- 6] Tested with $V_C = 0V$ to 3.3V unless otherwise stated in part description
- 7] Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples.
- 8] Phase Noise is measured with an Agilent E5052A.
- 9] The Output is Enabled if the Enable/Disable is left open.

Performance Specifications

Table 3. Electrical Performance - 3.3V LVPECL (201 MHz to 1 GHz) Crystal-Based Multiplier w/SAW					
Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage ¹		3.135	3.3	3.465	V
Current ²	I_{DD}			90	mA
Frequency					
Nominal Frequency ³	f_N	201		1000	MHz
Absolute Pull Range ^{2,6} , <i>ordering option</i>	APR	±50			ppm
Linearity ²	Lin		5	10	%
Gain Transfer ² (77.76 - 200 MHz)	K_V	+100			ppm/V
Temperature Stability	f_{STAB}		±20		ppm
Outputs					
Mid Level		$V_{DD}-1.5$	$V_{DD}-1.3$	$V_{DD}-1.2$	V
Single Ended Swing			750		mV-pp
Double Ended Swing			1.5		V-pp
Fall Time ^{2,4}	t_R			500	ps
Fall Time ^{2,4}	t_F			500	ps
Symmetry ²	SYM	45	50	55	%
Jitter, RMS ^{5,8} (12kHz to 20 MHz)	ϕ_J		0.1	0.250	ps
Jitter, RMS ^{5,8} (50kHz to 80MHz)	ϕ_J		0.12	0.300	ps
Period Jitter, RMS (622.08MHz) ⁷	ϕ_J		2.5	3.0	ps
Period Jitter, Peak-Peak (622.08MHz) ⁷	ϕ_J		16	24	ps
Spurious Suppression			-60	-50	dBc
Phase Noise ⁸ (614.4 MHz)					dBc/Hz
10Hz			-57		
100Hz			-88		
1kHz			-112		
10kHz			-131		
100kHz			-138		
1MHz			-142		
10MHz			-152		
Control Voltage					
Control Voltage Range for Pull Range	V_C	0.3		3.0	V
Control Voltage Input Impedance	Z_{IN}	75			k Ω
Control Voltage Modulation BW	BW	50			kHz
Output Enabled, Option A	V_{IH}	0.7* V_{DD}			V
Output Disabled, Option A	V_{IL}			0.3* V_{DD}	V
Output Enabled, Option C	V_{IH}	0.7* V_{DD}			V
Output Disabled, Option C	V_{IL}			0.3* V_{DD}	V
Operating Temp, Ordering Option	T_{OP}	0/70 or -40/85			°C
Package Size		14.0 x 9.0 x 4.5			mm

- 1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for examples 0.1 and 0.01 μ F
- 2] Parameters are tested with production test circuit below as shown in Figure 3.
- 3] See Standard Frequencies and Ordering Information tables for more specific information
- 4] Measured from 20% to 80% of a full output swing as shown in Figure 4.
- 5] Not tested in production, guaranteed by design, verified at qualification.
- 6] Tested with $V_C = 0V$ to 3.3V unless otherwise stated in part description
- 7] Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples.
- 8] Phase Noise is measured with an Agilent E5052A.
- 9] The Output is Enabled if the Enable/Disable is left open.

Performance Specifications

Table 4. Electrical Performance - 3.3V LVPECL (120 MHz to 1 GHz) SAW-Based

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage ¹		2.97	3.3	3.63	V
Current ² (No Load)	I_{DD}		60	75	mA
Frequency					
Nominal Frequency ³	f_N	120		1000	MHz
Absolute Pull Range ^{2,6} , <i>ordering option</i>	APR	±50			ppm
Linearity ²	Lin		±7		%
Gain Transfer ² (Standard Gain)	K_V	+445			ppm/V
Gain Transfer ² (Low Gain)	K_V	+325			ppm/V
Temperature Stability	f_{STAB}		±100		ppm
Outputs					
Output Logic Levels ² Mid Level Single Ended Swing Differential Swing		$V_{DD}-1.5$	$V_{DD}-1.3$ 750 1.5	$V_{DD}-1.1$	mV mV-pp V-pp
Rise Time ^{2,4}	t_R		180	250	ps
Fall Time ^{2,4}	t_F		180	250	ps
Symmetry ²	SYM	45	50	55	%
Jitter, RMS ^{5,8} (12kHz to 20 MHz)	ϕ_J		0.15	0.3	ps
Control Voltage					
Control Voltage Range for Pull Range	V_C	0.3		3.0	V
Control Voltage Input Impedance ⁵	Z_{IN}		123		k Ω
Control Voltage Modulation BW ⁵	BW		200		kHz
Output Enable/Disable ⁹ Output Enabled, Option A Output Disabled, Option A	V_{IH} V_{IL}	0.9* V_{DD}		0.1* V_{DD}	V
Start-Up Time	T_S			10	ms
Operating Temp, Ordering Option	T_{OP}	0/70 or -40/85			°C

- 1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for examples 0.1 and 0.01uF
- 2] Parameters are tested with production test circuit below as shown in Figure 3.
- 3] See Standard Frequencies and Ordering Information tables for more specific information
- 4] Measured from 20% to 80% of a full output swing as shown in Figure 4.
- 5] Not tested in production, guaranteed by design, verified at qualification.
- 6] Tested with $V_C = 0V$ to 3.3V unless otherwise stated in part description
- 7] Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples.
- 8] Phase Noise is measured with an Agilent E5052A.
- 9] The Output is Enabled if the Enable/Disable is left open.

Test Circuits

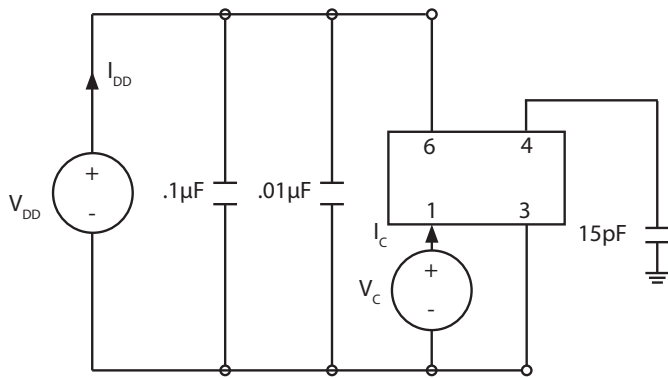
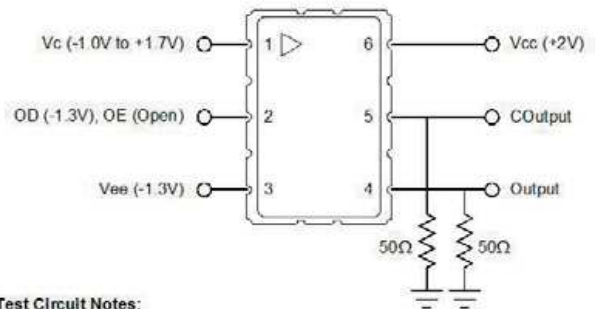


Figure 2. CMOS Test Circuit



Test Circuit Notes:
 1) To Permit 50Ω Measurement of Outputs, all DC Inputs are Biased Down 1.3V.
 2) All Voltage Sources Contain Bypass Capacitors to Minimize Supply Noise.
 3) 50Ω Terminations are Within Test Equipment.

Figure 3. LVPECL Test Circuit

Waveform

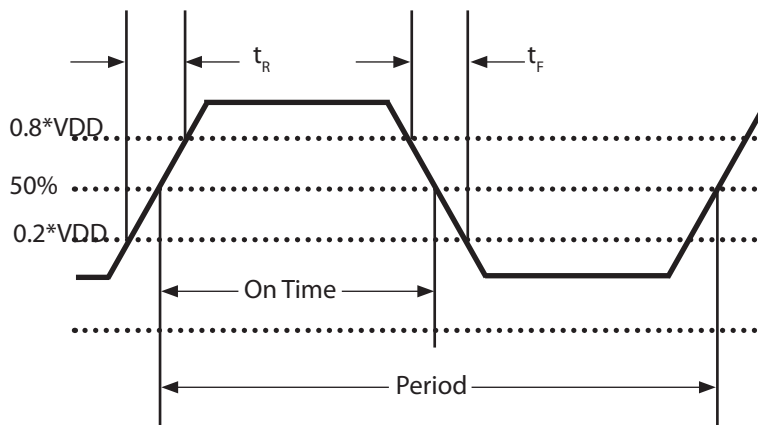


Figure 4. Output Waveform

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{DD}	0 to 6	V
Voltage Control Range	V_C	0 to V_{CC}	V
Storage Temperature	TS	-55 to 125	°C
Soldering Temp/Time	T_{LS}	260 / 20	°C / sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this datasheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if OD or Vc is applied before Vcc.

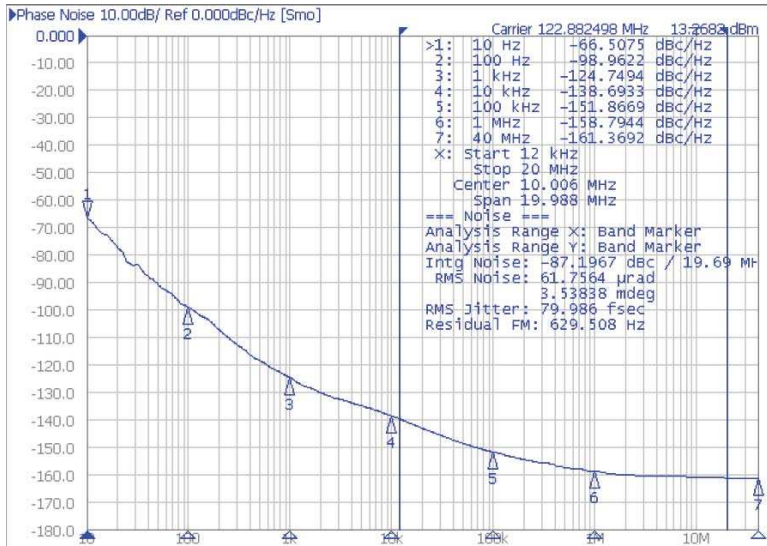


Figure 5. Typical Phase Noise - 122.88 MHz CMOS

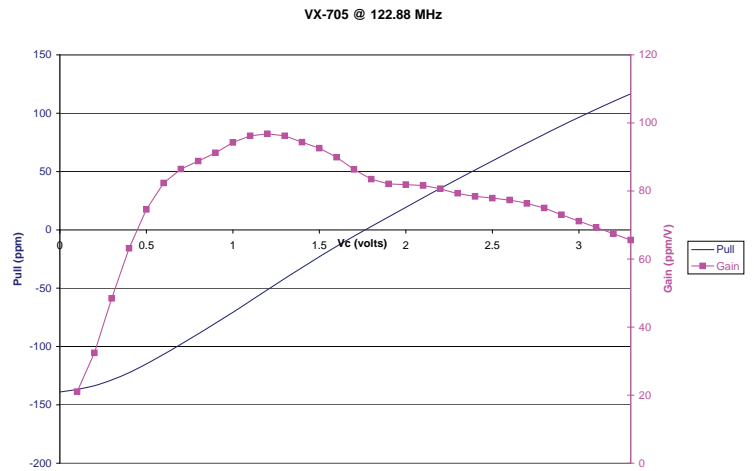


Figure 6. Typical Gain - 122.88 MHz CMOS

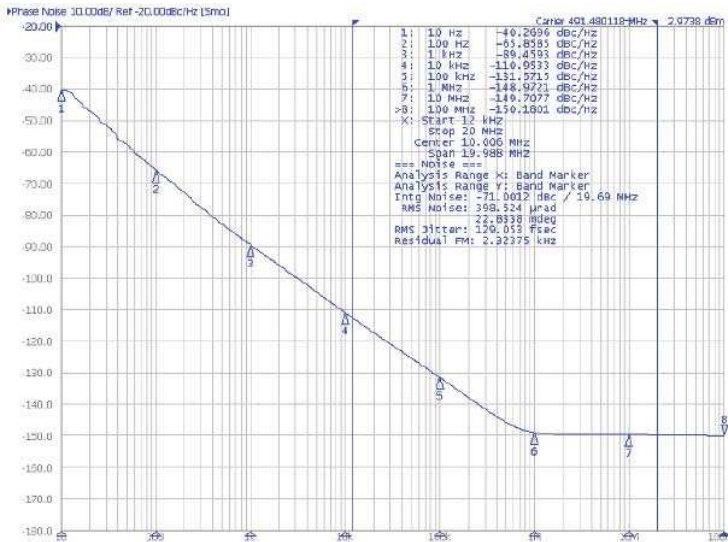


Figure 7. Typical Phase Noise - 491.52 MHz LVPECL (SAW)

Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VC-501 family is capable of meeting the following qualification tests:

Table 6. Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold over Nickel

Handling Precautions

Although ESD protection circuitry has been designed into the VC-501 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and design protection evaluation.

Table 7. ESD Ratings

Model	Minimum	Conditions
Human Body Model	500V	MIL-STD-883, Method 3015
Charged Device Model	500V	JESD22-C101

Table 8. Reflow Profile

Parameter	Symbol	Value
PreHeat Time Ts-min Ts-max	t_s	60 sec Min, 180 sec Max 150°C 200°C
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	T_{AMB-P}	480 sec Max
Time at 260 °C	t_p	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

Solderprofile:

The device is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VC-501 device is hermetically sealed so an aqueous wash is not an issue.

Termination Plating:
Electroless Gold Plate over Nickel Plate

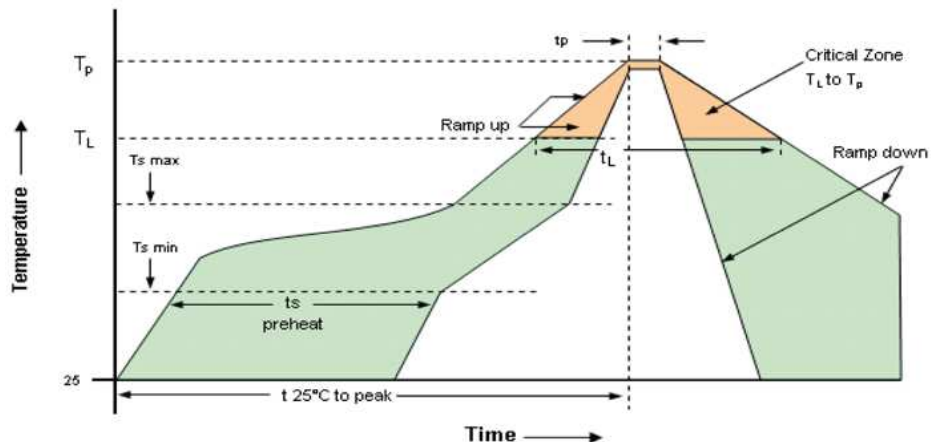


Figure 8. Recommended Reflow Profile

Outline Drawing & Pad Layout

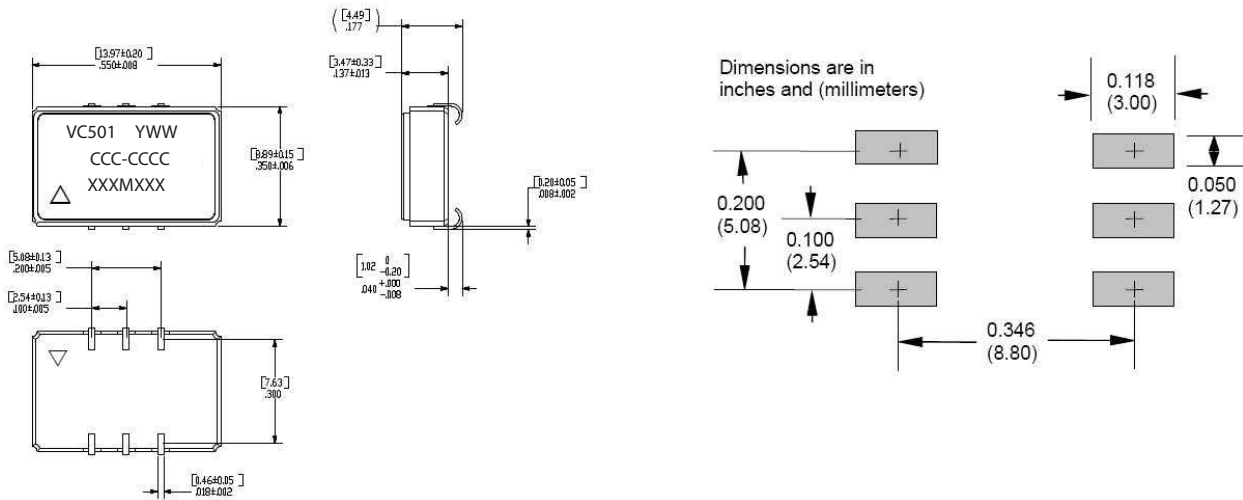


Figure 9. Outline Drawing and Pad Layout

Table 9a. Pin Out - 3.3V CMOS Option

Pin	Symbol	Function
1	V_C	VCXO Control Voltage
2	E/D	Enable Disable ** See Ordering Options**
3	GND	Case and Electrical Ground
4	Output	Output
5	N/C	No Connect
6	V_{DD}	Power Supply Voltage

Table 9b. Pin Out - 3.3V LVPECL Option

Pin	Symbol	Function
1	V_C	VCXO Control Voltage
2	E/D	Enable Disable **See Ordering Options**
3	GND	Case and Electrical Ground
4	Output	Output
5	COutput	Complementary Output
6	V_{DD}	Power Supply Voltage

Tape & Reel (EIA-481-2-A)

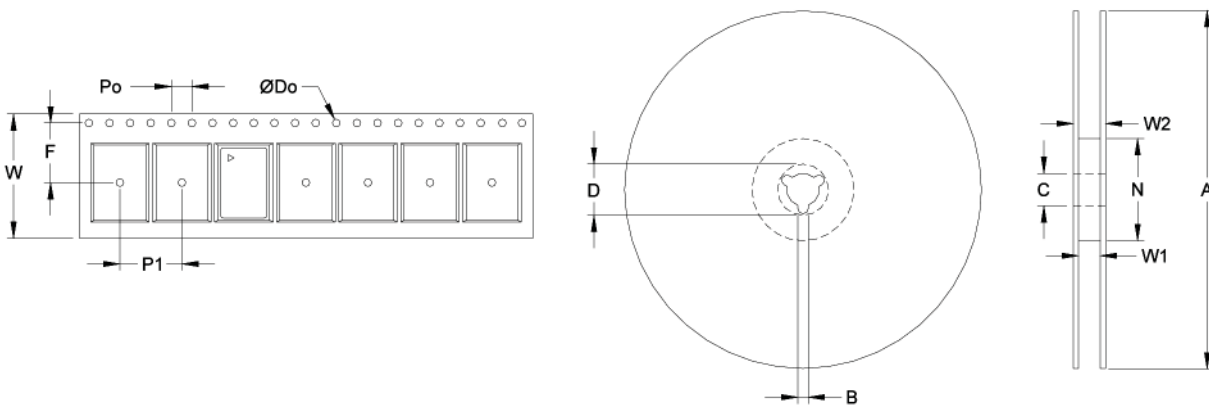


Figure 10. Tape and Reel Drawing

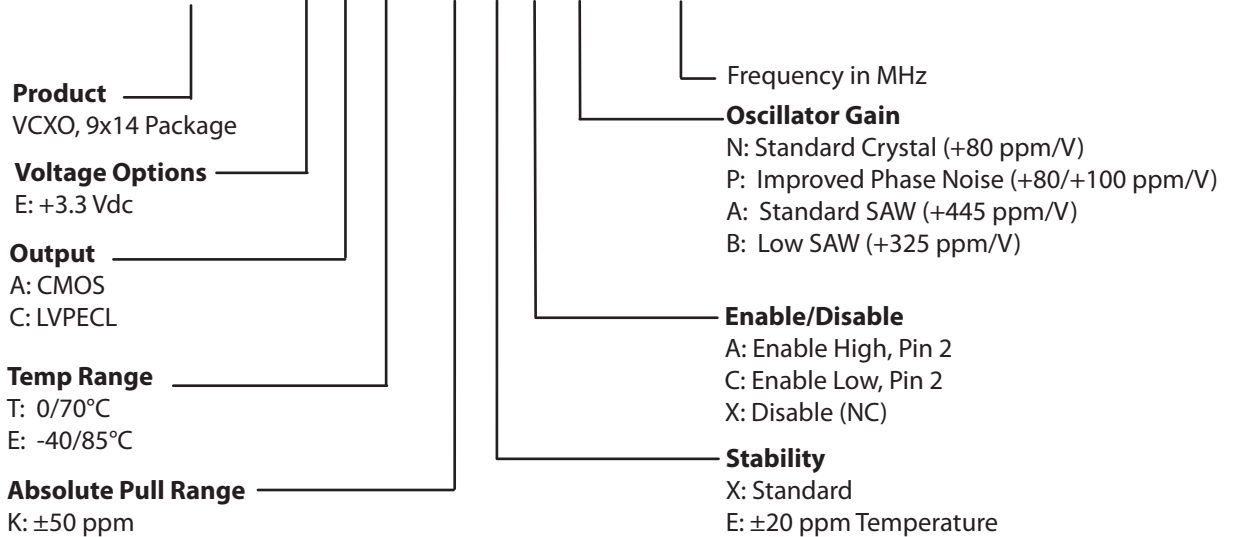
Table 10. Tape and Reel Information

Dimension	Tape Dimensions (mm)					Reel Dimensions (mm)							# Per Reel
	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	
VC-501	24	11.5	1.5	4	12	330	1.78	13	21	100	25	30	200

Table 11. Standard Output Frequencies (MHz)							
89.60000	93.31200	100.00000	122.88000	125.00000	127.79520	148.50000	155.52000
156.25000	161.13280	167.331600					

Ordering Information

VC-501- E A E - K X A N- 122M880000



**Note: not all combination of options are available.
Other specifications may be available upon request.*

Example: VC-501-EAE-KEXN-122M880000

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Revision History

Date	Approved	Description
30Jun2011	BW	Added 3.3V LVPECL (201 MHz to 1 GHz) Crystal-Based Multiplier w/SAW Electrical Specifications (Table 3) and Block Diagrams 1b and 1c.
29Jun2011	BW	Updated recommended solder reflow information, Table 6.
17May2011	BW	Added additional order option to the Oscillator Gain ordering code.
05Apr2011	BW	Added CMOS and oscillator gain ordering options. Ordering Codes updated to new universal scheme.