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### Description

The VX-702 is a Voltage Controlled Crystal Oscillator that operates at the fundamental frequency of the internal fundamental crystal which enables the circuit to achieve low phase jitter performance over a wide operating temperature range. The VX-702 is housed in an industry standard hermetically sealed LCC package and available in tape and reel.

### Features

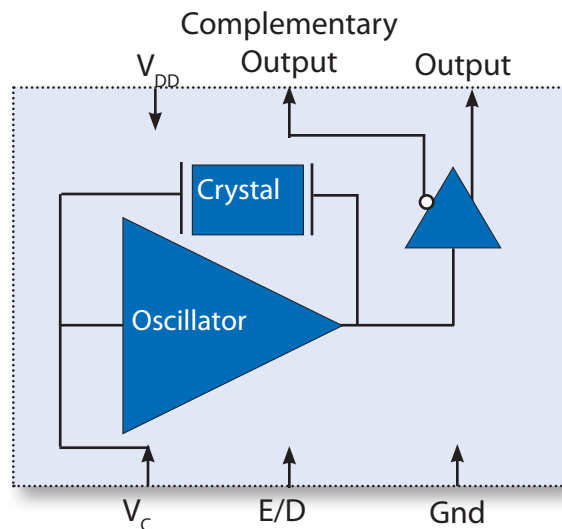
- Fundamental VCXO with no subharmonics or spurs
- Low Jitter, sub 1pS performance
- Output Frequencies from 1.024 MHz to 77.76 MHz
- 3.3 V Operation
- LVPECL Output
- Output Disable Feature
- Excellent  $\pm 20$ ppm temperature stability,
- 0/70°C or -40/85°C operating temperature
- Small Industry Standard Package, 5.0x7.5x1.8mm
- Product is free of lead and compliant to EC RoHS Directive



### Applications

- Ideal for PLL circuits for clock smoothing and frequency translation
- SONET, SDH
  - Synchronous Ethernet
  - Fiber Channel
  - LAN / WAN
  - Test and Measurement

### Block Diagram



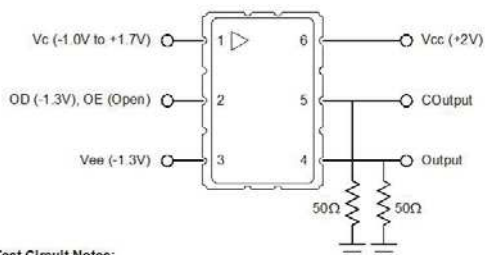
# Performance Specifications

**Table 1. Electrical Performance**

Parameter	Symbol	Min	Typical	Maximum	Units
<b>Supply</b>					
Voltage <sup>1</sup>	$V_{DD}$	3.135	3.3	3.465	V
Current (No Load)	$I_{DD}$			65	mA
<b>Frequency</b>					
Nominal Frequency <sup>2</sup>	$f_N$	1.024		77.76	MHz
Absolute Pull Range <sup>3,6</sup>	APR	$\pm 50$			ppm
Linearity <sup>3</sup>	Lin		5	10	%
Gain Transfer Positive (See pg 5) <sup>3</sup>	$K_V$		+90		ppm/V
Temperature Stability <sup>3</sup>	$f_{STAB}$		$\pm 20$		ppm
<b>Outputs</b>					
Output Logic Levels <sup>3</sup> Output Logic High Output Logic Low	$V_{OH}$ $V_{OL}$	$V_{DD}-1.025$ $V_{DD}-1.810$	$V_{DD}-0.950$ $V_{DD}-1.700$	$V_{DD}-0.880$ $V_{DD}-1.620$	V
Current	$I_{OUT}$			20	mA
Rise Time <sup>4</sup> Fall Time	$t_R$ $t_F$			1	ns
Symmetry <sup>3</sup>	SYM	45	50	55	%
Jitter (12 kHz - 20 MHz BW)50.00MHz <sup>5</sup>	$\phi_J$		0.8		ps
Jitter (50 kHz - 80 MHz BW) 50.00MHz <sup>5</sup>	$\phi_J$		1.0		ps
Period Jitter, RMS (50.00 MHz) <sup>7</sup>	$\phi_J$		3.0		ps
Period Jitter, Peak - Peak (50.00 MHz) <sup>7</sup>	$\phi_J$		20		ps
<b>Control Voltage</b>					
Control Voltage Range for APR	$V_C$	0.3		3.0	V
Control Voltage Input Leakage	$I_{IN}$			1	$\mu A$
Control Voltage Modulation BW	BW	20	100		kHz
<b>Enable/Disable</b>					
Output Enabled <sup>8</sup>	$V_{IH}$	$0.9 * V_{DD}$			V
Output Disabled	$V_{IL}$			$0.1 * V_{DD}$	
Operating Temperature	$T_{OP}$	0/70 or -40/85			$^{\circ}C$
Package Size		5.0 x 7.5 x 1.8			mm

- 1] The VX-702 power supply should be filtered, eg, 0.1 and 0.01  $\mu F$  to ground
- 2] See Standard Frequencies and Ordering Information tables for more specific information
- 3] Parameters are tested with production test circuit below (Fig 1).
- 4] Measured from 20% to 80% of a full output swing (Fig 2).
- 5] Integrated across stated bandwidth.
- 6] Tested with  $V_C = 0.3V$  to  $3.0V$  unless otherwise stated in part description
- 7] Broadband Period Jitter measured using Lecroy Wavemaster 8600A 6 GHz Oscilloscope, 25K samples taken
- 8] Output is Enabled if E/D is left floating

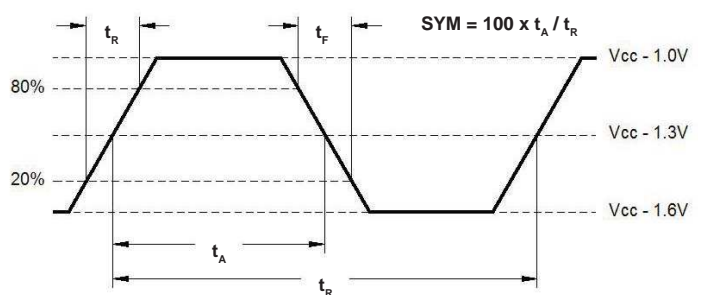
**Fig 1: Test Circuit**



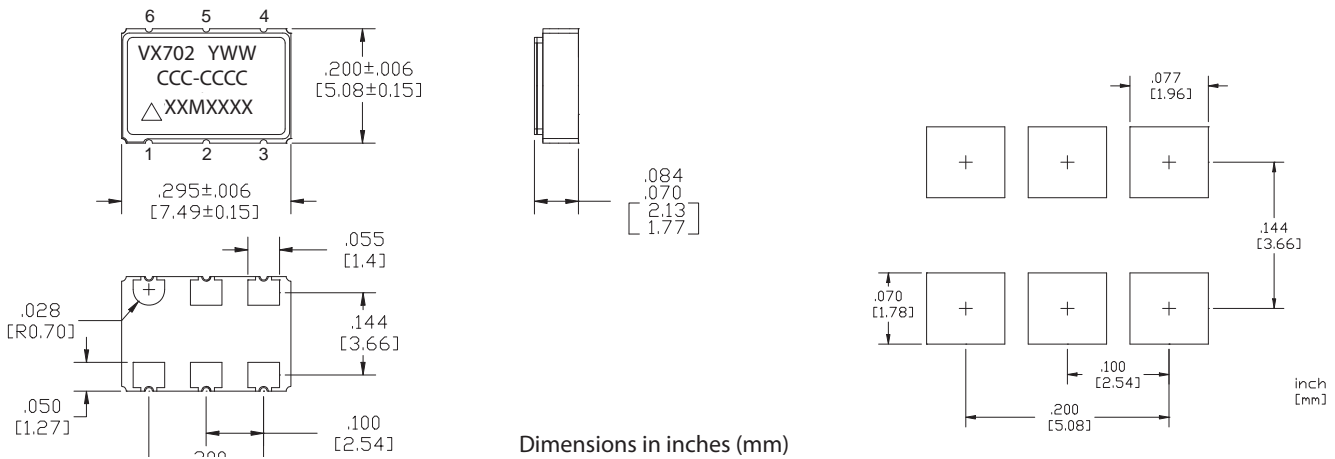
**Test Circuit Notes:**

- 1) To Permit 50 $\Omega$  Measurement of Outputs, all DC Inputs are Biased Down 1.3V.
- 2) All Voltage Sources Contain Bypass Capacitors to Minimize Supply Noise.
- 3) 50 $\Omega$  Terminations are Within Test Equipment.

**Fig 2: LVPECL Waveform**



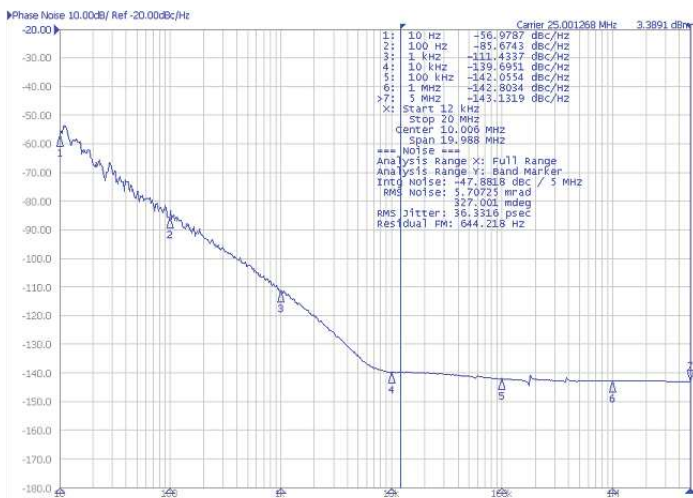
# Outline Drawing & Pad Layout



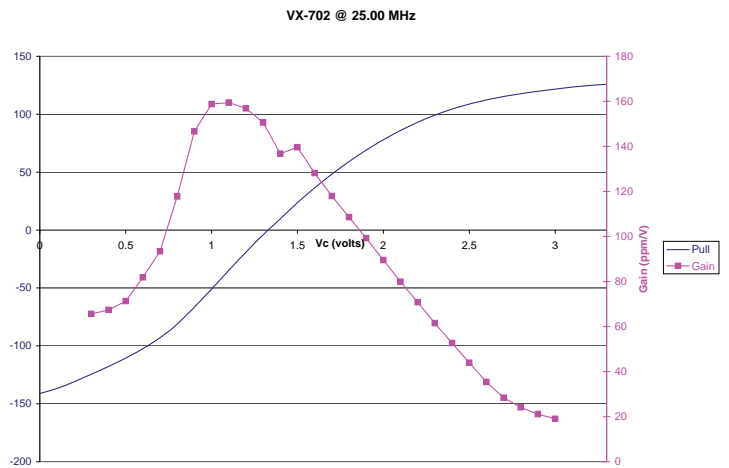
**Table 2. Pin Out**

Pin	Symbol	Function
1	$V_C$	VCXO Control Voltage
2	OE	Enable/Disable
3	GND	Case and Electrical Ground
4	Output	Output
5	COutput	Complementary Output
6	$V_{CC}$	Power Supply Voltage (3.3V ±10%)

## Typical Phase Noise



## Typical Gain



## Suggested Output Load Configurations

The VX-702 incorporates a standard PECL output scheme, which are un-terminated emitters as shown in Figure 3. There are numerous application notes on terminating and interfacing PECL logic and the two most common methods are a single resistor to ground, Figure 4, and a pull-up/pull-down scheme as shown in Figure 5. An AC coupling capacitor is optional, depending on the application and the input logic requirements of the next stage.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

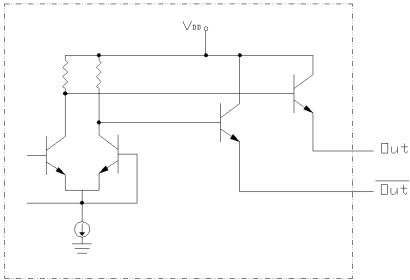


Figure 3 Standard PECL Output Configuration

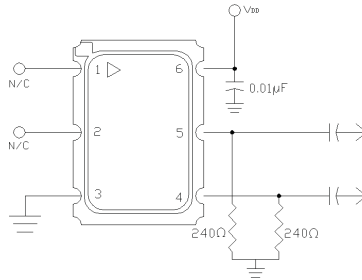


Figure 4 Single Resistor Termination Scheme  
Resistor values are typically 120 to 240 ohms

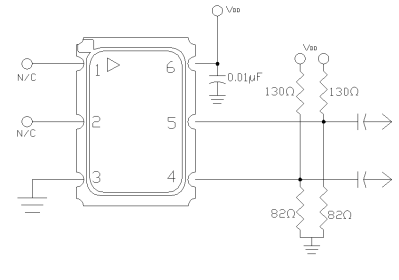


Figure 5 Pull-Up Pull-Down Termination

## Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VX-702 family is capable of meeting the following qualification tests:

Table 3. Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold over Nickel

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this datasheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if OD or Vc is applied before Vcc.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	$V_{DD}$	0 to 6	V
Output Current	$I_{OUT}$	25	mA
Voltage Control Range	$V_C$	0 to $V_{CC}$	V
Storage Temperature	$T_S$	-55 to 125	°C
Soldering Temp/Time	$T_{LS}$	260 / 40	°C / sec

Although ESD protection circuitry has been designed into the VX-702 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and design protection evaluation.

Table 5. ESD Ratings

Model	Minimum	Conditions
Human Body Model	500V	MIL-STD-883, Method 3015
Charged Device Model	500V	JESD22-C101

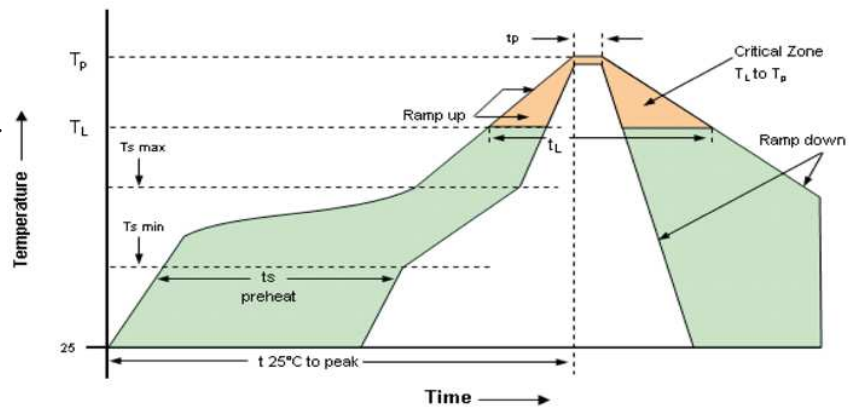
**Table 6. Reflow Profile**

Parameter	Symbol	Value
PreHeat Time Ts-min Ts-max	$t_s$	60 sec Min, 180 sec Max 150°C 200°C
Ramp Up	$R_{UP}$	3 °C/sec Max
Time Above 217 °C	$t_L$	60 sec Min, 150 sec Max
Time To Peak Temperature	$T_{AMB-P}$	480 sec Max
Time at 260 °C	$t_p$	20 sec Min, 40 sec Max
Ramp Down	$R_{DN}$	6 °C/sec Max

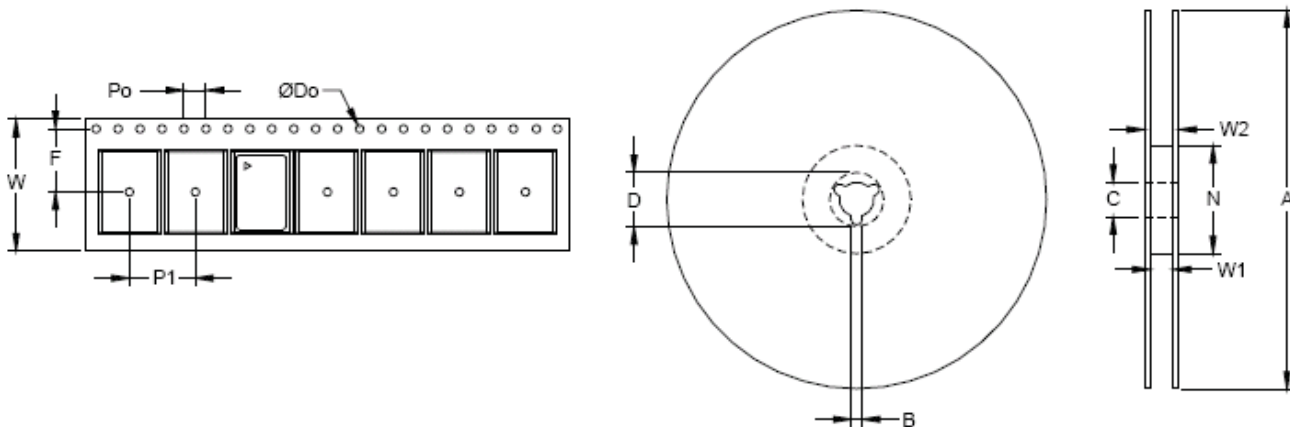
**Solderprofile:**

The device is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VX-702 device is hermetically sealed so an aqueous wash is not an issue.

Termination Plating:  
Electroless Gold Plate over Nickel Plate



## Tape & Reel (EIA-481-2-A)



**Table 7. Tape and Reel Information**

Dimension	Tape Dimensions (mm)					Reel Dimensions (mm)							# Per Reel
	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	
VX-702	16	7.5	1.5	4	8	178	1.5	13	20.2	50	16.4	22.4	200

**Table 8. Standard Output Frequencies (MHz)**

2.04800	10.00000	10.24000	16.38400	19.44000	21.12000	24.70400	25.00000
27.00000	27.12000	32.00000	36.00000	38.88000	40.00000	44.43430	47.85000
50.00000	51.200000	51.84000	54.00000	57.60000	61.44000	62.20800	62.50000
67.50000	70.00000	75.00000	76.80000	77.76000	78.64320		

## Ordering Information

### VX-702- E C E - K X A N - xxMxxxxxxx

**Product**

VCXO, 5x7 Package

**Voltage Options**

E: +3.3 Vdc ±5%,

**Output**

C: LVPECL

**Temp Range**

T: 0/70°C

E: -40/85°C

**Absolute Pull Range**

K: ±50ppm

Frequency in MHz

**Other (Future Use)**

N: Standard

**Enable/Disable**

A: Enable High

**Stability**

X: Standard

E: ±20ppm Temperature Stability

*\*Note: not all combination of options are available.  
Other specifications may be available upon request.*

**Example: VX-702-ECE-KXAN-51M8400000**

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