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### Description

Vectron's VV-701 Voltage Controlled Crystal Oscillator (VCXO) is a quartz stabilized square wave generator with a CMOS output. The VV-701 uses fundamental crystals resulting in low jitter performance and a monolithic IC which improves reliability and reduces cost.

### Features

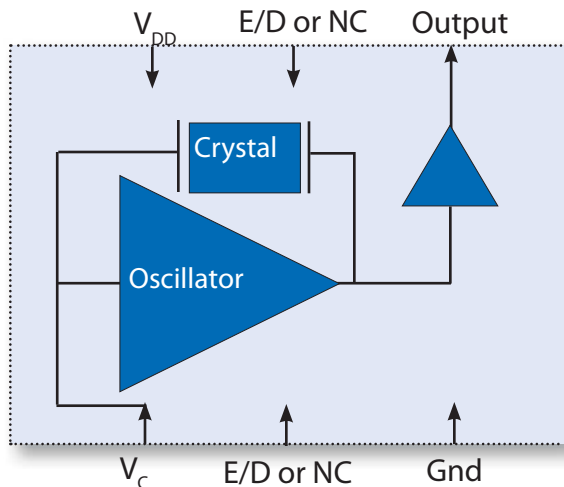
- CMOS output VCXO
- Output Frequencies from 1.544 MHz to 77.760 MHz
- 5.0 or 3.3 V Operation
- High Impedance Control Voltage Option
- Fundamental Crystal Design with Low Jitter Performance
- Output Disable Feature
- Excellent 20ppm Temperature Stability,
- 0/70°C or -40/85°C Operating Temperature
- Small Industry Standard Package, 5.0x7.0x1.8mm
- Product is free of lead and compliant to EC RoHS Directive



### Applications

- SONET/SDH/DWDM
- Ethernet, SynchE
- xDSL, PCMIA
- Digital Video
- Broadband Access
- Base Stations, Picocells

### Block Diagram



# Performance Specifications

**Table 1. Electrical Performance**

Parameter	Symbol	Min	Typical	Maximum	Units
<b>Supply</b>					
Voltage <sup>1</sup> , 5V option 3.3V option	$V_{DD}$	4.750 3.135	5.0 3.3	5.250 3.465	V
Current <sup>2</sup> , 5V option, 1.544-30MHz 30.001-50.000 50.001-77.760MHz 3.3V option, 1.544-30MHz 30.001-50.000 50.001-77.760MHz	$I_{DD}$			10 12 18 5 9 14	mA
<b>Frequency</b>					
Nominal Frequency <sup>3</sup>	$f_N$	1.544		77.760	MHz
Pull Range <sup>2,6</sup> , <i>ordering option</i>	APR TPR		$\pm 50, \pm 80, \pm 100$ $\pm 50, \pm 100, \pm 150$		ppm
Linearity <sup>2</sup>	Lin		5		%
Gain Transfer <sup>2</sup>	$K_V$		Positive, +65		ppm/V
Temperature Stability	$f_{STAB}$		$\pm 20$		ppm
<b>Outputs</b>					
Output Logic Levels <sup>2</sup> Output Logic High Output Logic Low		$0.9 * V_{DD}$		$0.1 * V_{DD}$	V
Load	$I_{OUT}$			15	pF
Rise Time <sup>2,4</sup>	$t_R$			5	ns
Fall Time <sup>2,4</sup>	$t_F$			5	ns
Symmetry <sup>2</sup>	SYM	45	50	55	%
Period Jitter <sup>5,7</sup> , RMS (61.44 MHz) Peak-Peak (61.440MHz)	$\phi_J$		3.0 23		ps
Jitter <sup>8</sup> , 12kHz-20MHz (61.44 MHz)	$\phi_J$		90		fs
Phase Noise <sup>8</sup> 10Hz 100Hz 1kHz 10kHz 100kHz 1MHz 10MHz			-63 -97 -129 -144 -157 -159 -164		dBc/Hz
<b>Control Voltage</b>					
Control Voltage Range for Pull Range	$V_C$	0.5 0.3		4.5 3.0	V
Control Voltage Input Impedance "E" Ordering option	$Z_{IN}$	2	100		K $\Omega$ M $\Omega$
Control Voltage Modulation BW	BW	10			kHz
Output Enable/Disable <sup>9</sup> Output Enabled Output Disabled		$0.9 * V_{DD}$		$0.1 * V_{DD}$	V
Start-Up Time				10	ms
Operating Temp, <i>ordering option</i>	$T_{OP}$	0/70 or -40/85			$^{\circ}C$
Package Size		5.0 x 7.0 x 1.8			mm

1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for examples 0.1 and 0.01uF

2] Parameters are tested with production test circuit (Fig 1).

3] See Standard Frequencies and Ordering Information tables for more specific information

4] Measured from 20% to 80% of a full output swing (Fig 2).

5] Not tested in production, guaranteed by design, verified at qualification.

6] Tested with  $V_C = 0.3V$  to  $3.0V$  unless otherwise stated in part description

7] Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples, see Application Note for Typical Phase Noise and Jitter Performance

8] Phase Noise is measured with an Agilent E5052A, see Application Note for Typical Phase Noise and Jitter Performance

9] The Output is Enabled if the Enable/Disable is left open.

## Test Circuit

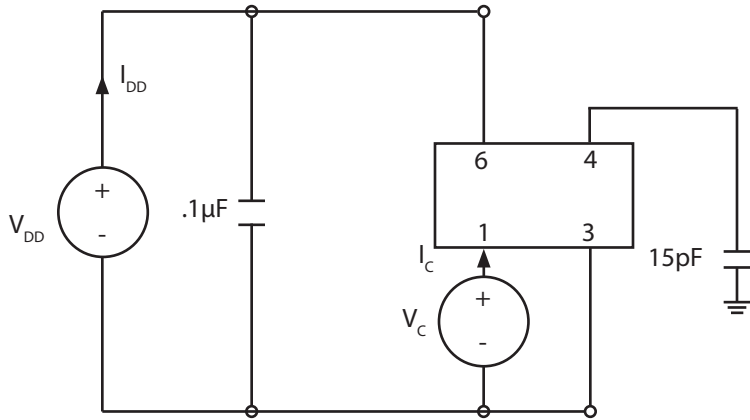


Fig 1: Test Circuit

## Waveform

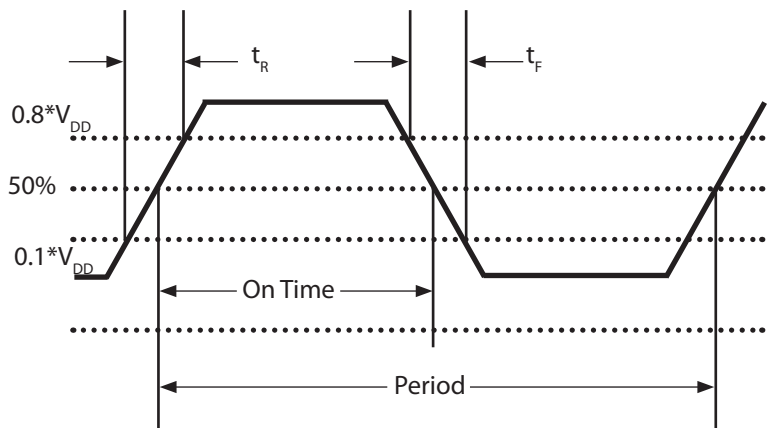


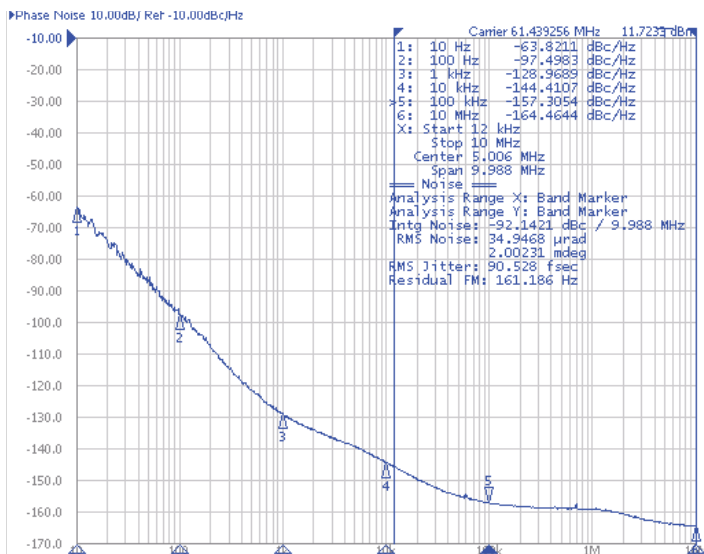
Fig 2: Output Waveform

Table 2. Absolute Maximum Ratings

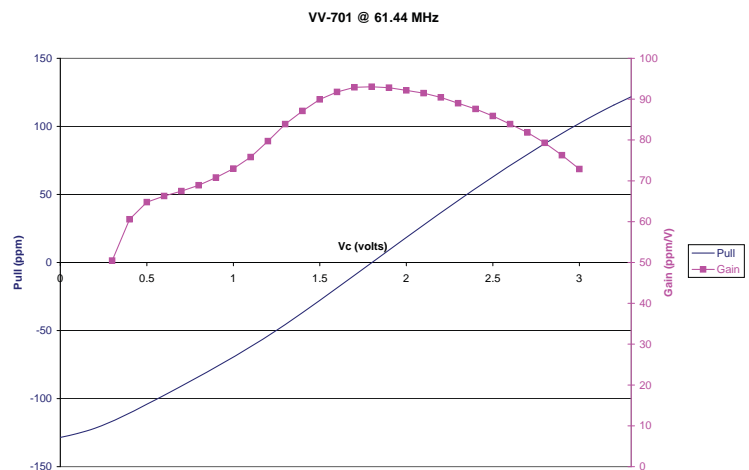
Parameter	Symbol	Ratings	Unit
Power Supply	$V_{CC}$	0 to 6	V
Voltage Control Range	$V_C$	0 to $V_{CC}$	V
Storage Temperature	TS	-55 to 125	°C
Soldering Temp/Time	$T_{LS}$	260 / 20	°C / sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this datasheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if OD or Vc is applied before Vcc.

## Typical Phase Noise



## Typical Gain



## Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VV-701 family is capable of meeting the following qualification tests:

**Table 3. Environmental Compliance**

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold over Nickel

## Handling Precautions

Although ESD protection circuitry has been designed into the VV-701 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and design protection evaluation.

**Table 4. ESD Ratings**

Model	Minimum	Conditions
Human Body Model	500V	MIL-STD-883, Method 3015
Charged Device Model	500V	JESD22-C101

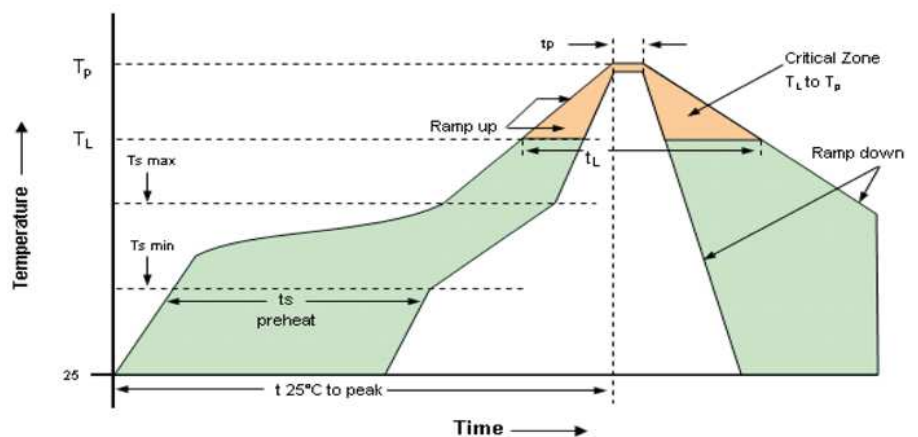
**Table 5. Reflow Profile**

Parameter	Symbol	Value
PreHeat Time Ts-min Ts-max	$t_s$	60 sec Min, 180 sec Max 150°C 200°C
Ramp Up	$R_{UP}$	3 °C/sec Max
Time Above 217 °C	$t_L$	60 sec Min, 150 sec Max
Time To Peak Temperature	$T_{25C\ to\ peak}$	480 sec Max
Time at 260 °C	$t_p$	20 sec Min, 40 sec Max
Ramp Down	$R_{DN}$	6 °C/sec Max

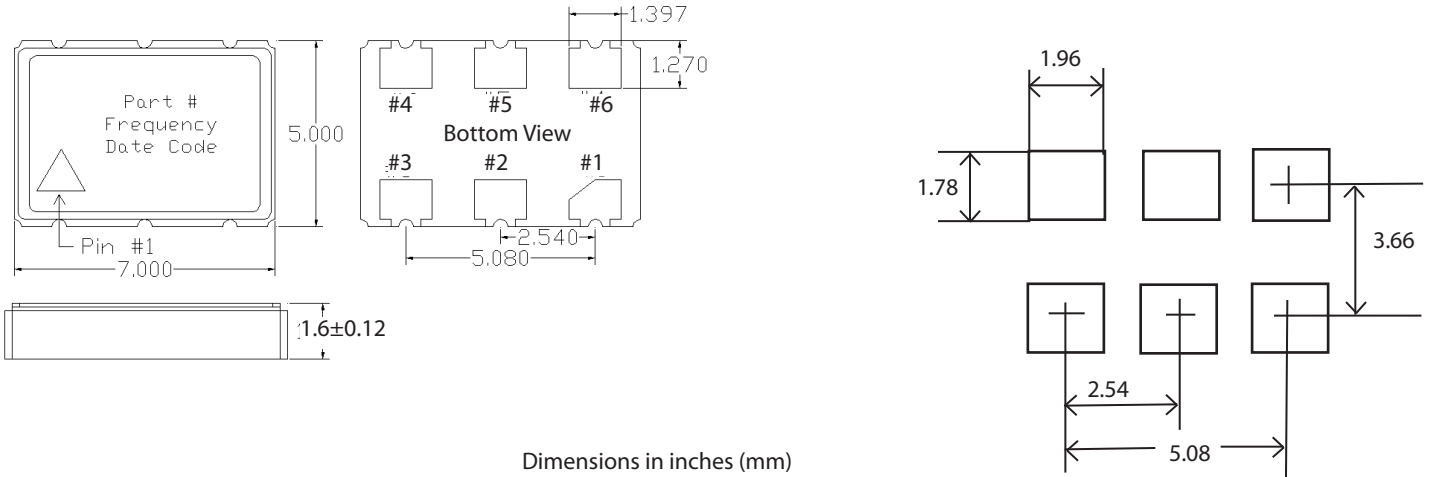
### Solderprofile:

The device is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VV-701 device is hermetically sealed so an aqueous wash is not an issue.

Termination Plating:  
Electroless Gold Plate over Nickel Plate



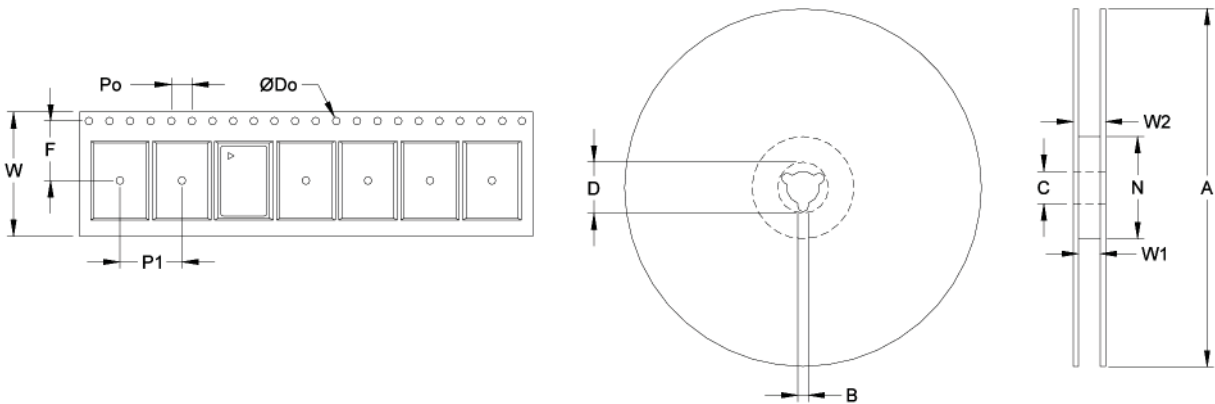
## Outline Drawing & Pad Layout



**Table 6. Pin Out**

Pin	Symbol	Function
1	$V_C$	VCXO Control Voltage
2	E/D	Enable Disable or NC
3	GND	Case and Electrical Ground
4	Output	Output
5	E/D	Enable Disable or NC
6	$V_{DD}$	Power Supply Voltage

## Tape & Reel (EIA-481-2-A)



**Table 7. Tape and Reel Information**

Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# Per Reel
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	
VV-701	12	5.5	1.5	4	8	178	1.78	13	20.6	55	12.4	22.4	500

**Table 8. Standard Output Frequencies (MHz)**

1.54400	2.04800	4.09600	6.17600	8.19200	10.00000	12.00000	12.28800
12.35200	13.00000	14.31800	15.44000	16.00000	16.38400	18.00000	18.43200
19.20000	19.44000	20.00000	20.48000	24.57600	24.70400	25.00000	27.00000
30.00000	32.00000	32.76800	34.36800	35.32800	38.88000	40.00000	40.96000
42.66000	44.73600	48.89600	50.00000	50.68800	51.84000	52.00000	54.00000
57.1429	62.20800	65.53600					

## Ordering Information

### VV-701- D A T - K N A B- 39M3216000

**Product**

VCXO, 5x7 Package

**Voltage Options**

D: +5 Vdc  
E: +3.3 Vdc

**Output**

A: CMOS

**Temp Range**

T: 0/70°C  
W: -10/70°C  
E: -40/85°C

Frequency in MHz

**Enable/Disable**

B: Pin 2  
E: Pin 5

**Enable/Disable**

A: Enable High  
E: Enable High, High Vc Impedance >2Mohm

**Temperature Stability (TPR Codes Only)**

E: ±20 ppm  
F: ±25 ppm  
K: ±50 ppm  
N: Undefined (APR code)

**Pull Range**

K: ±50ppm APR  
P: ±80ppm APR  
S: ±100ppm APR  
1: ±50ppm TPR  
2: ±100ppm TPR  
3: ±150ppm TPR

*\*Note: not all combination of options are available.  
Other specifications may be available upon request.*

**Example: VV-701-EAE-KNAB-51M8400000**

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Rev: 03/31/2010