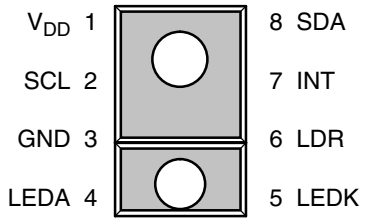
Features

- **Ambient Light Sensing, Proximity Detection, and IR LED in a Single Optical Module**
- **Ambient Light Sensing (ALS)**
  - **Approximates Human Eye Response**
  - **Programmable Analog Gain**
  - **Programmable Integration Time**
  - **Programmable Interrupt Function with Upper and Lower Threshold**
  - **Up to 16 Bits Resolution**
  - **Very High Sensitivity — Operates Behind Darkened Glass**
  - **Up to 1,000,000:1 Dynamic Range**
- **Proximity Detection**
  - **Calibrated to 100-mm Detection**
  - **Eliminates *Factory Calibration* of Prox**
  - **Programmable Number of IR Pulses**
  - **Programmable Current Sink for the IR LED — No Limiting Resistor Needed**
  - **Programmable Interrupt Function with Upper and Lower Threshold**
- **Programmable Wait Timer**
  - **Wait State — 65 μA Typical Current**
  - **Programmable from 2.72 ms to > 8 Seconds**

PACKAGE
MODULE–8
(TOP VIEW)



Package Drawing is Not to Scale

- **I²C Interface Compatible**
  - **Up to 400 kHz (I²C Fast Mode)**
- **Dedicated Interrupt Pin**
- **3.94 mm × 2.4 mm × 1.35 mm Package**
- **Sleep Mode — 2.5 μA Typical**

Applications

- **Cell Phone Backlight Dimming**
- **Cell Phone Touch Screen Disable**
- **Notebook/Monitor Security**
- **Automatic Speakerphone Enable**
- **Automatic Menu Popup**

Description

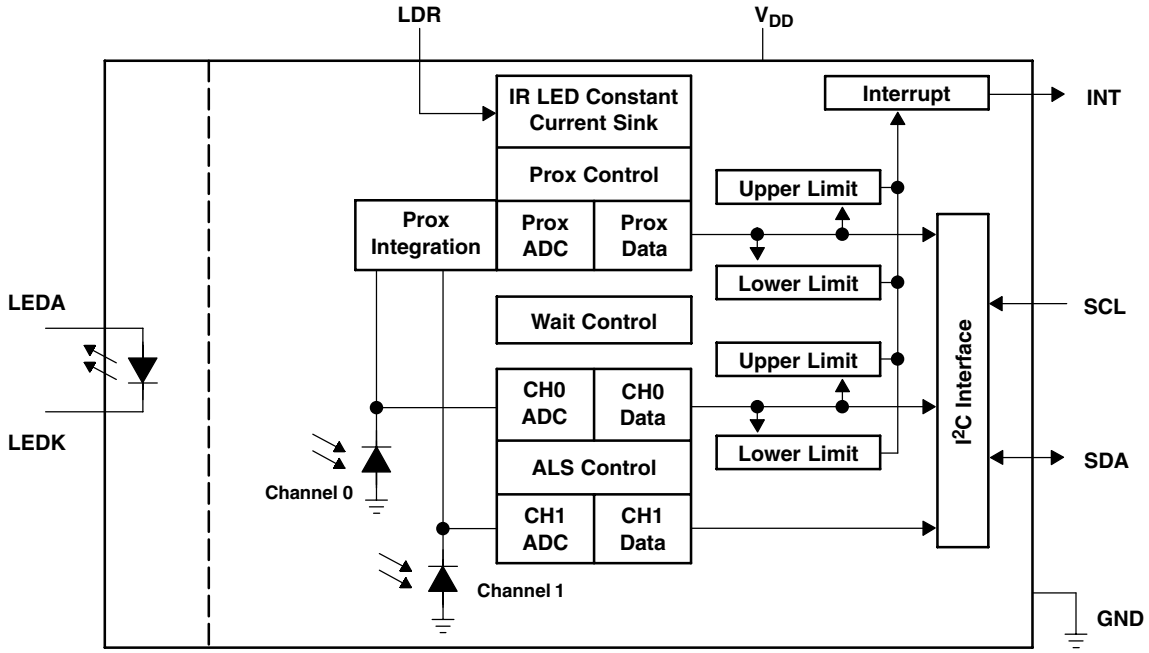
The TMD2771 family of devices provides digital ambient light sensing (ALS), a complete proximity detection system, and digital interface logic in a single 8-pin package. The proximity detector includes a digital proximity sensor, LED driver, and IR LED, which are trimmed to eliminate the need for end-equipment calibration due to component variations. Excellent background light rejection allows the device to operate in environments from sunlight to dark rooms. The wide dynamic range allows for operation in short distance detection such as a cell phone (behind dark glass). An internal state machine provides the ability to put the device into a low-power mode in between ALS and proximity measurements, providing very low average power consumption.

The device is particularly useful for display management with the purpose of extending battery life and providing optimum viewing in diverse lighting conditions. Display panel and keyboard backlighting can account for up to 30 to 40 percent of total platform power. The ALS features are ideal for use in notebook PCs, LCD monitors, flat-panel televisions, and cell phones.

The proximity function specifically targets near-field proximity applications. In cell phones, the proximity detection can detect when the user positions the phone close to their ear. The device is fast enough to provide proximity information at a high repetition rate needed when answering a phone call. This provides both improved *green* power saving capability and the added security to lock the computer when the user is not present. The addition of the micro-optics lenses within the device, provide highly efficient transmission and reception of infrared energy, which lowers overall power dissipation.

Texas Advanced Optoelectronic Solutions Inc.
1001 Klein Road • Suite 300 • Plano, TX 75074 • (972) 673-0759
www.taosinc.com

Functional Block Diagram



Detailed Description

The light-to-digital device provides on-chip photodiodes, integrating amplifiers, ADCs, accumulators, clocks, buffers, comparators, a state machine, and an I^2C interface. Each device combines one photodiode (CH0), which is responsive to both visible and infrared light, and a second photodiode (CH1), which is responsive primarily to infrared light. Two integrating ADCs simultaneously convert the amplified photodiode currents to a digital value providing up to 16-bits of resolution. Upon completion of the conversion cycle, the conversion result is transferred to the Ch0 and Ch1 data registers. This digital output can be read by a microprocessor where the luminance (ambient light level in lux) is derived using an empirical formula to approximate the human eye response.

A fully integrated proximity detection solution is provided with an 850-nm IR LED, LED driver circuit, and proximity detection engine. An internal LED driver (LDR) pin, is connected to the LED cathode (LEDK) to provide a factory calibrated proximity of 100 mm, ± 20 mm. This is accomplished with a proprietary current calibration technique that accounts for all variances in silicon, optics, package, and most important, IR LED output power. This eliminates or greatly reduces the need for factory calibration that is required for most discrete proximity sensor solutions. While the *device* is factory calibrated at a given pulse count, the number of proximity LED pulses can be programmed from 1 to 255 pulses, which allows different proximity distances to be achieved. Each pulse has a 16 µs period with a 7.2 µs on time.

Communication with the device is accomplished through a fast (up to 400 kHz), two-wire I^2C serial bus for easy connection to a microcontroller or embedded controller. The digital output of the device is inherently more immune to noise when compared to an analog photodiode interface.

The device provides a separate pin for level-style interrupts. When interrupts are enabled and a pre-set value is exceeded, the interrupt pin is asserted and remains asserted until cleared by the controlling firmware. The interrupt feature simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity or proximity value. An interrupt is generated when the value of an ALS or proximity conversion exceeds either an upper or lower threshold. In addition, a programmable interrupt persistence feature allows the user to determine how many consecutive exceeded thresholds are necessary to trigger an interrupt. Interrupt thresholds and persistence settings are configured independently for both ALS and proximity.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
GND	3		Power supply ground. All voltages are referenced to GND.
INT	7	O	Interrupt — open drain.
LDR	6	I	LED driver input for proximity IR LED, constant current source LED driver.
LEDA	4	I	LED anode.
LEDK	5	O	LED cathode. Connect to LDR pin when using internal LED driver circuit.
SCL	2	I	I^2C serial clock input terminal — clock signal for I^2C serial data.
SDA	8	I/O	I^2C serial data I/O terminal — serial data I/O for I^2C .
V_{DD}	1		Supply voltage.

Available Options

DEVICE	ADDRESS	PACKAGE – LEADS	INTERFACE DESCRIPTION	ORDERING NUMBER
TMD27711	0x39	Module–8	I^2C Vbus = V_{DD} Interface	TMD27711
TMD27713	0x39	Module–8	I^2C Vbus = 1.8 V Interface	TMD27713

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 3.8 V
Digital output voltage range, V_O . . . . . –0.5 V to 3.8 V
Digital output current, I_O . . . . . –1 mA to 20 mA
Analog voltage range, LDR . . . . . –0.5 V to 3.8 V
Storage temperature range, T_{stg} . . . . . –40°C to 85°C
ESD tolerance, human body model . . . . . 2000 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	2.6	3	3.6	V
Supply voltage accuracy, V_{DD} total error including transients	–3		3	%
Operating free-air temperature, T_A (Note 2)	–30		85	°C

NOTE 2: While the device is operational across the temperature range, functionality will vary with temperature. Specifications are stated only at 25°C unless otherwise noted.

Operating Characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	Active — ATIME = 100 ms		175	250	µA
		Wait mode		65		
		Sleep mode		2.5	4	
I_{DD}	Supply current — LDR pulse On			3		mA
V_{OL}	INT, SDA output low voltage	3 mA sink current	0		0.4	V
		6 mA sink current	0		0.6	
I_{LEAK}	Leakage current, SDA, SCL, INT pins		–5		5	µA
I_{LEAK}	Leakage current, LDR pin				10	µA
V_{IH}	SCL, SDA input high voltage	TMD27711	0.7 V_{DD}			V
		TMD27713	1.25			
V_{IL}	SCL, SDA input low voltage	TMD27711			0.3 V_{DD}	V
		TMD27713			0.54	

ALS Characteristics, V_{DD} = 3 V, T_A = 25°C, AGAIN = 16×, AEN = 1 (unless otherwise noted) (Note 1)

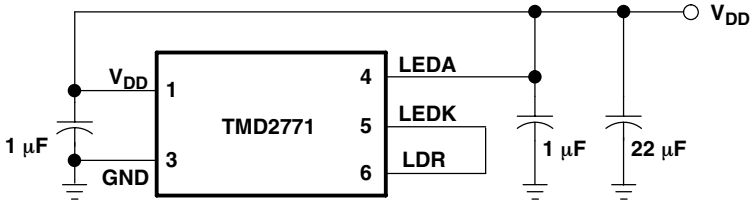
PARAMETER	TEST CONDITIONS	CHANNEL	MIN	TYP	MAX	UNIT
Dark ALS ADC count value	E_e = 0, AGAIN = 120×, ATIME = 0xDB (100 ms)	CH0	0	1	5	counts
		CH1	0	1	5	
ALS ADC integration time step size	ATIME = 0xFF		2.58	2.72	2.9	ms
ALS ADC Number of integration steps			1		256	steps
ADC counts per step	ATIME = 0xFF		0		1024	counts
ADC count value	ATIME = 0xC0		0		65535	counts
ALS ADC count value	λ_p = 625 nm, E_e = 60.5 µW/cm^2, ATIME = 0xF6 (27 ms) See note 2.	CH0	4000	5000	6000	counts
		CH1		790		
	λ_p = 850 nm, E_e = 82.7 µW/cm^2, ATIME = 0xF6 (27 ms) See note 3.	CH0	4000	5000	6000	
		CH1		2800		
ALS ADC count value ratio: CH1/CH0	λ_p = 625 nm, ATIME = 0xF6 (27 ms) See note 2.		10.8	15.8	20.8	%
	λ_p = 850 nm, ATIME = 0xF6 (27 ms) See note 3.		41	56	68	
R_e Irradiance responsivity	λ_p = 625 nm, ATIME = 0xF6 (27 ms) See note 2.	CH0		82.6		counts/(µW/cm^2)
		CH1		13.1		
	λ_p = 850 nm, ATIME = 0xF6 (27 ms) See note 3.	CH0		60.5		
		CH1		33.9		
Gain scaling, relative to 1× gain setting	8×		–10		10	%
	16×		–10		10	
	120×		–10		10	

NOTES: 1. Optical measurements are made using small-angle incident radiation from light-emitting diode optical sources. Visible 625 nm LEDs and infrared 850 nm LEDs are used for final product testing for compatibility with high-volume production.
2. The 625 nm irradiance E_e is supplied by an AlInGaP light-emitting diode with the following typical characteristics: peak wavelength λp = 625 nm and spectral halfwidth Δλ½ = 20 nm.
3. The 850 nm irradiance E_e is supplied by a GaAs light-emitting diode with the following typical characteristics: peak wavelength λp = 850 nm and spectral halfwidth Δλ½ = 42 nm.

Proximity Characteristics, V_{DD} = V_{LEDA} = 3 V, T_A = 25°C, PEN = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current — LDR pulse on			3		mA
	ADC conversion time step size	PTIME = 0xFF		2.72		ms
	ADC number of integration steps		1		256	steps
	ADC counts per step	PTIME = 0xFF	0		1023	counts
	Proximity IR LED pulse count		0		255	pulses
	Proximity pulse period			16.3		µs
I_{LEDA}	LED current @ V 600 mV, LDR pin sink (Note 1)	PDRIVE = 0 (100% current level)	75	100	150	mA
		PDRIVE = 1 (50% current level)		50		
		PDRIVE = 2 (25% current level)		25		
		PDRIVE = 3 (12.5% current level)		12.5		
T_{LDR}	On time per pulse	PDRIVE = 1		7.2		µs
	Proximity response, no target (offset)	PDRIVE = 0, PPULSE = 8 (Note 2)		100		counts
	Prox count, 100-mm target (Note 3)	73 mm × 83 mm, 90% reflective Kodak Gray Card, PPULSE = 8, PDRIVE = 0, PTIME = 0xFF (Note 4)	414	520	624	counts

NOTES: 1. Value is factory-adjusted to meet the Prox count specification. Considerable variation (relative to the typical value) is possible after adjustment.
2. No reflective surface above the module. Proximity offset varies with power supply characteristics and noise.
3. I_{LEDA} is factory calibrated to achieve this specification. Offset and crosstalk directly sum with this value and is system dependent.
4. No glass or aperture above the module. Tested value is the average of 5 consecutive readings.
5. These parameters are ensured by design and characterization and are not 100% tested.
6. Proximity test was done using the following circuit. See the **Application Information: Hardware** section for recommended application circuit.



IR LED Characteristics, V_{DD} = 3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_F	Forward Voltage	I_F = 20 mA		1.4	1.5	V
V_R	Reverse Voltage	I_R = 10 µA	5			V
P_O	Radiant Power	I_F = 20 mA	4.5			mW
λ_p	Peak Wavelength	I_F = 20 mA		850		nm
$\Delta\lambda$	Spectral Radiation Bandwidth	I_F = 20 mA		40		nm
T_R	Optical Rise Time	I_F = 100 mA, T_W = 125 ns, duty cycle = 25%		20	40	ns
T_F	Optical Fall Time	I_F = 100 mA, T_W = 125 ns, duty cycle = 25%		20	40	ns

Wait Characteristics, V_{DD} = 3 V, T_A = 25°C, WEN = 1 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Wait step size	WTIME = 0xFF		2.72	2.9	ms
Wait number of integration steps		1		256	steps

AC Electrical Characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER†		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SCL)}$	Clock frequency (I^2C only)		0		400	kHz
$t_{(BUF)}$	Bus free time between start and stop condition		1.3			µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.		0.6			µs
$t_{(SUSTA)}$	Repeated start condition setup time		0.6			µs
$t_{(SUSTO)}$	Stop condition setup time		0.6			µs
$t_{(HDDAT)}$	Data hold time		0			µs
$t_{(SUDAT)}$	Data setup time		100			ns
$t_{(LOW)}$	SCL clock low period		1.3			µs
$t_{(HIGH)}$	SCL clock high period		0.6			µs
t_F	Clock/data fall time				300	ns
t_R	Clock/data rise time				300	ns
C_i	Input pin capacitance				10	pF

† Specified by design and characterization; not production tested.

PARAMETER MEASUREMENT INFORMATION

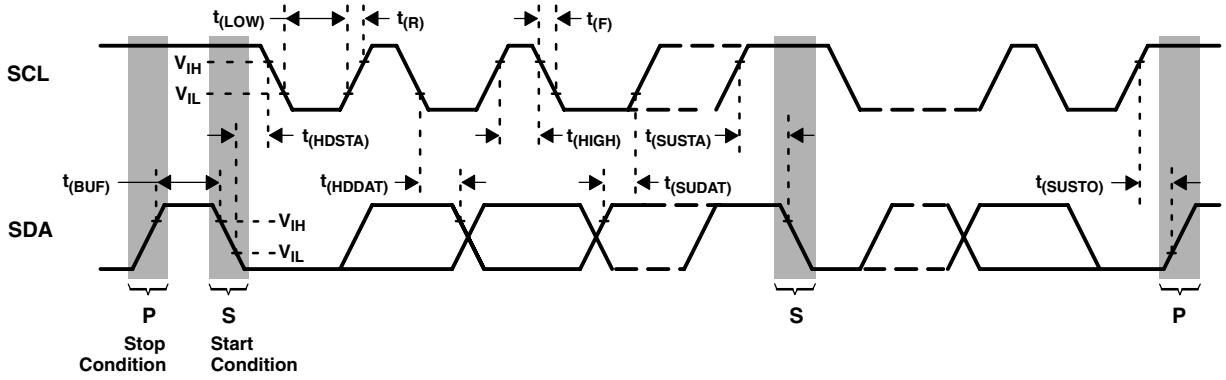


Figure 1. Timing Diagrams

TYPICAL CHARACTERISTICS

SPECTRAL RESPONSIVITY

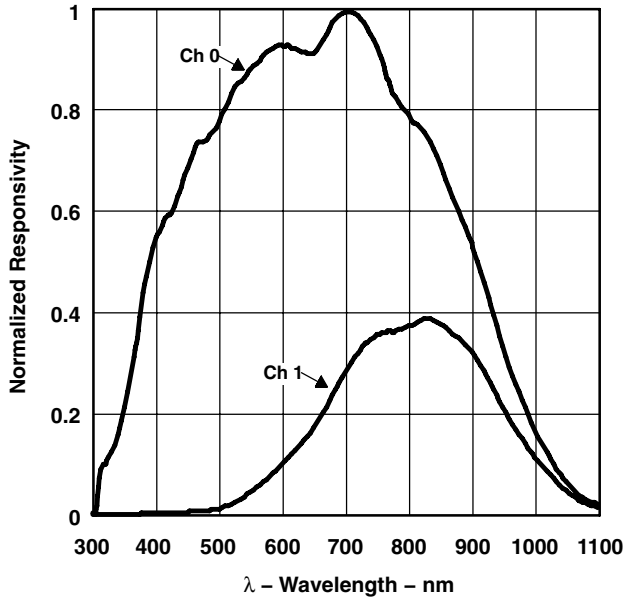


Figure 2

LDR OUTPUT COMPLIANCE

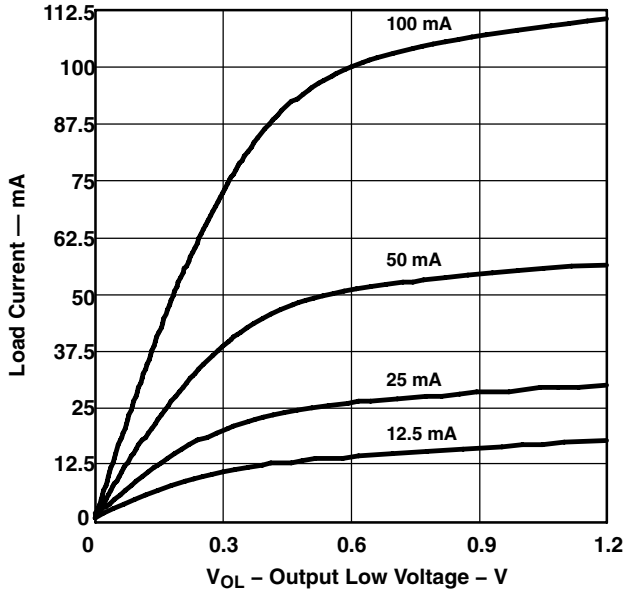


Figure 3

NORMALIZED I_{DD} vs. V_{DD} and TEMPERATURE

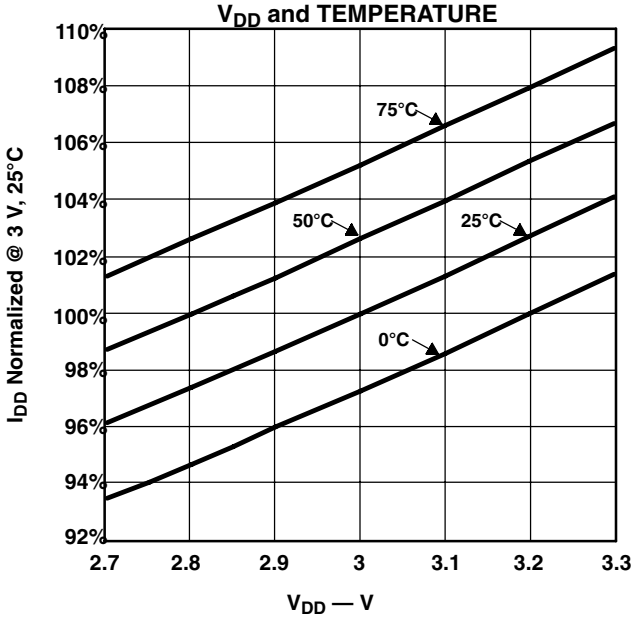


Figure 4

NORMALIZED RESPONSIVITY vs. ANGULAR DISPLACEMENT

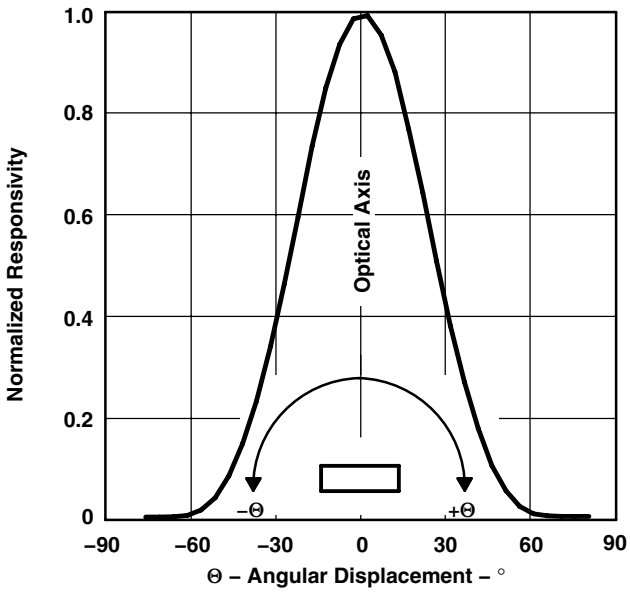


Figure 5

PRINCIPLES OF OPERATION

System State Machine

The device provides control of ALS, proximity detection and power management functionality through an internal state machine. After a power-on-reset, the device is in the sleep mode. As soon as the PON bit is set, the device will move to the start state. It will then continue through the Prox, Wait, and ALS states. If these states are enabled, the device will execute each function. If the PON bit is set to a 0, the state machine will continue until all conversions are completed and then go into a low-power sleep mode.

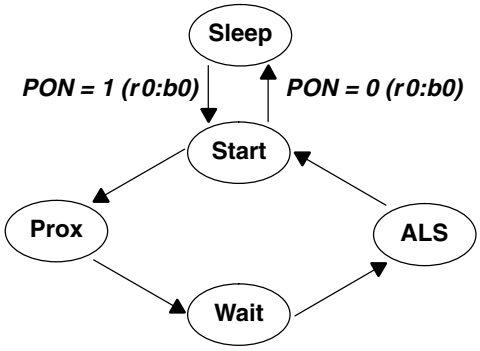


Figure 6. Simplified State Diagram

NOTE: In this document, the nomenclature uses the bit field name in italics followed by the register number and bit number to allow the user to easily identify the register and bit that controls the function. For example, the power on (PON) is in register 0, bit 0. This is represented as *PON (r0:b0)*.

Photodiodes

Conventional silicon detectors respond strongly to infrared light, which the human eye does not see. This can lead to significant error when the infrared content of the ambient light is high (such as with incandescent lighting) due to the difference between the silicon detector response and the brightness perceived by the human eye.

This problem is overcome through the use of two photodiodes. The Channel 0 photodiode is sensitive to both visible and infrared light, while the Channel 1 photodiode is sensitive primarily to infrared light. Two integrating ADCs convert the photodiode currents to digital outputs. The ADC digital outputs from the two channels are used in a formula to obtain a value that approximates the human eye response in units of lux.

ALS Operation

The ALS engine contains ALS gain control (AGAIN) and two integrating analog-to-digital converters (ADC) for the two photodiodes. The ALS integration time (ATIME) impacts both the resolution and the sensitivity of the ALS reading. Integration of both channels occurs simultaneously and upon completion of the conversion cycle, the results are transferred to the data registers (C0DATA and C1DATA). This data is also referred to as channel count. The transfers are double-buffered to ensure data integrity.

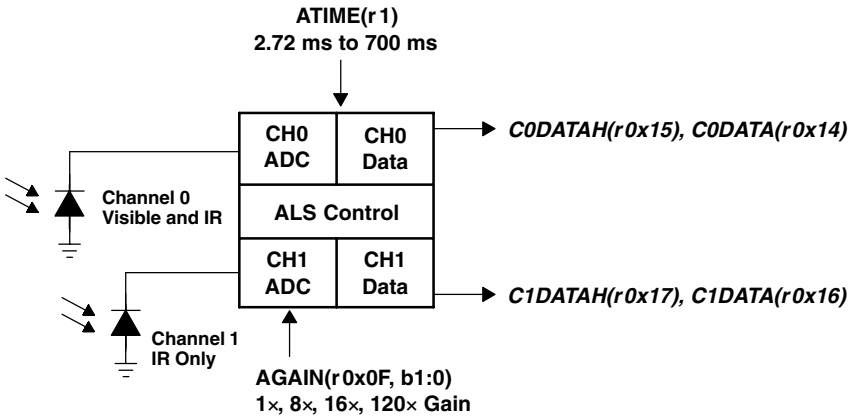


Figure 7. ALS Operation

The registers for programming the integration and wait times are a 2's compliment values. The actual time can be calculated as follows:

ATIME = 256 – Integration Time / 2.72 ms

Inversely, the time can be calculated from the register value as follows:

Integration Time = 2.72 ms × (256 – ATIME)

In order to reject 50/60-Hz ripple strongly present in fluorescent lighting, the integration time needs to be programmed in multiples of 10 / 8.3 ms or the half cycle time. Both frequencies can be rejected with a programmed value of 50 ms (ATIME = 0xED) or multiples of 50 ms (i.e. 100, 150, 200, 400, 700).

The registers for programming the AGAIN hold a two-bit value representing a gain of 1×, 8×, 16×, or 120×. The gain, in terms of amount of gain, will be represented by the value AGAINx, i.e. AGAINx = 1, 8, 16, or 120.

Lux Equation

The lux calculation is a function of CH0 channel count (C0DATA), CH1 channel count (C1DATA), ALS Gain (AGAINx), and ALS integration time in milliseconds (ATIME_ms). For a device in open air with no aperture or glass/plastic above the device, lux can be calculated using the following. If an aperture, glass/plastic, or a light pipe attenuates the light equally across the spectrum (300 nm to 1100 nm), then a scaling factor can be used (referred to as GA in the equation below). For open air with no aperture, GA = 1. If it is not spectrally flat, then a custom lux equation with new coefficients should be generated. (See TAOS application note.)

Counts per Lux (CPL) needs to be calculated only when ATIME or AGAIN is changed, otherwise it remains a constant. The first segment of the equation (Lux1) covers fluorescent and incandescent light. The second segment (Lux2) covers dimmed incandescent light. The final lux is the maximum of Lux1, Lux2, or 0.

CPL = (ATIME_ms × AGAINx) / (GA × 24)
Lux1 = (C0DATA – 2 × C1DATA) / CPL
Lux2 = (0.6 × C0DATA – C1DATA) / CPL
Lux = MAX(Lux1, Lux2, 0)

Proximity Detection

Proximity detection is accomplished by measuring the amount of IR energy, from the internal IR LED, reflected off an object to determine its distance. The internal proximity IR LED is driven by the integrated proximity LED current driver as shown in Figure 8.

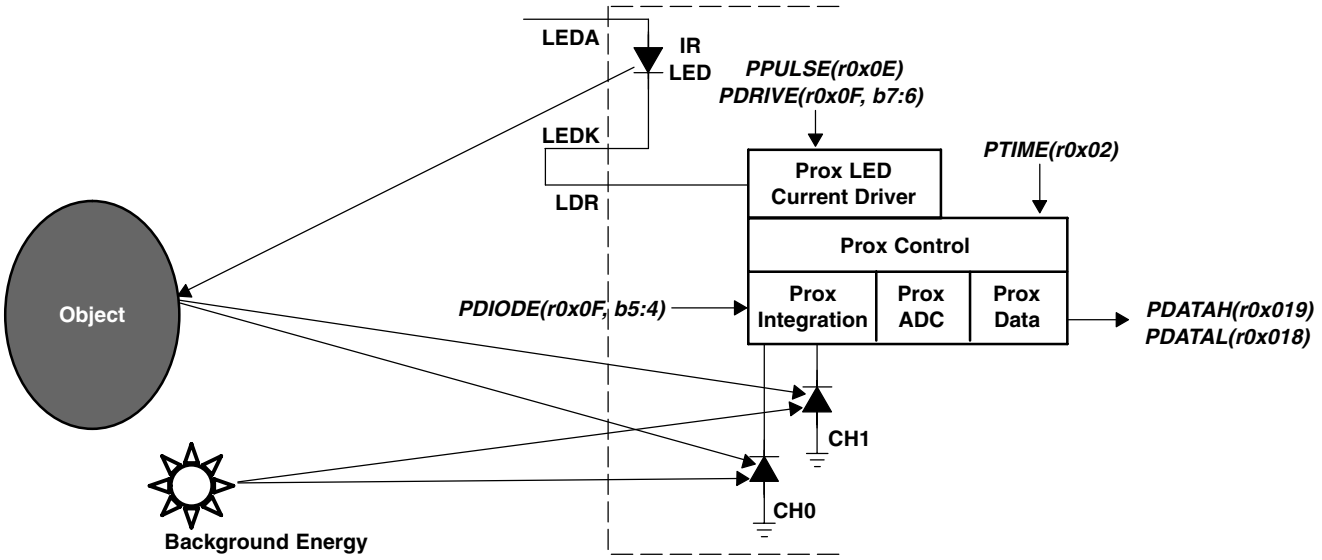


Figure 8. Proximity Detection

The LED current driver provides a regulated current sink on the LDR terminal that eliminates the need for an external current limiting resistor. The PDRIVE register setting sets the sink current to 100%, 50%, 25%, or 12.5% of the factory trimmed full scale current.

Referring to the Detailed State Machine figure, the LED current driver pulses the IR LED as shown in Figure 9 during the Prox Accum state. Figure 9 also illustrates that the LED On pulse has a fixed width of 7.3 μs and period of 16.0 μs. So, in addition to setting the proximity drive current, 1 to 255 proximity pulses (PPULSE) can be programmed. When deciding on the number of proximity pulses, keep in mind that the signal increases proportionally to PPULSE, while noise increases by the square root of PPULSE.

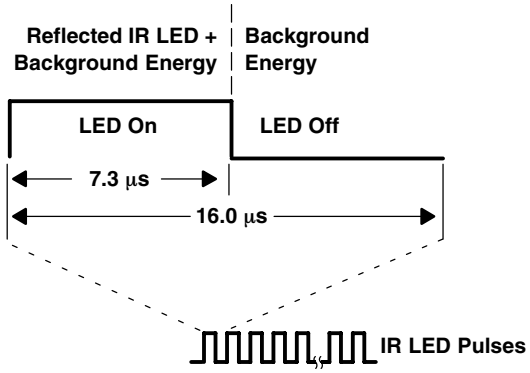


Figure 9. Proximity LED Current Driver Waveform

Figure 8 illustrates light rays emitting from the internal IR LED, reflecting off an object, and being absorbed by the CH0 and CH1 photodiodes. The proximity diode selector (PDIODE) determines which of the two photodiodes is used for a given proximity measurement. Note that neither photodiode is selected when the device first powers up, so PDIODE must be set for proximity detection to work.

Referring again to Figure 9, the reflected IR LED and the background energy is integrated during the LED On time, then during the LED Off time, the integrated background energy is subtracted from the LED On time energy, leaving the IR LED energy to accumulate from pulse to pulse.

After the programmed number of proximity pulses have been generated, the proximity ADC converts and scales the proximity measurement to a 16-bit value, then stores the result in two 8-bit proximity data (PDATAx) registers. ADC scaling is controlled by the proximity ADC conversion time (PTIME) which is programmable from 1 to 256 2.73-ms time units. However, depending on the application, scaling the proximity data will equally scale any accumulated noise. Therefore, in general, it is recommended to leave PTIME at the default value of one 2.73-ms ADC conversion time (0xFF).

For additional information on using the proximity detection function behind glass and for optical system design guidance, please see available TAOS application notes.

Optical Design Considerations

The TMD2771 device simplifies the optical system design by integrating an IR LED into the package, and also by providing an effective barrier between the LED and proximity sensor. In addition the package contains integrated lenses and apertures over both the LED and the sensor, which significantly extends the maximum proximity detection distance and helps to reduce optical crosstalk.

Although the package integrates an optical barrier between the IR LED and detector, placing the device behind a cover glass potentially provides another significant path for IR light to reach the detector, via reflection from the inside and outside faces of the cover glass. Because it is cost prohibitive to use anti-reflection coatings on the glass, the faces of the glass will reflect significantly (typically on the order of 4% of the light), and it is crucial that the system be designed so that this reflected light cannot find an efficient path back to the optical detector. See TAOS Application Note DN28: *Proximity Detection Behind Glass* for a detailed discussion of optical design considerations.

Interrupts

The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for a light intensity or proximity value. The interrupt mode is determined by the PIEN or AIEN field in the ENABLE register.

Four 16-bit-wide interrupt threshold registers allow the user to define thresholds above and below a desired light level. For ALS, an interrupt can be generated when the ALS C0DATA exceeds the upper threshold value (AIHTx) or falls below the lower threshold (AILTx). For proximity, an interrupt can be generated when the proximity data (PDATA) exceeds the upper threshold value (PIHTx) or falls below the lower threshold (PILTx).

To further control when an interrupt occurs, the device provides an interrupt persistence feature. This feature allows the user to specify a number of conversion cycles for which an event exceeding the ALS interrupt threshold must persist (APERS) or the proximity interrupt threshold must persist (PPERS) before actually generating an interrupt. Refer to the register descriptions for details on the length of the persistence.

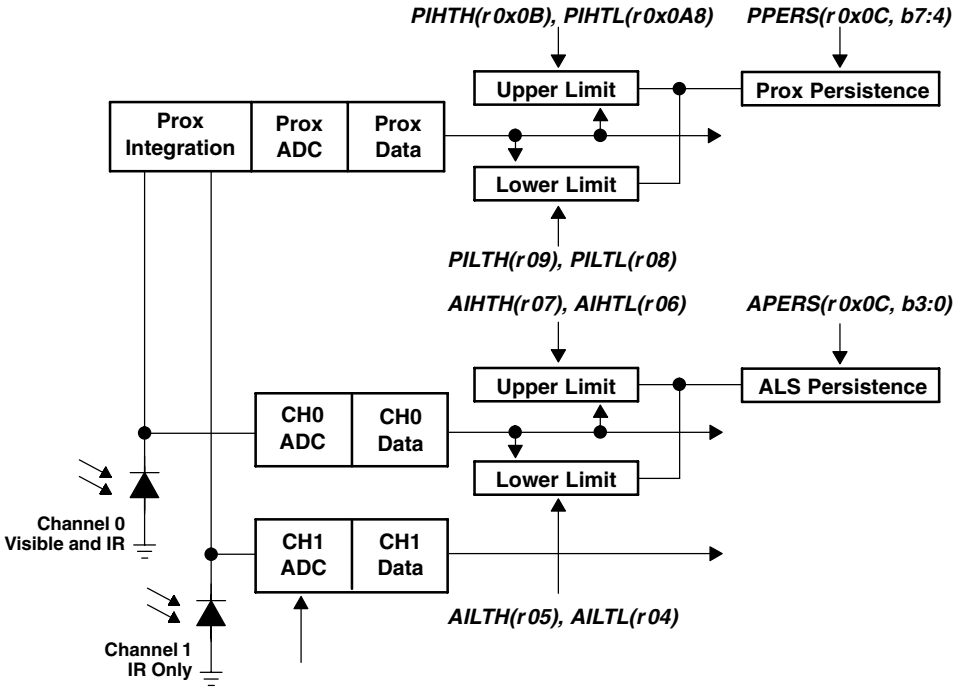


Figure 10. Programmable Interrupt

State Diagram

Figure 11 shows a more detailed flow for the state machine. The device starts in the sleep mode. The PON bit is written to enable the device. A 2.72-ms delay will occur before entering the start state. If the PEN bit is set, the state machine will step through the proximity states of proximity accumulate and then proximity ADC conversion. As soon as the conversion is complete, the state machine will move to the following state.

If the WEN bit is set, the state machine will then cycle through the wait state. If the WLONG bit is set, the wait cycles are extended by 12× over normal operation. When the wait counter terminates, the state machine will step to the ALS state.

The AEN should always be set, even in proximity-only operation. In this case, a minimum of 1 integration time step should be programmed. The ALS state machine will continue until it reaches the terminal count at which point the data will be latched in the ALS register and the interrupt set, if enabled.

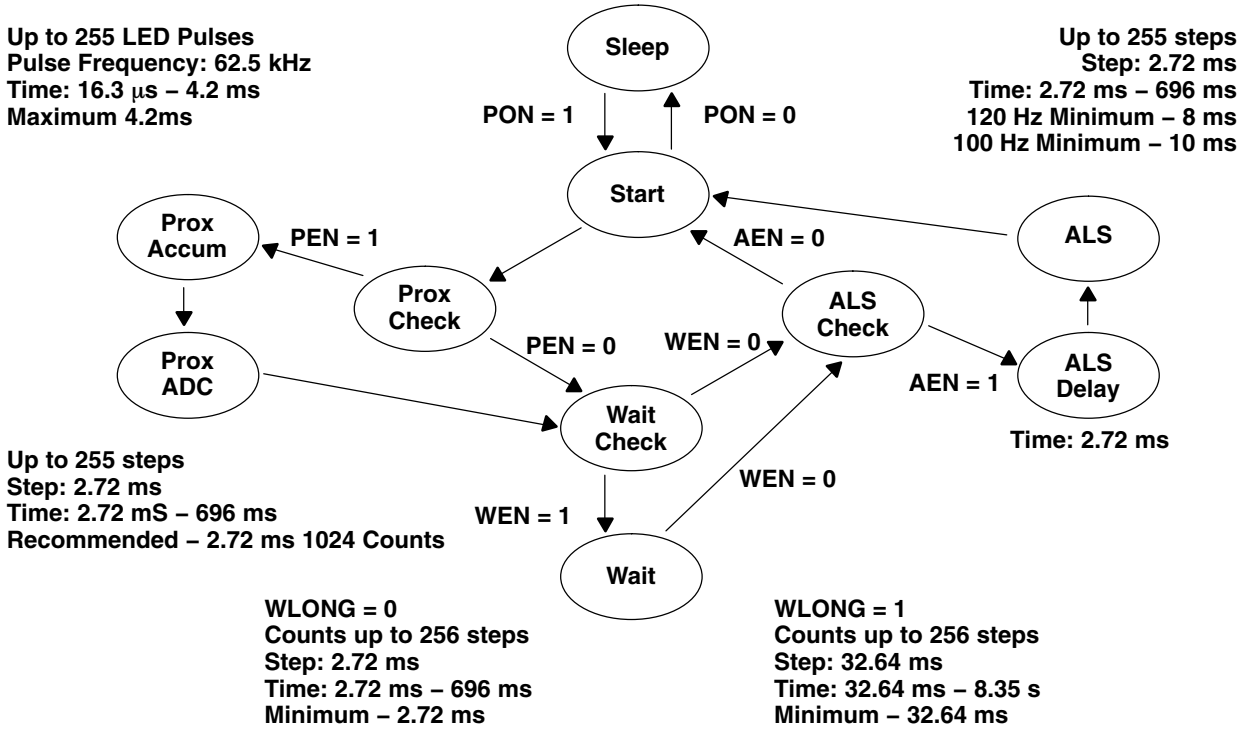
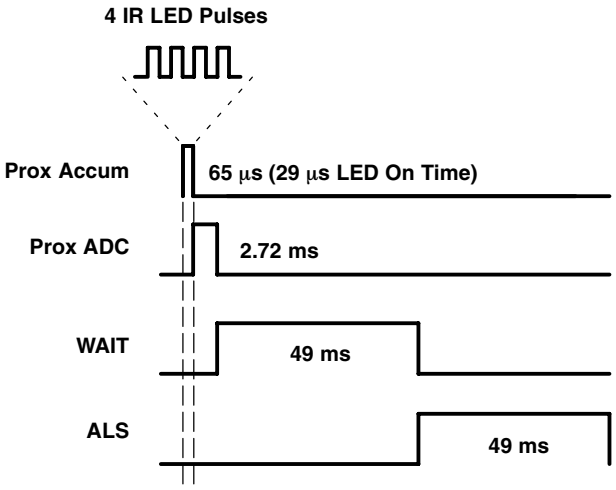


Figure 11. Expanded State Diagram

Power Management

Power consumption can be controlled through the use of the wait state timing because the wait state consumes only 65 μA of power. Figure 12 shows an example of using the power management feature to achieve an average power consumption of 151 μA current with four 100-mA pulses of proximity detection and 50 ms of ALS detection.



Example: ~100 ms Cycle TIme

State	Duration (ms)	Current (mA)
Prox Accum	0.065 (Note 1)	
LED On	0.029 (Note 2)	100.0
Prox ADC	2.72	0.175
Wait	49	0.065
ALS	49	0.175

Avg = ((0.029 × 100) + (2.72 × 0.175) + (49 × 0.065) + (49 × 0.175)) / 100 = 151 μA

Note 1: Prox Accum = 16.3 μs per pulse × 4 pulses = 65 μs = 0.065 ms

Note 2: LED On = 7.2 μs per pulse × 4 pulses = 29 μs = 0.029 ms

Figure 12. Power Consumption Calculations

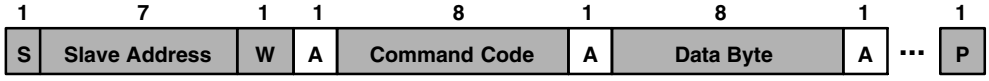
I²C Protocol

Interface and control are accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The device supports the 7-bit I²C addressing protocol.

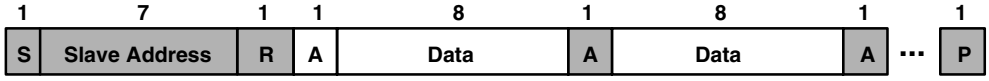
The I²C standard provides for three types of bus transaction: read, write, and a combined protocol (Figure 13). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at http://www.i2c–bus.org/references/.

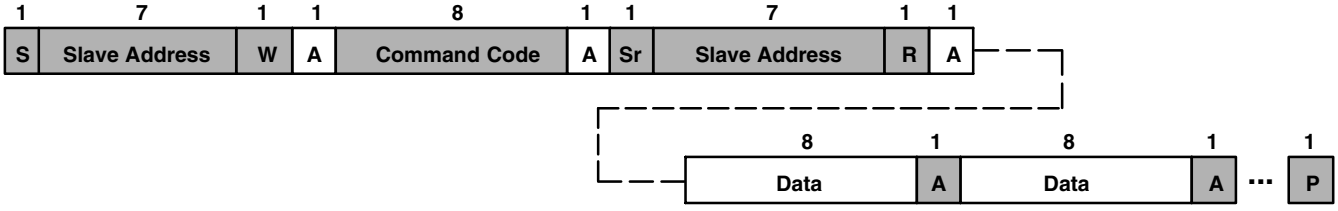
A Acknowledge (0)
N Not Acknowledged (1)
P Stop Condition
R Read (1)
S Start Condition
Sr Repeated Start Condition
W Write (0)
... Continuation of protocol
Master-to-Slave
Slave-to-Master



I²C Write Protocol



I²C Read Protocol



I²C Read Protocol — Combined Format

Figure 13. I²C Protocols

Register Set

The device is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Table 1.

Table 1. Register Address

ADDRESS	RESISTER NAME	R/W	REGISTER FUNCTION	RESET VALUE
––	COMMAND	W	Specifies register address	0x00
0x00	ENABLE	R/W	Enables states and interrupts	0x00
0x01	ATIME	R/W	ALS ADC time	0xFF
0x02	PTIME	R/W	Proximity ADC time	0xFF
0x03	WTIME	R/W	Wait time	0xFF
0x04	AILTL	R/W	ALS interrupt low threshold low byte	0x00
0x05	AILTH	R/W	ALS interrupt low threshold high byte	0x00
0x06	AIHTL	R/W	ALS interrupt high threshold low byte	0x00
0x07	AIHTH	R/W	ALS interrupt high threshold high byte	0x00
0x08	PILTL	R/W	Proximity interrupt low threshold low byte	0x00
0x09	PILTH	R/W	Proximity interrupt low threshold high byte	0x00
0x0A	PIHTL	R/W	Proximity interrupt high threshold low byte	0x00
0x0B	PIHTH	R/W	Proximity interrupt high threshold high byte	0x00
0x0C	PERS	R/W	Interrupt persistence filters	0x00
0x0D	CONFIG	R/W	Configuration	0x00
0x0E	PPULSE	R/W	Proximity pulse count	0x00
0x0F	CONTROL	R/W	Control register	0x00
0x12	ID	R	Device ID	ID
0x13	STATUS	R	Device status	0x00
0x14	C0DATA	R	CH0 ADC low data register	0x00
0x15	C0DATAH	R	CH0 ADC high data register	0x00
0x16	C1DATA	R	CH1 ADC low data register	0x00
0x17	C1DATAH	R	CH1 ADC high data register	0x00
0x18	PDATA	R	Proximity ADC low data register	0x00
0x19	PDATAH	R	Proximity ADC high data register	0x00

The mechanics of accessing a specific register depends on the specific protocol used. See the section on I^2C protocols on the previous pages. In general, the COMMAND register is written first to specify the specific control/status register for following read/write operations.

Command Register

The command registers specifies the address of the target register for future write and read operations.

Table 2. Command Register

	7	6	5	4	3	2	1	0	
COMMAND	**COMMAND**	**TYPE**		**ADD**					– –

FIELD	BITS	DESCRIPTION	
COMMAND	7	Select Command Register. Must write as 1 when addressing COMMAND register.	
TYPE	6:5	Selects type of transaction to follow in subsequent data transfers:	
		FIELD VALUE	**DESCRIPTION**
		00	Repeated byte protocol transaction
		01	Auto-increment protocol transaction
		10	Reserved — Do not use
		11	Special function — See description below
		Transaction type 00 will repeatedly read the same register with each data access. Transaction type 01 will provide an auto-increment function to read successive register bytes.	
ADD	4:0	Address register/special function register. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control-status-register for following write and read transactions:	
		FIELD VALUE	**DESCRIPTION**
		00000	Normal — no action
		00101	Proximity interrupt clear
		00110	ALS interrupt clear
		00111	Proximity and ALS interrupt clear
		other	Reserved — Do not write
		The ALS and Proximity Interrupt Clear clears any pending ALS/Proximity interrupt. This special function is self clearing.	

Enable Register (0x00)

The ENABLE register is used to power the device on/off, enable functions, and interrupts.

Table 3. Enable Register

	7	6	5	4	3	2	1	0	
ENABLE	Reserved		PIEN	AIEN	WEN	PEN	AEN	PON	Address 0x00

FIELD	BITS	DESCRIPTION
Reserved	7:6	Reserved. Write as 0.
PIEN	5	Proximity interrupt mask. When asserted, permits proximity interrupts to be generated.
AIEN	4	ALS interrupt mask. When asserted, permits ALS interrupts to be generated.
WEN	3	Wait Enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
PEN	2	Proximity enable. This bit activates the proximity function. Writing a 1 enables proximity. Writing a 0 disables proximity.
AEN	1	ALS Enable. This bit actives the two channel ADC. Writing a 1 activates the ALS. Writing a 0 disables the ALS.
PON [1, 2]	0	Power ON. This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator.

NOTES: 1. See Power Management section for more information.
2. A minimum interval of 2.72 ms must pass after PON is asserted before either a proximity or ALS can be initiated. This required time is enforced by the hardware in cases where the firmware does not provide it.

ALS Timing Register (0x01)

The ALS timing register controls the internal integration time of the ALS channel ADCs in 2.72 ms increments.

Table 4. ALS Timing Register

FIELD	BITS	DESCRIPTION			
		VALUE	INTEG_CYCLES	TIME	MAX COUNT
ATIME	7:0	0xFF	1	2.72 ms	1024
		0xF6	10	27.2 ms	10240
		0xDB	37	101 ms	37888
		0xC0	64	174 ms	65535
		0x00	256	696 ms	65535

Proximity Time Control Register (0x02)

The proximity timing register controls the integration time of the proximity ADC in 2.72 ms increments. It is recommended that this register be programmed to a value of 0xFF (1 integration cycle).

Table 5. Proximity Time Control Register

FIELD	BITS	DESCRIPTION			
PTIME	7:0	VALUE	INTEG_CYCLES	TIME	MAX COUNT
		0xFF	1	2.72 ms	1023

Wait Time Register (0x03)

Wait time is set 2.72 ms increments unless the WLONG bit is asserted in which case the wait times are 12× longer. WTIME is programmed as a 2's complement number.

Table 6. Wait Time Register

FIELD	BITS	DESCRIPTION			
WTIME	7:0	REGISTER VALUE	WAIT TIME	TIME (WLONG = 0)	TIME (WLONG = 1)
		0xFF	1	2.72 ms	0.032 sec
		0xB6	74	200 ms	2.4 sec
		0x00	256	700 ms	8.3 sec

NOTE: The Proximity Wait Time Register should be configured before PEN and/or AEN is/are asserted.

ALS Interrupt Threshold Registers (0x04 – 0x07)

The ALS interrupt threshold registers provides the values to be used as the high and low trigger points for the comparison function for interrupt generation. If C0DATA crosses below the low threshold specified, or above the higher threshold, an interrupt is asserted on the interrupt pin.

Table 7. ALS Interrupt Threshold Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
AILTL	0x04	7:0	ALS low threshold lower byte
AILTH	0x05	7:0	ALS low threshold upper byte
AIHTL	0x06	7:0	ALS high threshold lower byte
AIHTH	0x07	7:0	ALS high threshold upper byte

Proximity Interrupt Threshold Registers (0x08 – 0x0B)

The proximity interrupt threshold registers provide the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by proximity channel crosses below the lower threshold specified, or above the higher threshold, an interrupt is signaled to the host processor.

Table 8. Proximity Interrupt Threshold Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
PILTL	0x08	7:0	Proximity low threshold lower byte
PILTH	0x09	7:0	Proximity low threshold upper byte
PIHTL	0x0A	7:0	Proximity high threshold lower byte
PIHTH	0x0B	7:0	Proximity high threshold upper byte

Persistence Register (0x0C)

The persistence register controls the filtering interrupt capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after each ADC integration cycle or if the ADC integration has produced a result that is outside of the values specified by threshold register for some specified amount of time. Separate filtering is provided for proximity and ALS functions. ALS interrupts are generated using C0DATA.

Table 9. Persistence Register

	7	6	5	4	3	2	1	0	
PERS	PPERS				APERS				Address 0x0C

FIELD	BITS	DESCRIPTION		
PPERS	7:4	Proximity interrupt persistence. Controls rate of proximity interrupt to the host processor.		
		FIELD VALUE	MEANING	INTERRUPT PERSISTENCE FUNCTION
		0000	–––	Every proximity cycle generates an interrupt
		0001	1	1 proximity value out of range
		0010	2	2 consecutive proximity values out of range
		...	...	...
		1111	15	15 consecutive proximity values out of range
APERS	3:0	Interrupt persistence. Controls rate of interrupt to the host processor.		
		FIELD VALUE	MEANING	INTERRUPT PERSISTENCE FUNCTION
		0000	Every	Every ALS cycle generates an interrupt
		0001	1	1 value outside of threshold range
		0010	2	2 consecutive values out of range
		0011	3	3 consecutive values out of range
		0100	5	5 consecutive values out of range
		0101	10	10 consecutive values out of range
		0110	15	15 consecutive values out of range
		0111	20	20 consecutive values out of range
		1000	25	25 consecutive values out of range
		1001	30	30 consecutive values out of range
		1010	35	35 consecutive values out of range
		1011	40	40 consecutive values out of range
		1100	45	45 consecutive values out of range
		1101	50	50 consecutive values out of range
		1110	55	55 consecutive values out of range
		1111	60	60 consecutive values out of range

Configuration Register (0x0D)

The configuration register sets the wait long time.

Table 10. Configuration Register

	7	6	5	4	3	2	1	0	
CONFIG	Reserved						WLONG	Reserved	Address 0x0D

FIELD	BITS	DESCRIPTION
Reserved	7:2	Reserved. Write as 0.
WLONG	1	Wait Long. When asserted, the wait cycles are increased by a factor 12× from that programmed in the WTIME register.
Reserved	0	Reserved. Write as 0.

Proximity Pulse Count Register (0x0E)

The proximity pulse count register sets the number of proximity pulses that will be transmitted. When proximity detection is enabled, a proximity detect cycle occurs after each ALS cycle. PPULSE defines the number of pulses to be transmitted at a 62.5-kHz rate.

While the value can be programmed up to 255 pulses, the practical limit of the device is 32 pulses. It is recommended that 32 or fewer pulses be used to achieve maximum signal-to-noise ratio.

NOTE: The ATIME register will be used to time the interval between proximity detection events even if the ALS function is disabled.

Table 11. Proximity Pulse Count Register

	7	6	5	4	3	2	1	0	
PPULSE	PPULSE								Address 0x0E

FIELD	BITS	DESCRIPTION
PPULSE	7:0	Proximity Pulse Count. Specifies the number of proximity pulses to be generated.

Control Register (0x0F)

The Control register provides eight bits of miscellaneous control to the analog block. These bits typically control functions such as gain settings and/or diode selection.

Table 12. Control Register

	7	6	5	4	3	2	1	0	
CONTROL	PDRIVE		PDIODE		Reserved		AGAIN		Address 0x0F

FIELD	BITS	DESCRIPTION	
PDRIVE	7:6	LED Drive Strength.	
		FIELD VALUE	LED STRENGTH
		00	100%
		01	50%
		10	25%
		11	12.5%
PDIODE	5:4	Proximity Diode Select.	
		FIELD VALUE	DIODE SELECTION
		00	Reserved
		01	Proximity uses the Channel 0 diode
		10	Proximity uses the Channel 1 diode
		11	Proximity uses both diodes
Reserved	3:2	Reserved. Write bits as 0 (0:0)	
AGAIN	1:0	ALS Gain Control.	
		FIELD VALUE	ALS GAIN VALUE
		00	1× gain
		01	8× gain
		10	16× gain
		11	120× gain

NOTE: The PDRIVE values are relative to the factory-trimmed current necessary to meet the Prox Count specification shown on page 4.

ID Register (0x12)

The ID Register provides the value for the part number. The ID register is a read-only register.

Table 13. ID Register

	7	6	5	4	3	2	1	0	
ID	ID								Address 0x12

FIELD	BITS	DESCRIPTION	
ID	7:0	Part number identification	0x20 = TMD27711
			0x29 = TMD27713

Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

Table 14. Status Register

	7	6	5	4	3	2	1	0	
STATUS	Reserved		PINT	AINT	Reserved			AVALID	Address 0x13

FIELD	BIT	DESCRIPTION
Reserved	7:6	Reserved.
PINT	5	Proximity Interrupt. Indicates that the device is asserting a proximity interrupt.
AINT	4	ALS Interrupt. Indicates that the device is asserting an ALS interrupt.
Reserved	3:1	Reserved.
AVALID	0	ALS Valid. Indicates that the ALS channels have completed an integration cycle.

ADC Channel Data Registers (0x14 – 0x17)

ALS data is stored as two 16-bit values. To ensure the data is read correctly, a two-byte read I^2C transaction should be used with auto increment protocol bits set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored in a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Table 15. ADC Channel Data Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
C0DATA	0x14	7:0	ALS Channel 0 data low byte
C0DATAH	0x15	7:0	ALS Channel 0 data high byte
C1DATA	0x16	7:0	ALS Channel 1 data low byte
C1DATAH	0x17	7:0	ALS Channel 1 data high byte

Proximity Data Register (0x18 – 0x19h)

Proximity data is stored as a 16-bit value. To ensure the data is read correctly, a two-byte read I^2C transaction should be utilized with auto increment protocol bits set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if the next ADC cycle ends between the reading of the lower and upper registers.

Table 16. PDATA Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
PDATAL	0x18	7:0	Proximity data low byte
PDATAH	0x19	7:0	Proximity data high byte

APPLICATION INFORMATION: HARDWARE

LED Driver Pin with Proximity Detection

In a proximity sensing system, the included IR LED can be pulsed with more than 100 mA of rapidly switching current, therefore, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise coupled back into the device during the LED pulses. Averaging of multiple proximity samples is recommended to reduce the proximity noise.

The first recommendation is to use two power supplies; one for the device V_{DD} and the other for the IR LED. In many systems, there is a quiet analog supply and a noisy digital supply. By connecting the quiet supply to the V_{DD} pin and the noisy supply to the LEDA pin, the key goal can be met. Place a 1-μF low-ESR decoupling capacitor as close as possible to the V_{DD} pin and another at the LEDA pin, and a 22-μF capacitor at the output of the LED voltage regulator to supply the 100-mA current surge.

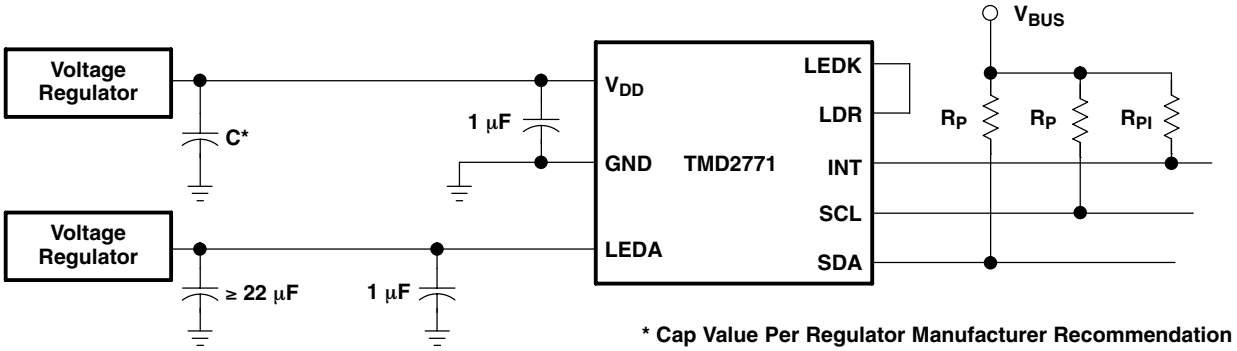


Figure 14. Proximity Sensing Using Separate Power Supplies

If it is not possible to provide two separate power supplies, the device can be operated from a single supply. A 22-Ω resistor in series with the V_{DD} supply line and a 1-μF low ESR capacitor effectively filter any power supply noise. The previous capacitor placement considerations apply.

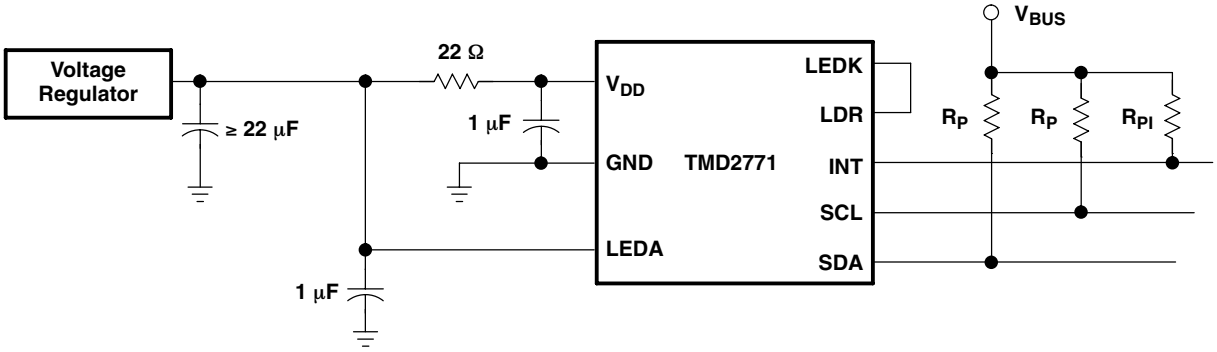


Figure 15. Proximity Sensing Using Single Power Supply

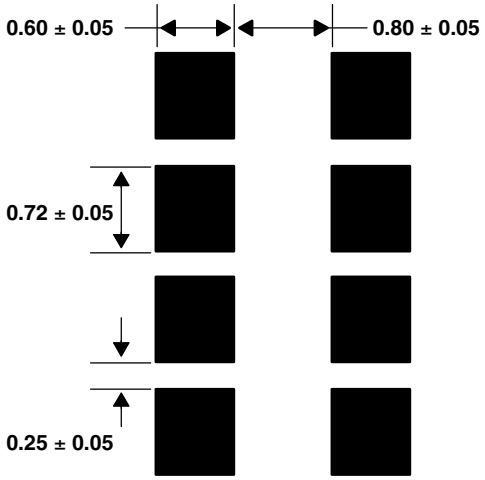
V_{BUS} in the above figures refers to the I^2C bus voltage which is either V_{DD} or 1.8 V. Be sure to apply the specified I^2C bus voltage shown in the Available Options table for the specific device being used.

The I^2C signals and the Interrupt are open-drain outputs and require pull–up resistors. The pull-up resistor (R_P) value is a function of the I^2C bus speed, the I^2C bus voltage, and the capacitive load. The TAOS EVM running at 400 kbps, uses 1.5-kΩ resistors. A 10-kΩ pull-up resistor (R_{PI}) can be used for the interrupt line.

APPLICATION INFORMATION: HARDWARE

PCB Pad Layout

Suggested PCB pad layout guidelines for the surface mount module are shown in Figure 16. Flash Gold is recommended surface finish for the landing pads.



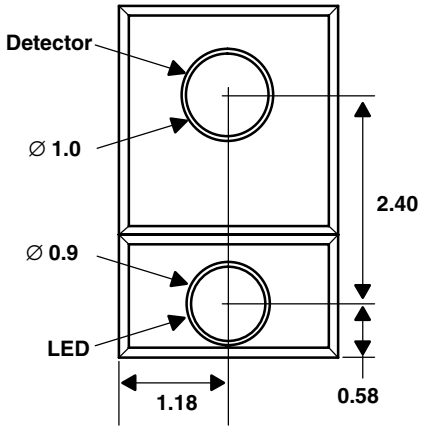
NOTES: A. All linear dimensions are in mm.
B. This drawing is subject to change without notice.

Figure 16. Suggested Module PCB Layout

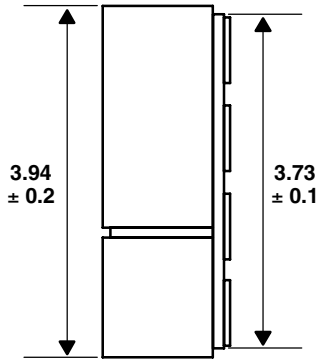
MECHANICAL DATA

MODULE **Dual Flat No-Lead**

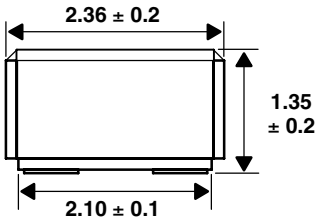
TOP VIEW



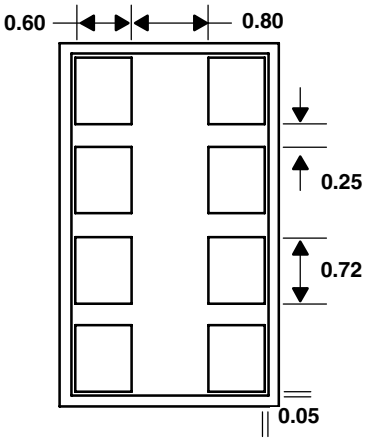
SIDE VIEW



END VIEW



BOTTOM VIEW



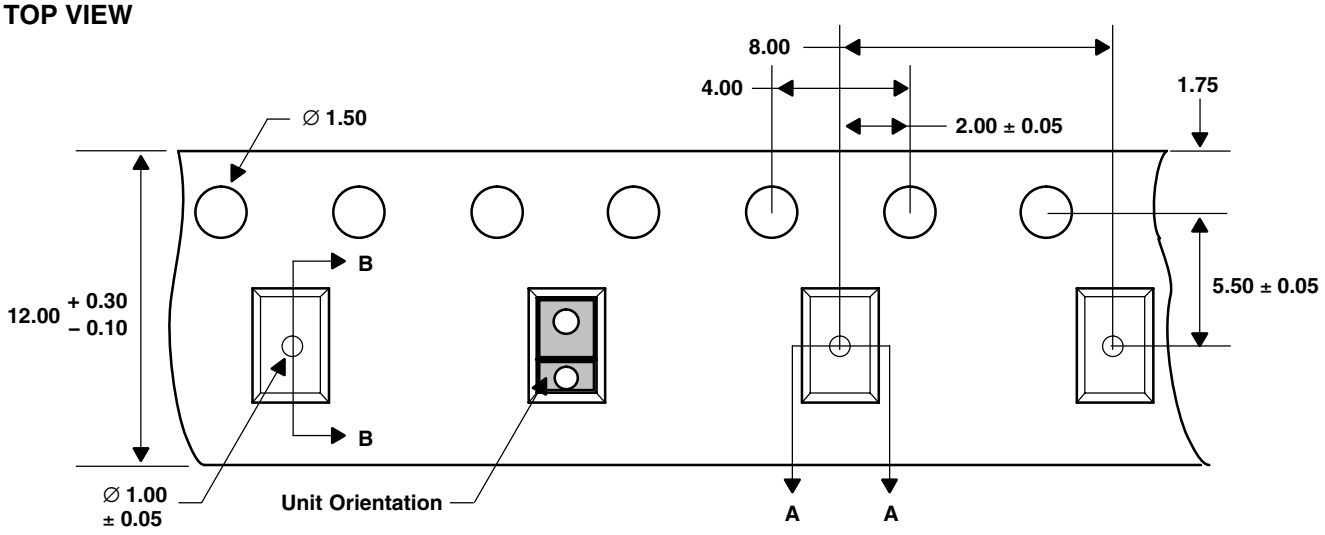
Lead Free

NOTES: A. All linear dimensions are in millimeters. Dimension tolerance is ± 0.05 mm unless otherwise noted.
B. Contacts are copper with NiPdAu plating.
C. This package contains no lead (Pb).
D. This drawing is subject to change without notice.

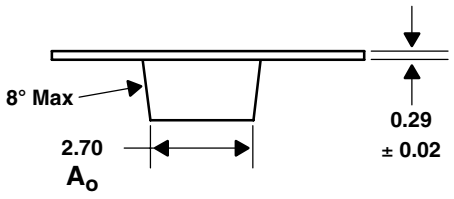
Figure 17. Module Packaging Configuration

MECHANICAL DATA

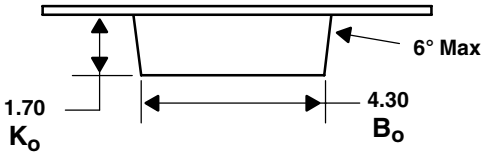
TOP VIEW



DETAIL A



DETAIL B



NOTES:
A. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
B. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
C. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481–B 2001.
D. Each reel is 330 millimeters in diameter and contains 2500 parts.
E. TAOS packaging tape and reel conform to the requirements of EIA Standard 481–B.
F. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
G. This drawing is subject to change without notice.

Figure 18. Module Carrier Tape

MANUFACTURING INFORMATION

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The process, equipment, and materials used in these test are detailed below.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Table 17. Solder Reflow Profile

PARAMETER	REFERENCE	DEVICE
Average temperature gradient in preheating		2.5°C/sec
Soak time	t_{soak}	2 to 3 minutes
Time above 217°C (T_1)	t_1	Max 60 sec
Time above 230°C (T_2)	t_2	Max 50 sec
Time above T_{peak} –10°C (T_3)	t_3	Max 10 sec
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max –5°C/sec

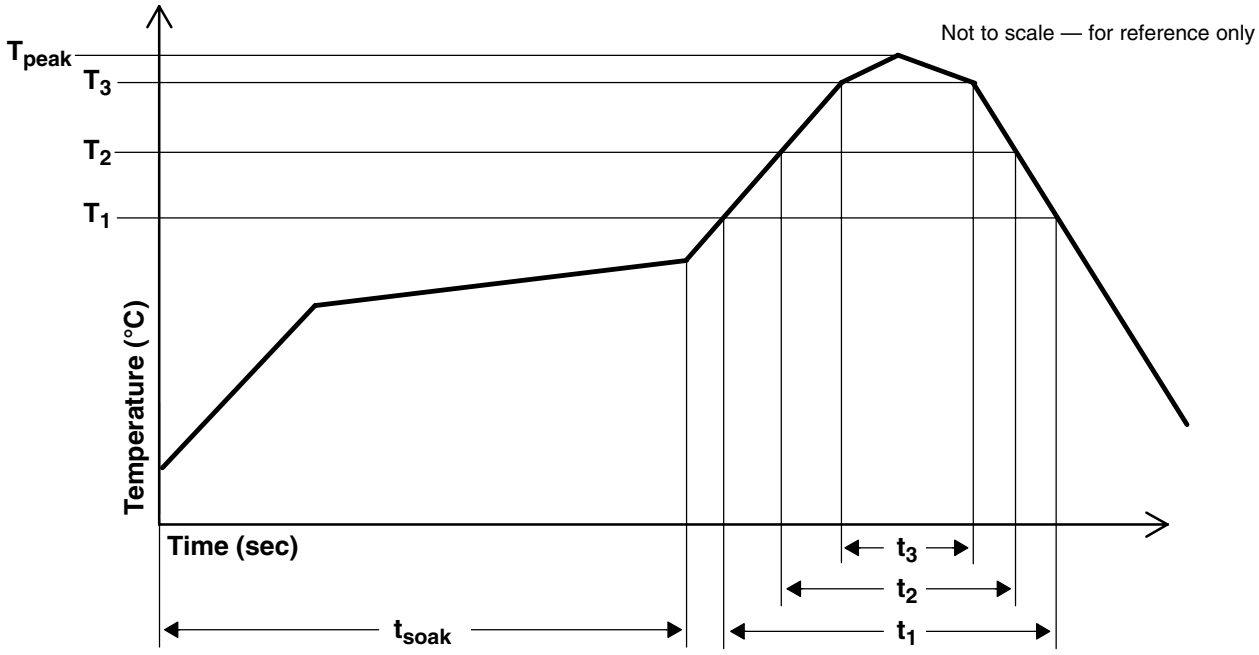


Figure 19. Solder Reflow Profile Graph

MANUFACTURING INFORMATION

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is dry-baked prior to being packed for shipping. Devices are packed in a sealed aluminized envelope called a moisture barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

The Moisture Barrier Bags should be stored under the following conditions:

Temperature Range	< 40°C
Relative Humidity	< 90%
Total Time	No longer than 12 months from the date code on the aluminized envelope if unopened.

Rebaking of the reel will be required if the devices have been stored unopened for more than 12 months and the Humidity Indicator Card shows the parts to be out of the allowable moisture region.

Opened reels should be used within 168 hours if exposed to the following conditions:

Temperature Range	< 30°C
Relative Humidity	< 60%

If rebaking is required, it should be done at 50°C for 12 hours.

The Module has been assigned a moisture sensitivity level of MSL 3.

PRODUCTION DATA — information in this document is current at publication date. Products conform to specifications in accordance with the terms of Texas Advanced Optoelectronic Solutions, Inc. standard warranty. Production processing does not necessarily include testing of all parameters.

LEAD-FREE (Pb-FREE) and GREEN STATEMENT

Pb-Free (RoHS) TAOS' terms *Lead-Free* or *Pb-Free* mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TAOS Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br) TAOS defines *Green* to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

Important Information and Disclaimer The information provided in this statement represents TAOS' knowledge and belief as of the date that it is provided. TAOS bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TAOS has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TAOS and TAOS suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

NOTICE

Texas Advanced Optoelectronic Solutions, Inc. (TAOS) reserves the right to make changes to the products contained in this document to improve performance or for any other purpose, or to discontinue them without notice. Customers are advised to contact TAOS to obtain the latest product information before placing orders or designing TAOS products into systems.

TAOS assumes no responsibility for the use of any products or circuits described in this document or customer product design, conveys no license, either expressed or implied, under any patent or other right, and makes no representation that the circuits are free of patent infringement. TAOS further makes no claim as to the suitability of its products for any particular purpose, nor does TAOS assume any liability arising out of the use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages.

TEXAS ADVANCED OPTOELECTRONIC SOLUTIONS, INC. PRODUCTS ARE NOT DESIGNED OR INTENDED FOR USE IN CRITICAL APPLICATIONS IN WHICH THE FAILURE OR MALFUNCTION OF THE TAOS PRODUCT MAY RESULT IN PERSONAL INJURY OR DEATH. USE OF TAOS PRODUCTS IN LIFE SUPPORT SYSTEMS IS EXPRESSLY UNAUTHORIZED AND ANY SUCH USE BY A CUSTOMER IS COMPLETELY AT THE CUSTOMER'S RISK.