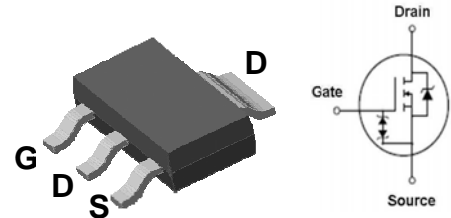


## Logic Level Gate Drive Application

### Features

- Logic level gate drive
- Max.  $R_{DS(ON)} = 135m\Omega$  at  $V_{GS} = 10V$ ,  $I_D = 0.5A$
- Low  $R_{DS(on)}$  provides higher efficiency
- ESD protected: 1000V (HBM  $\pm 500V$ )
- Halogen free and RoHS compliant device

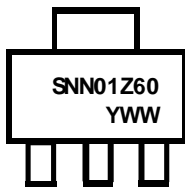


### Ordering Information

Part Number	Marking	Package
SNN01Z60Q	SNN01Z60	SOT-223

**SOT-223**

### Marking Information



Column 1: Device Code  
 Column 2: Production Information  
 e.g.) YWW  
 -. Y: Year Code  
 -. WW: Week Code

### Absolute maximum ratings ( $T_C=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	$V_{DSS}$	60	V	
Gate-source voltage	$V_{GSS}$	$\pm 20$	V	
Drain current (DC) *	$I_D$	$T_C=25^\circ C$	1	A
		$T_C=100^\circ C$	0.63	A
Drain current (Pulsed) *	$I_{DM}$	4	A	
Single pulsed avalanche energy <sup>(Note 2)</sup>	$E_{AS}$	35	mJ	
Repetitive avalanche current <sup>(Note 1)</sup>	$I_{AR}$	1	A	
Repetitive avalanche energy <sup>(Note 1)</sup>	$E_{AR}$	0.18	mJ	
Power dissipation	$P_D$	1.8	W	
Junction temperature	$T_J$	150	$^\circ C$	
Storage temperature range	$T_{stg}$	-55-150	$^\circ C$	

\* Limited only maximum junction temperature

## Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 69	°C/W

\* When mounted on the minimum pad size recommended (PCB).

## Electrical Characteristics ( $T_J=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	$BV_{DSS}$	$I_D=250\mu\text{A}$ , $V_{GS}=0\text{V}$	60	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$ , $V_{DS}=V_{GS}$	1	-	2.5	V
Drain-source cut-off current	$I_{DSS}$	$V_{DS}=60\text{V}$ , $V_{GS}=0\text{V}$	-	-	1	$\mu\text{A}$
Gate leakage current	$I_{GSS}$	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 20\text{V}$	-	-	$\pm 10$	$\mu\text{A}$
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=0.5\text{A}$	-	90	135	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$ , $I_D=0.5\text{A}$	-	109	165	$\text{m}\Omega$
Forward transfer conductance (Note 3)	$g_{fs}$	$V_{DS}=10\text{V}$ , $I_D=0.5\text{A}$	-	3	-	S
Input capacitance	$C_{iss}$	$V_{DS}=25\text{V}$ , $V_{GS}=0\text{V}$ , $f=1\text{MHz}$	-	314	-	pF
Output capacitance	$C_{oss}$		-	28	-	
Reverse transfer capacitance	$C_{rss}$		-	21	-	
Turn-on delay time (Note 3,4)	$t_{d(on)}$	$V_{DS}=30\text{V}$ , $I_D=1\text{A}$ , $R_G=25\Omega$	-	4.7	-	ns
Rise time (Note 3,4)	$t_r$		-	6.9	-	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		-	22.1	-	
Fall time (Note 3,4)	$t_f$		-	6.1	-	
Total gate charge (Note 3,4)	$Q_g$	$V_{DS}=48\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=1\text{A}$	-	8	10	nC
Gate-source charge (Note 3,4)	$Q_{gs}$		-	1.1	-	
Gate-drain charge (Note 3,4)	$Q_{gd}$		-	1.7	-	

## Source-Drain Diode Ratings and Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	$I_S$	Integral reverse diode in the MOSFET	-	-	1	A
Source current (Pulsed)	$I_{SM}$		-	-	4	A
Forward voltage	$V_{SD}$	$V_{GS}=0\text{V}$ , $I_S=1\text{A}$	-	-	1.2	V
Reverse recovery time (Note 3,4)	$t_{rr}$	$I_S=1\text{A}$ , $V_{GS}=0\text{V}$ $di_S/dt=-100\text{A}/\mu\text{s}$	-	25	-	ns
Reverse recovery charge (Note 3,4)	$Q_{rr}$		-	18.8	-	$\mu\text{C}$

Note:

1. Repeated rating: Pulse width limited by safe operating area
2.  $L=35\text{mH}$ ,  $I_{AS}=1\text{A}$ ,  $V_{DD}=50\text{V}$ ,  $R_G=25\Omega$ , Starting  $T_J=25^\circ\text{C}$
3. Pulse test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycles  $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

# Electrical Characteristics Curves

Fig. 1  $I_D - V_{DS}$

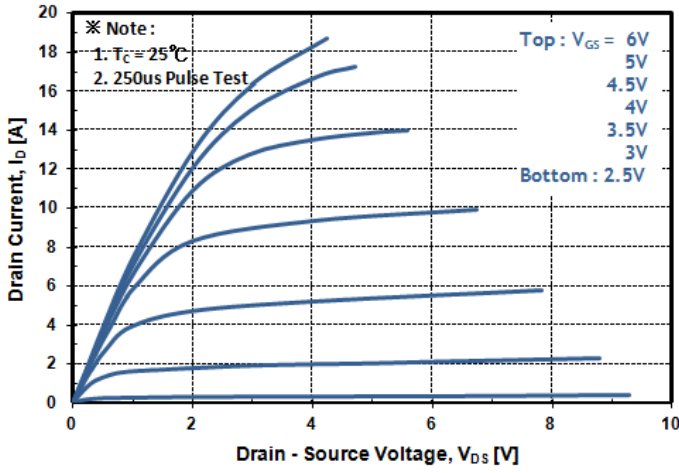


Fig. 2  $I_D - V_{GS}$

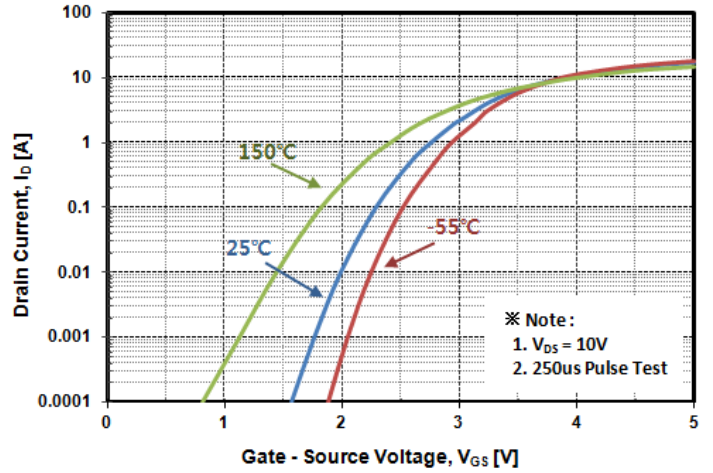


Fig. 3  $R_{DS(ON)} - I_D$

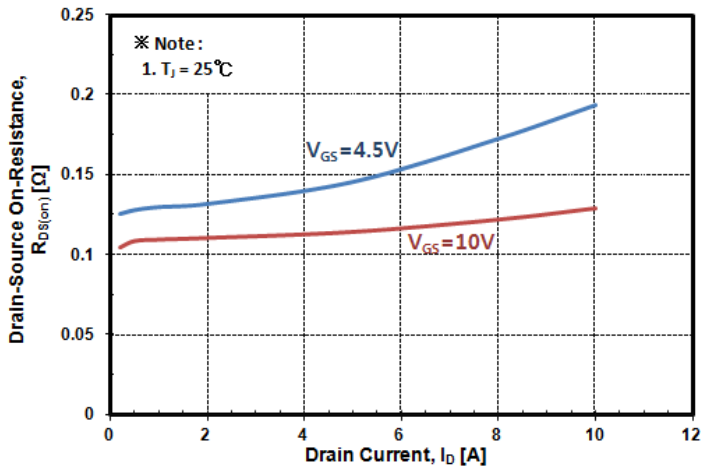


Fig. 4  $I_S - V_{SD}$

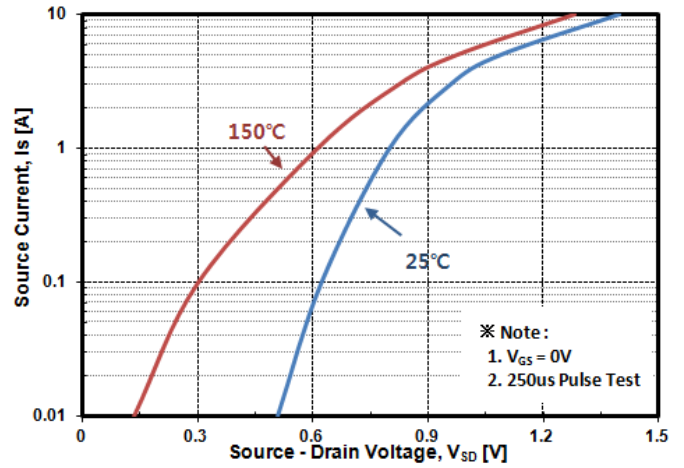


Fig. 5 Capacitance -  $V_{DS}$

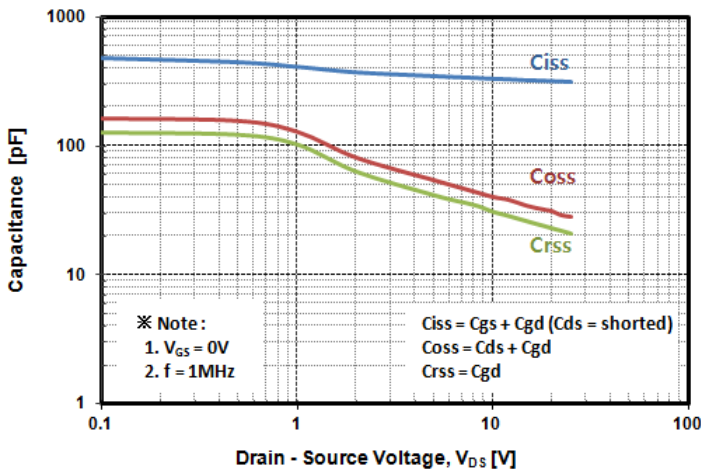


Fig. 6  $V_{GS} - Q_G$

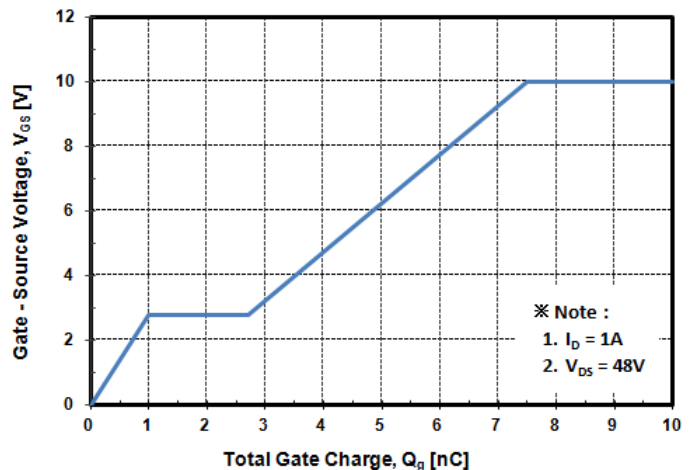


Fig. 7  $BV_{DSS} - T_J$

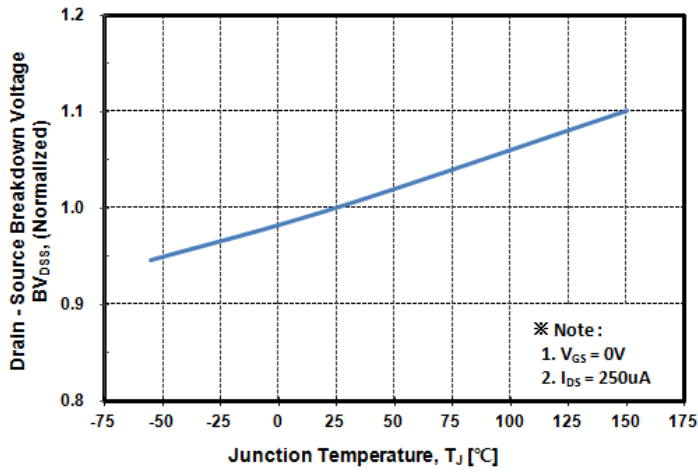


Fig. 8  $R_{DS(on)} - T_J$

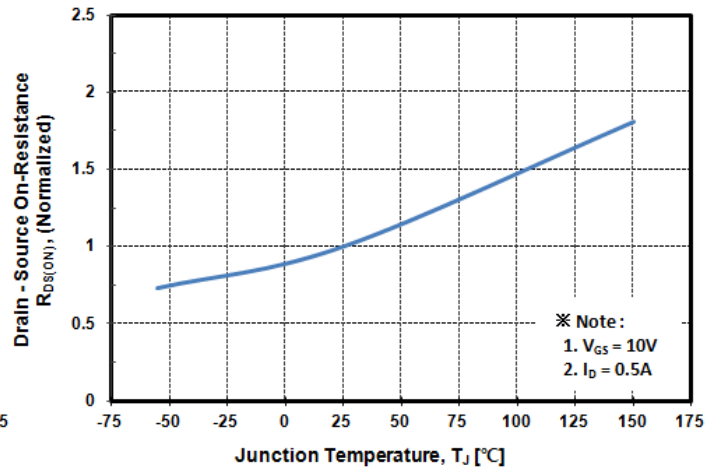


Fig. 9  $I_D - T_C$

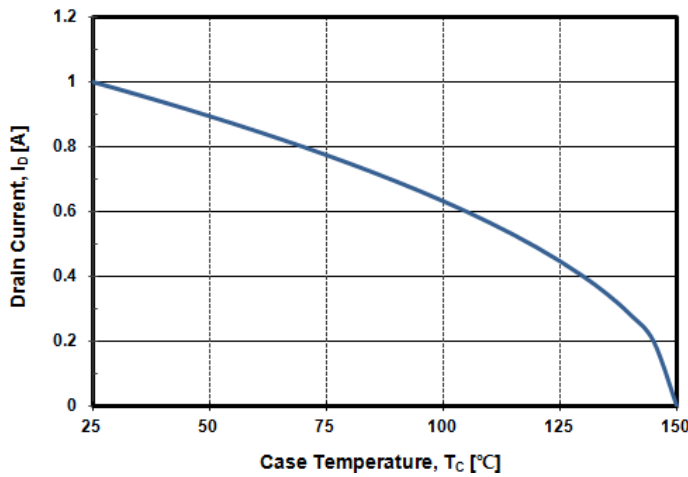


Fig. 10 Safe Operating Area

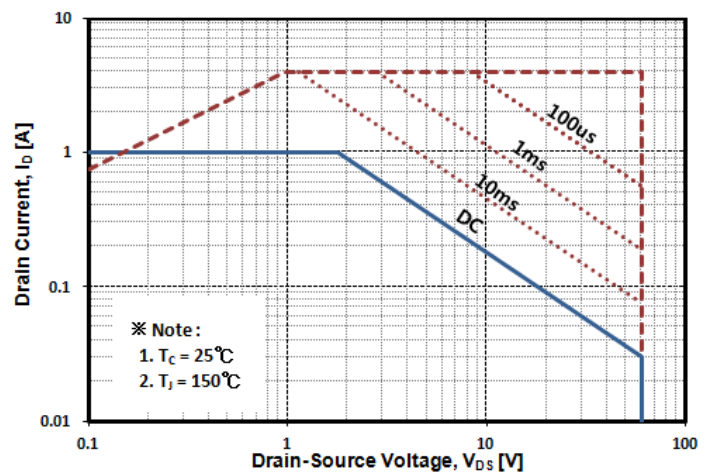


Fig. 11 Transient Thermal Impedance

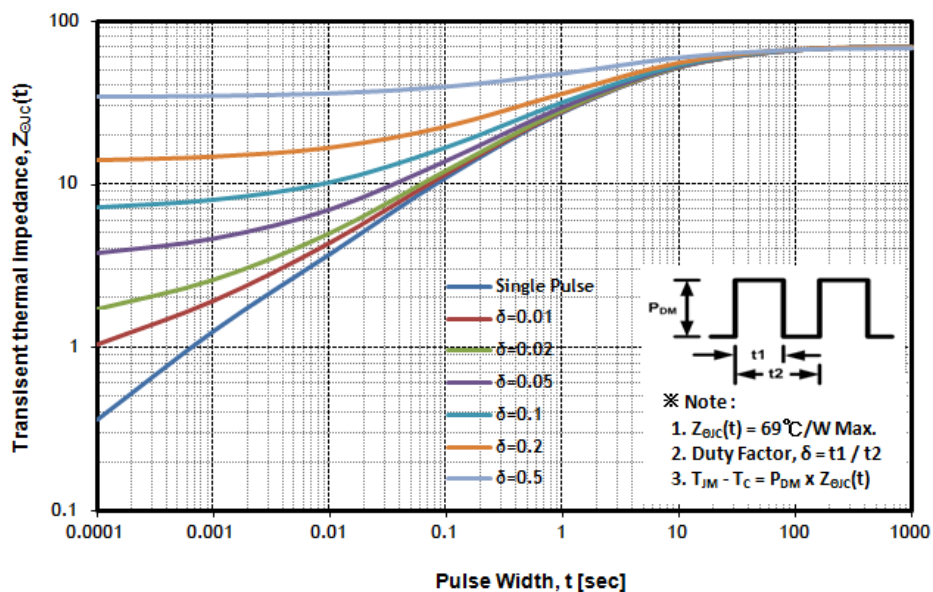


Fig. 12 Gate Charge Test Circuit & Waveform

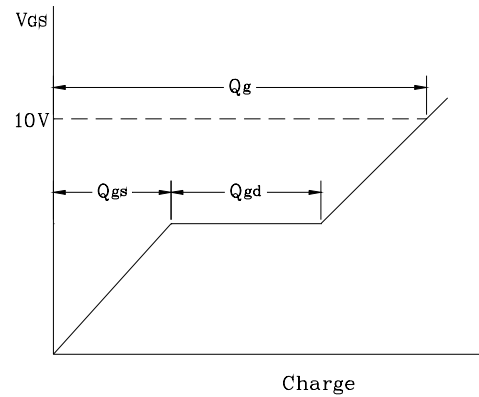
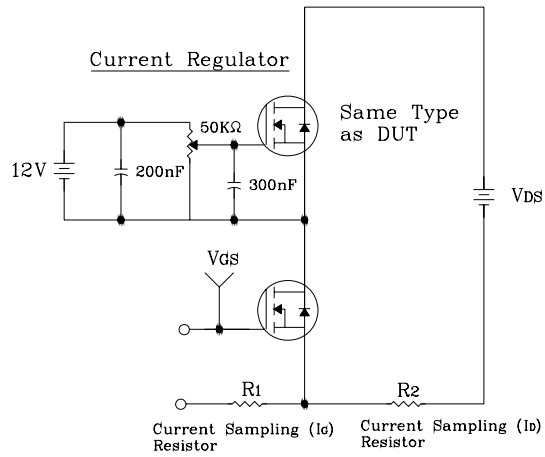


Fig. 13 Resistive Switching Test Circuit & Waveform

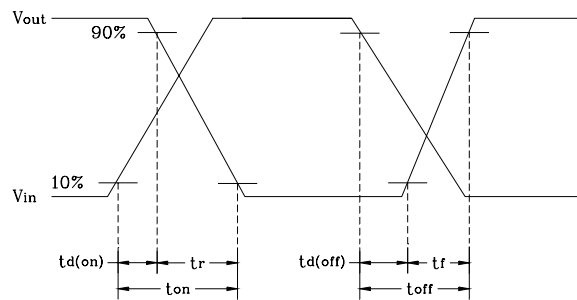
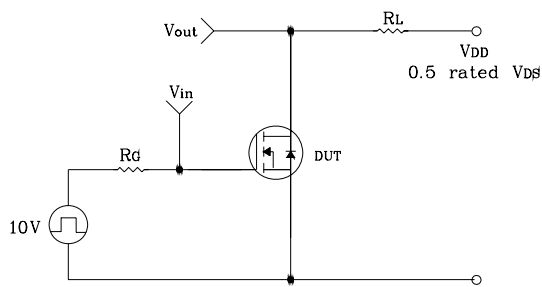


Fig. 14 E<sub>AS</sub> Test Circuit & Waveform

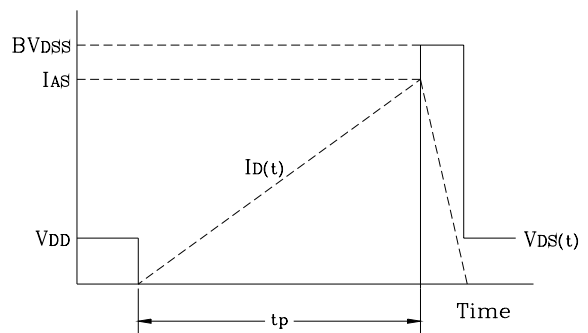
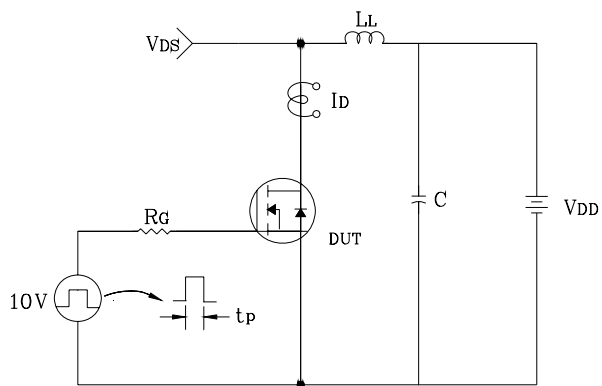
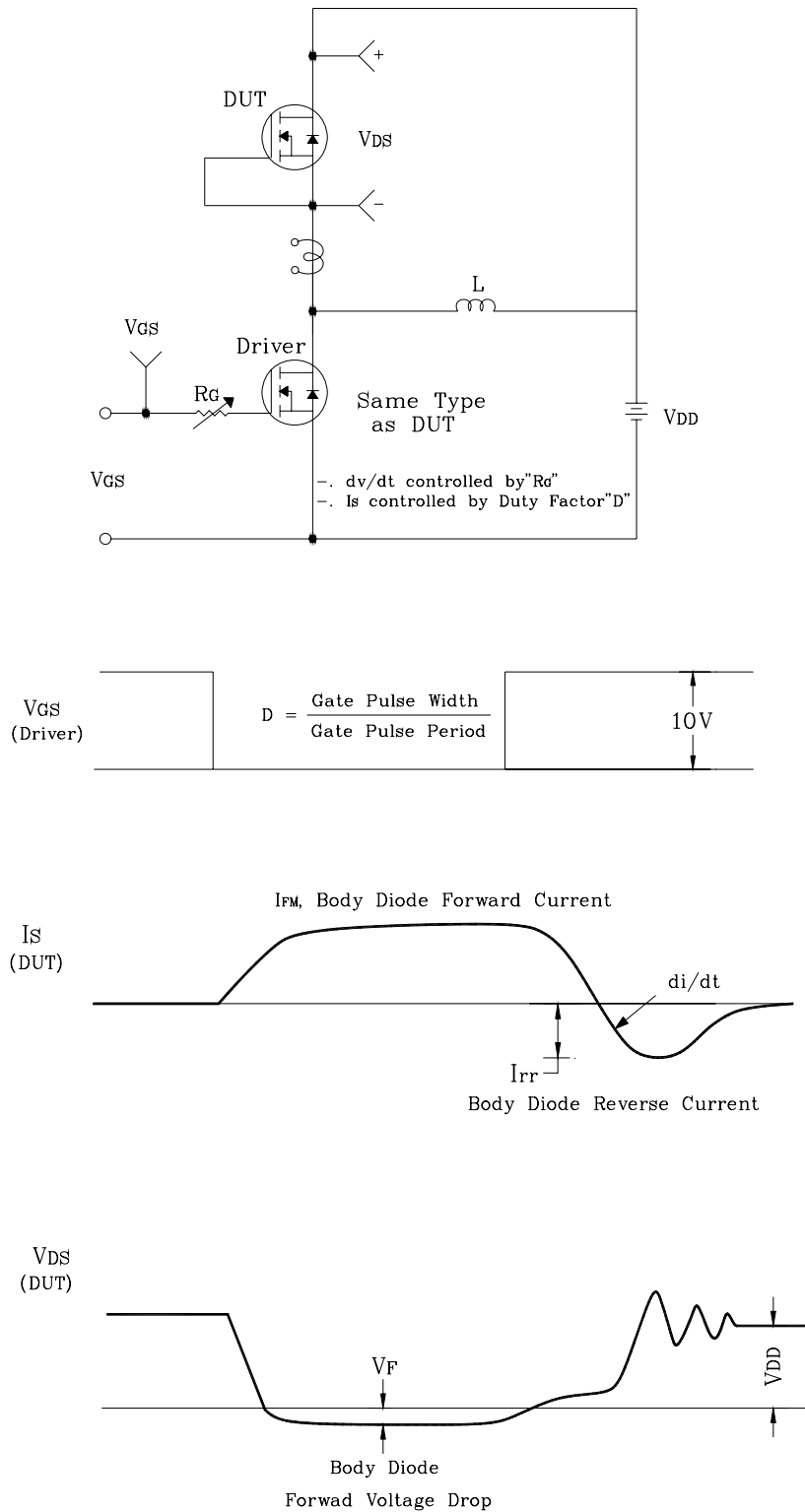
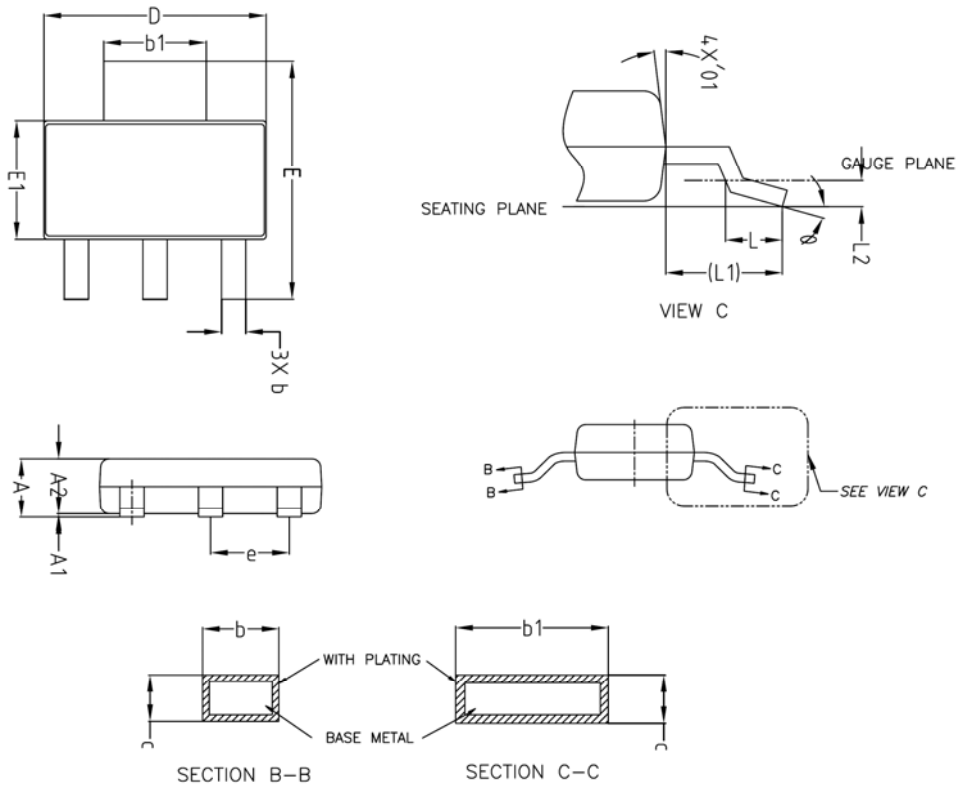


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform

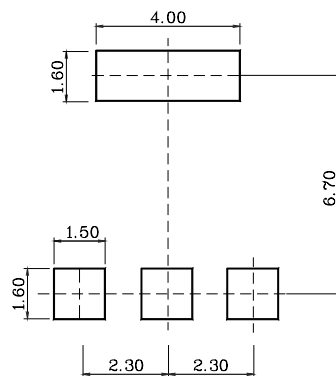


Package Outline Dimensions



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	—	—	1.80	
A1	0.00	—	0.10	
A2	1.60	1.65	1.70	
b	0.68	—	0.76	
b1	2.95	—	3.07	
c	0.23	—	0.28	
D	6.40	6.50	6.60	
E	6.80	7.00	7.20	
E1	3.40	3.50	3.60	
e	2.30 BSC			
L	0.45	—	0.65	
L1	1.75 REF			
L2	0.10 BSC			
$\theta$	0°	—	10°	
$\theta1$	5°	—	10°	

※ Recommended Land Pattern (unit: mm)



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