32Mbit, 3V Suspend/Resume, Dual/Quad-I/O Serial Flash Memory with 100MHz Uniform 4KB Sectors

Document Title

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Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	June 8, 2011	Preliminary
1.0	Final version release	July 18, 2011	Final
1.1	P.21: For instruction BB, remove mode bit function P.46: For SFDP, change data of byte 1E	August 29, 2011	
1.2	Add 8-pin DIP package type	16 September 2011	
1.3	Change t_{SE}(typ.) from 150ms to 80ms Change t_{SE}(max.) from 280ms to 200s Change t_{BE}(typ,) from 0.7s to 0.5s Change t_{CE}(typ.) from 40s to 32s	November 10, 2011	
1.4	P50: Change I_{CC6} & I_{CC7}(max.) from 15mA to 25mA	March 29, 2012	

A25LQ32A Series

32Mbit, 3V Suspend/Resume, Dual/Quad-I/O Serial Flash Memory with 100MHz Uniform 4KB Sectors

FEATURES

- Family of Serial Flash Memories
  - A25LQ32A: 32M-bit /4M-byte
- Flexible Sector Architecture with 4KB sectors
  - Sector Erase (4K-bytes) in 80ms (typical)
  - Block Erase (64K-bytes) in 0.5s (typical)
  - Program/Erase Suspend & Resume
- Page Program (up to 256 Bytes) in 1.5ms (typical)
- 2.7 to 3.6V Single Supply Voltage
- Dual input / output instructions resulting in an equivalent clock frequency of 200MHz:
  - FAST_READ_DUAL_OUTPUT Instruction
  - FAST_READ_DUAL_INPUT_OUTPUT Instruction
  - Dual Input Fast Program (DIFP) Instruction
- Quad input / output instructions resulting in an equivalent clock frequency of 400MHz:
  - FAST_READ_QUAD_ OUTPUT Instruction
  - FAST_READ_QUAD_INPUT_OUTPUT Instruction
  - Quad Input Fast Program (QIFP) Instruction
- SPI Bus Compatible Serial Interface
- 100MHz Clock Rate (maximum)
- Deep Power-down Mode 15μA (Max.)
- Advanced Protection Features
  - Software and Hardware Write-Protect
  - Top/Bottom, 4KB Complement Array Protection
- Additional 64-byte user-lockable, one-time programmable (OTP) area
- 32Mbit Flash memory
  - Uniform 4-Kbyte Sectors
  - Uniform 64-Kbyte Blocks
- Electronic Signatures
  - JEDEC Standard Two-Byte Signature
    A25LQ32A: (4016h)
  - RES Instruction, One-Byte, Signature, for backward compatibility
    A25LQ32A: (15h)
- Package options
  - 8-pin DIP (300mil), 8-pin SOP (209mil) and 8-pin WSON (6*5mm)
  - All Pb-free (Lead-free) products are RoHS compliant

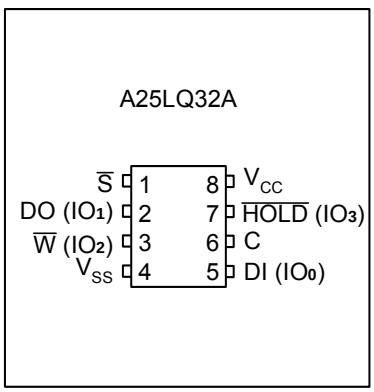
GENERAL DESCRIPTION

The A25LQ32A is 32M bit Serial Flash Memory, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus.

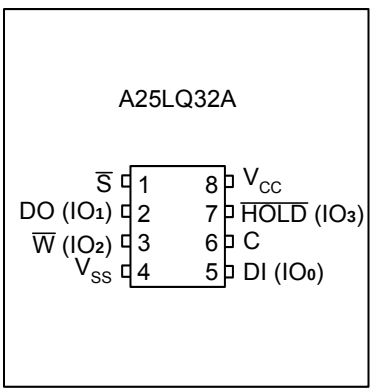
The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.
The memory is organized as 64 blocks, each containing 16 sectors. Each sector is composed of 16 pages. Each page is 256 bytes wide. Thus, the whole memory can be viewed as consisting of 16,384 pages, or 4,194,304 bytes.
The whole memory can be erased using the Chip Erase instruction, a block at a time, using Block Erase instruction, or a sector at a time, using the Sector Erase instruction.

Pin Configurations

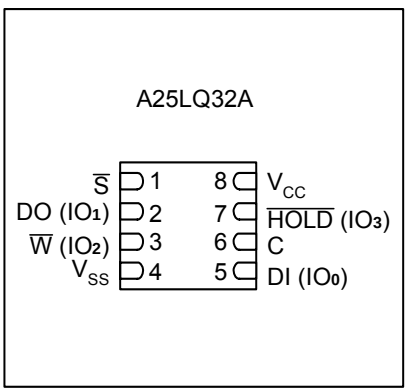
■ **DIP8 Connections**



■ **SOP8 Connections**



■ **WSON8 Connections**

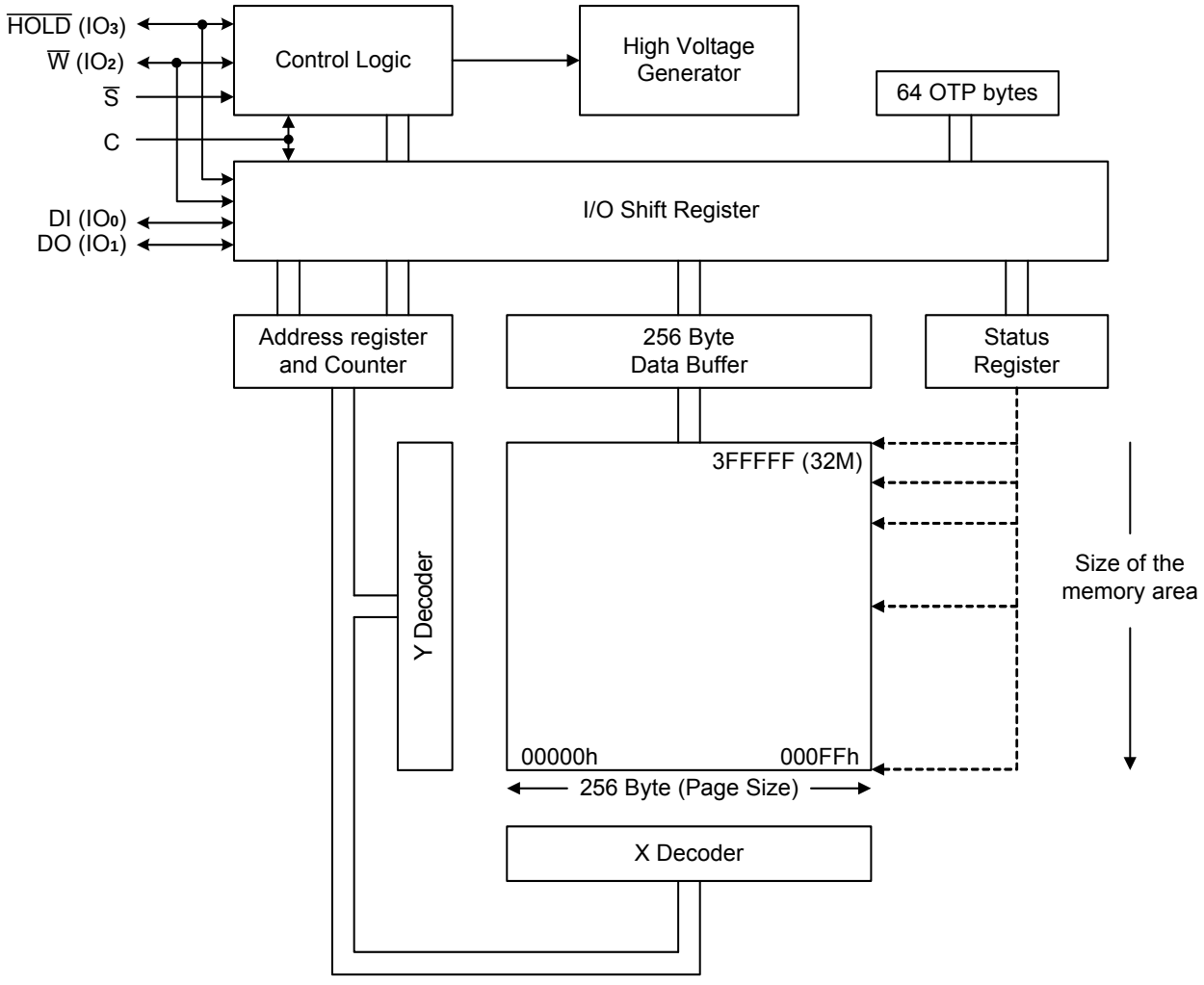


Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	$\overline{S}$	I	Chip Select Input
2	DO (IO_1)	I/O	Data Output (Data Input Output 1)(1)
3	$\overline{W}$ (IO_2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	V_{SS}		Ground
5	DI (IO_0)	I/O	Data Input (Data Input Output 0) (1)
6	C	I	Serial Clock Input
7	$\overline{HOLD}$ (IO_3)	I/O	Hold Input (Data Input Output 3) (2)
8	V_{CC}		Power Supply

Notes:
(1) IO_0 and IO_1 are used for Dual and Quad Instructions
(2) IO_0 ~ IO_3 are used for Quad Instructions

Block Diagram



PIN DESCRIPTION

Chip Select ($\overline{S}$)

The SPI Chip Select ($\overline{S}$) pin enables and disables device operation. When Chip Select ($\overline{S}$) is high the device is deselected and the Serial Data Output (DO, or IO_0, IO_1, IO_2, IO_3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress.

When Chip Select ($\overline{S}$) is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, Chip Select ($\overline{S}$) must transition from high to low before a new instruction will be accepted.

Serial Data Input, Output and IOs (DI, DO and IO_0, IO_1, IO_2, IO_3)

The A25LQ32A support standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (C) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of Serial Clock (C).

Dual and Quad SPI instruction use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of Serial clock (C) and read data or status from the device on the falling edge of Serial Clock (C).

Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1 the Write Protect ($\overline{W}$) pin becomes IO_2 and Hold ($\overline{HOLD}$) pin becomes IO_3.

Write Protect ($\overline{W}$)

The Write Protect ($\overline{W}$) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP1, SRP0) bits, a portion or the entire memory array can be hardware protected. The Write Protect ($\overline{W}$) pin is active low.

When the QE bit of Status Register-2 is set for Quad I/O, the Write Protect ($\overline{W}$) pin (Hardware Write Protect) function is not available since this pin is used for IO_2. See the Pin Configurations for Quad I/O operation.

Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) pin allows the device to be paused while it is actively selected. When Hold ($\overline{HOLD}$) pin is brought low, while Chip Select ($\overline{S}$) pin is low, the DO pin will be at high impedance and signals on the DI and Serial Clock (C) pins will be ignored (don't care). When Hold ($\overline{HOLD}$) pin is brought high, device operation can resume. The Hold function can be useful when multiple devices are sharing the same SPI signals. The Hold ($\overline{HOLD}$) pin is active low.

When the QE bit of Status Register-2 is set for Quad I/O. the Hold ($\overline{HOLD}$) pin function is not available since this pin is used for IO_3. See the Pin Configurations for Quad I/O operation.

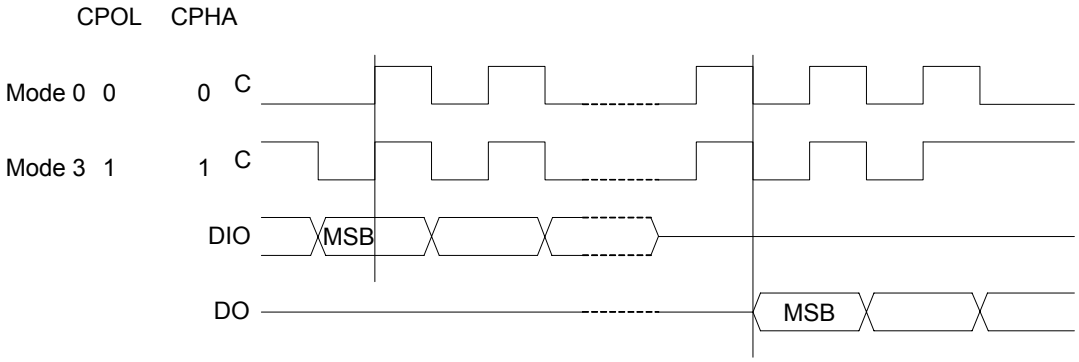
Serial Clock (C)

The SPI Serial Clock Input (C) pin provides the timing for serial input and output operations.

SPI MODES

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:
– CPOL=0, CPHA=0
– CPOL=1, CPHA=1
For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).
The difference between the two modes, as shown in Figure 1, is the clock polarity when the bus master is in Stand-by mode and not transferring data:
– C remains at 0 for (CPOL=0, CPHA=0) → Mode 0
– C remains at 1 for (CPOL=1, CPHA=1) → Mode 3

Figure 1. SPI Modes Supported



SPI OPERATIONS

Standard SPI Instructions

The A25LQ32A is accessed through an SPI compatible bus consisting of four signals: Serial Clock (C), Chip Select ($\overline{S}$), Serial Data Input (DI), and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of Serial Clock (C). The DO output pin is used to read data or status from the device on the falling edge of Serial Clock (C).

Dual SPI Instructions

The A25LQ32A supports Dual SPI operation when using the "FAST_READ_DUAL_OUTPUT and FAST_READ_DUAL_INPUT_OUTPUT" (3B and BB hex) instructions. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions the DI and DO pins become bidirectional I/O pins; IO_0 and IO_1.

Quad SPI Instructions

The A25LQ32A supports Quad SPI operation when using the "FAST_READ_QUAD_OUTPUT" (6B hex) and "FAST_READ_QUAD_INPUT_OUTPUT" (EB hex) instructions. This instruction allows data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. These 2 instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bi-directional IO_0 and IO_1, and the $\overline{W}$ and $\overline{HOLD}$ pins become IO_2 and IO_3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

Hold Condition

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence. However, taking this signal Low does not terminate any Write Status Register, Program or Erase cycle that is currently in progress. The $\overline{HOLD}$ function is only available for standard SPI and Dual SPI operation, not during Quad SPI.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) Low.

The Hold condition starts on the falling edge of the Hold ($\overline{HOLD}$) signal, provided that this coincides with Serial Clock (C) being Low (as shown in Figure 2.).

The Hold condition ends on the rising edge of the Hold ($\overline{HOLD}$) signal, provided that this coincides with Serial Clock (C) being Low.

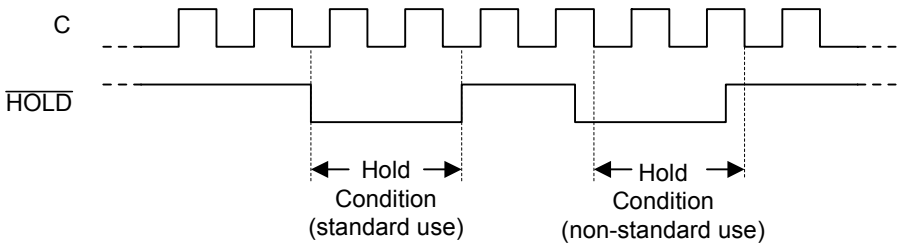
If the falling edge does not coincide with Serial Clock (C) being Low, the Hold condition starts after Serial Clock (C) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (C) being Low, the Hold condition ends after Serial Clock (C) next goes Low. This is shown in Figure 2.

During the Hold condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (C) are Don't Care.

Normally, the device is kept selected, with Chip Select ($\overline{S}$) driven Low, for the whole duration of the Hold condition. This is to ensure that the state of the internal logic remains unchanged from the moment of entering the Hold condition.

If Chip Select ($\overline{S}$) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold ($\overline{HOLD}$) High, and then to drive Chip Select ($\overline{S}$) Low. This prevents the device from going back to the Hold condition.

Figure 2. Hold Condition Activation



OPERATING FEATURES

Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration t_{PP}).
To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided that they lie in consecutive addresses on the same page of memory.

Dual Input Fast Program

The Dual Input Fast Program (DIFP) instruction makes it possible to program up to 256 bytes using two input pins at the same time (by changing bits from 1 to 0).
For optimized timings, it is recommended to use the Dual Input Fast Program (DIFP) instruction to program all consecutive targeted bytes in a single sequence rather to using several Dual Input Fast Program (DIFP) sequences each containing only a few bytes.

Quad Input Fast Program

The Quad Input Fast Program (QIFP) instruction makes it possible to program up to 256 bytes using four input pins (IO_3, IO_2, IO_1, and IO_0) at the same time (by changing bits from 1 to 0).
For optimized timings, it is recommended to use the Quad Input Fast Program (QIFP) instruction to program all consecutive targeted bytes in a single sequence rather to using several Quad Input Fast Program (QIFP) sequences each containing only a few bytes.

Sector Erase, Block Erase, and Chip Erase

The Page Program (PP) instruction, Dual Input Fast Program (DIFP) instruction, and Quad Input Fast Program (QIFP) instruction allow bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved, a sector at a time, using the Sector Erase (SE) instruction, a block at a time, using the Block Erase (BE) instruction, or throughout the entire memory, using the Chip Erase (CE) instruction. This starts an internal Erase cycle (of duration t_{SE}, t_{BE}, or t_{CE}).
The Erase instruction must be preceded by a Write Enable (WREN) instruction.

Polling During a Write, Program or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program OTP (POTP), Program (PP, DIFP, QIFP), or Erase (SE, BE, or CE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SE}, t_{BE}, t_{CE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

Active Power, Stand-by Power and Deep Power-Down Modes

When Chip Select ($\overline{S}$) is Low, the device is enabled, and in the Active Power mode.

When Chip Select ($\overline{S}$) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write Status Register). The device then goes in to the Stand-by Power mode. The device consumption drops to I_{CC1}.
The Deep Power-down mode is entered when the specific instruction (the Deep Power-down Mode (DP) instruction) is executed. The device consumption drops further to I_{CC2}. The device remains in this mode until another specific instruction (the Release from Deep Power-down Mode and Read Electronic Signature (RES) instruction) is executed.
All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program or Erase instructions.

Status Register

The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. See Read Status Register (RDSR) for a detailed description of the Status Register bits.

Protection Modes

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. To help combat this, the A25LQ32A boasts the following data protection mechanisms:

- Power-On Reset and an internal timer (t_{PUW}) can provide protection against inadvertent changes while the power supply is outside the operating specification.
- Program, Erase and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion
  - Write Status Register (WRSR) instruction completion
  - Program OTP (POTP) instruction completion
  - Page Program (PP) instruction completion
  - Dual Input Fast Program (DIFP) instruction completion
  - Quad input Fast Program (QIFP) instruction completion
  - Sector Erase (SE) instruction completion
  - Block Erase (BE) instruction completion
  - Chip Erase (CE) instruction completion
- The Block Protect (BP2, BP1, BP0) bits conjunction with Sector Protect (SEC) bit , Top/Bottom (TB) bit and Complement Protect (CMP) bit allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).
- The Write Protect ($\overline{W}$) signal allows the Block Protect (BP2, BP1, BP0) bits, Sector Protect (SEC) bit, Top/Bottom (TB) bit, All Protect (APT), Complement Protect (CMP) bit and Status Register Protect (SRP1, SRP0) bits to be protected. This is the Hardware Protected Mode (HPM).
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertent Write, Program and Erase instructions, as all instructions are ignored except one particular instruction (the Release from Deep Power-down instruction).

Table 1-1. Protected Area Sizes (CMP=0)

A25LQ32A

Status Register Content					(32M-Bit) Memory Protection			
SEC	**TB**	**BP2**	**BP1**	**BP0**	**Block(s)**	**Addresses**	**Density(Byte)**	**Portion**
X	X	0	0	0	None	None	None	None
0	0	0	0	1	63	3F0000h – 3FFFFFh	64KB	Upper 1/64
0	0	0	1	0	62 – 63	3E0000h – 3FFFFFh	128KB	Upper 1/32
0	0	0	1	1	60 – 63	3C0000h – 3FFFFFh	256KB	Upper 1/16
0	0	1	0	0	56 – 63	380000h – 3FFFFFh	512KB	Upper 1/8
0	0	1	0	1	48 – 63	300000h – 3FFFFFh	1MB	Upper 1/4
0	0	1	1	0	32 – 63	200000h – 3FFFFFh	2MB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64KB	Lower 1/64
0	1	0	1	0	0 – 1	000000h – 01FFFFh	128KB	Lower 1/32
0	1	0	1	1	0 – 3	000000h – 03FFFFh	256KB	Lower 1/16
0	1	1	0	0	0 – 7	000000h – 07FFFFh	512KB	Lower 1/8
0	1	1	0	1	0 – 15	000000h – 0FFFFFh	1MB	Lower 1/4
0	1	1	1	0	0 – 31	000000h – 1FFFFFh	2MB	Lower 1/2
X	X	1	1	1	0 – 63	000000h – 3FFFFFh	4MB	ALL
1	0	0	0	1	63	3FF000h – 3FFFFFh	4KB	Top Block
1	0	0	1	0	63	3FE000h – 3FFFFFh	8KB	Top Block
1	0	0	1	1	63	3FC000h – 3FFFFFh	16KB	Top Block
1	0	1	0	X	63	3F8000h – 3FFFFFh	32KB	Top Block
1	0	1	1	0	63	3F0000h – 3FFFFFh	64KB	Top Block
1	1	0	0	1	0	000000h – 000FFFh	4KB	Bottom Block
1	1	0	1	0	0	000000h – 001FFFh	8KB	Bottom Block
1	1	0	1	1	0	000000h – 003FFFh	16KB	Bottom Block
1	1	1	0	X	0	000000h – 007FFFh	32KB	Bottom Block
1	1	1	1	0	0	000000h – 00FFFFh	64KB	Bottom Block

Note:

1. X = don't care
2. When CMP is 0, the device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP2, BP1, BP0) bits are 0.

Table 1-2. Protected Area Sizes (CMP=1)

A25LQ32A

Status Register Content					(32M-Bit) Memory Protection			
SEC	TB	BP2	BP1	BP0	Block(s)	Addresses	Density(Byte)	Portion
X	X	0	0	0	0 - 63	000000h – 3FFFFFh	4MB	All
0	0	0	0	1	0 - 62	000000h – 3EFFFFh	4032KB	Lower 63/64
0	0	0	1	0	0 – 61	000000h – 3DFFFFh	3968KB	Lower 31/32
0	0	0	1	1	0 – 59	000000h – 3BFFFFh	3840KB	Lower 15/16
0	0	1	0	0	0 – 55	000000h – 37FFFFh	3584KB	Lower 7/8
0	0	1	0	1	0 – 47	000000h – 2FFFFFh	3MB	Lower 3/4
0	0	1	1	0	0 – 31	000000h – 1FFFFFh	2MB	Lower 1/2
0	1	0	0	1	1 - 63	010000h – 3FFFFFh	4032KB	Upper 63/64
0	1	0	1	0	2 - 63	020000h – 3FFFFFh	3968KB	Upper 31/32
0	1	0	1	1	4 - 63	040000h – 3FFFFFh	3840KB	Upper 15/16
0	1	1	0	0	8 - 63	080000h – 3FFFFFh	3584KB	Upper 7/8
0	1	1	0	1	16 - 63	100000h – 3FFFFFh	3MB	Upper 3/4
0	1	1	1	0	32 - 63	200000h – 3FFFFFh	2MB	Upper 1/2
X	X	1	1	1	None	None	None	None
1	0	0	0	1	0 - 62	000000h – 3FEFFFh	4092KB	Lower 1023/1024
1	0	0	1	0	0 - 62	000000h – 3FDFFFh	4088KB	Lower 511/512
1	0	0	1	1	0 - 62	000000h – 3FBFFFh	4080KB	Lower 255/256
1	0	1	0	X	0 - 62	000000h – 3F7FFFh	4064KB	Lower 127/128
1	0	1	1	0	0 - 62	000000h – 3EFFFFh	4032KB	Lower 63/64
1	1	0	0	1	1 – 63	001000h – 3FFFFFh	4092KB	Upper 1023/1024
1	1	0	1	0	1 – 63	002000h – 3FFFFFh	4088KB	Upper 511/512
1	1	0	1	1	1 – 63	004000h – 3FFFFFh	4080KB	Upper 255/256
1	1	1	0	X	1 – 63	008000h – 3FFFFFh	4064KB	Upper 127/128
1	1	1	1	0	1 - 63	010000h – 3FFFFFh	4032KB	Upper 63/64

Note:

1. X = don’t care
2. When CMP is 1, the device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP2, BP1, BP0) bits are 1.

MEMORY ORGANIZATION

The memory is organized as:
- 4,194,304 bytes (8 bits each)
- 64 blocks (64 Kbytes each)
- 1024 sectors (4 Kbytes each)
- 16384 pages (256 bytes each)
- 64 bytes OTP located outside the main memory array

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector, Block, or Chip Erasable (bits are erased from 0 to 1) but not Page Erasable.

Table 2. Memory Organization

A25LQ32A Address Table

Block	Sector	Address range	
63	1023	3FF000h	3FFFFFh
	⋮	⋮	⋮
	1008	3F0000h	3F0FFFh
62	1007	3EF000h	3EFFFFh
	⋮	⋮	⋮
	992	3E0000h	3E0FFFh
⋮	⋮	⋮	⋮
28	463	1CF000h	1CFFFFh
	⋮	⋮	⋮
	448	1C0000h	1C0FFFh
27	447	1BF000h	1BFFFFh
	⋮	⋮	⋮
	432	1B0000h	1B0FFFh
26	431	1AF000h	1AFFFFh
	⋮	⋮	⋮
	416	1A0000h	1A0FFFh
25	415	19F000h	19FFFFh
	⋮	⋮	⋮
	400	190000h	190FFFh
24	399	18F000h	18FFFFh
	⋮	⋮	⋮
	384	180000h	180FFFh
23	383	17F000h	17FFFFh
	⋮	⋮	⋮
	368	170000h	170FFFh
22	367	16F000h	16FFFFh
	⋮	⋮	⋮
	352	160000h	160FFFh
21	351	15F000h	15FFFFh
	⋮	⋮	⋮
	336	150000h	150FFFh

Block	Sector	Address range	
20	335	14F000h	14FFFFh
	⋮	⋮	⋮
	320	140000h	140FFFh
19	319	13F000h	13FFFFh
	⋮	⋮	⋮
	304	130000h	130FFFh
18	303	12F000h	12FFFFh
	⋮	⋮	⋮
	288	120000h	120FFFh
17	287	11F000h	11FFFFh
	⋮	⋮	⋮
	272	110000h	110FFFh
16	271	10F000h	10FFFFh
	⋮	⋮	⋮
	256	100000h	100FFFh
15	255	FF000h	FFFFFh
	⋮	⋮	⋮
	240	F0000h	F0FFFh
14	239	EF000h	EFFFFh
	⋮	⋮	⋮
	224	E0000h	E0FFFh
13	223	DF000h	DFFFFh
	⋮	⋮	⋮
	208	D0000h	D0FFFh
12	207	CF000h	CFFFFh
	⋮	⋮	⋮
	192	C0000h	C0FFFh
11	191	BF000h	BFFFFh
	⋮	⋮	⋮
	176	B0000h	B0FFFh
10	175	AF000h	AFFFFh
	⋮	⋮	⋮
	160	A0000h	A0FFFh

Memory Organization (Continued)

Block	Sector	Address range	
9	159	9F000h	9FFFFh
	⋮	⋮	⋮
	144	90000h	90FFFh
8	143	8F000h	8FFFFh
	⋮	⋮	⋮
	128	80000h	80FFFh
7	127	7F000h	7FFFFh
	⋮	⋮	⋮
	112	70000h	70FFFh
6	111	6F000h	6FFFFh
	⋮	⋮	⋮
	96	60000h	60FFFh
5	95	5F000h	5FFFFh
	⋮	⋮	⋮
	80	50000h	50FFFh
4	79	4F000h	4FFFFh
	⋮	⋮	⋮
	64	40000h	40FFFh

Block	Sector	Address range	
3	63	3F000h	3FFFFh
	⋮	⋮	⋮
	48	30000h	30FFFh
2	47	2F000h	2FFFFh
	⋮	⋮	⋮
	32	20000h	20FFFh
1	31	1F000h	1FFFFh
	⋮	⋮	⋮
	16	10000h	10FFFh
0	15	0F000h	0FFFFh
	⋮	⋮	⋮
	4	04000h	04FFFh
	3	03000h	03FFFh
	2	02000h	02FFFh
	1	01000h	01FFFh
	0	00000h	00FFFh

INSTRUCTIONS

All instructions, addresses and data are shifted in and out of the device, most significant bit first.

Serial Data Input(s) IO_0 (IO_1, IO_2, IO_3) is (are) sampled on the first rising edge of Serial Clock (C) after Chip Select ($\overline{S}$) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input(s) IO_0 (IO_1, IO_2, IO_3), each bit being latched on the rising edges of Serial Clock (C).

The instruction set is listed in Table 3.

Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by dummy bytes (don't care), or by a combination or none.

In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (Fast_Read), Read Data Bytes at Higher Speed by Dual Output (FAST_READ_DUAL_OUTPUT), Read Data Bytes at Higher Speed by Dual Input and Dual Output (FAST_READ_DUAL_INPUT_OUTPUT) , Read Data Bytes at Higher Speed by Quad Output (FAST_READ_QUAD _OUTPUT), Read Data Bytes at Higher Speed by Quad Input and Quad Output (FAST_READ_QUAD_INPUT_OUTPUT), Read OTP (ROTP), Read Identification (RDID), Read Electronic Manufacturer and Device Identification (REMS), Read Status Register (RDSR) or Release from Deep Power-down, Read Device Identification and Read Electronic Signature (RES) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select ($\overline{S}$) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a Page Program (PP), Program OTP (POTP), Dual Input Fast Program (DIFP), Quad Input Fast Program (QIFP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), Write Enable (WREN), Write Disable (WRDI) or Deep Power-down (DP) instruction, Chip Select ($\overline{S}$) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select ($\overline{S}$) must driven High when the number of clock pulses after Chip Select ($\overline{S}$) being driven Low is an exact multiple of eight.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected.

Table 3. Instruction Set

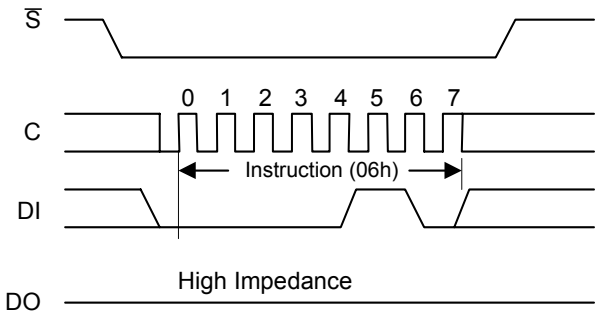
Instruction	Description	One-byte Instruction Code		Address Bytes	Dummy Bytes	Data Bytes
WREN	Write Enable	0000 0110	06h	0	0	0
WRDI	Write Disable	0000 0100	04h	0	0	0
RDSR-1	Read Status Register-1	0000 0101	05h	0	0	1 to ∞
RDSR-2	Read Status Register-2	0011 0101	35h	0	0	1 to ∞
WRSR	Write Status Register	0000 0001	01h	0	0	2
READ	Read Data Bytes	0000 0011	03h	3	0	1 to ∞
FAST_READ	Read Data Bytes at Higher Speed	0000 1011	0Bh	3	1	1 to ∞
FAST_READ_DUAL_OUTPUT	Read Data Bytes at Higher Speed by Dual Output (1)	0011 1011	3Bh	3	1	1 to ∞(1)
FAST_READ_DUAL_INPUT_OUTPUT	Read Data Bytes at Higher Speed by Dual Input and Dual Output (1)(2)	1011 1011	BBh	3(2)	1(2)	1 to ∞(1)
FAST_READ_QUAD_OUTPUT	Read Data Bytes at Higher Speed by Quad Output (4)	0110 1011	6Bh	3	1	1 to ∞(4)
FAST_READ_QUAD_INPUT_OUTPUT	Read Data Bytes at Higher Speed by Quad Input and Quad Output (3)(4)	1110 1011	EBh	3(3)	1(3)	1 to ∞(4)
ROTP	Read OTP (Read 64 bytes of OTP area)	0100 1011	4Bh or 48h	3	1	1 to ∞
POTP	Program OTP (Program 64 bytes of OTP area)	0100 0010	42h	3	0	1 to 64
PP	Page Program	0000 0010	02h	3	0	1 to 256
DIFP	Dual Input Fast Program	1010 0010	A2h	3	0	1 to 256(5)
QIFP	Quad Input Fast Program	0011 0010	32h	3	0	1 to 256(6)
SE	Sector Erase	0010 0000	20h	3	0	0
BE	Block Erase	1101 1000	D8h or 52h	3	0	0
CE	Chip Erase	1100 0111	C7h or 60h	0	0	0
DP	Deep Power-down	1011 1001	B9h	0	0	0
RDID	Read Device Identification	1001 1111	9Fh	0	0	1 to ∞
REMS	Read Electronic Manufacturer & Device Identification	1001 0000	90h	1(7)	2	1 to ∞
RES	Release from Deep Power-down, and Read Electronic Signature	1010 1011	ABh	0	3	1 to ∞
	Release from Deep Power-down			0	0	0
HPM	High Performance Mode	1010 0011	A3h	0	3	0
Continuous Read Mode Reset(8)	Reset Mode Bit M<4> to 1	1111 1111	FFh or FFFFh	0	0	0
SUSPEND	Program / Erase Suspend	0111 0101	75h	0	0	0
		1011 0000	B0h			
RESUME	Program / Erase Resume	0111 1010	7Ah	0	0	0
		0011 0000	30h			
SFDP	Read SFDP	0101 1010	5Ah	3	1	1 to 64

Note: (1) Dual Output Data
IO_0 = (D_6, D_4, D_2, D_0)
IO_1 = (D_7, D_5, D_3, D_1)
(2) Dual Input Address
IO_0 = (A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0)
IO_1 = (A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1)
(3) Quad Input Address
IO_0 = (A20, A16, A12, A8, A4, A0, M4, M0)
IO_1 = (A21, A17, A13, A9, A5, A1, M5, M1)
IO_2 = (A22, A18, A14, A10, A6, A2, M6, M2)
IO_3 = (A23, A19, A15, A11, A7, A3, M7, M3)
(4) Quad Output Data
IO_0 = (D_4, D_0, …..)
IO_1 = (D_5, D_1, …..)
IO_2 = (D_6, D_2, …..)
IO_3 = (D_7, D_3, …..)
(5) Dual Input Fast Program Input Data
IO_0 = (D_6, D_4, D_2, D_0)
IO_1 = (D_7, D_5, D_3, D_1)
(6) Quad Input Fast Program Input Data
IO_0 = (D_4, D_0, …..)
IO_1 = (D_5, D_1, …..)
IO_2 = (D_6, D_2, …..)
IO_3 = (D_7, D_3, …..)
(7) ADD= (00h) will output manufacturer's ID first and ADD=(01h) will output device ID first
(8) This instruction is recommended when using the Dual or Quad "Continuous Read Mode" features. See page 22&25 for more information.

Write Enable (WREN)

The Write Enable (WREN) instruction (Figure 3.) sets the Write Enable Latch (WEL) bit.
The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Dual Input Fast Program (DIFP), Quad Input Fast Program (QIFP), Program OTP (POTP), Sector Erase (SE), Block Erase (BE), and Chip Erase (CE) and Write Status Register (WRSR) instruction.
The Write Enable (WREN) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

Figure 3. Write Enable (WREN) Instruction Sequence

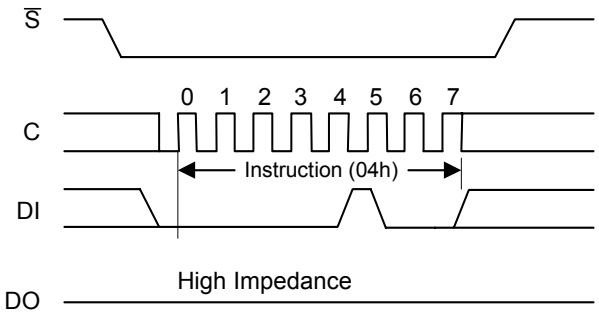


Write Disable (WRDI)

The Write Disable (WRDI) instruction (Figure 4.) resets the Write Enable Latch (WEL) bit.
The Write Disable (WRDI) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip The Write Enable Latch (WEL) bit is reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Dual Input Fast Program (DIFP) instruction completion
- Quad Input Fast Program (QIFP) instruction completion
- Program OTP (POTP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE) instruction completion
- Chip Erase (CE) instruction completion

Figure 4. Write Disable (WRDI) Instruction Sequence



Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The instruction code of "05h" is for Status Register-1 and "35h" is for Status Register-2. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in Figure 5.

Table 4-a Status Register-1 Format

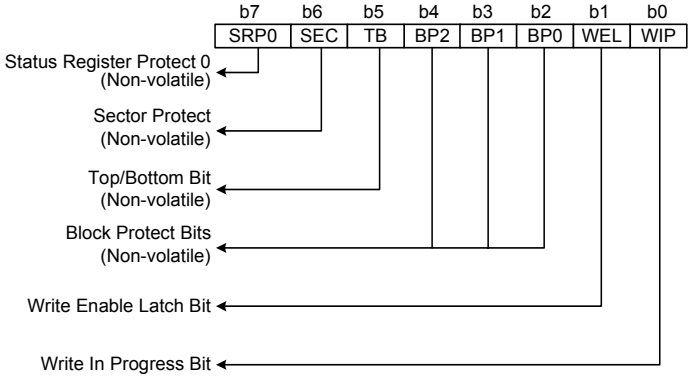
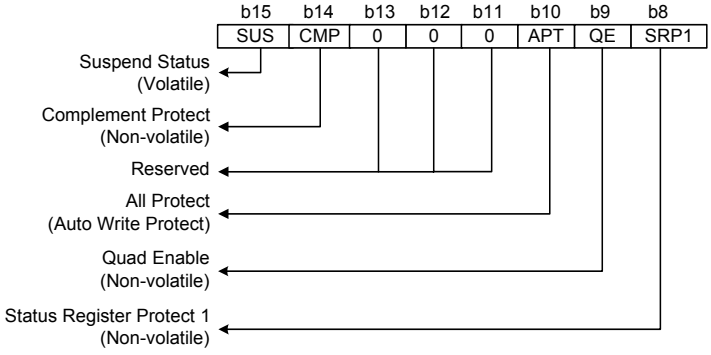


Table 4-b Status Register-2 Format



The status and control bits of the Status Register are as follows:

WIP bit. The Write In Progress (WIP) bit is a read only bit in the status register (b0) that is set to a 1 state when the device is busy with a Write Status Register, Program or Erase cycle. During this time the device will ignore further instructions except for the Read Status Register , Suspend and Resume instructions (see t_W, t_{PP}, t_{SE}, t_{BE}, and t_{CE} in AC Characteristics). When the program, erase, write status register instruction has completed or Program/Erase Suspend instruction is executed, the WIP bit will be cleared to a 0 state indicating the device is ready for further instructions.

WEL bit. The Write Enable Latch (WEL) bit is a read only bit in the status register (b1) that is set to a 1 after executing a Write Enable Instruction. The WEL status bit is cleared to a 0 when the device is write disabled or Program/Erase suspended. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Dual Input Fast Program, Quad Input Fast Program, Sector Erase, Block Erase, Chip Erase, and Write Status Register.

BP2, BP1, BP0 bits. The Block Protect (BP2, BP1, and BP0) bits are non-volatile read/write bits in the status register (b4, b3, and b2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see t_W in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Table 1. Protected Area Sizes). These bits can be set with the Write Status Register Instruction depending on the state of the SRP1, SRP0, and WEL bit. The factory default setting for the Block Protect Bits is 0 which means none of the array protected. For value of BP2, BP1, BP0 after power-on, see note please.

TB bit. The non-volatile Top/Bottom (TB) bit controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in Table 1. Protected Area Sizes. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP1, SRP0, and WEL bit.

SEC bit. The non-volatile Sector Protect (SEC) bit in the status register (b6) controls if the Block Protect Bits (BP2, BP1, BP0) protect 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in Table 1. Protected Area Sizes. This bit can be set with the Write Status Register Instruction depending on the state of the SRP1, SRP0, and WEL bit. The factory default setting for SEC is 0.

SRP1, SRP0 bits. The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register (b8 and b7). The SRP bits control the method of write protection: software protection, hardware protection, or one time programmable protection.

QE bit. The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (b9) that allows Quad SPI operation. When QE is set to 0(factory default), the $\overline{W}$ pin and $\overline{HOLD}$ pin are enabled. When QE is set to 1, the $\overline{W}$ pin and $\overline{HOLD}$ pin become IO_2 and IO_3. This bit can be set with the Write Status Register Instruction depending on the state of the SRP1, SRP0, and WEL bit. The factory default setting for QE is 0.

APT bit. The All Protect (APT) bit is a non-volatile read/write bit in the status register (b10). Whole chip will be kept in write-protect state after power-on if this bit is set to 1. This bit can be set with the Write Status Register Instruction depending on the state of the SRP1, SRP0, and WEL bit. The factory default setting for APT is 0.

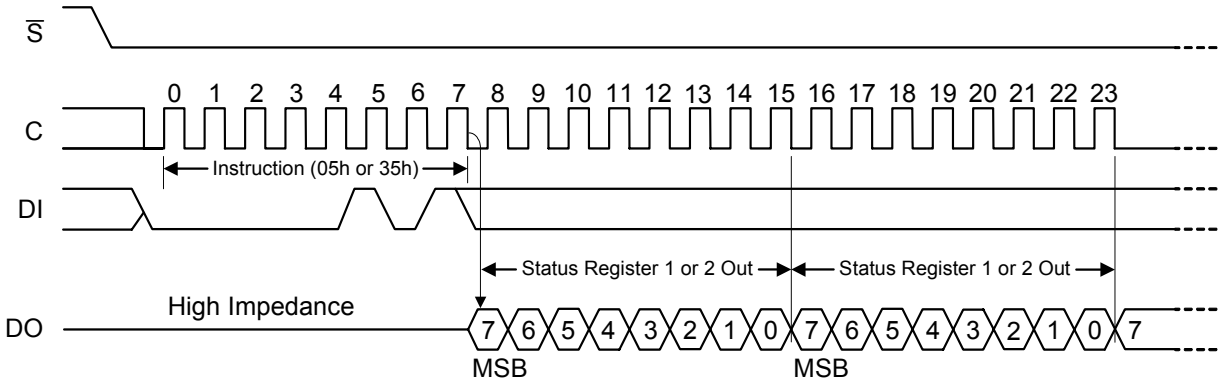
CMP bit. The Complement Protect (CMP) bit is a non-volatile read/write bit in the status register (b14). It's used in conjunction with SEC, TB, BP2, BP1, BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0

will be reversed. Please refer to table 1 for more details. The factory default setting for CMP is 0.

SUS bit. The Suspend Status (SUS) bit is a volatile read only bit in the status register (b15) which is set to 1 after executing a Program/Erase Suspend instruction. The SUS bit is cleared to 0 by Program/Erase Resume instruction as well as a power-down, power-up cycle.

Note:
1. When APT is 0, BP2, BP1, BP0 won't be changed after power-on.
2. When APT is 1 and CMP is 0, all BP2, BP1, BP0 will be set to 1 after power-on.
3. When APT is 1 and CMP is 1, all BP2, BP1, BP0 will be set to 0 after power-on.

Figure 5. Read Status Register (RDSR) Instruction Sequence and Data-Out Sequence



Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code and the data byte on Serial Data Input (DI).

The instruction sequence is shown in Figure 6. Only non-volatile Status Register bits SRP0, SEC, TB, BP2, BP1, BP0 (bits 7, 6, 5, 4, 3, 2 of Status Register-1) and CMP, APT, QE, SRP1 (bits 14, 10, 9 and 8 of Status Register-2) can be written. All other Status Register bits are always read as '0' and will not be affected by the Write Status Register instruction.

Chip Select ($\overline{S}$) must be driven High after the eighth or sixteenth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed.

If Chip Select ($\overline{S}$) is driven high after the eighth clock the CMP, QE and SRP1 bits will be cleared to 0.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (APT, CMP, SEC, TB, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 1. The Write Status Register (WRSR) instruction also allows the user to set the Status Register Protect (SRP1, SRP0) bits. Those bits are used in conjunction with the Write Protect ($\overline{W}$) pin to disable writes to the Status Register. Factory default for all Status Register bits are 0.

Figure 6. Write Status Register (WRSR) Instruction Sequence

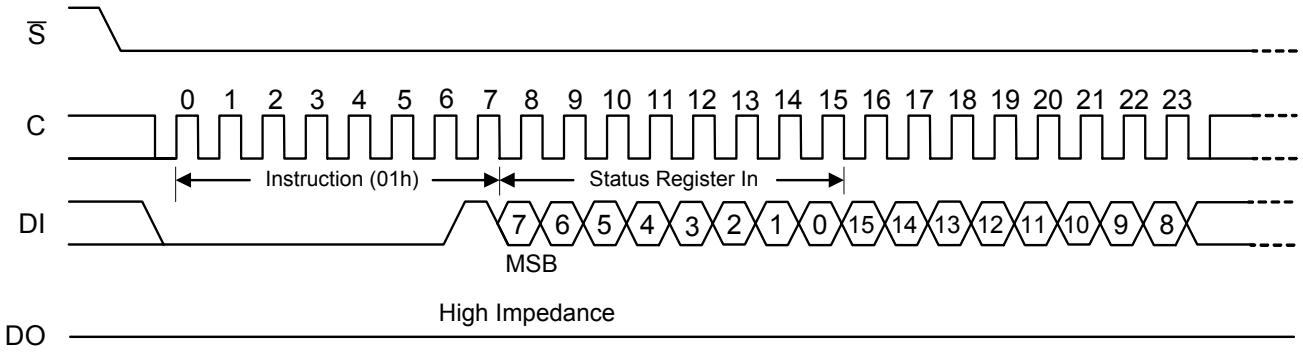


Table 5. Protection Modes

SRP1	SRP0	$\overline{W}$	Status Register	Description
0	0	X	Software Protection	Status Register is Writable (if the WREN instruction has set the WEL bit). The values in the CMP, APT, SRP1, SRP0, SEC, TB, BP2, BP1, BP0 bits can be changed.
0	1	0	Hardware Protection	Status Register is hardware write protected. The values in the CMP, APT, SRP1, SRP0, SEC, TB, BP2, BP1, BP0 bits cannot be changed.
0	1	1	Software Protection	When $\overline{W}$ pin is high. Status Register is Writable (if the WREN instruction has set the WEL bit). The values in the CMP, APT, SRP1, SRP0, SEC, TB, BP2, BP1, BP0 bits can be changed.
1	1	X	One Time Program	Status Register is permanently protected. The values in the CMP, APT, SRP1, SRP0, SEC, TB, BP2, BP1, BP0 bits cannot be changed.

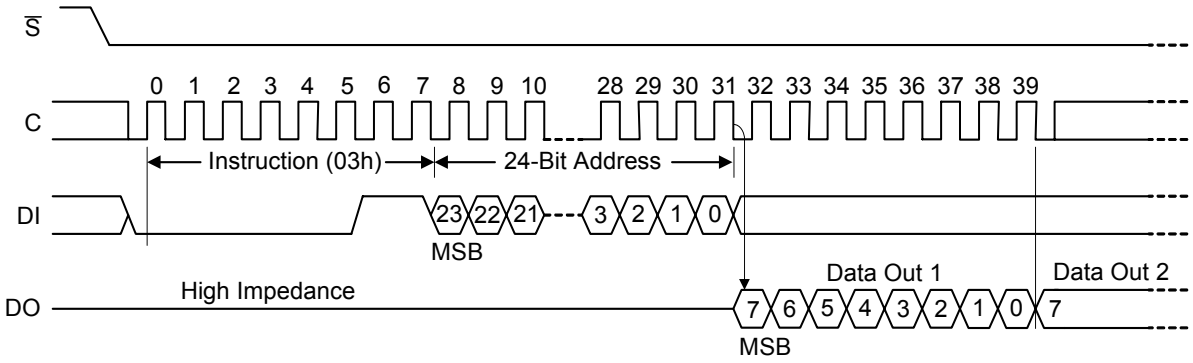
Read Data Bytes (READ)

The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 7. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 7. Read Data Bytes (READ) Instruction Sequence and Data-Out Sequence



Note: Address bits A23 to A22 are Don't Care, for A25LQ32A.

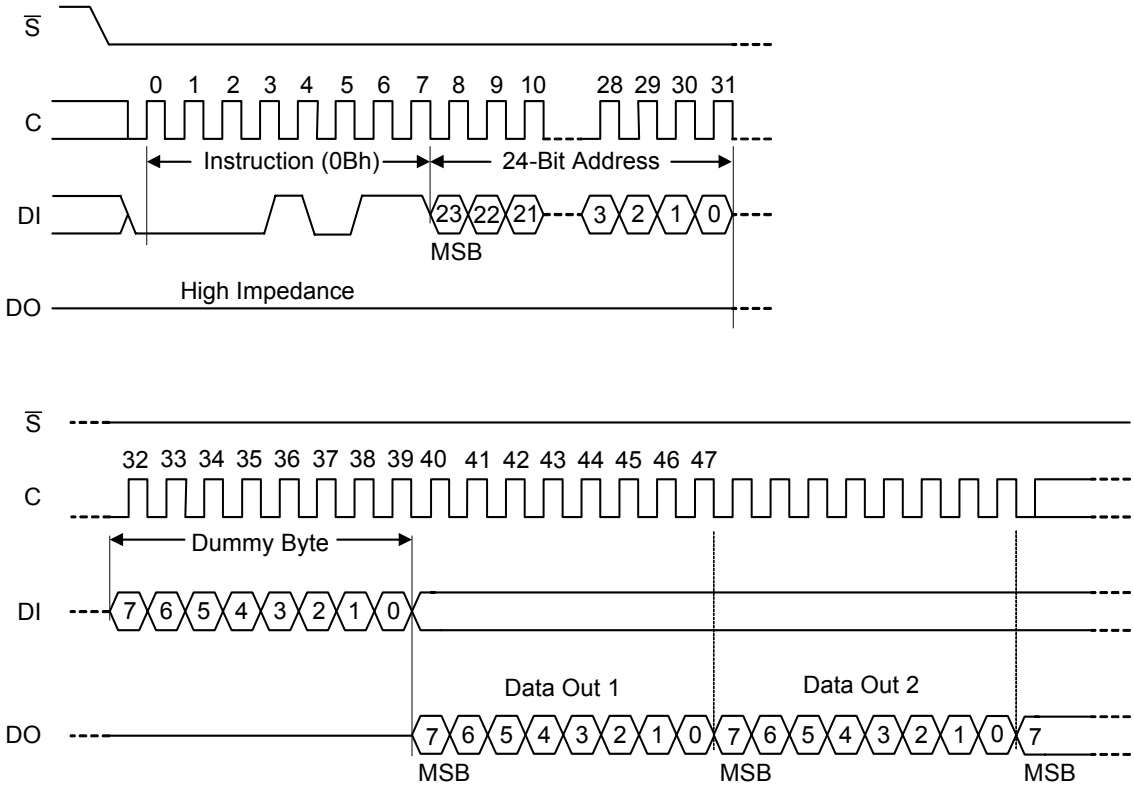
Read Data Bytes at Higher Speed (FAST_READ)

The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency f_C, during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 8. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes at Higher Speed (FAST_READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 8. Read Data Bytes at Higher Speed (FAST_READ) Instruction Sequence and Data-Out Sequence

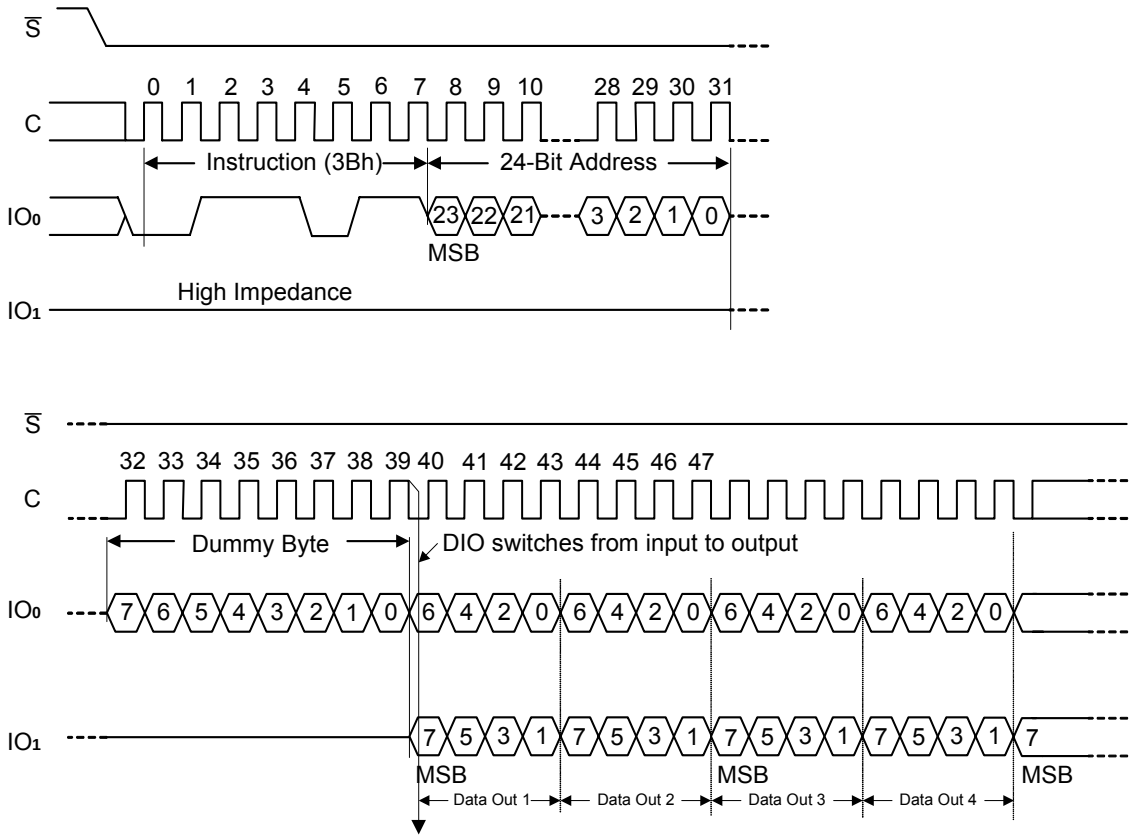


Note: Address bits A23 to A22 are Don't Care, for A25LQ32A.

Read Data Bytes at Higher Speed by Dual Output (FAST_READ_DUAL_OUTPUT)

The FAST_READ_DUAL_OUTPUT (3Bh) instruction is similar to the FAST_READ (0Bh) instruction except the data is output on two pins, IO_0 and IO_1, instead of just DO. This allows data to be transferred from the A25LQ32A at twice the rate of standard SPI devices.
Similar to the FAST_READ instruction, the FAST_READ_DUAL_OUTPUT instruction can operate at the highest possible frequency of f_C (See AC Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in figure 9. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO_0 and IO_1 pins should be high-impedance prior to the falling edge of the first data out clock.

Figure 9. FAST_READ_DUAL_OUTPUT Instruction Sequence and Data-Out Sequence



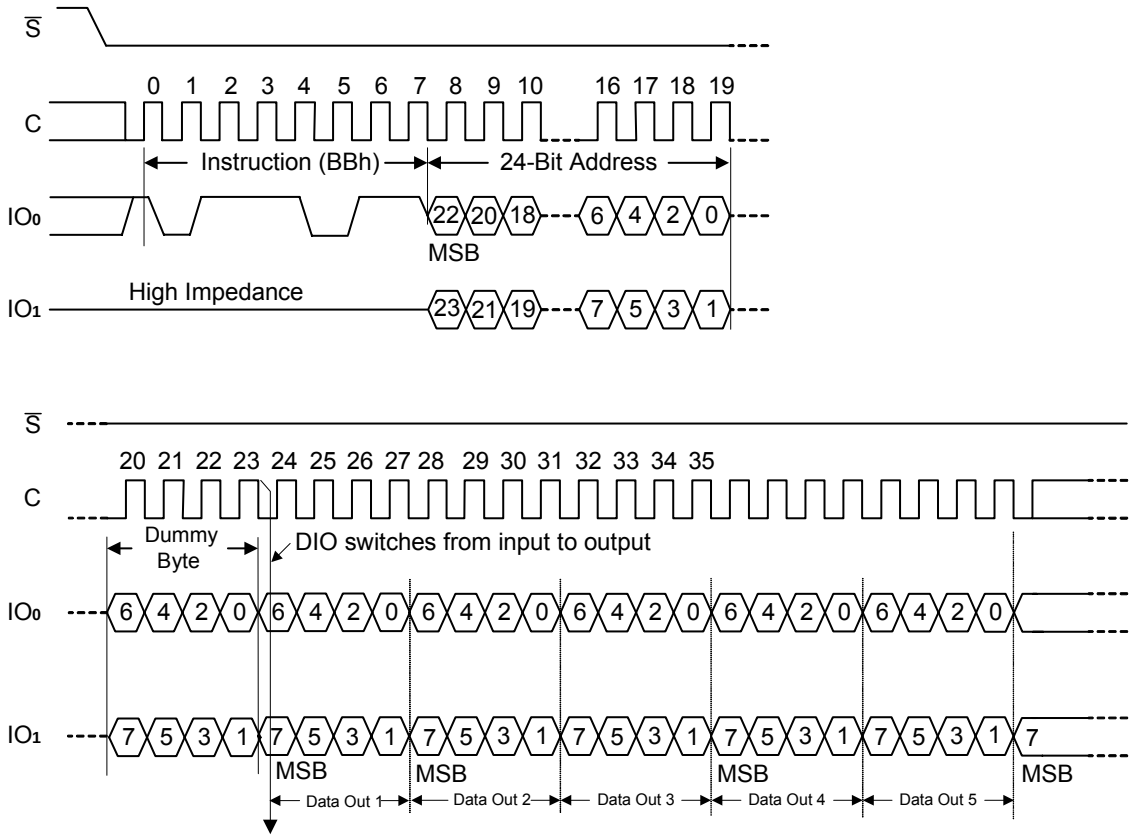
Note: Address bits A23 to A22 are Don't Care, for A25LQ32A.

Read Data Bytes at Higher Speed by Dual Input and Dual Output (FAST_READ_DUAL_INPUT_OUTPUT)

The FAST_READ_DUAL_INPUT_OUTPUT (BBh) instruction is similar to the FAST_READ (0Bh) instruction except the data is input and output on two pins, IO_0 and IO_1, instead of just DO. This allows data to be transferred from the A25LQ32A at twice the rate of standard SPI devices.

Similar to the FAST_READ instruction, the FAST_READ_DUAL_INPUT_OUTPUT instruction can operate at the highest possible frequency of f_C (See AC Characteristics).

Figure 10. FAST_READ_DUAL_INPUT_OUTPUT Instruction Sequence and Data-Out Sequence



Note: Address bits A23 to A22 are Don't Care, for A25LQ32A.

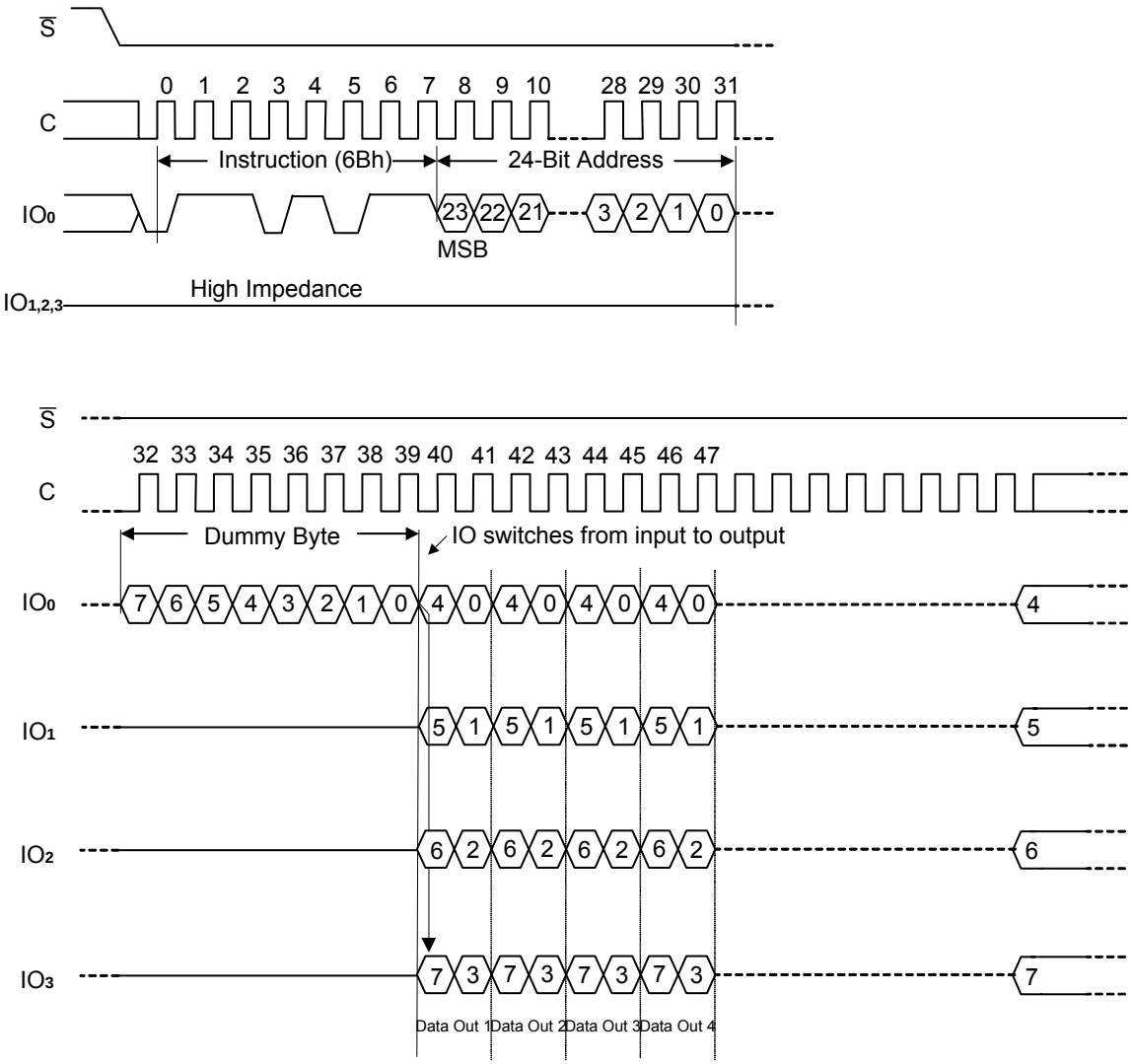
Read Data Bytes at Higher Speed by Quad Output (FAST_READ_QUAD_OUTPUT)

The FAST_READ_QUAD_OUTPUT (6Bh) instruction is similar to the FAST_READ (0Bh) instruction except the data is output on four pins (IO_0, IO_1, IO_2, IO_3), instead of just DO. This allows data to be transferred from the A25LQ32A at quadruple the rate of standard SPI devices.

Similar to the FAST_READ instruction, the FAST_READ_QUAD_OUTPUT instruction can operate at the highest possible frequency of f_C (See AC Characteristics).

This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in figure 11. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

Figure 11. FAST_READ_QUAD_OUTPUT Instruction Sequence and Data-Out Sequence



Note: Address bits A23 to A22 are Don't Care, for A25LQ32A.

Read Data Bytes at Higher Speed by Quad Input and Quad Output (FAST_READ_QUAD_INPUT_OUTPUT)

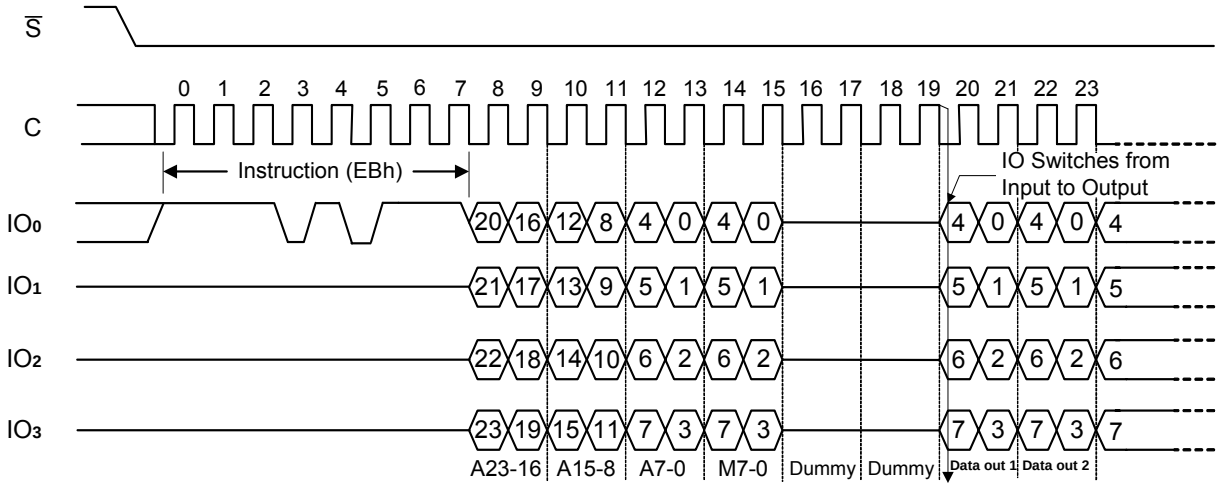
The FAST_READ_QUAD_INPUT_OUTPUT (EBh) instruction is similar to the FAST_READ (0Bh) instruction except the data is input and output on four pins (IO_3, IO_2, IO_1, IO_0) instead of just DO. This allows data to be transferred from the A25LQ32A at quadruple the rate of standard SPI devices. The Quad Enable bit (QE) of Status Register-2 must be set to enable the FAST_READ_QUAD_INPUT_OUTPUT Instruction.

Similar to the FAST_READ instruction, the FAST_READ_QUAD_INPUT_OUTPUT instruction can operate at the highest possible frequency of f_C (See AC Characteristics).

The FAST_READ_QUAD_INPUT_OUTPUT instruction can further reduce instruction overhead through setting the Mode bits (M7-0) after the input Address bits (A23-0), as shown in Figure 12-a. The upper nibble of the Mode (M7-4) bits controls the length of the next FAST_READ_QUAD_INPUT-OUTPUT instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the Mode (M3-0) bits are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

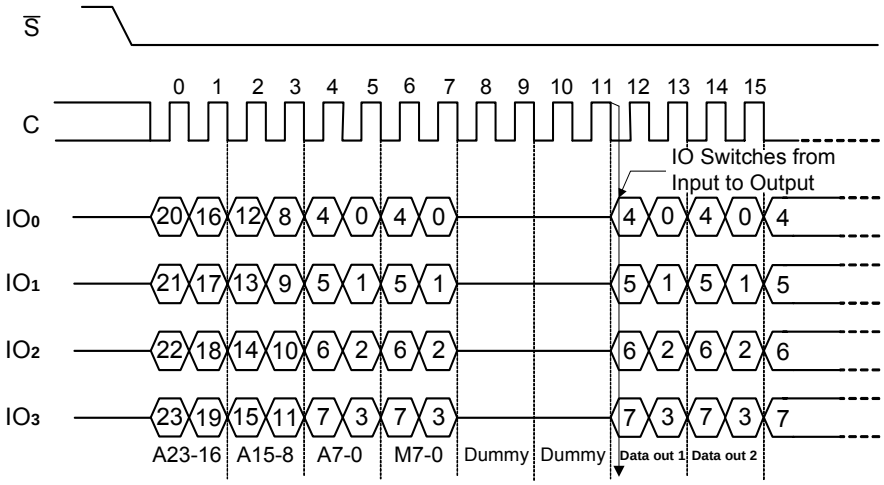
If the Mode bits (M5-4) equal "10" hex, then the chip is into "Continuous Read" Mode and the next FAST_READ_QUAD_INPUT_OUTPUT instruction (after $\overline{S}$ is raised and then lowered) does not require the EBh instruction code, as shown in figure 12-b. This reduces the instruction sequence by eight clocks and allows the address to be immediately entered after $\overline{S}$ is asserted low. If the Mode bits (M5-4) are any value other than "10" hex, the next instruction (after $\overline{S}$ is raised and then lowered) requires the first byte instruction code, thus returning to normal operation.

Figure 12-a. FAST_READ_QUAD_INPUT_OUTPUT Instruction and Data-Out Sequence (M5-4≠10h)



Note: Address bits A23 to A22 are Don't Care, for A25LQ32A.

Figure 12-b. FAST_READ_QUAD_INPUT_OUTPUT Instruction and Data-Out Sequence Continuous Read Mode, (M5-4=10h)

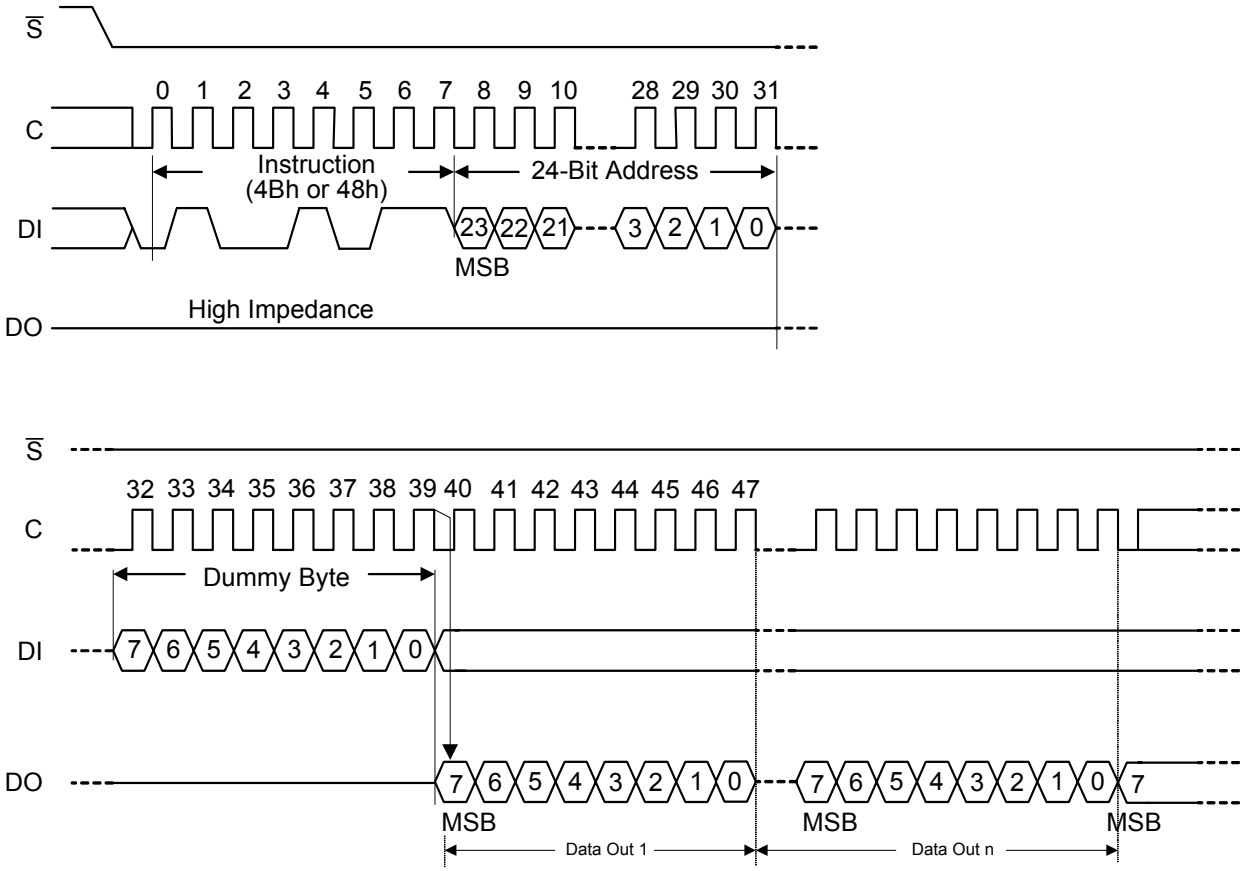


Note: Address bits A23 to A22 are Don't Care, for A25LQ32A.

Read OTP (ROTP)

The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the Read OTP (ROTP) instruction is followed by a 3-byte address (A23- A0) and a dummy byte. Each bit is latched in on the rising edge of Serial Clock (C).
Then the memory contents at that address are shifted out on Serial Data output (DO).
Each bit is shifted out at the maximum frequency, fc(Max.) on the falling edge of Serial Clock (C).
The instruction sequence is shown in Figure 13.
The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.
The Read OTP (ROTP) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any Read OTP (ROTP) instruction issued while an Erase, Program or Write Status Register cycle is in progress, is rejected without having any effect on the cycle that is in progress.

Figure 13. Read OTP (ROTP) instruction and data-out sequence



Note: A23 to A6 are don't care. ($1 \le n \le 64$)

Program OTP (POTP)

The Program OTP instruction (POTP) is used to program at most 64 bytes to the OTP memory area (by changing bits from 1 to 0, only). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL) bit.
The Program OTP instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data input (DI).

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Program OTP instruction is not executed.
The instruction sequence is shown in Figure 14.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Program OTP cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program OTP cycle, and it is 0 when it is completed. At some unspecified time before the cycle is complete, the Write Enable Latch (WEL) bit is reset.

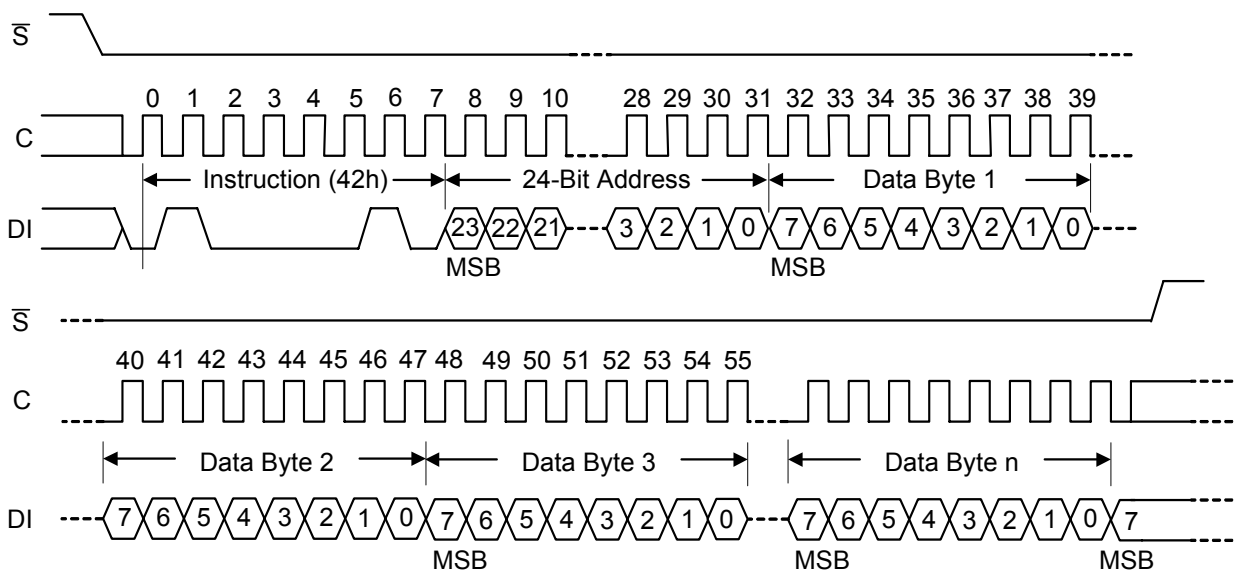
To lock the OTP memory:

Bit 0 of the OTP control byte, that is byte 63, (see Figure 14) is used to permanently lock the OTP memory array.

- When bit 0 of byte 63 = '1', the OTP memory array can be programmed.
- When bit 0 of byte 63 = '0', the OTP memory array are read-only and cannot be programmed anymore.

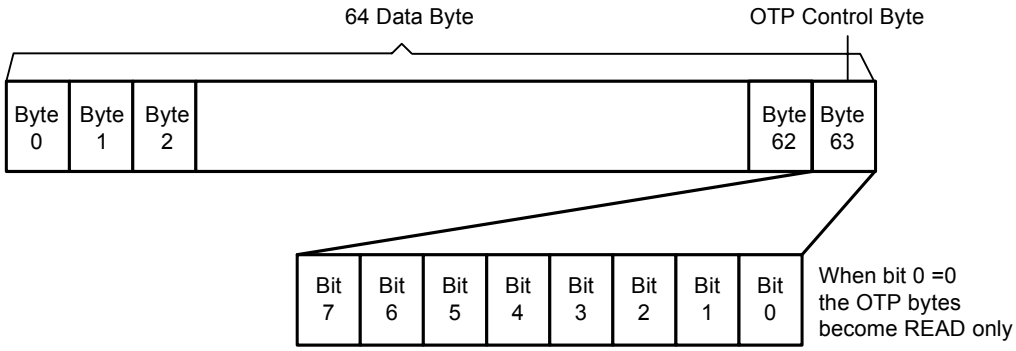
Once a bit of the OTP memory has been programmed to '0', it can no longer be set to '1'.
Therefore, as soon as bit 0 of address 63h (control byte) is set to '0', the 64 bytes of the OTP memory array become read-only in a permanent way.
Any Program OTP (POTP) instruction issued while an Erase, Program or Write Status Register cycle is in progress is rejected without having any effect on the cycle that is in progress.

Figure 14. Program OTP (POTP) instruction sequence



Note: A23 to A6 are don't care. ($1 \le n \le 64$)

Figure 15. How to permanently lock the 64 OTP bytes



Page Program (PP)

The Page Program (PP) instruction allows bytes to be programmed in the memory (changing bits from 1 to 0). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data Input (DI). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

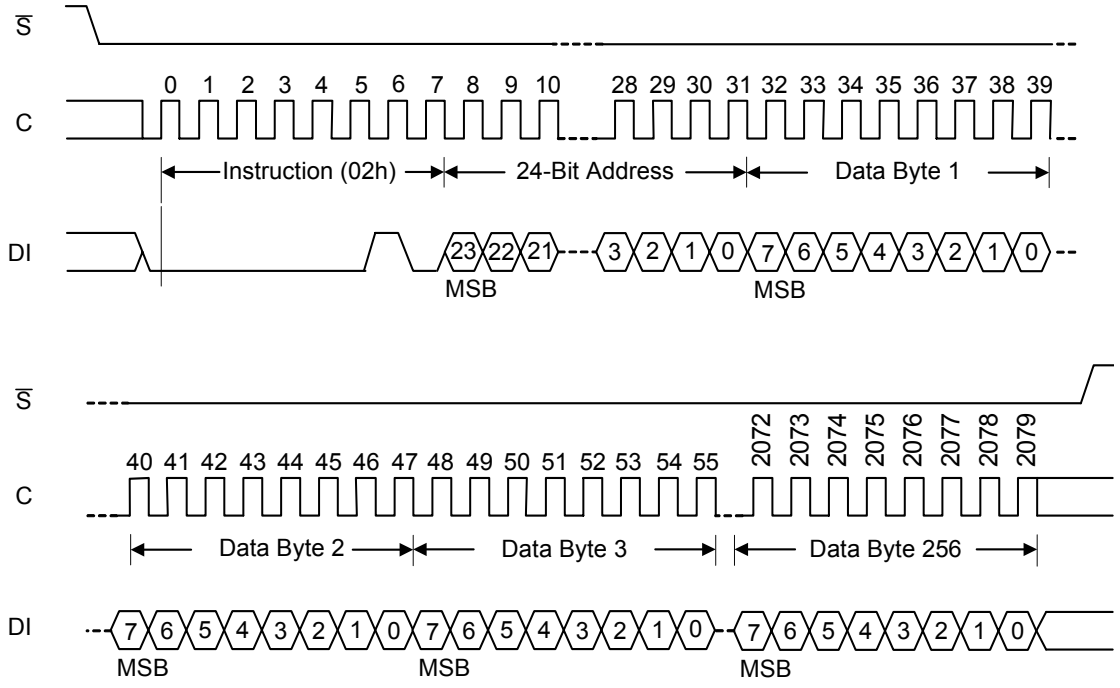
The instruction sequence is shown in Figure 16. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page which is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, BP0) bits (see table 1) is not executed.

Figure 16. Page Program (PP) Instruction Sequence



Note: Address bits A23 to A22 are Don't Care, for A25LQ32A.

Dual Input Fast Program (DIFP)

The Dual Input Fast Program (DIFP) instruction is very similar to the Page Program (PP) instruction, except that the data are entered on two pins IO_0 and IO_1 instead of only one. Inputting the data on two pins instead of one doubles the data transfer bandwidth compared to the Page Program (PP) instruction.

The Dual Input Fast Program (DIFP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data Output (IO_0 and IO_1).

If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 17.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes in the same page.

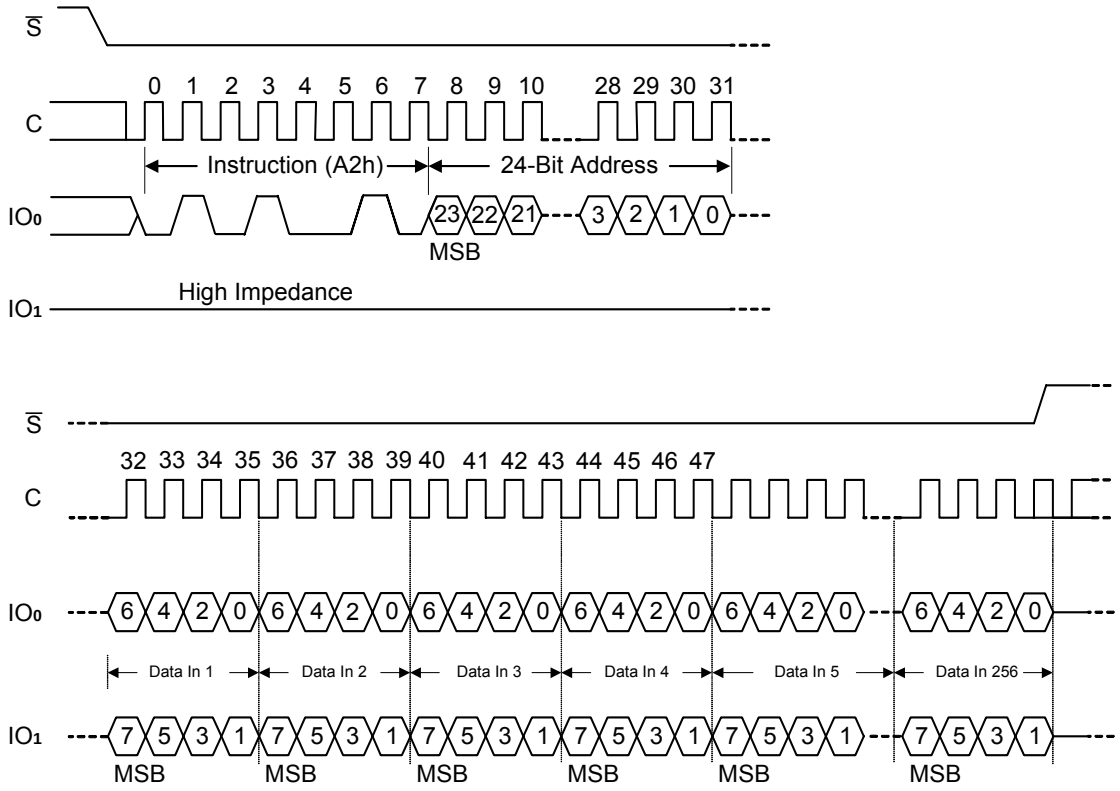
For optimized timings, it is recommended to use the Dual Input Fast Program (DIFP) instruction to program all consecutive targeted bytes in a single sequence rather to using several Dual Input Fast Program (DIFP) sequences each containing only a few bytes.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Dual Input Fast Program (DIFP) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Dual Input Fast Program (DIFP) cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Dual Input Fast Program (DIFP) instruction applied to a page that is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, BP0) bits (see Table 1) is not executed.

Figure 17. Dual Input Fast Program (DIFP) instruction sequence



Note: Address bits A23 to A22 are Don't Care, for A25LQ32A.

Quad Input Fast Program (QIFP)

The Quad Input Fast Program (QIFP) instruction is very similar to the Page Program (PP) instruction, except that the data are entered on four pins (IO_3, IO_2, IO_1, IO_0) instead of only one. Inputting the data on four pins instead of one quadruples the data transfer bandwidth compared to the Page Program (PP) instruction. To use Quad Input Fast Program the Quad Enable bit (QE) of Status Register-2 must be set.

The Quad Input Fast Program (QIFP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on Data Input Output (IO_3, IO_2, IO_1, IO_0).

If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 18.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes in the same page.

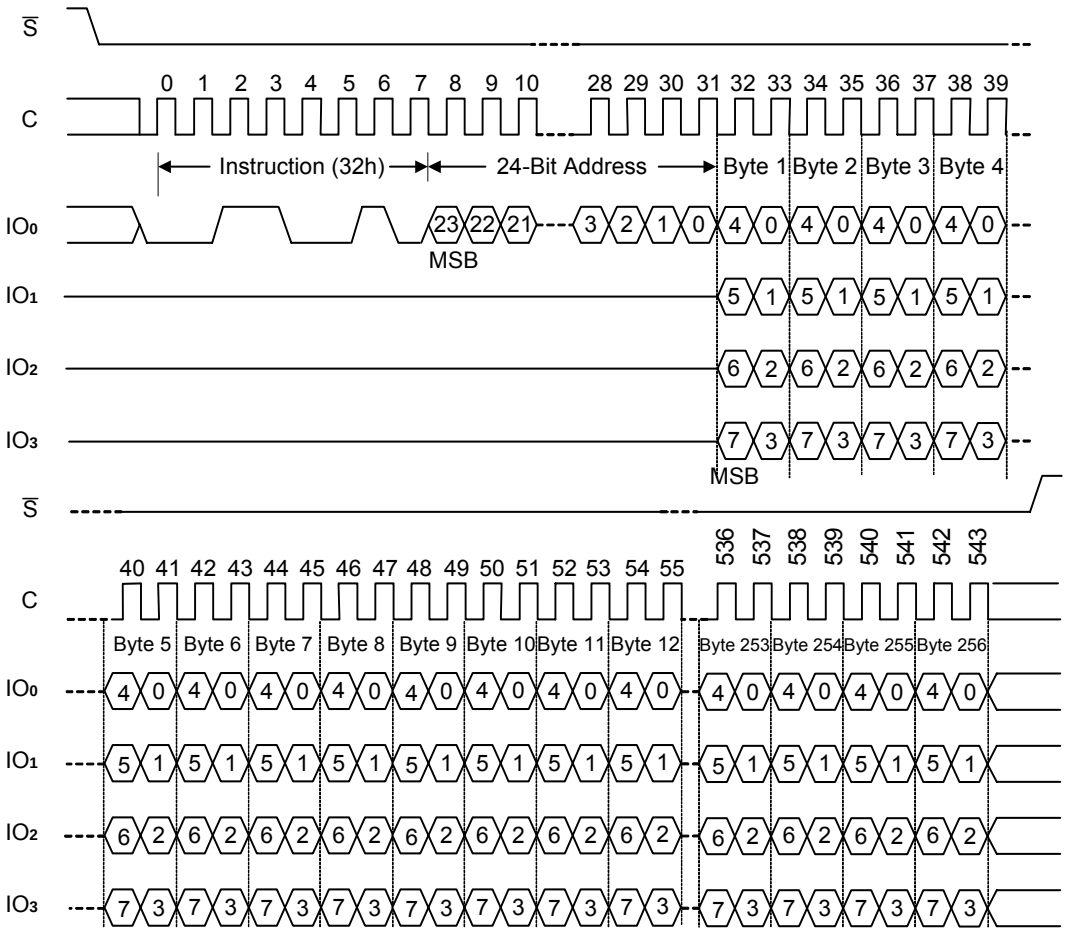
For optimized timings, it is recommended to use the Quad Input Fast Program (QIFP) instruction to program all consecutive targeted bytes in a single sequence rather to using several Quad Input Fast Program (QIFP) sequences each containing only a few bytes.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Quad Input Fast Program (QIFP) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Quad Input Fast Program (QIFP) cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Input Fast Program (QIFP) instruction applied to a page that is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, BP0) bits (see Table 1) is not executed.

Figure 18. Quad Input Fast Program (QIFP) instruction sequence



Note: Address bits A23 to A22 are Don't Care, for A25LQ32A

Sector Erase (SE)

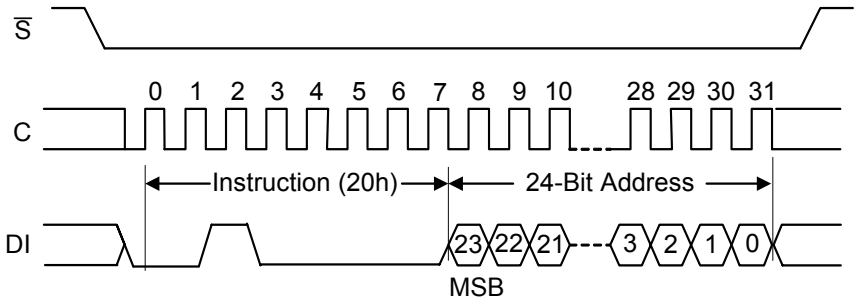
The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Sector Erase (SE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data Input (DI). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 19. Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Sector Erase instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Sector Erase (SE) instruction applied to a page which is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, BP0) bits (see table 1) is not executed.

Figure 19. Sector Erase (SE) Instruction Sequence



Note: Address bits A23 to A22 are Don't Care, for A25LQ32A.

Block Erase (BE)

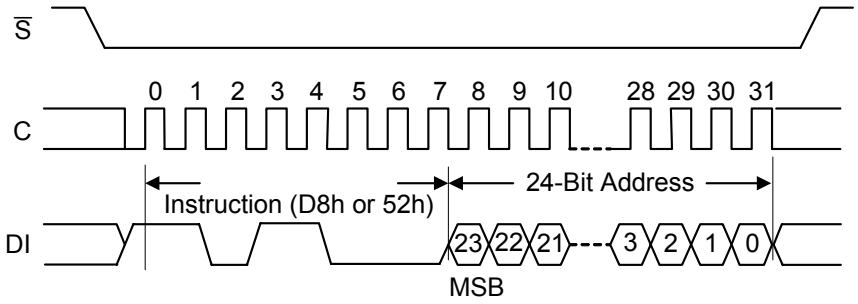
The Block Erase (BE) instruction sets to 1 (FFh) all bits inside the chosen block. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Block Erase (BE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data Input (DI). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 20. Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Block Erase instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Block Erase (BE) instruction applied to a page which is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, BP0) bits (see table 1) is not executed.

Figure 20. Block Erase (BE) Instruction Sequence



Note: Address bits A23 to A22 are Don't Care, for A25LQ32A.

Chip Erase (CE)

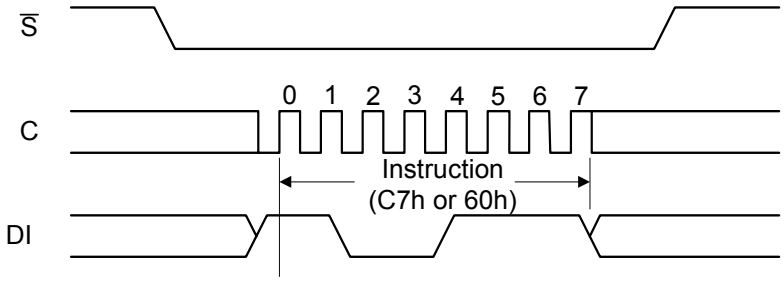
The Chip Erase (CE) instruction sets all bits to 1 (FFh). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Chip Erase (CE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data Input (DI). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 21. Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Chip Erase instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

The Chip Erase (CE) instruction is ignored if one, or more, sectors/blocks are protected.

Figure 21. Chip Erase (CE) Instruction Sequence



Deep Power-down (DP)

Executing the Deep Power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase instructions.

Driving Chip Select ($\overline{S}$) High deselects the device, and puts the device in the Standby mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) instruction, to reduce the standby current (from I_{CC1} to I_{CC2}, as specified in DC Characteristics Table.).

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Electronic Signature (RES) instruction. This releases the device from this mode. The Release from Deep Power-down and Read Electronic Signature (RES) instruction also allows the Electronic Signature of the device to be output on Serial Data Output (DO).

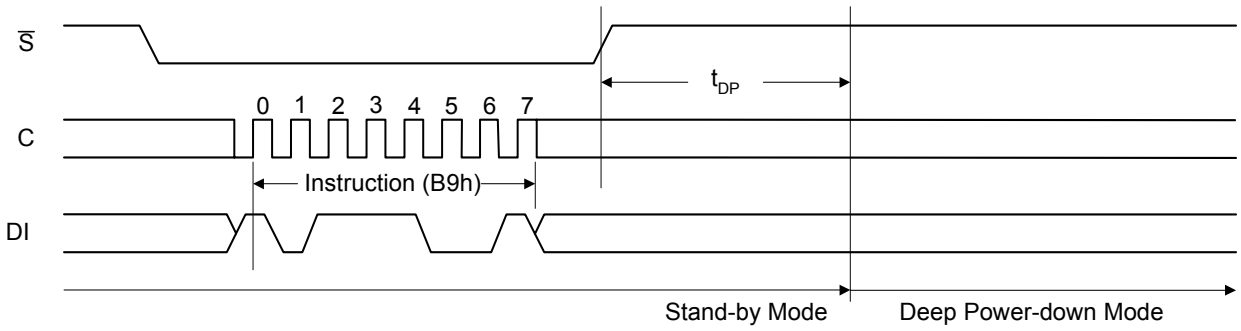
The Deep Power-down mode automatically stops at Power-down, and the device always Powers-up in the Standby mode.

The Deep Power-down (DP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data Input (DI). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence. The instruction sequence is shown in Figure 22.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-down mode is entered.

Any Deep Power-down (DP) instruction, while an Erase, Program or Write Status Register cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 22. Deep Power-down (DP) Instruction Sequence



Read Device Identification (RDID)

The Read Identification (RDID) instruction allows the 8-bit manufacturer identification code to be read, followed by two bytes of device identification. The manufacturer identification is assigned by JEDEC, and has the value 37h. The device identification is assigned by the device manufacturer, and indicates the memory in the first byte (40h), and the memory capacity of the device in the second byte (16h for A25LQ32A).

Any Read Identification (RDID) instruction while an Erase, or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The device is first selected by driving Chip Select ($\overline{S}$) Low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output (DO), each bit being shifted out during the falling edge of Serial Clock (C).

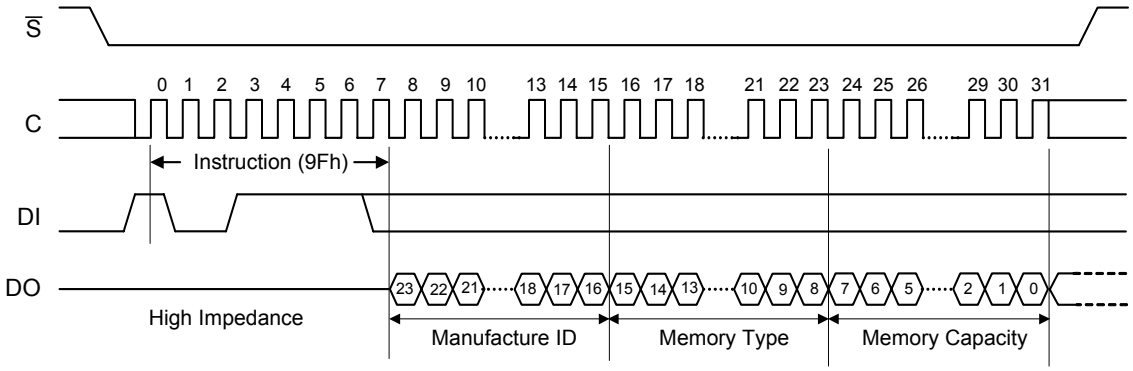
The instruction sequence is shown in Figure 23. The Read Identification (RDID) instruction is terminated by driving Chip Select ($\overline{S}$) High at any time during data output.

When Chip Select ($\overline{S}$) is driven High, the device is put in the Stand-by Power mode. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Table 6. Read Identification (READ_ID) Data-Out Sequence

Manufacture Identification	Device Identification	
Manufacture ID	Memory Type	Memory Capacity
37h	40h	16h (A25LQ32A)

Figure 23. Read Identification (RDID) Instruction Sequence and Data-Out Sequence



Read Electronic Manufacturer ID & Device ID (REMS)

The Read Electronic Manufacturer ID & Device ID (REMS) instruction allows the 8-bit manufacturer identification code to be read, followed by one byte of device identification. The manufacturer identification is assigned by JEDEC, and has the value 37h for AMIC. The device identification is assigned by the device manufacturer, and has the value 15h for A25LQ32A.

Any Read Electronic Manufacturer ID & Device ID (REMS) instruction while an Erase, or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The device is first selected by driving Chip Select ($\overline{S}$) Low. The 8-bit instruction code is followed by 2 dummy bytes and one byte address (A7~A0), each bit being latched-in on Serial Data Input (DI) during the rising edge of Serial Clock (C).

If the one-byte address is set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. On the other hand, if the one-byte address is set to 00h, then the Manufacturer ID will be read first and then followed by the device ID.

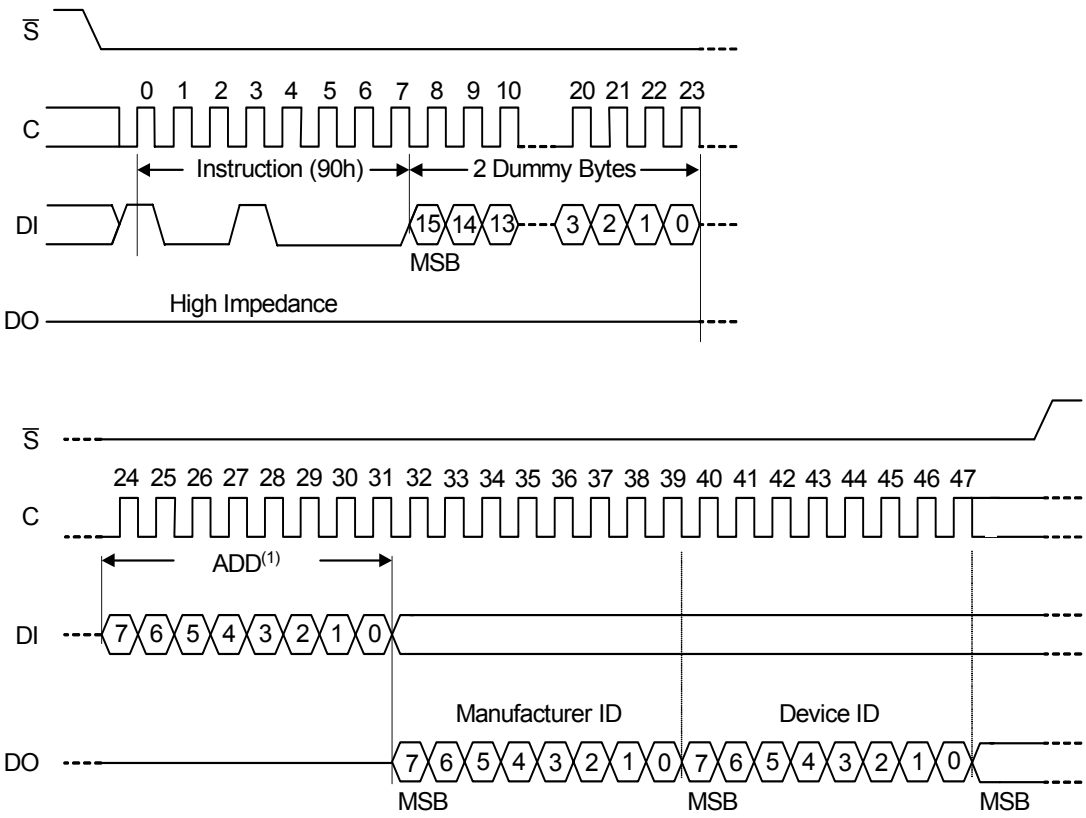
The instruction sequence is shown in Figure 24. The Read Electronic Manufacturer ID & Device ID (REMS) instruction is terminated by driving Chip Select ($\overline{S}$) High at any time during data output.

When Chip Select ($\overline{S}$) is driven High, the device is put in the Stand-by Power mode. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Table 7. Read Electronic Manufacturer ID & Device ID (REMS) Data-Out Sequence

Manufacture Identification	Device Identification
37h	15h (A25LQ32A)

Figure 24. Read Electronic Manufacturer ID & Device ID (REMS) Instruction Sequence and Data-Out Sequence



Notes:
(1) ADD=00h will output the manufacturer ID first and ADD=01h will output device ID first

Release from Deep Power-down and Read Electronic Signature (RES)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Electronic Signature (RES) instruction. Executing this instruction takes the device out of the Deep Power-down mode.

The instruction can also be used to read, on Serial Data Output (DO), the 8-bit Electronic Signature, whose value for A25LQ32A is 15h.

Except while an Erase, Program or Write Status Register cycle is in progress, the Release from Deep Power-down and Read Electronic Signature (RES) instruction always provides access to the 8-bit Electronic Signature of the device, and can be applied even if the Deep Power-down mode has not been entered.

Any Release from Deep Power-down and Read Electronic Signature (RES) instruction while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

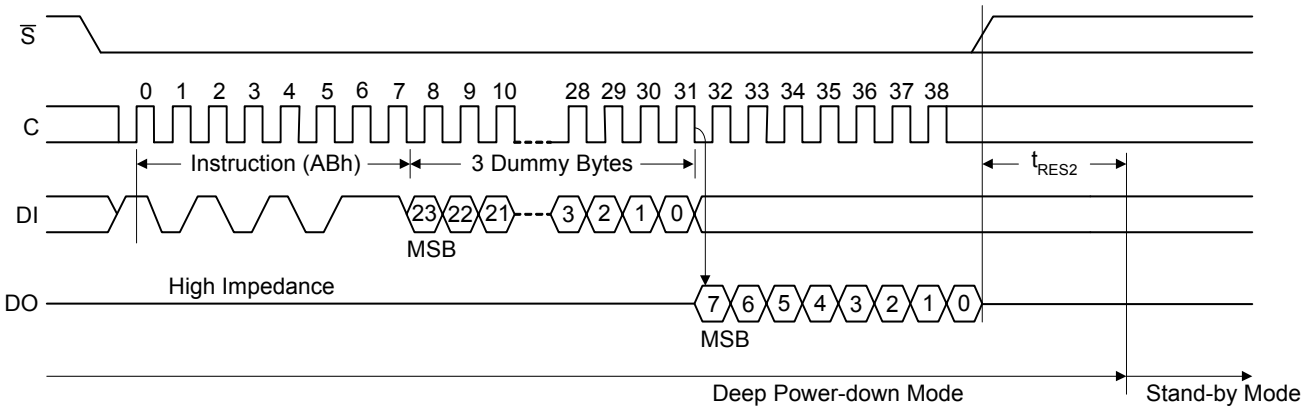
The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code is followed by 3 dummy bytes, each bit being latched-in on Serial Data Input (DI) during the rising edge of Serial Clock (C). Then, the 8-bit Electronic Signature, stored in the memory, is shifted out on Serial Data Output (DO), each bit being shifted out during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 25.

The Release from Deep Power-down and Read Electronic Signature (RES) instruction is terminated by driving Chip Select ($\overline{S}$) High after the Electronic Signature has been read at least once. Sending additional clock cycles on Serial Clock (C), while Chip Select ($\overline{S}$) is driven Low, cause the Electronic Signature to be output repeatedly.

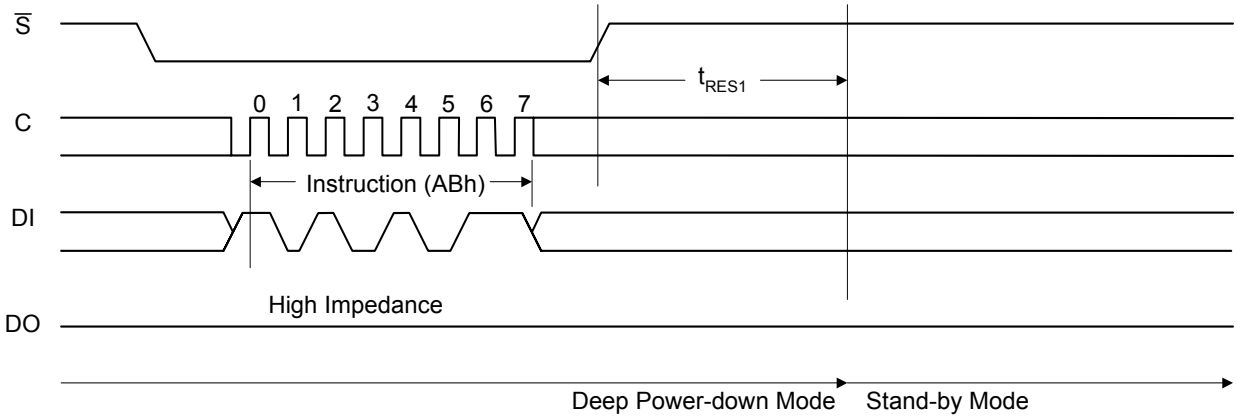
When Chip Select ($\overline{S}$) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by t_{RES2}, and Chip Select ($\overline{S}$) must remain High for at least t_{RES2} (max), as specified in AC Characteristics Table . Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Figure 25. Release from Deep Power-down and Read Electronic Signature (RES) Instruction Sequence and Data-Out Sequence



Note: The value of the 8-bit Electronic Signature, for A25LQ32A is 15h.

Figure 26. Release from Deep Power-down (RES) Instruction Sequence

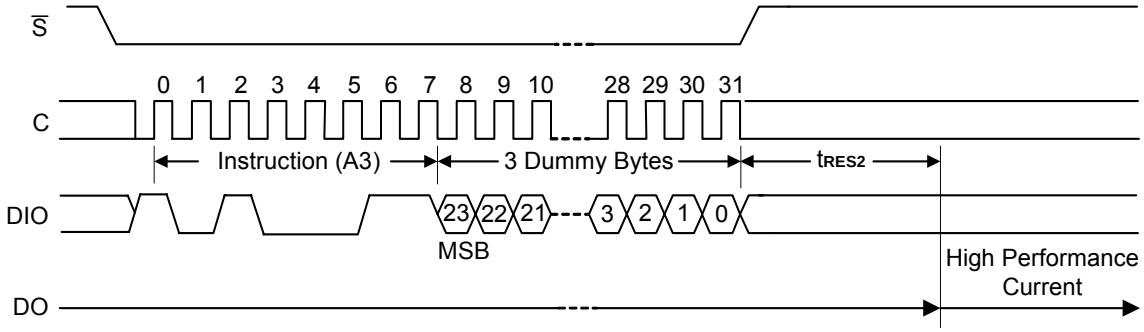


Driving Chip Select ($\overline{S}$) High after the 8-bit instruction byte has been received by the device, but before the whole of the 8-bit Electronic Signature has been transmitted for the first time (as shown in Figure 26.), still insures that the device is put into Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by t_{RES1}, and Chip Select ($\overline{S}$) must remain High for at least t_{RES1} (max), as specified in AC Characteristics Table. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

High Performance Mode (A3h)

The High Performance Mode (HPM) instruction can be executed prior to Dual or Quad I/O instructions if chip is operated at high frequencies. This instruction allows pre-charging of internal charge pumps so the voltages required for accessing the Flash memory array are readily available. The instruction sequence includes the A3h instruction code followed by three dummy byte clocks shown in Fig.28. After the HPM instruction is executed, the device will maintain a slightly higher standby current than standard SPI operation. The Release from Power-down (ABh) can be used to return to standard SPI standby current (I_{CC1}). In addition, Write Enable instruction (06h) and Power Down instruction (B9h) will also release the device from HPM mode back to standard SPI standby state.

Figure 27. High Performance Mode Instruction Sequence



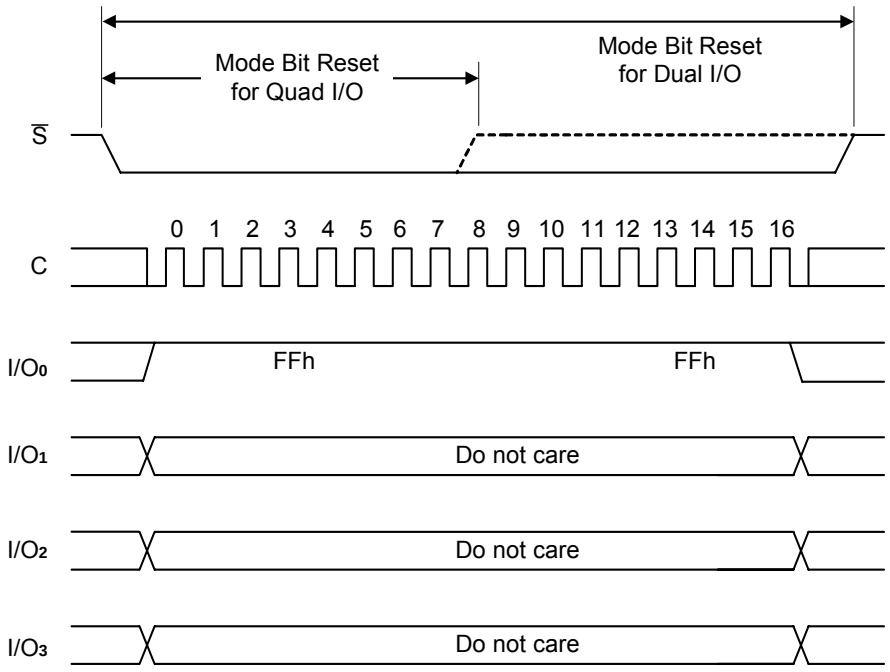
Continuous Read Mode Reset (FFh or FFFFh)

Continuous Read Mode Reset instruction can be used to set mode bit M4 to 1, thus the device will release the Continuous Read Mode and return to normal SPI operation, as shown in Fig.29.

If user wants to issue a new command after A25LQ32A is set to Continuous Mode Read, it is recommended to issue a Continuous Read Mode Reset instruction before any command. Doing so will release the device from the Continuous Read Mode and allow Standard SPI instructions to be recognized.

To reset "Continuous Read Mode" during Quad I/O operation, only eight clocks are needed. The instruction is "FFh". To reset "Continuous Read Mode" during Dual I/O operation, sixteen clocks are needed to shift in instruction "FFFFh". Mode bit M5, M4 will be reset to 0 after power-on, so it's unnecessary to issue Continuous Read Mode Reset instruction even the controller resets while A25LQ32A is set to Continuous Mode Read.

Figure 28. Continuous Read Mode Reset for Fast Read Dual/Quad I/O



Program / Erase Suspend

The Suspend instruction allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program data to, any other sectors or blocks. The Suspend instruction sequence is shown in figure 29.

The Write Status Register instruction (01h) and Erase instructions (20h, 52h, D8h, C7h, 60h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend instruction is ignored.

The Write Status Register instruction (01h) and Page Program instructions (02h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program operation.

The Suspend instruction will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the WIP bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of "tsus" (See AC Characteristics) is required to suspend the erase or program operation. The WIP bit in the Status Register will be cleared from 1 to 0 within "tsus" and the SUS bit in the Status Register will be set from 0 to 1 immediately after Program/Erase Suspend. For a previously resumed Program/Erase operation, it is also required that the Suspend instruction is not issued earlier than a minimum of time of "tsus" following the preceding Resume instruction.

Unexpected power off during the Program/Erase suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during Program/Erase suspend state.

Figure 29. Suspend Instruction Sequence

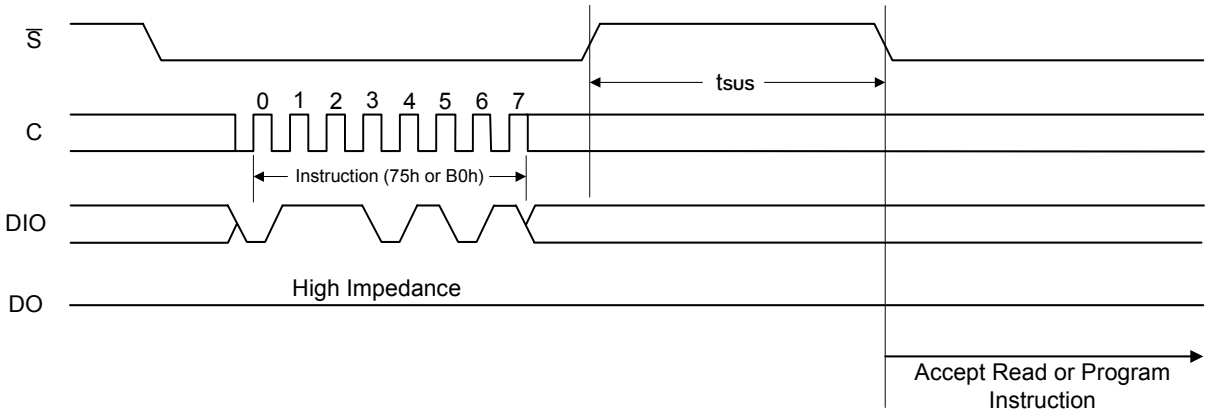


Table 8. Operations Allowed and Not Allowed During a Program or Erase Suspend

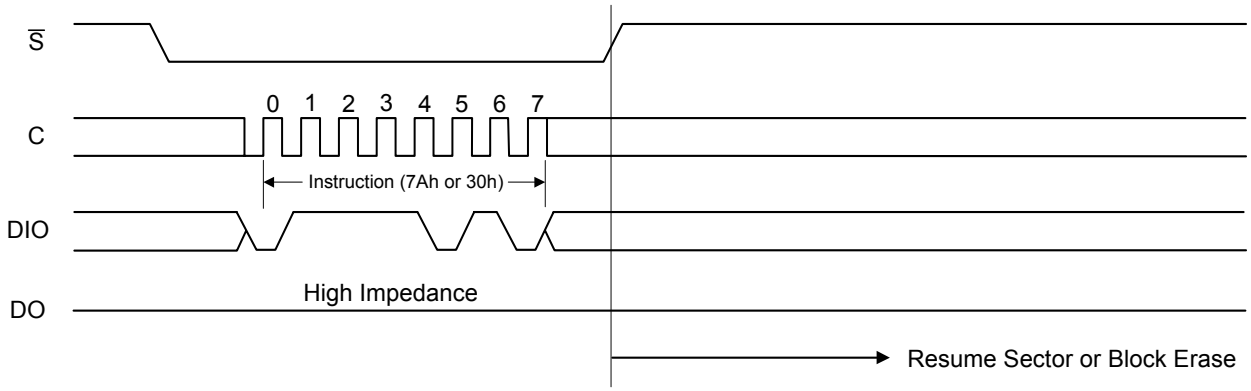
Command	Operation During Program Suspend	Operation During Erase Suspend
Read Commands		
Read Data	Allowed	Allowed
Program and Erase Commands		
PP	Not Allowed	Allowed
SE/ BE/ CE	Not Allowed	Not Allowed
Status Register Commands		
RDSR-1/ RDSR-2	Allowed	Allowed
WRSR	Not Allowed	Not Allowed
Other Commands		
SUSPEND	Not Allowed	Not Allowed
RESUME	Allowed	Allowed
HPM	Allowed	Allowed
WREN	Allowed	Allowed
WRDI	Allowed	Allowed
RDID/ REMS/ RES/ SFDP	Allowed	Allowed
DP	Not Allowed	Not Allowed

Program / Erase Resume

The Resume instruction must be written to resume the Sector or Block Erase operation or the Page Program operation after a Program/Erase Suspend. The Resume instruction will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the WIP bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the WIP bit equals to 1, the Resume instruction will be ignored by the device. The Resume instruction sequence is shown in figure 30.

Resume instruction is ignored if the previous Program/Erase Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Program/Erase Suspend instruction not to be issued within a minimum of time of "tsus" following a previous Resume instruction.

Figure 30. Resume Instruction Sequence



Read SFDP Register (5Ah)

The A25LQ32A features a 64-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about devices operational capability such as available commands, timing and other features.

The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified but more may be added in the future. The Read SFDP Register instruction is compatible with the JEDEC SFDP standard (JESD216) established in 2011.

The Read SFDP instruction is initiated by driving Chip Select ($\overline{S}$) Low and shifting the instruction code "5Ah" followed by a 24-bit address (A23-A0)(1) into the DIO pin. Eight "dummy" clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th Serial Clock (C) with most significant bit (MSB) first as shown in figure 31. For SFDP register values and descriptions, refer to the following SFDP Definition table.

Note: 1. A23-A6 = 0; A5-A0 are used to define the starting byte address for the 64-Byte SFDP Register.

Figure 31. Read SFDP Register Instruction Sequence Diagram

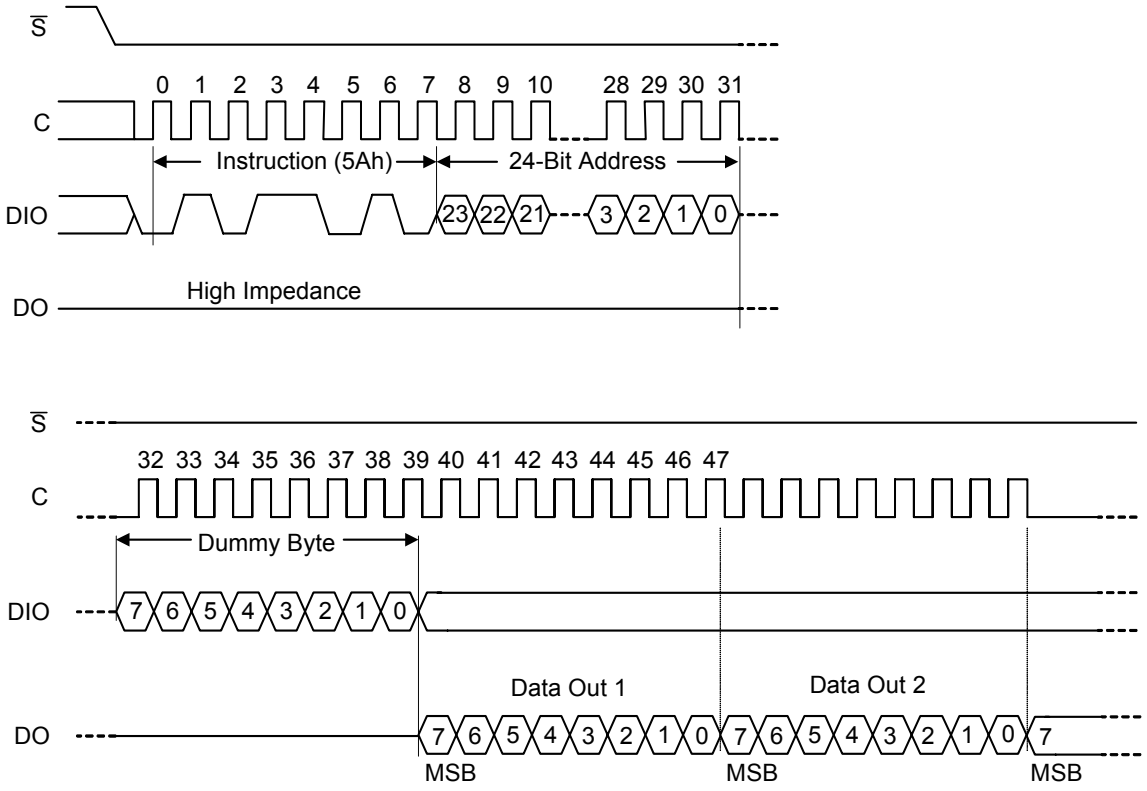


Table 9. SFDP Definition table

Description		Address(h) (Byte Mode)	Address (Bit)	Data	Comment
SPI Flash Discoverability Parameters (SFDP) Signature		00h	7:0	53h	Hex: 50444653
		01h	15:8	46h	
		02h	23:16	44h	
		03h	31:24	50h	
SFDP Revision	Minor Revision	04h	7:0	00h	Start from 0x00
	Major Revision	05h	15:8	01h	Start from 0x01
Number of Parameter Header		06h	23:16	00h	
Reserved		07h	31:24	FFh	Reserved
Parameter ID(0)		08h	7:0	00h	
Parameter Minor Revision		09h	15:8	00h	Start from 0x00
Parameter Major Revision		0Ah	23:16	01h	Start from 0x01
Parameter Length (in DW)		0Bh	31:24	09h	
Parameter Table Pointer		0Eh:0Ch	23:00	000010h	
Reserved		0Fh	31:24	FFh	Reserved

Parameter ID (0)

Description	Address(h) (Byte Mode)	Address (Bit)	Data	Comment
Block/Sector Erase Sizes	10h	01:00	01	00= reserved 01=4KB erase 10= reserved 11=64KB erase
Write Granularity		02	1	0=1Byte 1=64Byte
Write Enable Command Required for Writing to Volatile Status Register		03	0	
Write Enable Opcode Select for Writing to Volatile Status Register		04	0	
Unused		07:05	7h	Reserved
4Kilo Byte Erase Opcode	11h	15:08	20h	4KB Erase Support (FFh=not supported)
Supports Single Input Address Dual Output Fast read	12h	16	1	0=not supported 1=support
Number of bytes used in addressing for flash array read, write and erase		18:17	00	00=3 byte 01=3 byte or 4byte 10= 4-byte only 11= reserved
Supports Dual Transfer Rate Clocking		19	0	0=not supported 1=support
Supports Dual Input Address Dual Output Fast read		20	1	0=not supported 1=support
Supports Quad Input Address Quad Output Fast read		21	1	0=not supported 1=support
Supports Single Input Address Quad Output Fast read		22	1	0=not supported 1=support
Unused		23	1	Reserved
	13h	31:24	FFh	
Flash Size in bits	17h to 14h	31:00	01FFFFFFh	32Mb

Parameter ID (0) (Continued)

Description	Address(h) (Byte Mode)	Address (Bit)	Data	Comment
Quad Input Address Quad Output Fast Read Number of Wait States(dummy bits) needed before valid output	18h	04:00	00100	This filed should be counted in clocks.
Quad Input Address Quad Output Fast Read Number of Mode Bits		07:05	010	
Quad Input Address Quad Output Fast Read Opcode	19h	15:08	EBh	
Single Input Address Quad Output Fast Read Number of Wait States(dummy bits) needed before valid output	1Ah	20:16	01000	This filed should be counted in clocks.
Single Input Address Quad Output Fast Read Number of Mode Bits		23:21	000	
Single Input Address Quad Output Fast Read Opcode	1Bh	31:24	6Bh	
Single Input Address Dual Output Fast Read Number of Wait States(dummy bits) needed before valid output	1Ch	04:00	01000	This filed should be counted in clocks.
Single Input Address Dual Output Fast Read Number of Mode Bits		07:05	000	
Single Input Address Dual Output Fast Read Opcode	1Dh	15:08	3Bh	
Dual Input Address Dual Output Fast Read Number of Wait States(dummy bits) needed before valid output	1Eh	20:16	00100	This filed should be counted in clocks.
Dual Input Address Dual Output Fast Read Number of Mode Bits		23:21	000	
Dual Input Address Dual Output Fast Read Opcode	1Fh	31:24	BBh	

Parameter ID (0) (Continued)

Description	Address(h) (Byte Mode)	Address (Bit)	Data	Comment
Supports (2-2-2) Fast Read	20h	0	0	not supported
Reserved		03:01	7h	
Supports (4-4-4) Fast Read		04	0	not supported
Reserved		07:05	7h	
Reserved	23h to 21h	31:08	FFFFFFh	
Reserved	25h to 24h	15:0	FFFFh	
(2-2-2) Fast Read Number of Wait States	26h	20:16	00000	not supported
(2-2-2) Fast Read Number of Mode Bits		23:21	000	
(2-2-2) Fast Read Opcode	27h	31:24	00h	
Reserved	29h to 28h	15:0	FFFFh	
(4-4-4) Fast Read Number of Wait States	2Ah	20:16	00000	not supported
(4-4-4) Fast Read Number of Mode Bits		23:21	000	
(4-4-4) Fast Read Opcode	2Bh	31:24	00h	
Sector Type 1 Size (4KB)	2Ch	07:00	0Ch	
Sector Type 1 Opcode	2Dh	15:08	20h	
Sector Type 2 Size (32KB)	2Eh	23:16	00h	not supported
Sector Type 2 Opcode	2Fh	31:24	00h	
Sector Type 3 Size (64KB)	30h	07:00	10h	
Sector Type 3 Opcode	31h	15:08	D8h	
Sector Type 4 Size (256KB)	32h	23:16	00h	not supported
Sector Type 4 Opcode	33h	31:24	00h	

Notes:
1. Data stored in Byte Address 34h to 3Fh are Reserved, the value is FFh.

POWER-UP AND POWER-DOWN

At Power-up and Power-down, the device must not be selected (that is Chip Select ($\overline{S}$) must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value:

- V_{CC} (min) at Power-up, and then for a further delay of t_{VSL}
- V_{SS} at Power-down

Usually a simple pull-up resistor on Chip Select ($\overline{S}$) can be used to insure safe and proper Power-up and Power-down.

To avoid data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The logic inside the device is held reset while V_{CC} is less than the POR threshold value, V_{WI} – all operations are disabled, and the device does not respond to any instruction.

Moreover, the device ignores all Write Enable (WREN), Program OTP (POTP), Page Program (PP), Dual Input Fast Program (DIFP), Quad Input Fast Program (QIFP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) instructions until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the V_{WI} threshold. However, the correct operation of the device is not guaranteed if, by this time, V_{CC} is still below V_{CC}(min). No Write Status Register, Program or Erase instructions should be sent until the later of:

- t_{PUW} after V_{CC} passed the V_{WI} threshold
- t_{VSL} afterV_{CC} passed the V_{CC}(min) level

These values are specified in Table 10.

If the delay, t_{VSL}, has elapsed, after V_{CC} has risen above V_{CC}(min), the device can be selected for Read instructions even if the t_{PUW} delay is not yet fully elapsed.

At Power-up, the device is in the following state:

- The device is in the Standby mode (not the Deep Power-down mode).
- The Write Enable Latch (WEL) bit is reset.

Normal precautions must be taken for supply rail decoupling, to stabilize the V_{CC} feed. Each device in a system should have the V_{CC} rail decoupled by a suitable capacitor close to the package pins. (Generally, this capacitor is of the order of 0.1µF).

At Power-down, when V_{CC} drops from the operating voltage, to below the POR threshold value, V_{WI}, all operations are disabled and the device does not respond to any instruction. (The designer needs to be aware that if a Power-down occurs while a Write, Program or Erase cycle is in progress, some data corruption can result.)

Figure 32. Power-up Timing

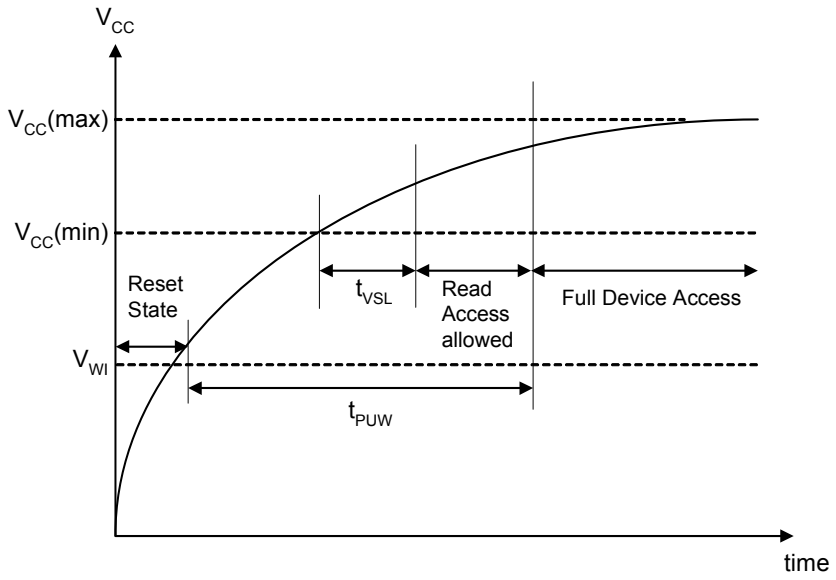


Table 10. Power-Up Timing

Symbol	Parameter	Min.	Max.	Unit
t_{VSL}	$V_{CC(min)}$ to $\overline{S}$ Low	10		μs
t_{PUW}	Time Delay Before Write Instruction	3		ms
V_{WI}	Write Inhibit Threshold Voltage	2.3	2.5	V

Note: These parameters are characterized only.

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

Absolute Maximum Ratings*

Storage Temperature (TSTG) . . . . . -65°C to + 150°C
Lead Temperature during Soldering (Note 1)
D.C. Voltage on Any Pin to Ground Potential . . . . -0.6V to V_{CC}+0.6V
Transient Voltage (<20ns) on Any Pin to Ground Potential . . . . -2.0V to V_{CC}+2.0V
Supply Voltage (V_{CC}) . . . . . -0.6V to +4.0V
Electrostatic Discharge Voltage (Human Body model) (VESD) (Note 2) . . . . . -2000V to 2000V

Notes:
1. Compliant with JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly).
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500Ω, R2=500Ω)

*Comments

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the AMIC SURE Program and other relevant quality documents.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 11. Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.7	3.6	V
T_A	Ambient Operating Temperature	–40	85	°C

Table 12. Data Retention and Endurance

Parameter	Condition	Min.	Max.	Unit
Erase/Program Cycles	At 85°C	100,000		Cycles
Data Retention	At 85°C	20		Years

Table 13. Capacitance

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{OUT}	Output Capacitance (DO)	V_{OUT} = 0V		8	pF
C_{IN}	Input Capacitance (other pins)	V_{IN} = 0V		6	pF

Note: Sampled only, not 100% tested, at T_A=25°C and a frequency of 33 MHz.

Table 14. DC Characteristics

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current			± 2	µA
I_{LO}	Output Leakage Current			± 2	µA
I_{CC1}	Standby Current	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}	1	15	µA
I_{CC2}	Deep Power-down Current	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}	1	15	µA
I_{CC3}	Operating Current (Read)	C= 0.1V_{CC} / 0.9.V_{CC} at 100MHz, DO = open		24	mA
		C= 0.1V_{CC} / 0.9.V_{CC} at 50MHz, DO = open		21	mA
		C= 0.1V_{CC} / 0.9.V_{CC} at 33MHz, DO = open		17	mA
	Operating Current (Dual Read)	C= 0.1V_{CC} / 0.9.V_{CC} at 100MHz, IO_0, IO_1 = open		26	mA
	Operating Current (Quad Read)	C= 0.1V_{CC} / 0.9.V_{CC} at 100MHz, IO_0 ~ IO_3 = open		28	mA
I_{CC4}	Operating Current (PP)	$\overline{S}$ = V_{CC}		15	mA
I_{CC5}	Operating Current (WRSR)	$\overline{S}$ = V_{CC}		12	mA
I_{CC6}	Operating Current (SE)	$\overline{S}$ = V_{CC}		25	mA
I_{CC7}	Operating Current (BE)	$\overline{S}$ = V_{CC}		25	mA
V_{IL}	Input Low Voltage		–0.5	0.3V_{CC}	V
V_{IH}	Input High Voltage		0.7V_{CC}	V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{CC}–0.2		V

Note: 1. This is preliminary data at 85°C

Table 15. AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}		V
	Input Timing Reference Voltages	0.3V_{CC} to 0.7V_{CC}		V
	Output Timing Reference Voltages	V_{CC} / 2		V

Note: Output Hi-Z is defined as the point where data out is no longer driven.

Figure 33. AC Measurement I/O Waveform

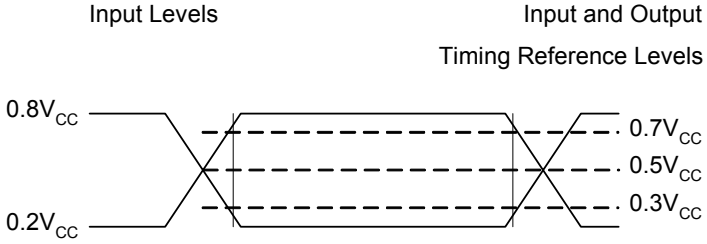


Table 16. AC Characteristics

Symbol	Alt.	Parameter	Min.	Typ.	Max.	Unit
f_C	f_C	Clock Frequency for all instructions, except READ (03h)	D.C.		100	MHz
f_R		Clock Frequency for READ (03h) instruction	D.C.		50	MHz
t_{CH} [1]	t_{CLH}	Clock High Time	5			ns
t_{CL} [1]	t_{CLL}	Clock Low Time	5			ns
t_{CLCH} [2]		Clock Rise Time[3] (peak to peak)	0.1			V/ns
t_{CHCL} [2]		Clock Fall Time[3] (peak to peak)	0.1			V/ns
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time (relative to C)	5			ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time (relative to C)	5			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	3			ns
t_{CHDX}	t_{DH}	Data In Hold Time	3			ns
t_{CHSH}		$\overline{S}$ Active Hold Time (relative to C)	5			ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time (relative to C)	5			ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect Time	30			ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time			7	ns
t_{CLQV}	t_V	Clock Low to Output Valid			7	ns
t_{CLQX}	t_{HO}	Output Hold Time	0			ns
t_{HLCH}		$\overline{HOLD}$ Setup Time (relative to C)	5			ns
t_{CHHH}		$\overline{HOLD}$ Hold Time (relative to C)	5			ns
t_{HHCH}		HOLD Setup Time (relative to C)	5			ns
t_{CHHL}		HOLD Hold Time (relative to C)	5			ns
t_{HHQX} [2]	t_{LZ}	HOLD to Output Low-Z			7	ns
t_{HLQZ} [2]	t_{HZ}	$\overline{HOLD}$ to Output High-Z			7	ns
t_{WHSL} [4]		Write Protect Setup Time	20			ns
t_{SHWL} [4]		Write Protect Hold Time	100			ns
t_{DP} [2]		$\overline{S}$ High to Deep Power-down Mode			3	µs
t_{RES1} [2]		$\overline{S}$ High to Standby Mode without Electronic Signature Read			1	µs
t_{RES2} [2]		$\overline{S}$ High to Standby Mode with Electronic Signature Read			1	µs
t_W		Write Status Register Cycle Time		5	20	ms
t_{pp}		Page Program Cycle Time		2	6	ms
		Program OTP Cycle Time		2	3	ms
t_{SE}		Sector Erase Cycle Time		80	200	ms
t_{BE}		Block Erase Cycle Time		0.5	2	s
t_{CE}		Chip Erase Cycle Time of A25LQ32A		32	64	s

Note: 1. $t_{CH} + t_{CL}$ must be greater than or equal to $1/f_C$
2. Value guaranteed by characterization, not 100% tested in production.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for WRSR instruction when Status Register Protect bits (SRP1, SRP0) = (0, 1)

Figure 34. Serial Input Timing

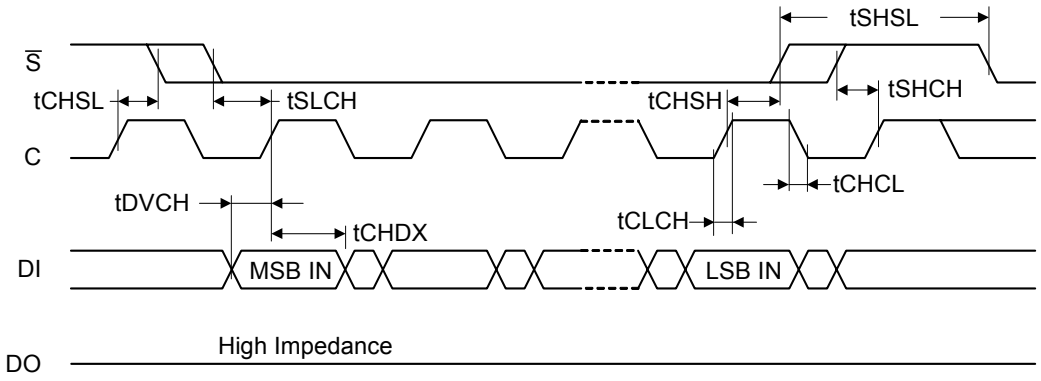


Figure 35. Write Protect Setup and Hold Timing during WRSR when (SRP1, SRP0) = (0, 1)

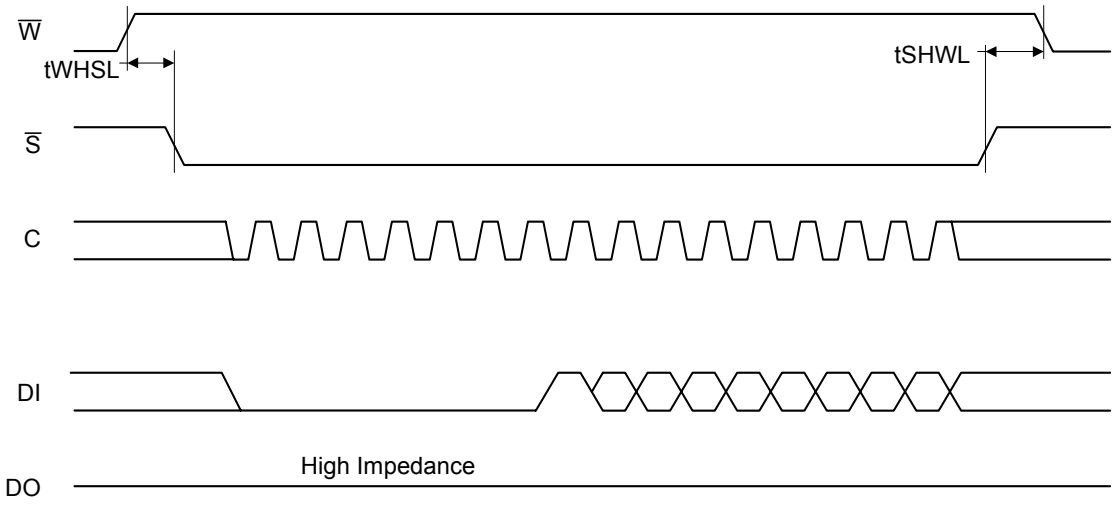


Figure 36. Hold Timing

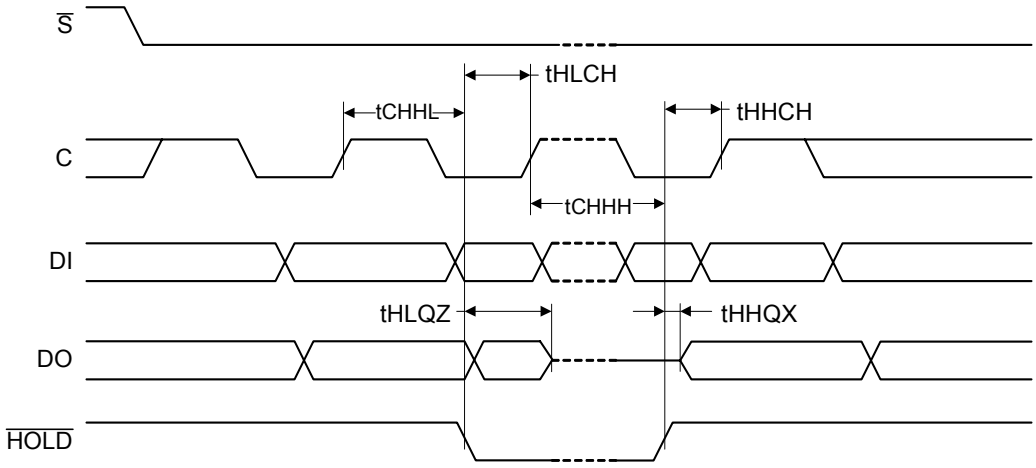
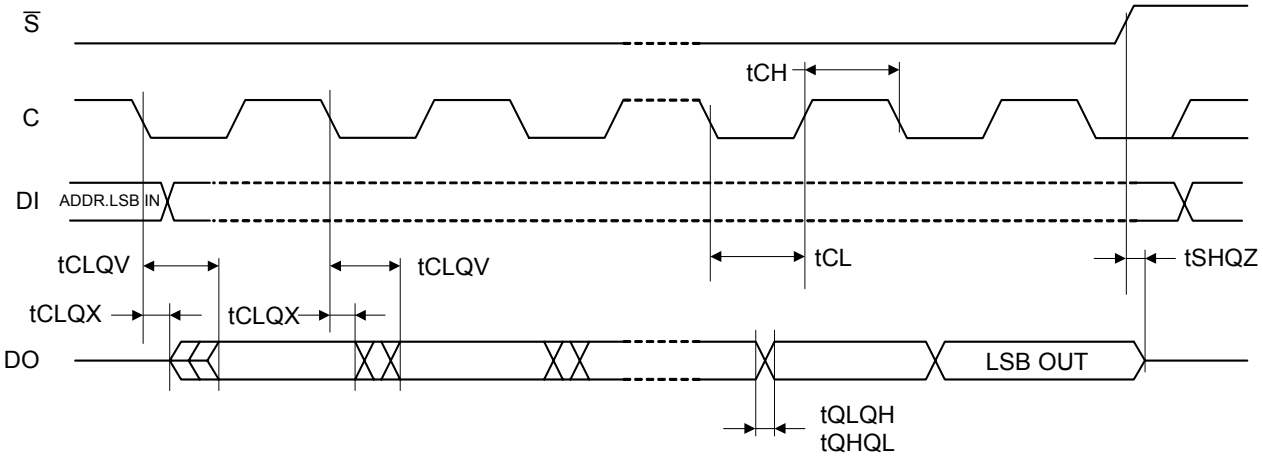
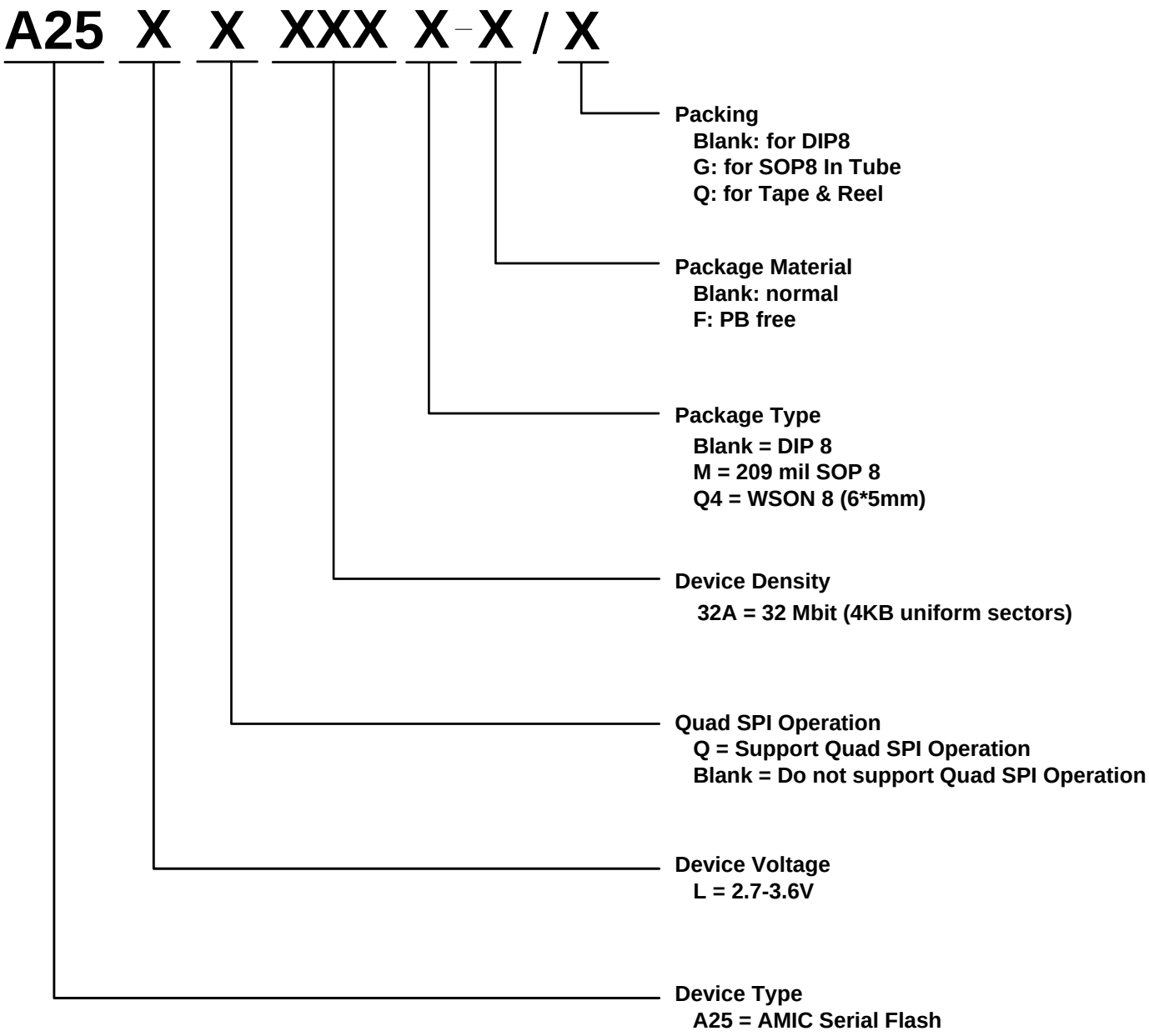


Figure 37. Output Timing



Part Numbering Scheme



*** Optional**

Ordering Information

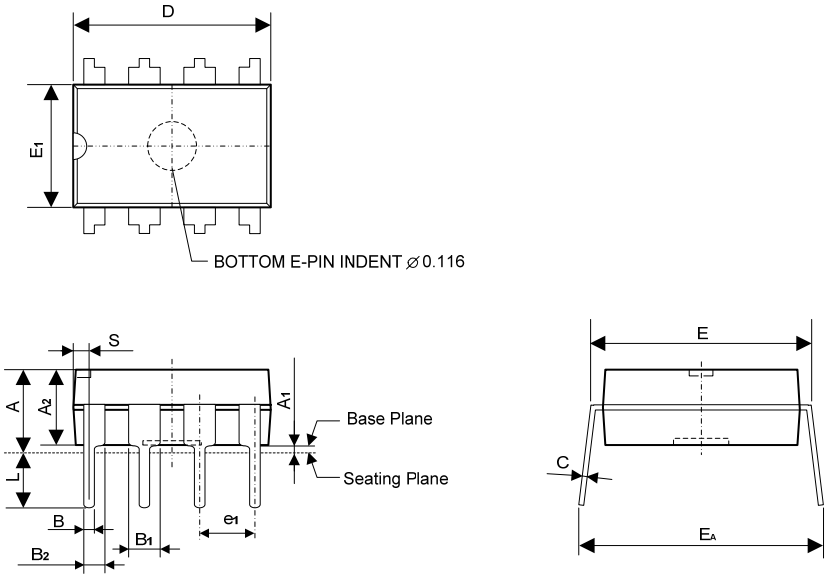
Part No.	Speed (MHz)	Active Read Current Max. (mA)	Program/Erase Current Max. (mA)	Standby Current Max. (μA)	Package
A25LQ32A-F	100	24	15	15	8 Pin Pb-Free DIP (300 mil)
A25LQ32AM-F					8 Pin Pb-Free SOP (209mil)
A25LQ32AQ4-F					8 Pin Pb-Free WSON (6*5mm)

Operating temperature range: -40°C ~ +85°C

Package Information

P-DIP 8L Outline Dimensions

unit: inches/mm



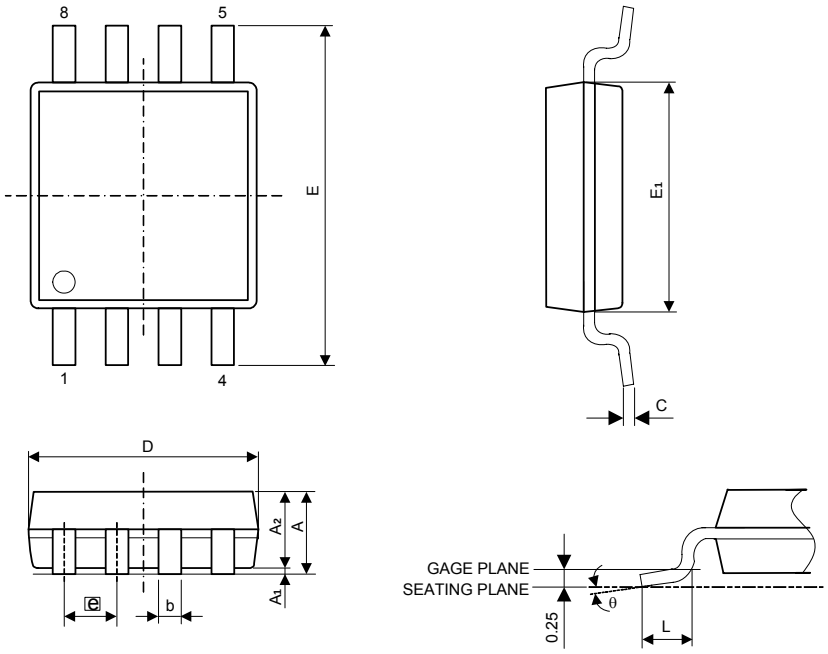
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.180	-	-	4.57
A_1	0.015	-	-	0.38	-	-
A_2	0.128	0.130	0.136	3.25	3.30	3.45
B	0.014	0.018	0.022	0.36	0.46	0.56
B_1	0.050	0.060	0.070	1.27	1.52	1.78
B_2	0.032	0.039	0.046	0.81	0.99	1.17
C	0.008	0.010	0.013	0.20	0.25	0.33
D	0.350	0.360	0.370	8.89	9.14	9.40
E	0.290	0.300	0.315	7.37	7.62	8.00
E_1	0.254	0.260	0.266	6.45	6.60	6.76
e_1	-	0.100	-	-	2.54	-
L	0.125	-	-	3.18	-	-
E_A	0.345	-	0.385	8.76	-	9.78
S	0.016	0.021	0.026	0.41	0.53	0.66

Notes:
1. Dimension D and E_1 do not include mold flash or protrusions.
2. Dimension B_1 does not include dambar protrusion.
3. Tolerance: ±0.010” (0.25mm) unless otherwise specified.

Package Information

SOP 8L (209mil) Outline Dimensions

unit: mm



Symbol	Dimensions in mm		
	Min	Nom	Max
A	1.75	1.95	2.16
A_1	0.05	0.15	0.25
A_2	1.70	1.80	1.91
b	0.35	0.42	0.48
C	0.19	0.20	0.25
D	5.13	5.23	5.33
E	7.70	7.90	8.10
E_1	5.18	5.28	5.38
e	1.27 BSC		
L	0.50	0.65	0.80
θ	0°	-	8°

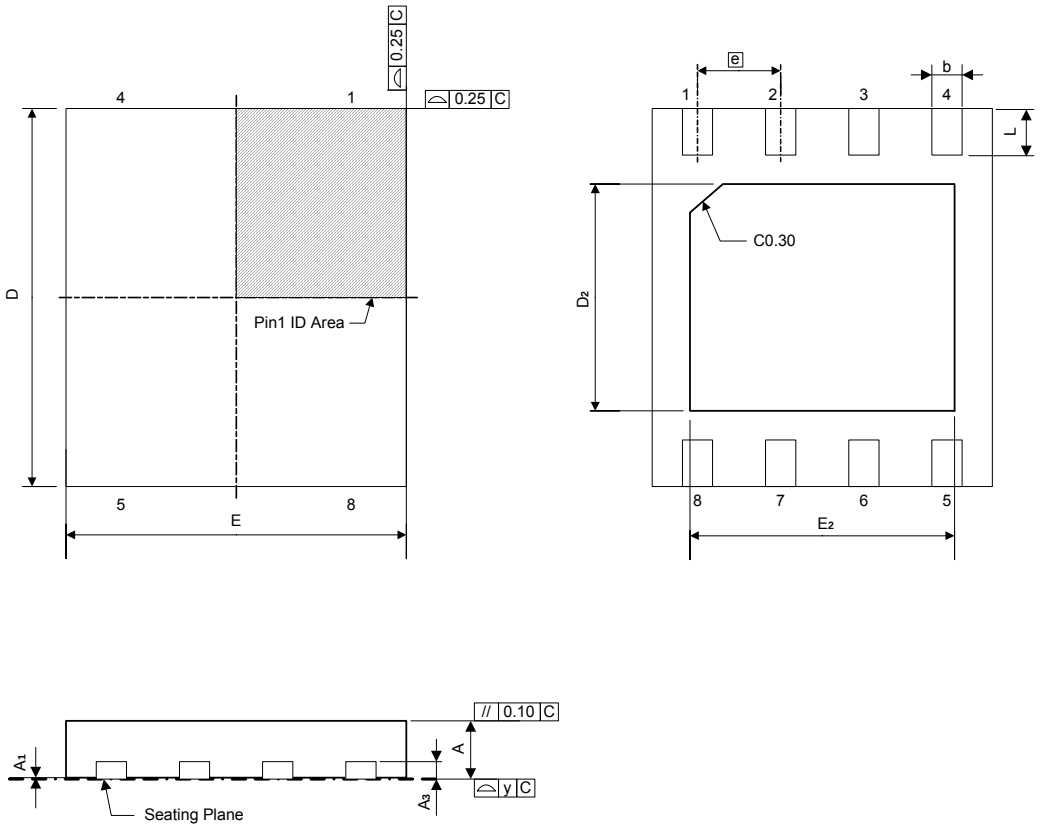
Notes:

Maximum allowable mold flash is 0.15mm at the package ends and 0.25mm between leads

Package Information

WSON 8L (6 X 5 X 0.8mm) Outline Dimensions

unit: mm/mil



Symbol	Dimensions in mm			Dimensions in mil		
	Min	Nom	Max	Min	Nom	Max
A	0.700	0.750	0.800	27.6	29.5	31.5
A_1	0.000	0.020	0.050	0.0	0.8	2.0
A_3	0.203 REF			8.0 REF		
b	0.350	0.400	0.480	13.8	15.8	18.9
D	5.900	6.000	6.100	232.3	236.2	240.2
D_2	3.200	3.400	3.600	126.0	133.9	141.7
E	4.900	5.000	5.100	192.9	196.9	200.8
E_2	3.800	4.000	4.200	149.6	157.5	165.4
L	0.500	0.600	0.750	19.7	23.6	29.5
e	1.270 BSC			50.0 BSC		
y	0	-	0.080	0	-	3.2

Note:

1. Controlling dimension: millimeters
2. Leadframe thickness is 0.203mm (8mil)